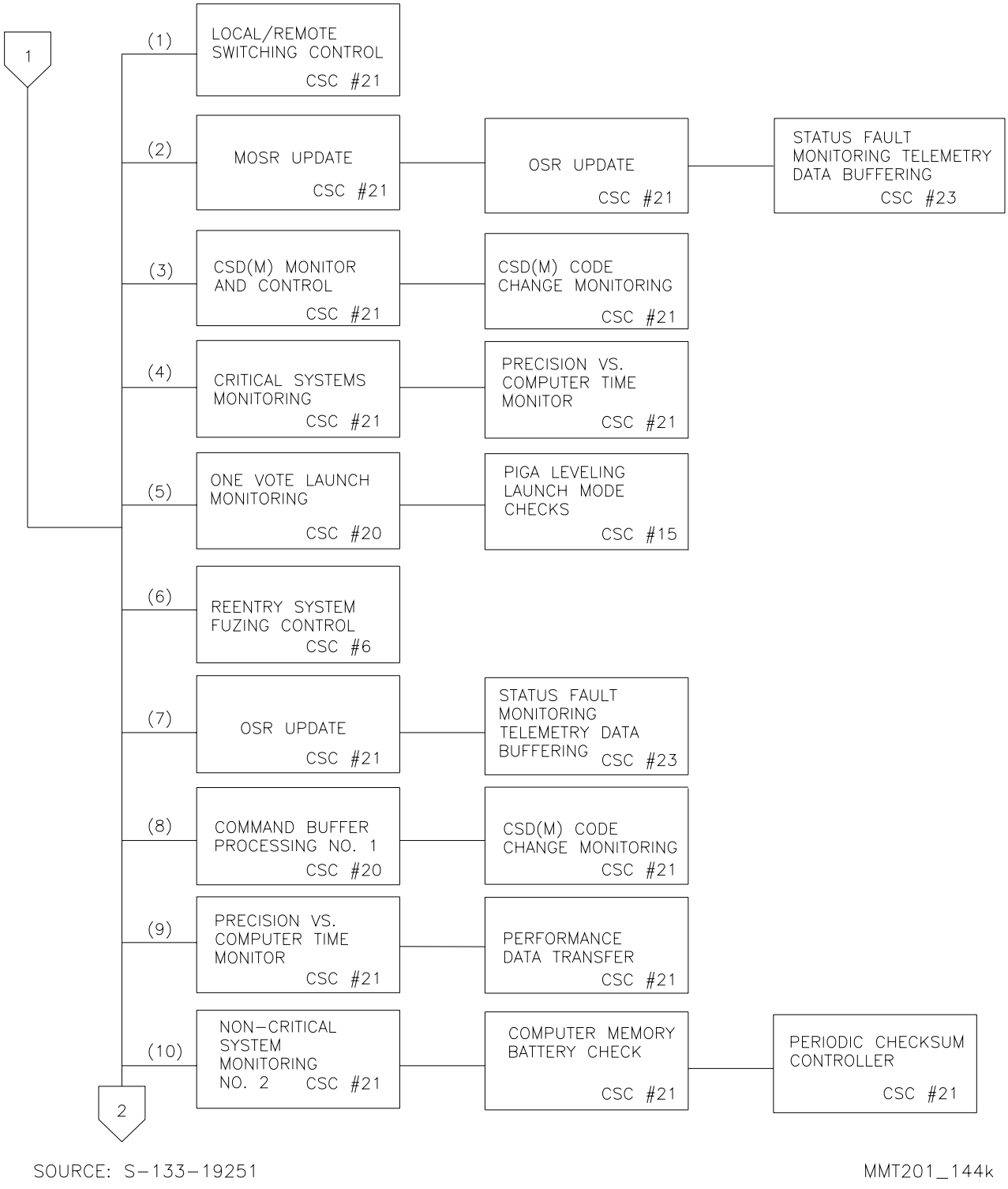
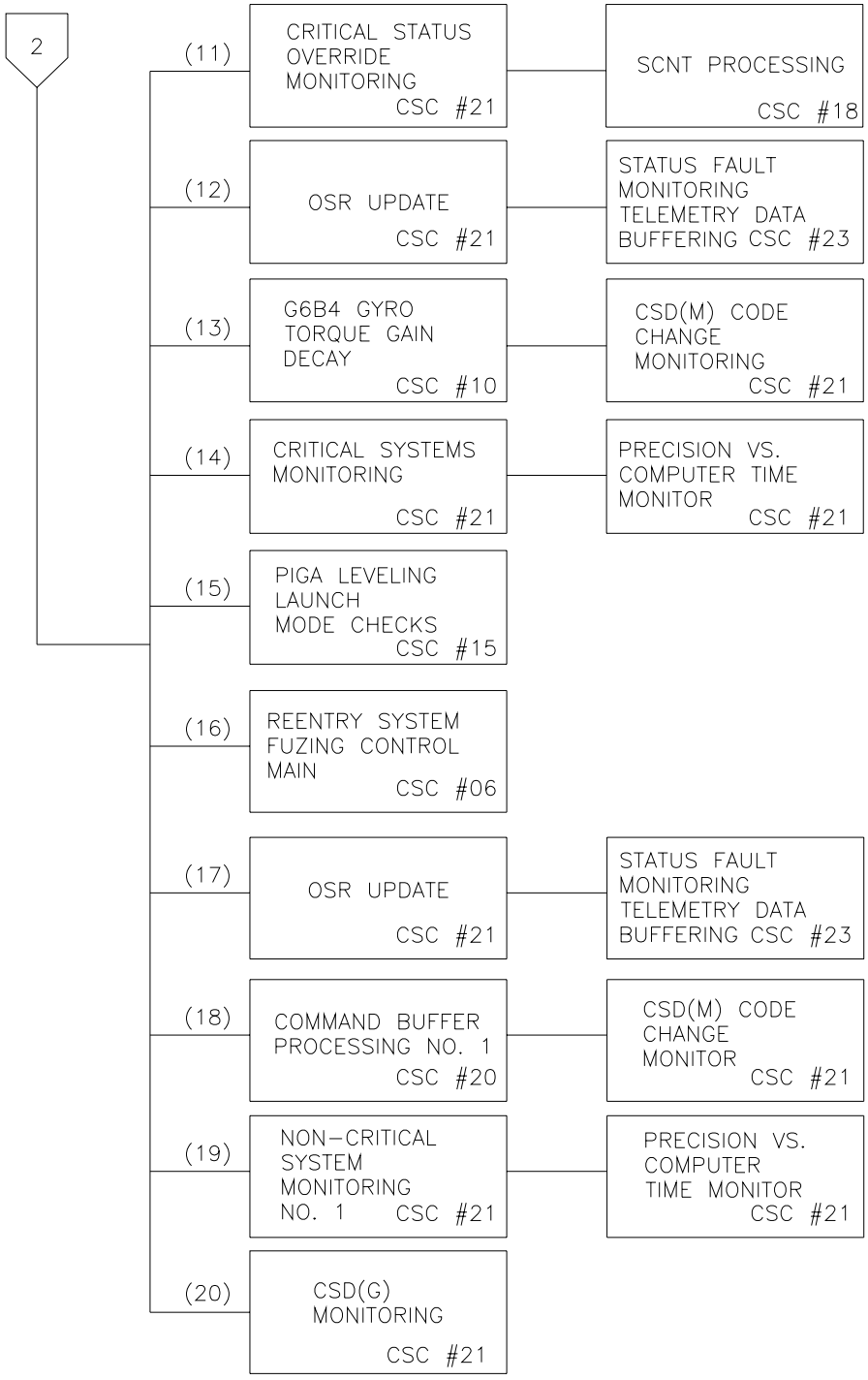


Figure 2-36. 90-msec Task Controller (CSC #7) (Sheets 2 of 3)



SOURCE: S-133-19251 MMT201_143k

Figure 2-36. 90-msec Task Controller (CSC #7) (Sheets 3 of 3)

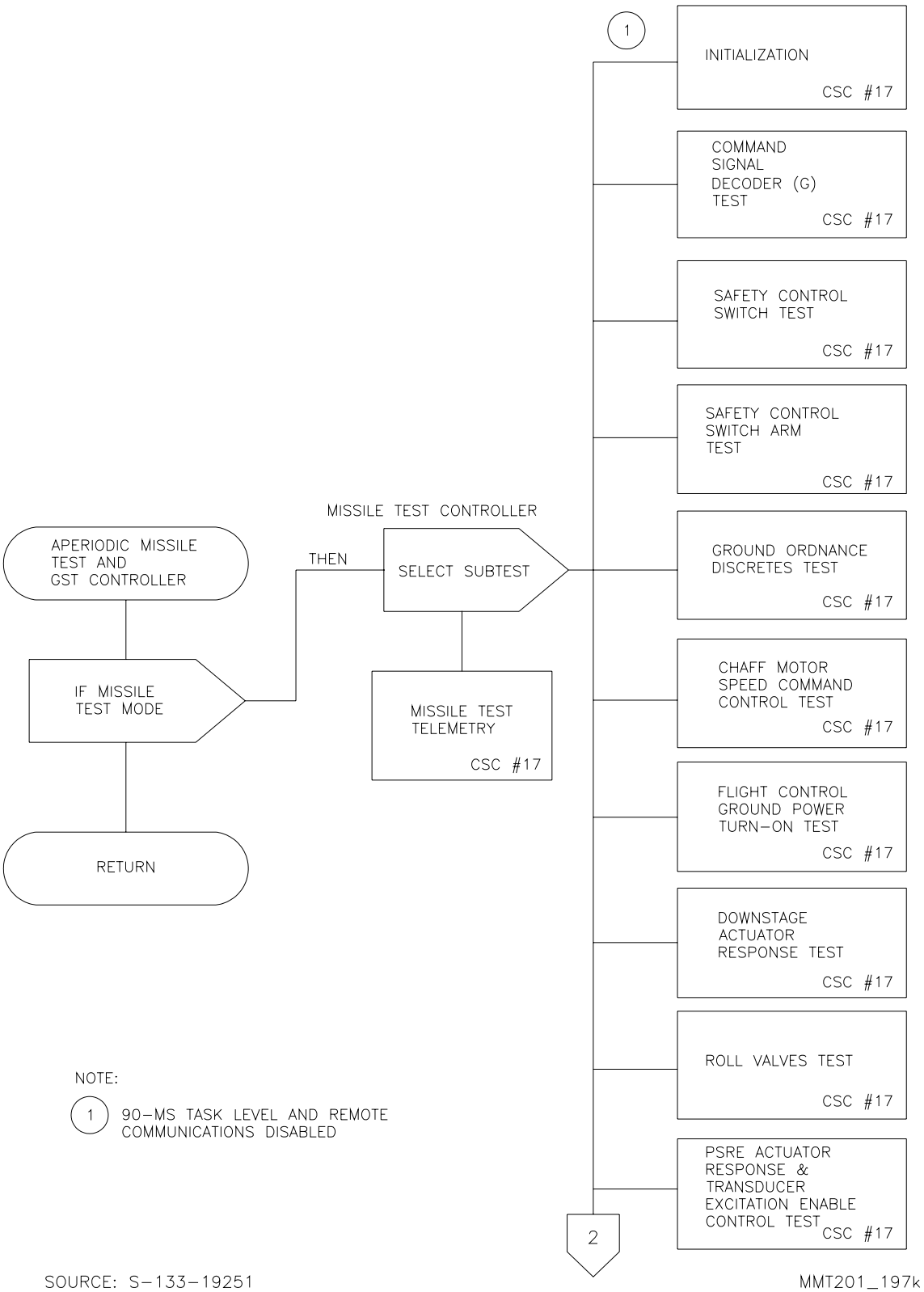
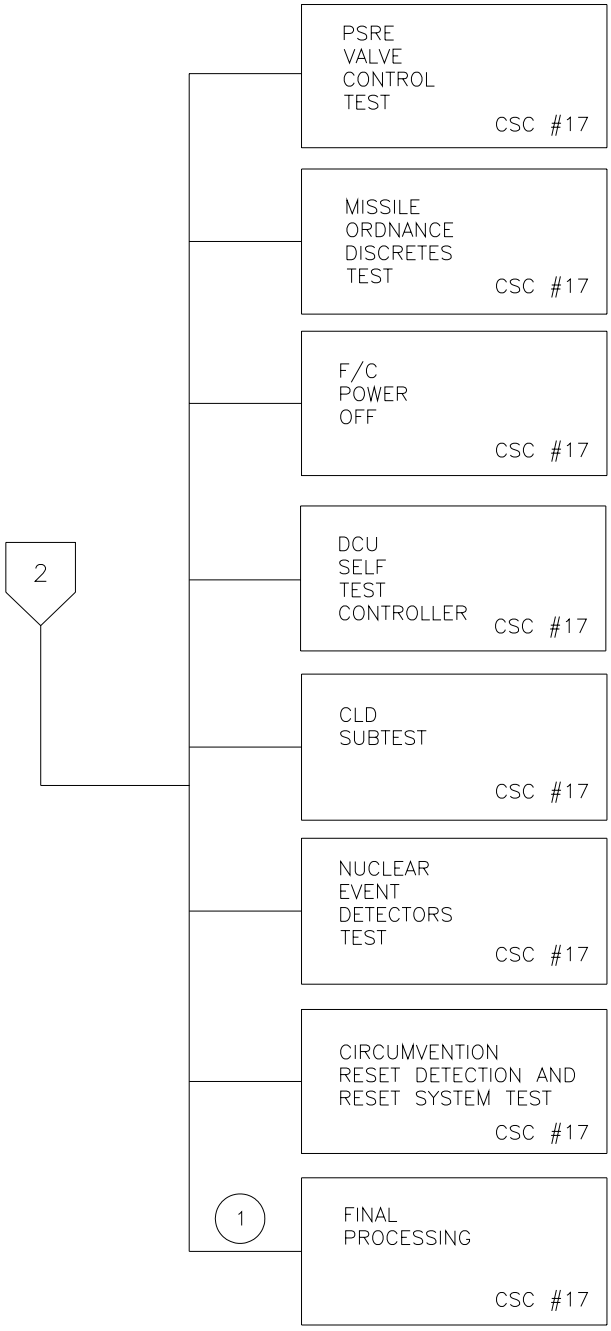


Figure 2-37. Aperiodic Missile Test and GST Controller (Sheets 1 of 2)

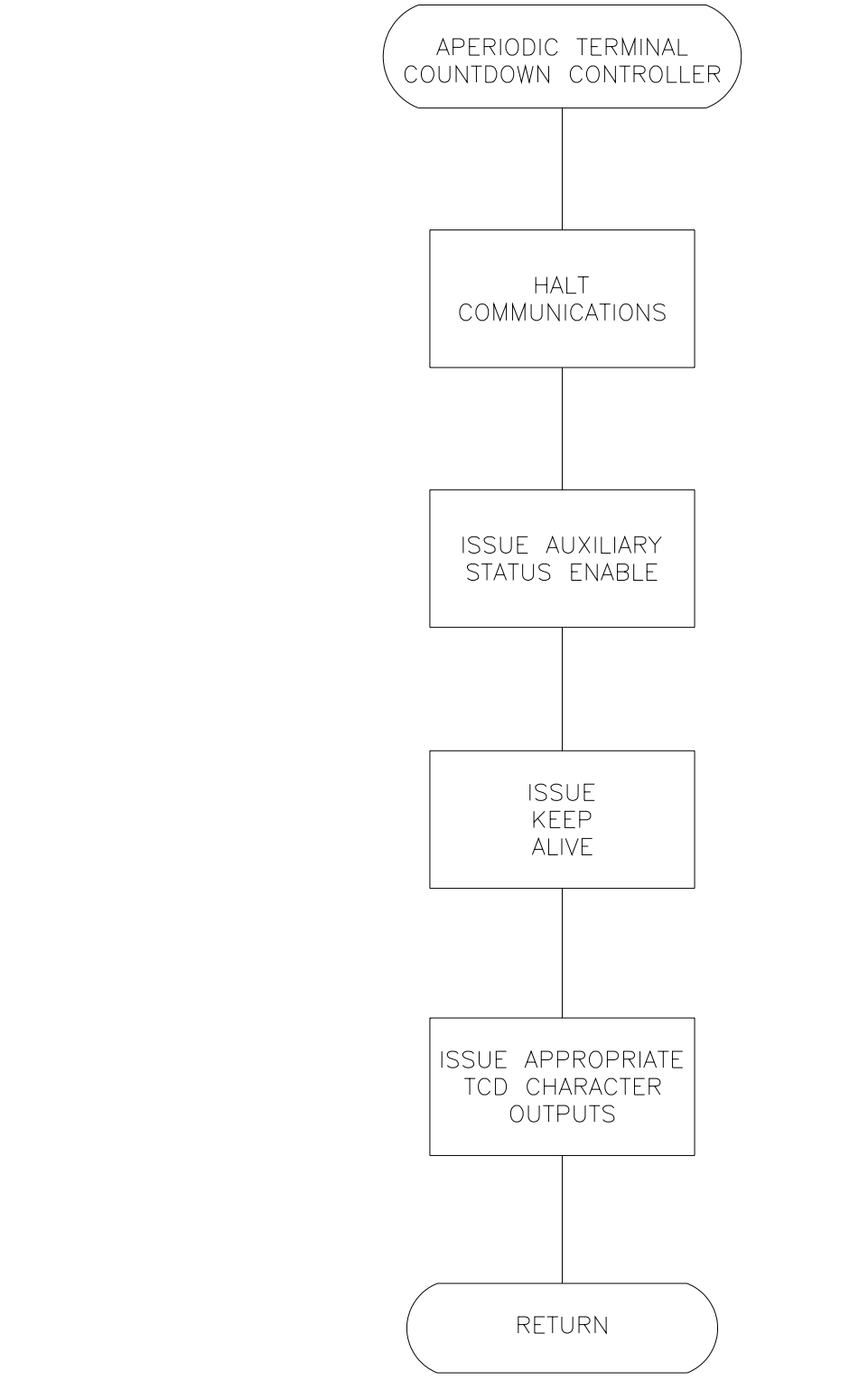


NOTE:

(1) REMOTE COMMUNICATIONS AND 90-MS TASK LEVEL ENABLED

SOURCE: S-133-19251 MMT201_146k

Figure 2-37. Aperiodic Missile Test and GST Controller (Sheets 2 of 2)



SOURCE: S-133-19251 MMT201_147k

Figure 2-38. Aperiodic Terminal Countdown Controller (CSC #7)

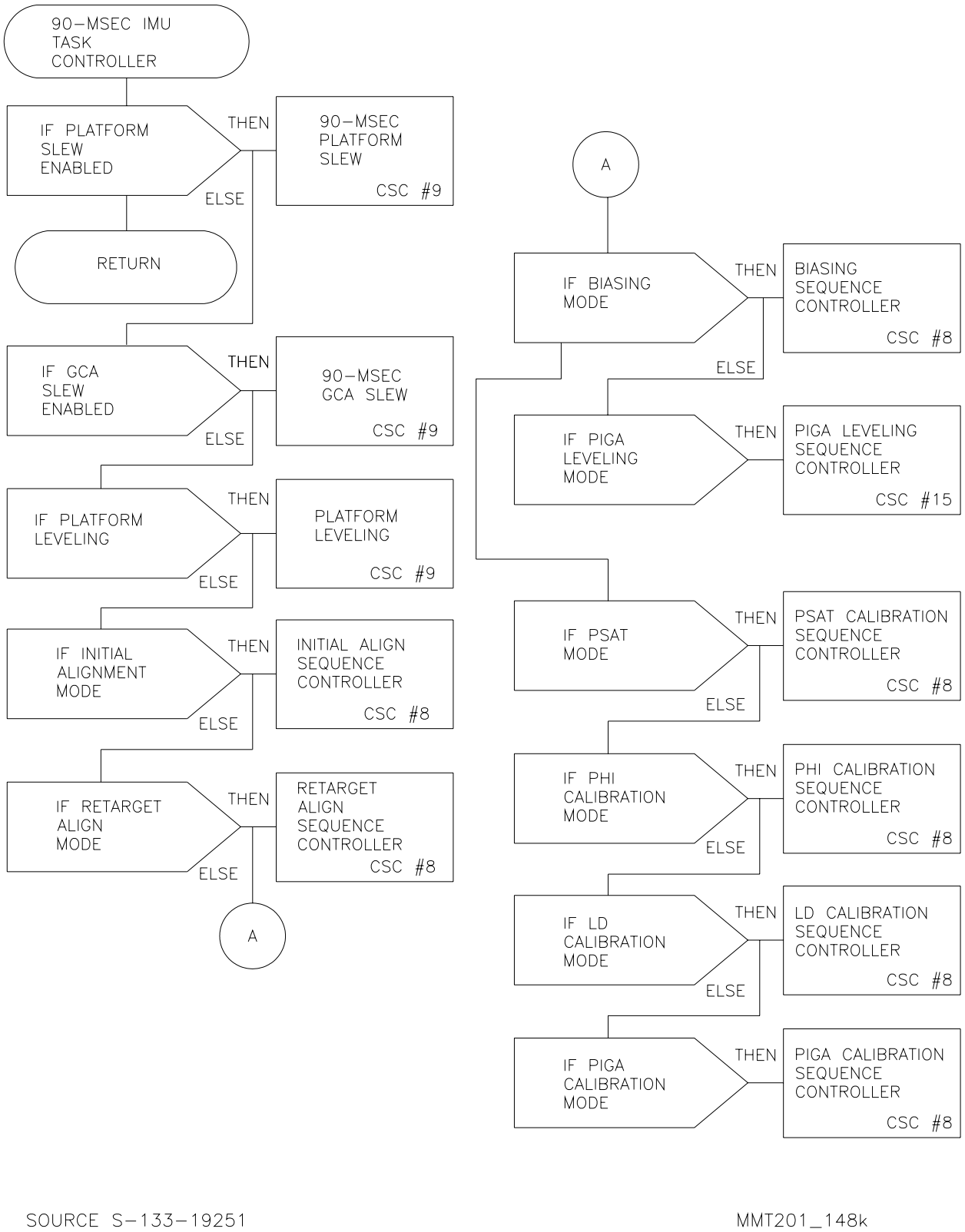


Figure 2-39. 90-msec IMU Task Controller (CSC #7)

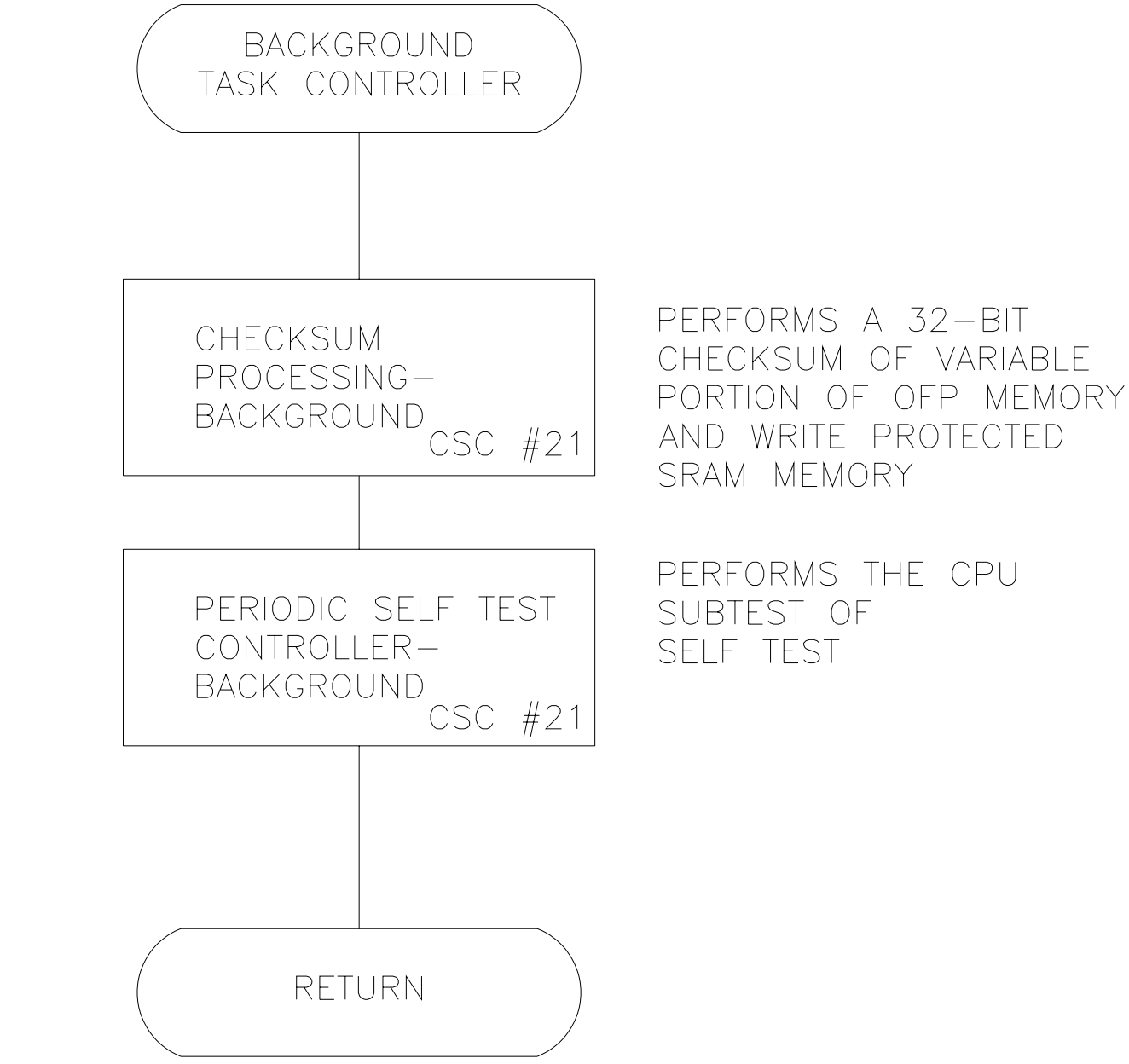


Figure 2-40. Background Task Controller

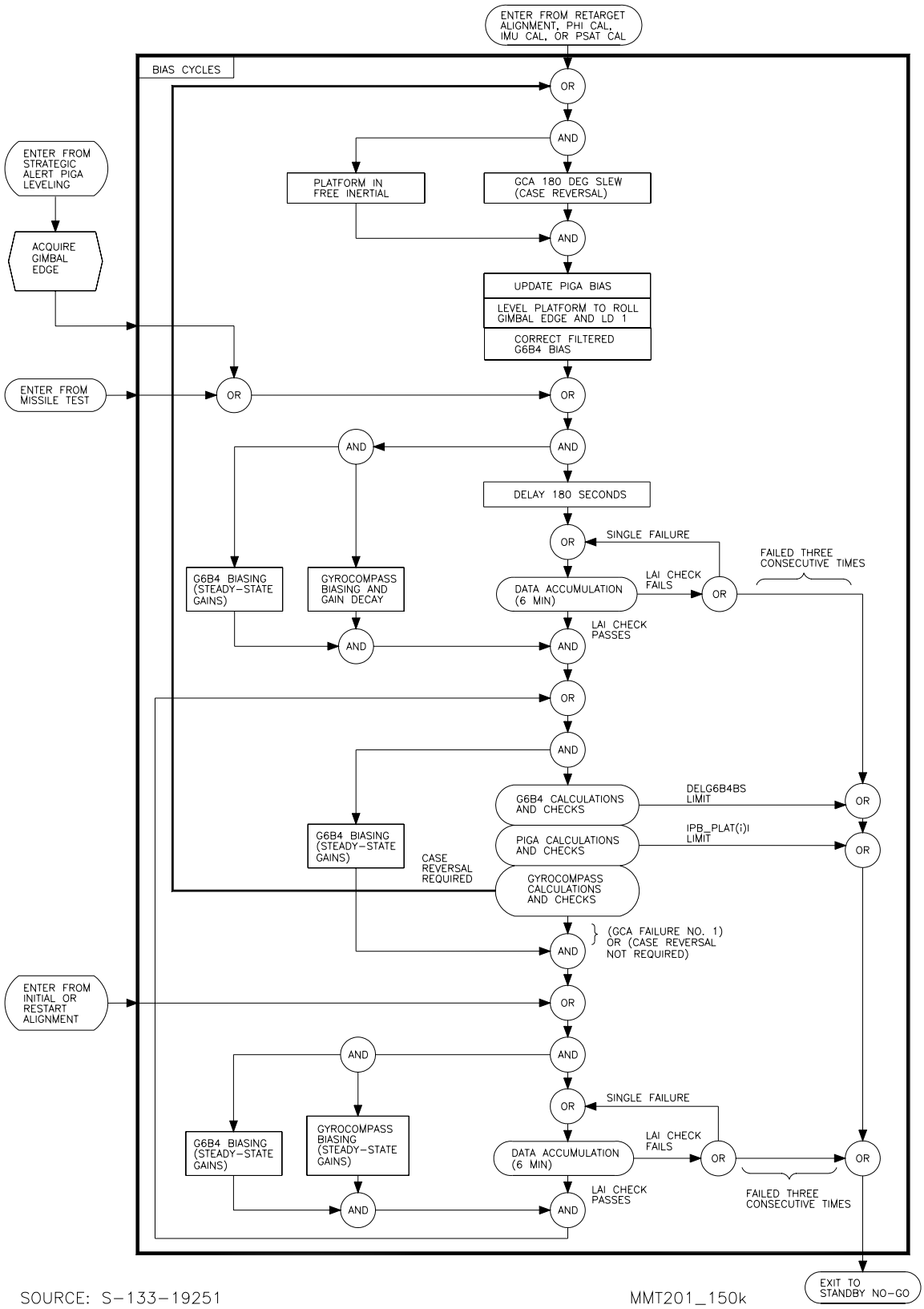


Figure 2-41. Strategic Alert Biasing Sequence

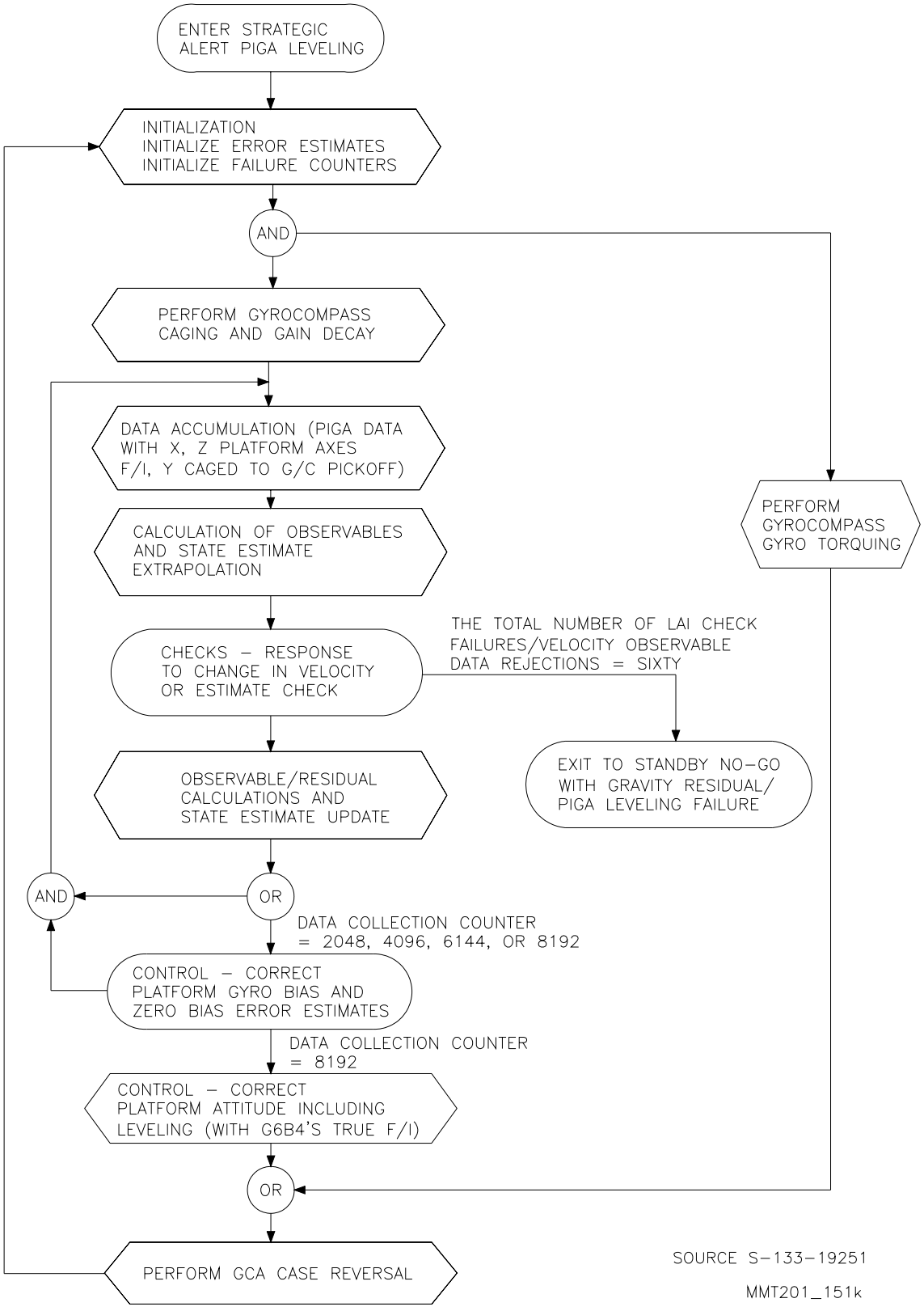


Figure 2-42. Strategic Alert PIGA Leveling Sequence (Sheet 1 of 2)

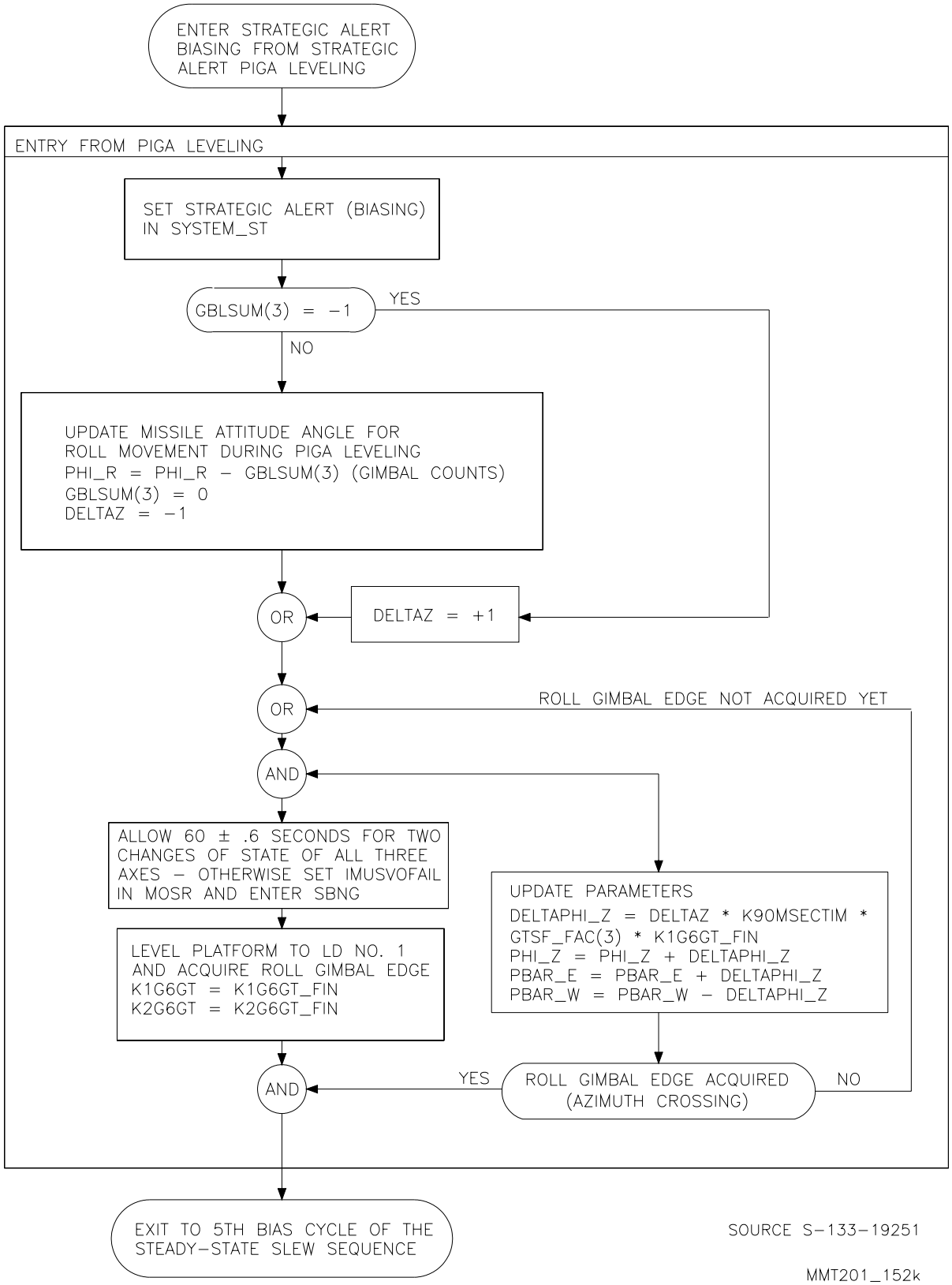
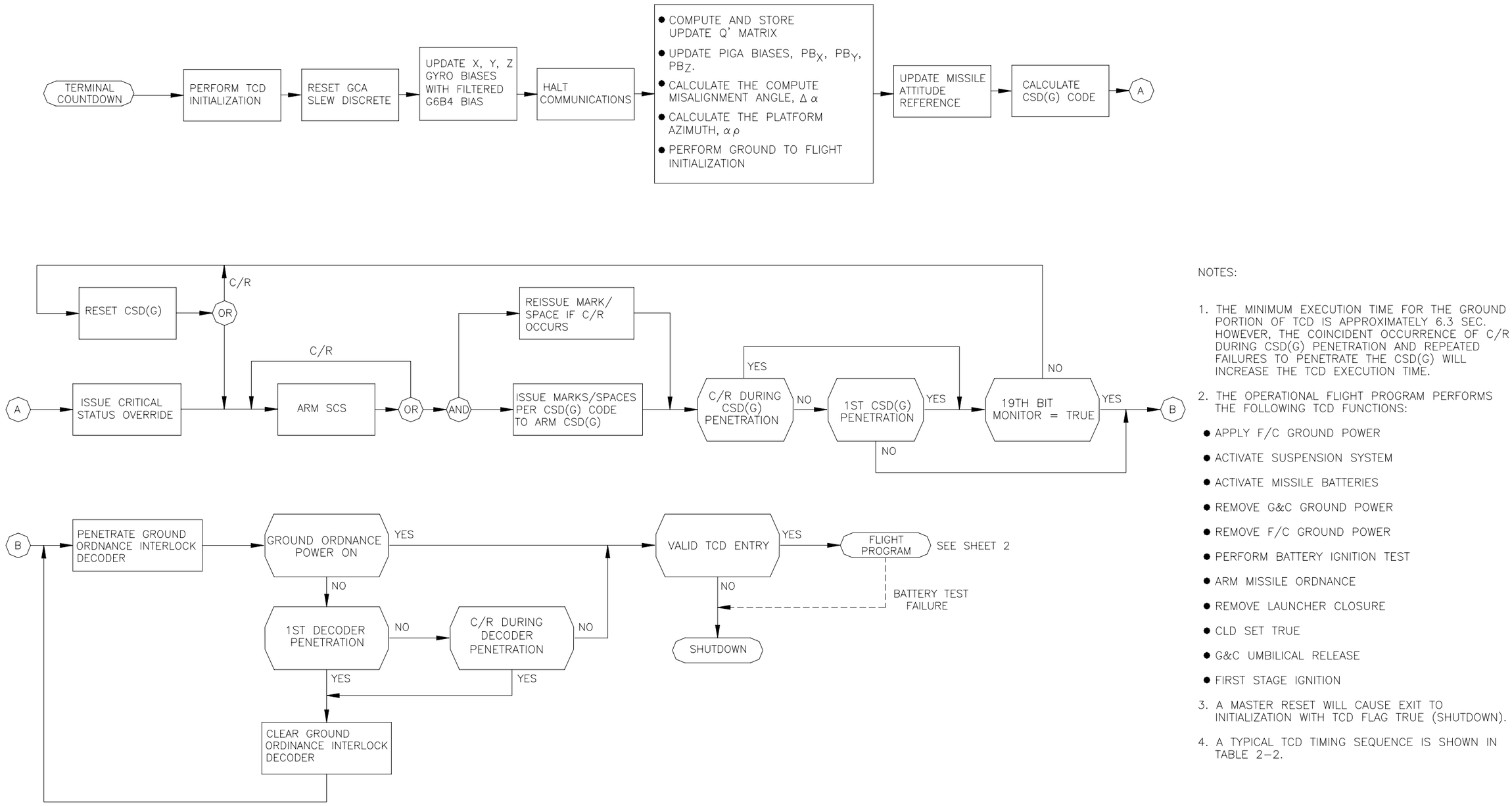


Figure 2-42. Strategic Alert PIGA Leveling Sequence (Sheet 2 of 2)



NOTES:

1. THE MINIMUM EXECUTION TIME FOR THE GROUND PORTION OF TCD IS APPROXIMATELY 6.3 SEC. HOWEVER, THE COINCIDENT OCCURRENCE OF C/R DURING CSD(G) PENETRATION AND REPEATED FAILURES TO PENETRATE THE CSD(G) WILL INCREASE THE TCD EXECUTION TIME.
2. THE OPERATIONAL FLIGHT PROGRAM PERFORMS THE FOLLOWING TCD FUNCTIONS:
   - APPLY F/C GROUND POWER
   - ACTIVATE SUSPENSION SYSTEM
   - ACTIVATE MISSILE BATTERIES
   - REMOVE G&C GROUND POWER
   - REMOVE F/C GROUND POWER
   - PERFORM BATTERY IGNITION TEST
   - ARM MISSILE ORDNANCE
   - REMOVE LAUNCHER CLOSURE
   - CLD SET TRUE
   - G&C UMBILICAL RELEASE
   - FIRST STAGE IGNITION
3. A MASTER RESET WILL CAUSE EXIT TO INITIALIZATION WITH TCD FLAG TRUE (SHUTDOWN).
4. A TYPICAL TCD TIMING SEQUENCE IS SHOWN IN TABLE 2–2.

MMT201_060K

SOURCE: S–133–19240

Figure 2-43. Terminal Countdown (Sheet 1 of 2)

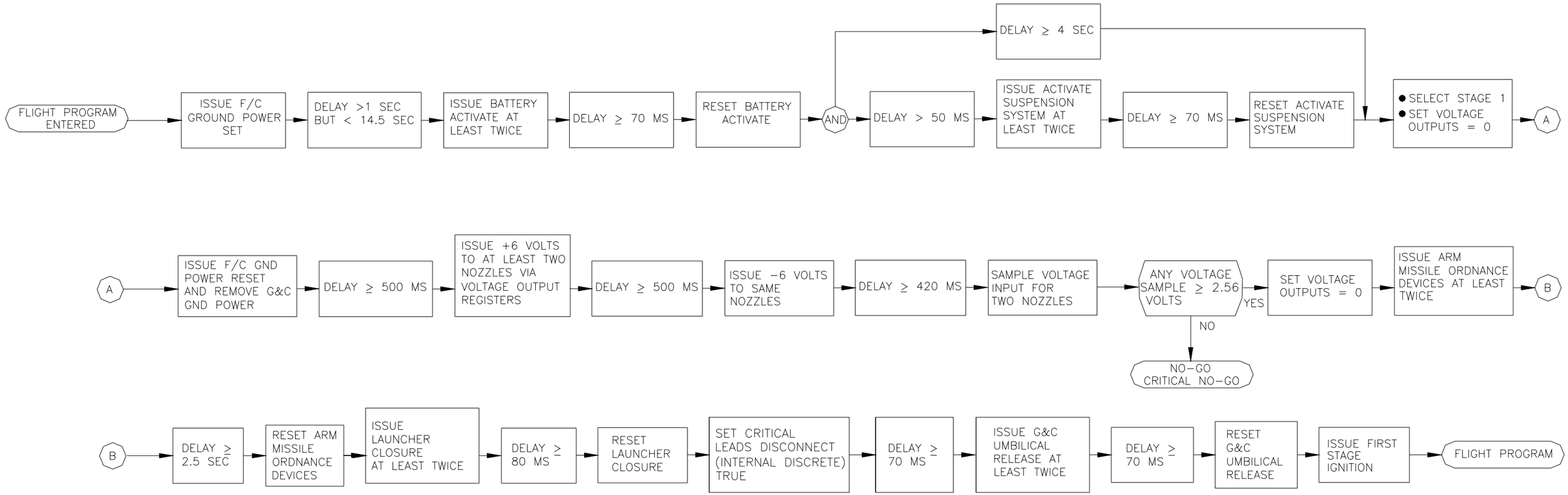
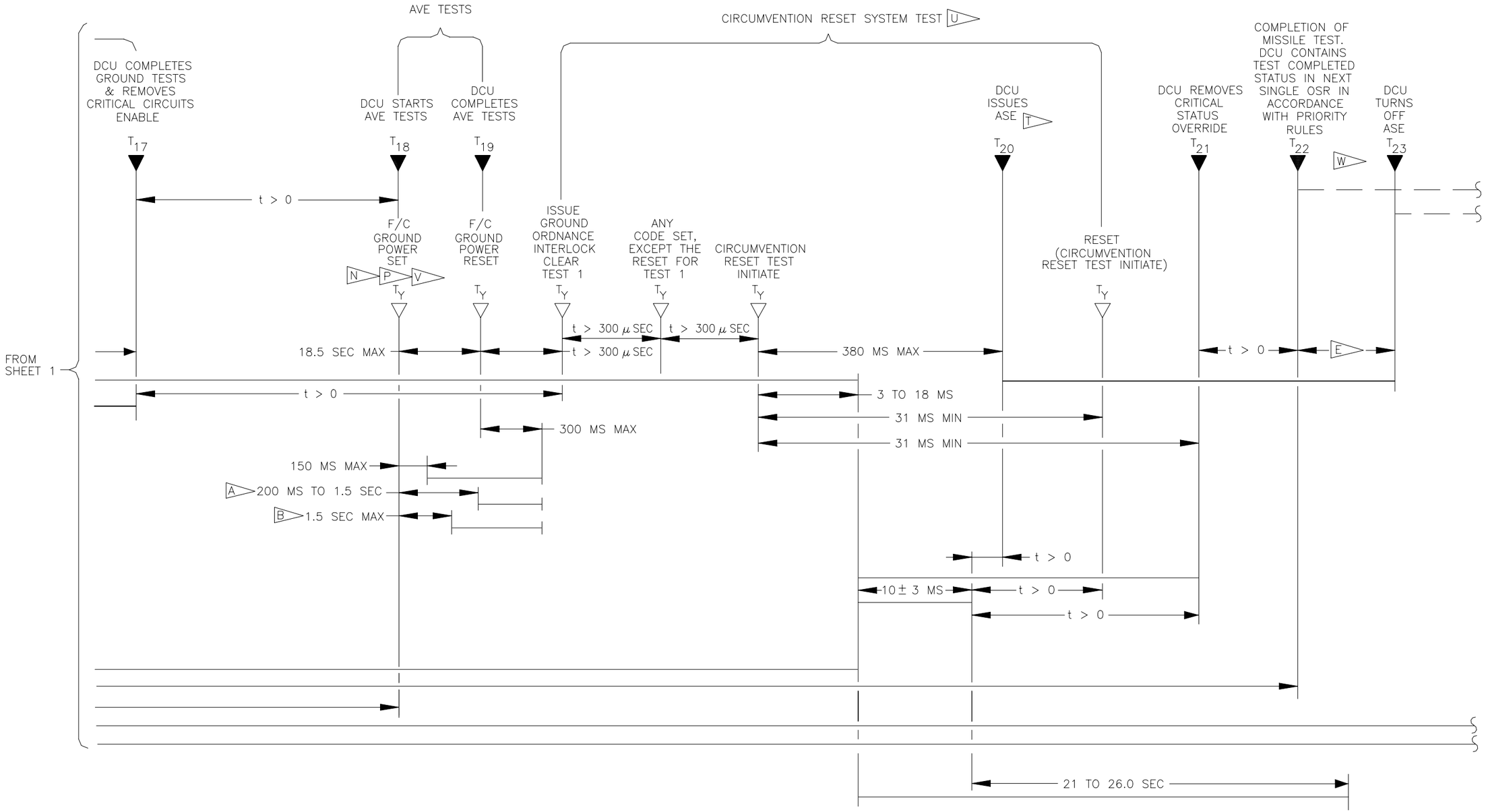


Figure 2-43. Terminal Countdown (Sheet 2 of 2)



SOURCE: ICD 25–65000, VOLUME IX

Figure 2-44. Missile Test Sequence – Sequential Timing Diagram (Sheet 2 of 2)

SECTION III - MGS OPERATION

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

LIST OF TABLES (Continued)

3-1. SCOPE. This section contains a general description of the guidance and control functions of the Minuteman III system. The hardware functions are performed by the Missile Guidance Set (MGS) and the Propulsion System Rocket Engine (PSRE). The software functions are performed by various operational tapes loaded into the MGS by the Cartridge Tape Unit (CTU). The capabilities of the C-MON equipment to issue commands and readout data is also described.

3-2. MISSILE GUIDANCE SET. The NS50A missile guidance set provides the stable ground reference and the flight inertial guidance for the LGM30G missile. It performs this task by use of a gyro stabilized inertial platform including appropriate sensing and control instruments, a digital computer, and associated electronics for interfacing among the MGS components and the downstage control elements. The MGS electronics are packaged primarily in the Missile Guidance Computer and the Missile Guidance Set Control. Figure 3-1 is an interface block diagram identifying the functional interfaces of the MGS. Figure 3-2 and Figure 3-3 show the physical layout of cables and units within the MGS.

3-2.1. Missile Guidance Computer (MGC). The MGC, a major component of the Minuteman (MM) III Guidance Replacement Program (GRP) Missile Guidance Set (MGS), is a programmable, radiation-hardened, missile-borne controller. It provides MIL-STD 1750 computational capability and input/output platform for ground and flight software to perform data handling, computation, communication, ordnance control, and flight control functions. The MGC is also referred to as the Digital Computer Unit (DCU) in this section and other sections. When programmed with ground and flight software, the MGC provides the following functions:

a. Performs real-time guidance and control (G&C) functions during ground and flight operations.

b. Communications with GRP MGSC or the Gyro Stabilized Platform (GSP) Inertial Measurement Unit (IMU), MK12/MK12A Reentry System (RS), ground equipment, Permutation Plug (PPlug), and telemetry subsystems external to the MGC.

c. Nozzle command generation and inner loop closure for thrust vector actuators on four missile stages.

d. Attitude Control System (ACS) and axial engine on-off command generation for post-boost maneuvering.

e. Ordnance select and fire sequence command generation.

f. Circumvention and Recovery (C&R) from upset due to external environments.

g. Self-test and monitoring of selected internal operations, including fault isolation.

h. Communications with the Advanced Inertial Measurement System (AIMS).

i. Stage II and Stage III roll valve commands for roll control.

j. Analog voltage commands for chaff motor speed (2) control.

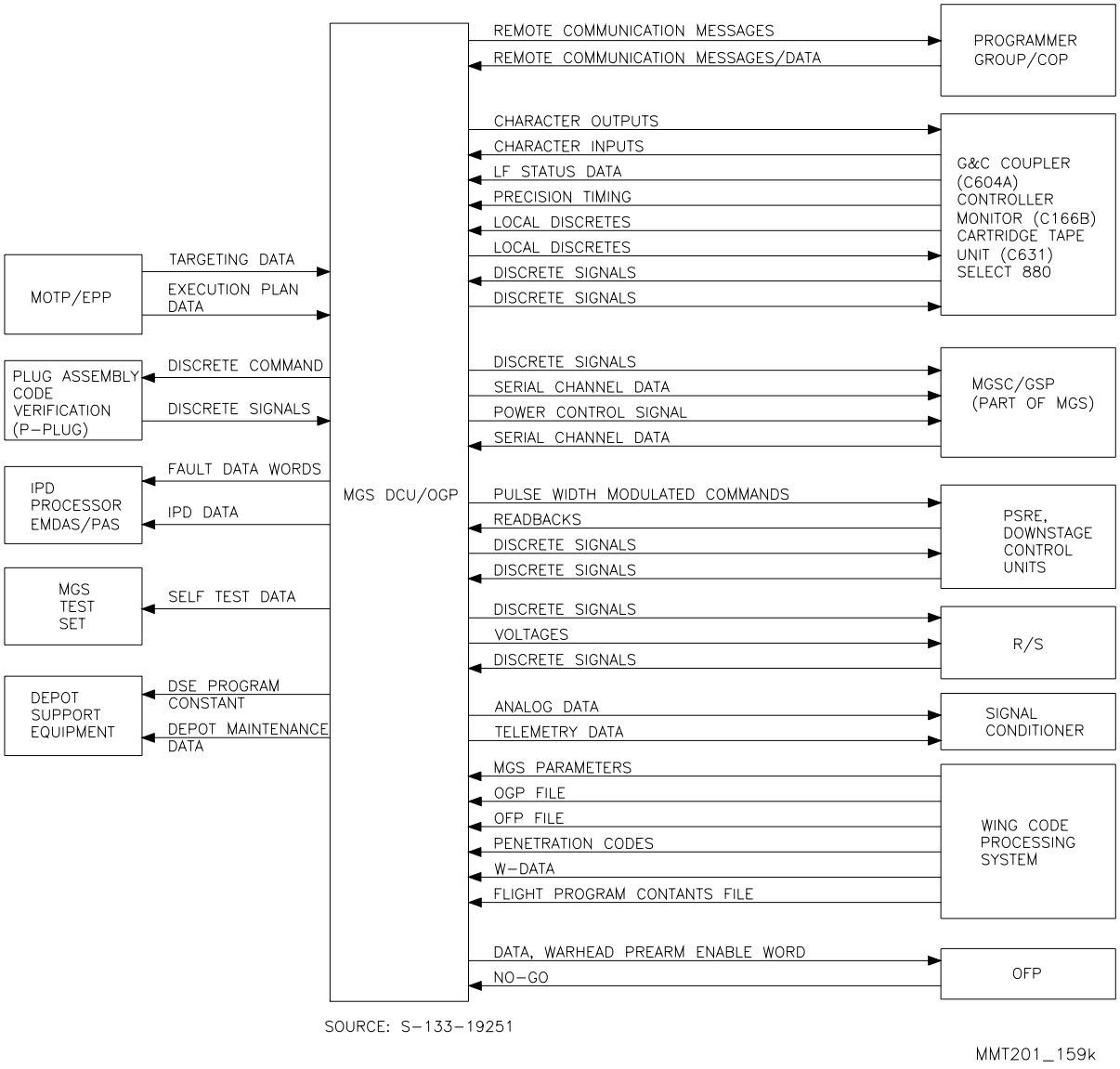


Figure 3-1. Interface Block Diagram

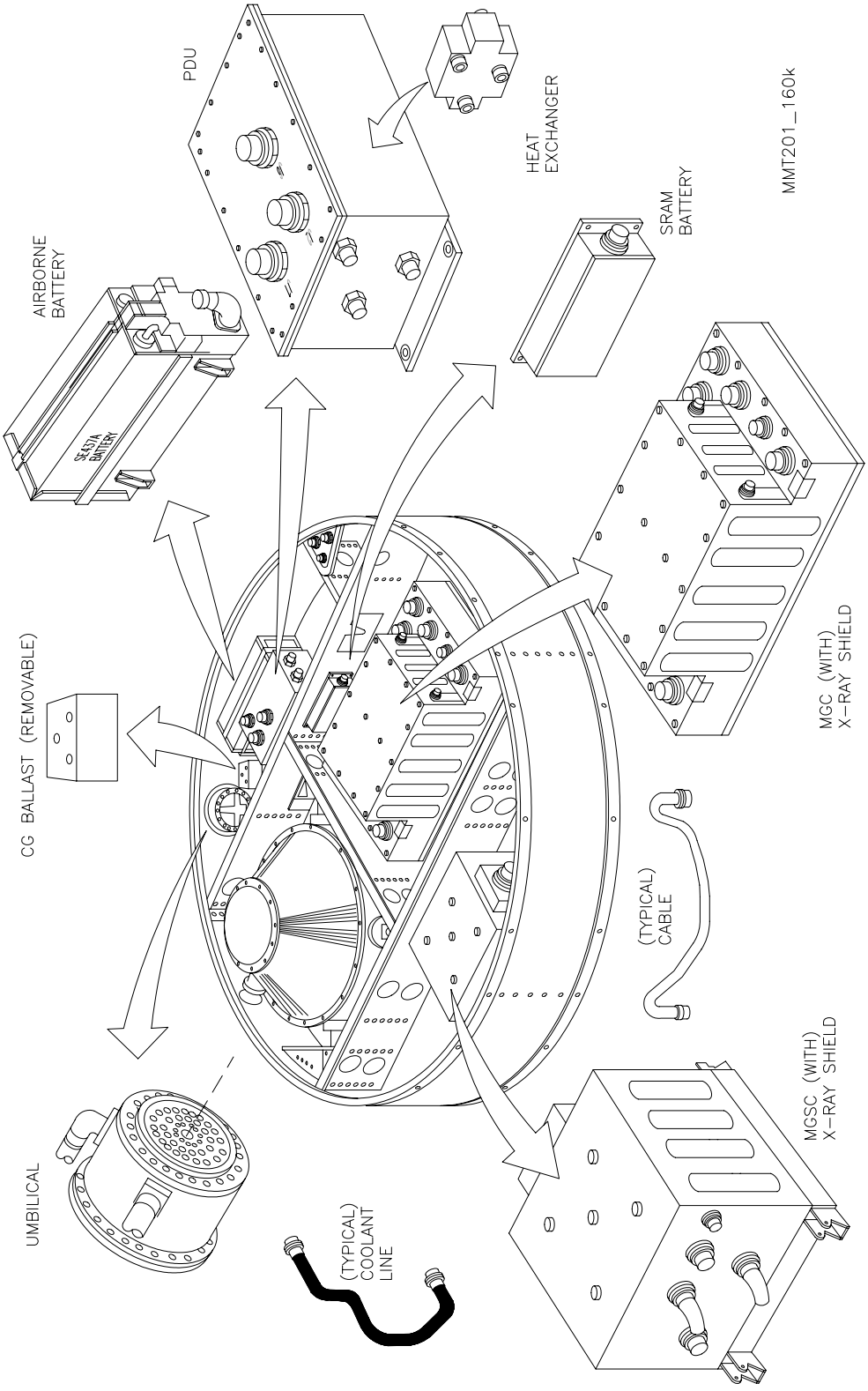


Figure 3-2. NS50 Guidance Set Components

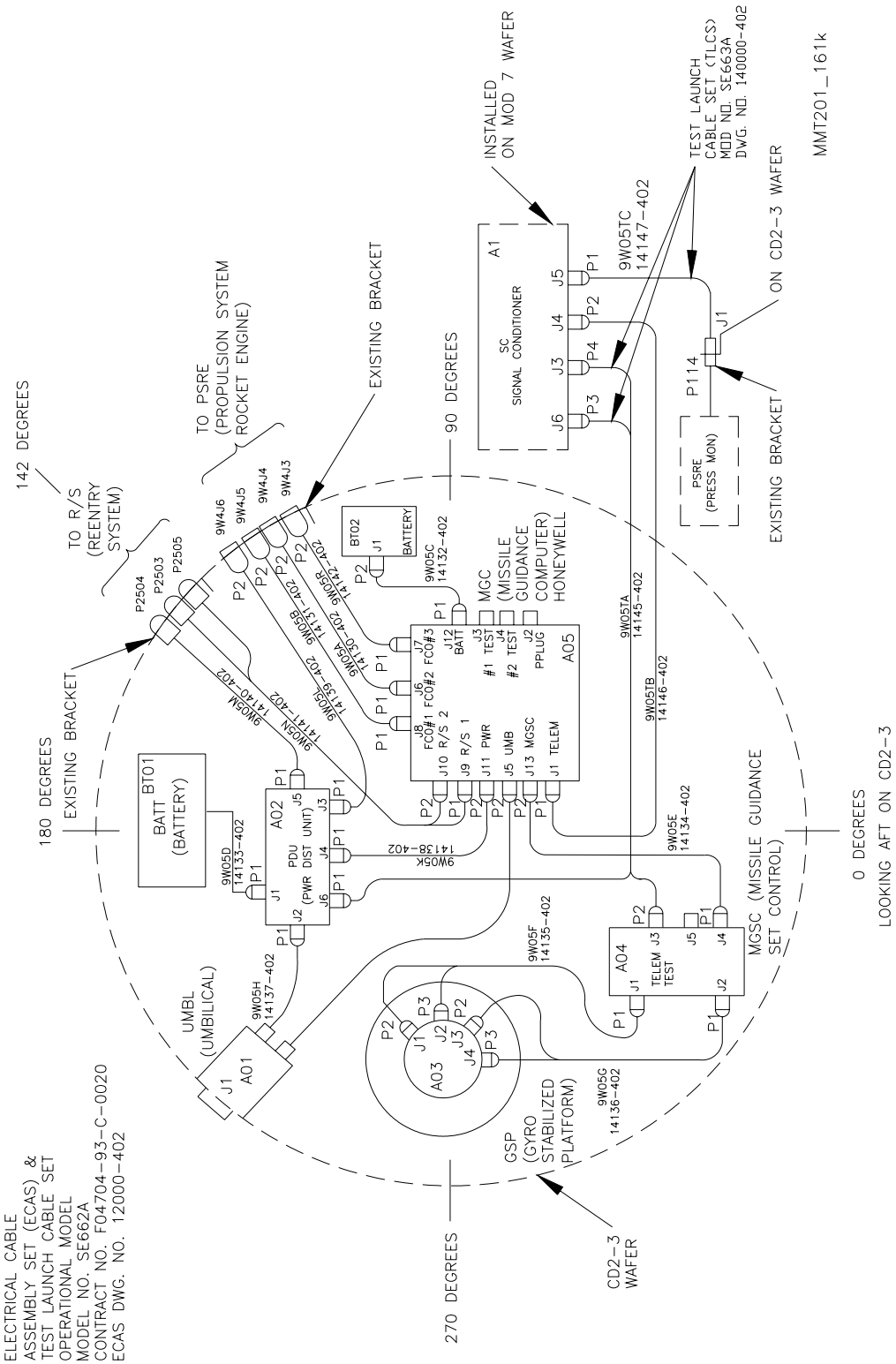


Figure 3-3. Electrical Cable Assembly Set Layout

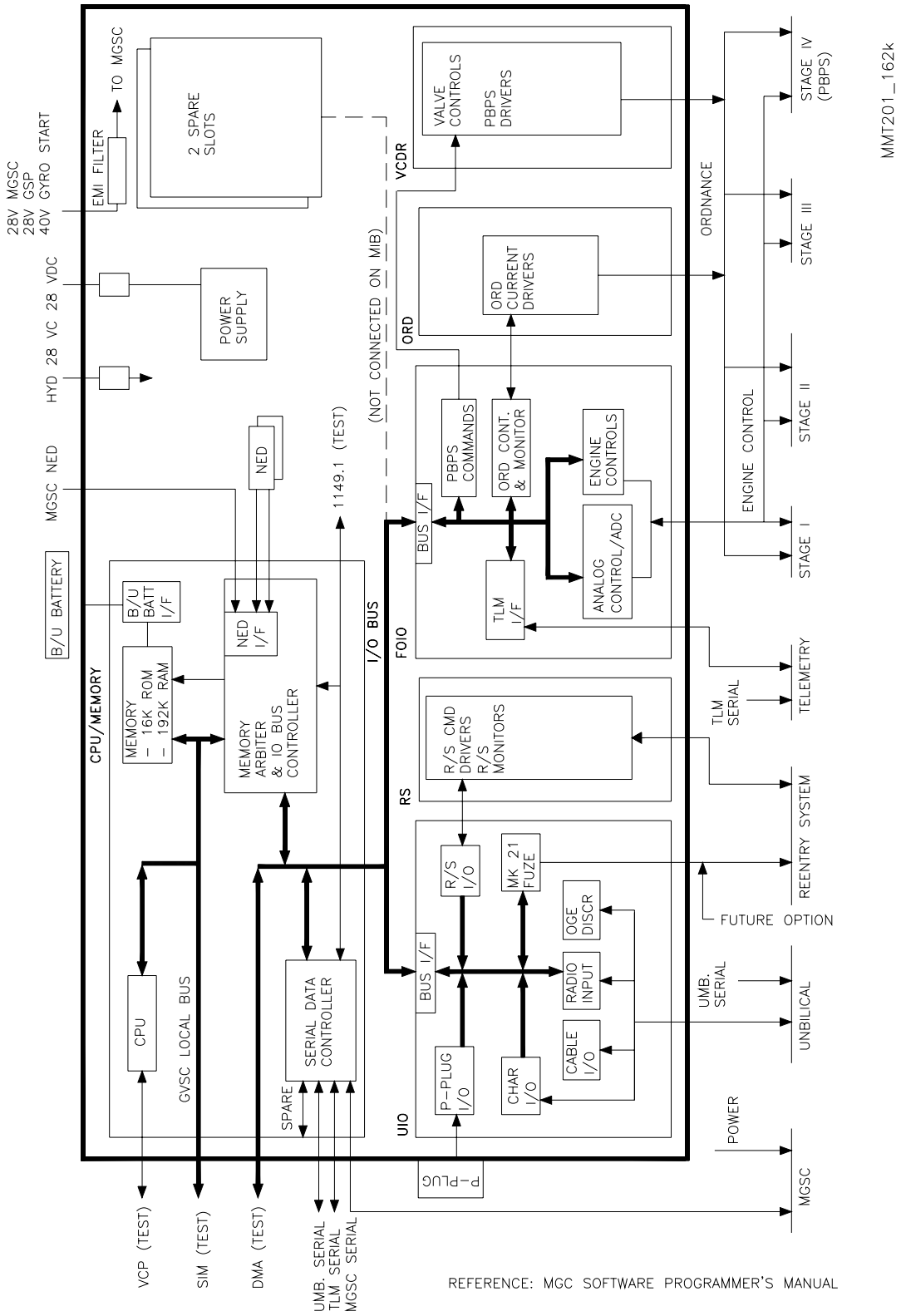


Figure 3-4. MGC Functional Block Diagram

3-2.2. MGC Architecture. A functional block diagram of the MGC is shown in Figure 3-4. Also shown in this figure is the interface of the MGC to its operating environment. Functionally, the MGC consists of eleven functional submodules where seven are connected to the time-multiplexed MGC I/O Bus.

Functionally, MGC submodules are grouped into three categories:

a. the MGC-1750A computer

b. the input/output devices peripheral to the computer, and

c. the serial-discrete-TLM channel.

The MGC-1750A computer consists of 1) the Central Processing Unit (CPU), 2) the main memory, and 3) the MGC I/O Bus and Memory Arbiter Control. The I/O devices are the seven MGC functions connected to the MGC I/O Bus: 1) the Test-DMA-Port Control, 2) the serial data channel A, 3) the serial data channel B, 4) the Flight Control, 5) the Ordnance Control, 6) the R/S Control, and 7) the OGE Communications Control. The Serial-Discrete-TLM Channel functions automatically without computer involvement.

Physically, the MGC-1750A computer functions reside on the same module as serial data channels A and B, and the Test-DMA-Port Control. This module is referred to as the Computer/Memory Module (CMM). The Flight and Ordnance control functions reside on the Flight/Ordnance Input/Output Module referred to as the FOIO. However, the ordnance current driver circuits and flight vector control current driver circuits reside on separate modules referred to as ORD and VCDR respectively. The OGE communication functions and the Reentry System (RS) control functions reside on the Umbilical Input/Output module referred to as the UIO. The RS discrete output drivers reside on a separate module referred to as the RS.

The Computer/Memory Module (CMM) communicates primarily with the Flight and Ordnance Input/Output Module (FOIO) and the Umbilical Input/Output Module (UIO) via the MGC Input/Out Bus. The FOIO communicates with the Ordnance Module (ORD) and the Flight Vector Control Module (VCDR) utilizing command discretes and monitor feedbacks. The UIO communicates to the RS Driver Module (RSD) via command discretes and monitors.

3-2.2.1. CPU Overview. The central processing unit, CPU is the controlling center of the MGC 1750A computer. Some of the principal functions performed by the CPU are as follows:

a. Reset actions as directed by the MGC mode control signals

b. Program instruction execution

c. Program interruption

d. Program trap/halt

e. Timer A & B facilities

f. Execution monitoring support

g. Detection of operating faults

h. Program input/output

As directed by program instructions, the CPU performs the following kinds of data operations:

a. Arithmetic operations on 16-bit and 32-bit two(s) complement integers

b. Arithmetic operations on 32-bit and 48-bit floating point numbers

c. Bit-wise logical operations on 16-bit and 32-bit words

3-2.2.2. Main Memory Overview. The main memory is composed of read-only memory (ROM), which consists of 16K locations of 16-bit words, (organized as 8K x 32 bits), and random-access memory (RAM), which consists of 192K locations where each location holds a 16-bit word (organized as 96K x 32 bits). The main memory holds the programs and their data for execution by the computer. Programs must reside in main memory before they can be executed by the computer. Programs can be built-in to ROM areas or can be loaded into writable RAM areas by the Virtual Control Processor (VCP) interface, the DMA interface, or the umbilical character input interface.

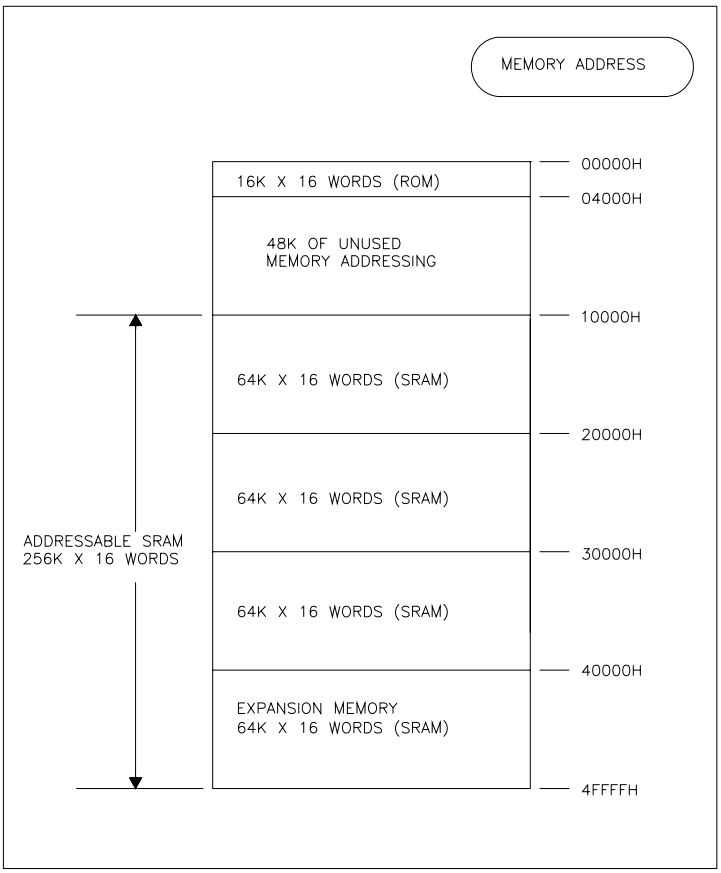
The main memory interfaces to the CPU and the Memory Interface Arbiter (MIA) via the CPU Local Bus. The MIA controls access to the Local Bus and arbitrates between the CPU and three I/O functions which may request access to memory. The I/O functions that access memory are the Serial Data Channels A and B, and the Test-DMA port.

The CPU reads and executes the program’s instructions from the main memory and may, in the course of instruction execution, transfer data to or from memory as specified by the instruction. Programs can also use the general CPU registers as well as memory to hold

data. These registers have faster access than the memory, but there are only sixteen such registers, so normally, only temporary data is held in the registers and the more permanent data is held in memory.

The serial data channels transfer blocks of data to and from the memory using DMA as initiated by programmed instruction. After being initiated, the transfer of each word of a block is performed independent of the program and the CPU.

The Memory mapping scheme (Figure 3-5) is partitioned into five 64K x 16 blocks. The 1st block contains 16K of addressable ROM and 48K of unused memory addressing. The 2nd, 3rd, 4th, and 5th (expanded memory) can be clamp protected if Circumvention & Recovery is implemented. (However, it is not utilized in current MGC configuration.)



SOURCE: MGC SOFTWARE PROGRAMMER'S MANUAL

MMT201_163k

Figure 3-5. Memory Map

The expanded-memory addressing feature of the 1750A Standard is used in the MGC to all memory addressing of up to 256K words which is significantly larger than the 64K words allowed for the physical address space.

3-2.2.3. Critical Leads Disconnect Flag. Critical Leads Disconnect (CLD) Flag allows software to control internal MIA functions, MGSC subsystems, NEP reset outputs, and logically isolate umbilical discrete functions. Figure 3-6 illustrates the functionality of CLD within the MIA and some of it external interfaces. The CLD flag is a bit in the CLD register. The bit in this register is initialized to zero after a power-on reset by its own unique hardware reset coming into the MIA. The state of CLD is used to inhibit system power resets and mode controls in flight. In order for this register to participate in functional resets it requires its own RC controlled power-on reset separate from the power-on reset. If NEP occurs while CLD is true, reset signals are issued to the UIO, FOIO, and MGSC.

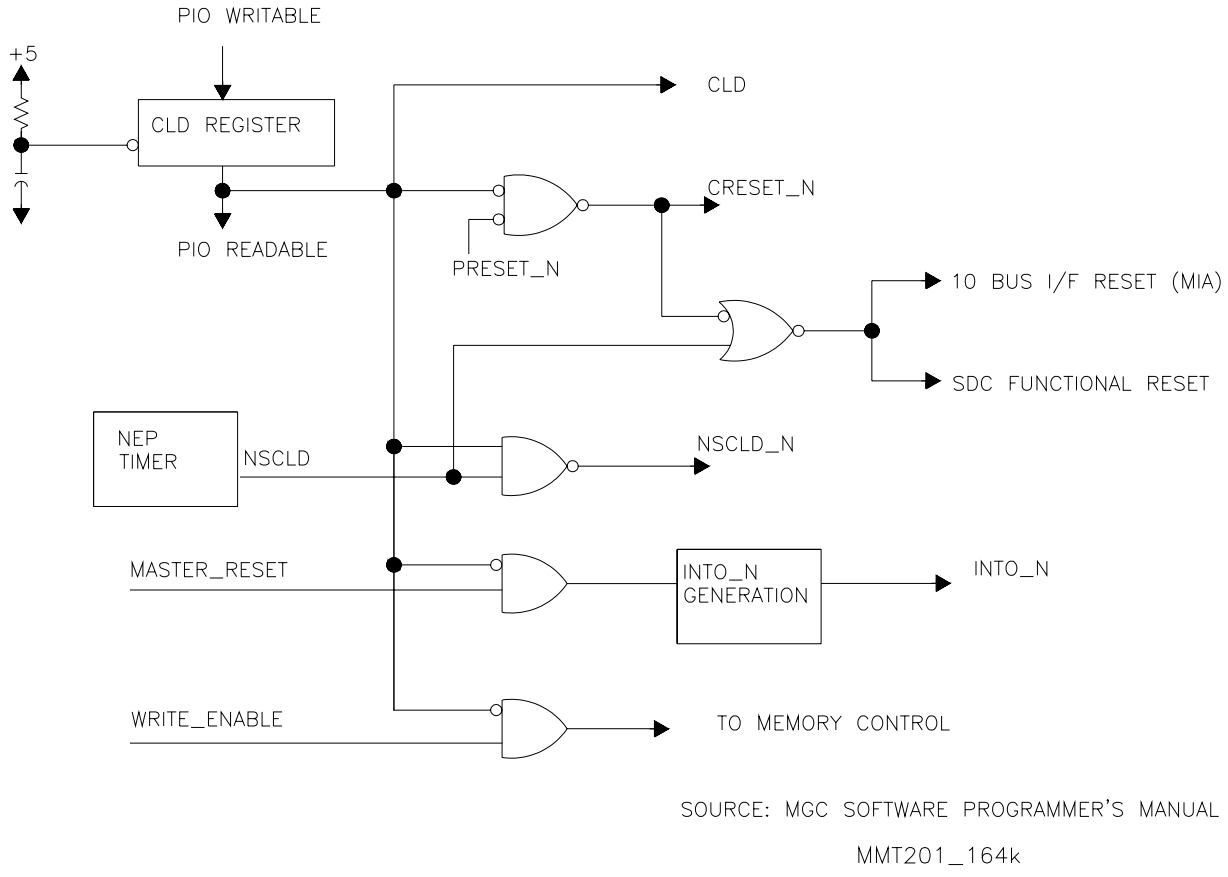


Figure 3-6. Critical Leads Disconnect

3-2.2.4. MGSC/Telemetry Serial Data I/O. The serial data communication link is a five wire asynchronous communication link that interfaces with the MGSC to control and monitor the MGSC/GSP subsystems and interfaces with the Telemetry System. The communication link uses a 16 bit word protocol and operates at a nominal frequency of 819.5 kHz. Data transfers are controlled by the software in the CPU and are planned to operate every 10 msec during both ground and flight operations. The MGC controls all data transfers.

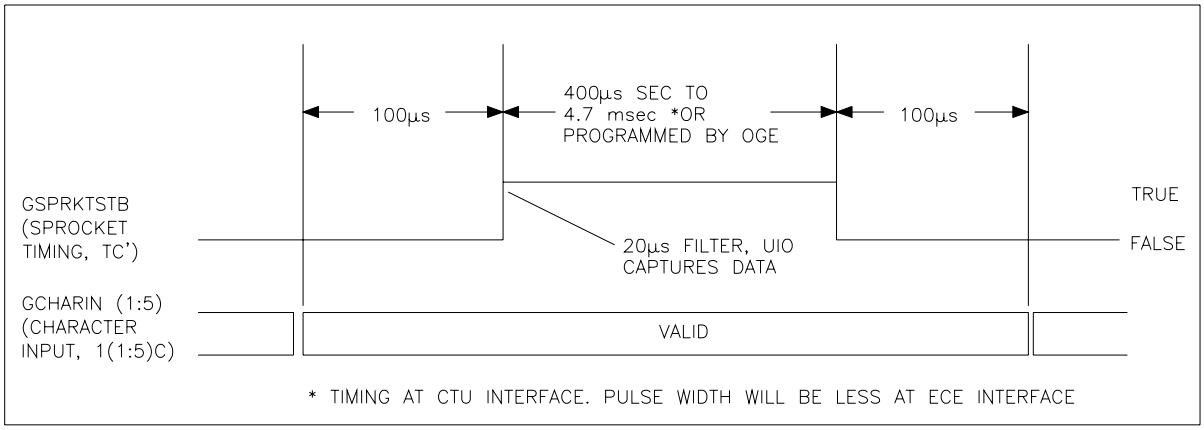
3-2.2.5. Flight Control I/O. The flight control interface provides the necessary low-power discrete signals (drivers) to control the attitude control valves and the roll control valves and provides the PWM signals to control the actuators and pintle valves. Actuator positions (analog feedbacks) are processed by the MGC hardware and provided as digital inputs to the software for use in the control loop calculations and for test purposes. The flight control system consists of both an inner loop and an outer loop which are both closed digitally by the software. The outer loop processes missile attitude and velocity data obtained from the MGSC/GSP over the serial communication link and generates the appropriate actuator position command to steer and to maintain a stable missile. The inner loop processes the actuator position command with the actuator feedback signal to generate a PWM actuator rate command to position the nozzle or injector pintle. The inner loop operates at a 2 msec rate with the outer loop processing performed at a 10 msec rate.

3-2.2.6. Ordnance I/O. The ordnance interface provides the necessary high-power signals to activate the Heated Bridge-Wire (HBW) ordnance devices on the missile. Each ordnance driver is individually commanded and provides a monitor that can be read by the appropriate PIO instruction, indicating delivery of output current. Two hazardous current monitor are also provided to indicate load current in excess of 100 milliamps into the safe load of the safety devices.

3-2.2.7. Reentry System I/O. The RS interface provides the necessary high powered signals and low-powered discretes to prearm the RVs, activate the batteries, start the HAF timers, deploy the chaff, and finally deploy the RVs. Twelve drivers are provided to perform the functions required by the MK12/MK12A RS. A thirteenth driver is also provided to issue the warhead prearm signal to the MK12A RS. Like the ordnance system, driver monitors and hazardous current monitors are provided. The RS interface also provides the chaff system analog voltage signals to control the chaff motor speed.

3-2.2.8. Umbilical I/O. The MGC interfaces with the OGE via the missile umbilical to obtain program load data and commands for controlling missile operation in the silo and provides status data for operator monitoring of the missile and the Launch Facility (LF). The character I/O interface is four bit parallel, with a parity bit and a timing bit, and operates at a maximum rate of 1600 characters per second. The cable I/O interface is a serial interface that operates at a maximum rate of 1600 bits/sec and can accommodate a variable message length of from 1 to 127 bits.

a. Character Input. The Character Input interface is used to load and verify programs and data from the Cartridge Tape Unit into the MGC memory. It is a six wire interface consisting of four data bit lines (I1c-I4c), a parity bit line (I5c), and a timing signal line (T'c). The four data bits represent a single character which consists of either a command or data as shown in Table 3-1. The OGE can send data at a rate up to 1600 characters per second. Refer to Figure 3-7 for character input timing.



SOURCE: MGC SOFTWARE PROGRAMMER'S MANUAL

MMT201_165k

Figure 3-7. Character Input Timing Diagram

Table 3-1. Cartridge Tape Unit DCU Commands and Characters

ITEM NO.	DESCRIPTION	UIO REGISTER (BITS 11-15)*
DCU Commands		
1	Block Fill	01000
2	Block Verify	11001
3	Fill	11010
4	Verify	01011
5	Compute	11100
6	Penetration Code Update	01101
7	Penetration Code Unlock	01110
8	Penetration Code Verify	11111
DCU Characters		
9	Hexadecimal Character 0 (0)	10000
10	Hexadecimal Character 1 (1)	00001
11	Hexadecimal Character 2 (2)	00010
12	Hexadecimal Character 3 (3)	10011
13	Hexadecimal Character 4 (4)	00100
14	Hexadecimal Character 5 (5)	10101
15	Hexadecimal Character 6 (6)	10110
16	Hexadecimal Character 7 (7)	00111
17	Hexadecimal Character 8 (8)	01000
18	Hexadecimal Character 9 (9)	11001
19	Hexadecimal Character A (10)	11010
20	Hexadecimal Character B (11)	01011
21	Hexadecimal Character C (12)	11100
22	Hexadecimal Character D (13)	01101
23	Hexadecimal Character E (14)	01110
24	Hexadecimal Character F (15)	11111

* Bit 11 set to give odd parity

SOURCE: S-133-19251

b. Launch facility status monitor inputs. The OGP monitors inputs which are multiplexed into the DCU through the Guidance and Control Coupler (C604A) on the umbilical status monitor lines 1, 2, 3, 4 and 5 of the Umbilical Input/Output (UIO) discrete input monitor #1 (Bits 15 through 11). In order to sample any particular status monitor, the OGP is required by the C604A to issue the appropriate character output code pair of Table 3-2 and then execute a UIO Discrete Input instruction to sample the Umbilical Status. When the Multiplexer Test Mode is not in effect, the 5 bits in Bits 11 through 15 of the UIO Discrete Input are specified by Table 3-2 (LF Status Inputs (Normal)). When the Multiplexer Test Mode is in effect by issuance of the Multiplexer Test Command (Character Output 6-9), the 5 bits in the UIO Discrete Input are specified by Table 3-3 (LF Status Inputs (Multiplexer Test Mode)). The Multiplexer Test Mode is exited by issuing the Multiplexer Test Command Reset (Character Output 6-8).

Table 3-2. LF Multiplexer Status Inputs (Normal)

CHARACTER OUTPUT	STATUS SET AND BIT NO.	MULTIPLEXER STATUS INPUT DESCRIPTION		UIO REGISTER UMBILICAL STATUS NO.
		SYMBOL	NAME [SYSTEM]	
0-0	A1	GRDORDPRON	Ground Ordnance Power On Monitor	1
	A2	ARGDORDOMN	Any Ground Ordnance Driver On Monitor	2
	A3	CSDG19BMON	CSD(G) 19th Bit Monitor	3
	A4	SDUALARMON	SDU Alarm Monitor	4
	A5	CR_HW_IND	Circumvention Reset Indicator	5
0-1	B1	SCS_ARMED	SCS Armed Monitor	1
	B2	SCSSAFEMON	SCS Safe Monitor	2
	B3	ALCCACCMON	ALCC Access Allowed	3
	B4	CLRTXT_MON	Clear Text Allowed	4
	B5	AUXSTENMON	Auxiliary Status Enable	5
0-2	C1	RSGPWRONMN	R/S Ground Power On Monitor	1
	C2	RSMONRDYMN	R/S Monitor Ready Signal	2
	C3	(None)	Spare	3
	C4	(None)	Spare	4
	C5	(None)	Spare	5
0-3	D1	(None)	Spare	1
	D2	(None)	Spare	2
	D3	(None)	Spare	3
	D4	(None)	Spare	4
	D5	(None)	Spare	5

Table 3-2. LF Multiplexer Status Inputs (Normal) (Continued)

CHARACTER OUTPUT	STATUS SET AND BIT NO.	MULTIPLEXER STATUS INPUT DESCRIPTION		UIO REGISTER UMBILICAL STATUS NO.
		SYMBOL	NAME [SYSTEM]	
0-4	E1	AVE_NG_MON	AVE No-Go	1
	E2	SCSTSTCDMN	SCS Test Command	2
	E3	PGMONFLMON	P/G Monitor Failure	3
	E4	CSDGHOMEMN	CSD(G) Home	4
	E5	(None)	Spare	5
0-5	F1	CPLRTSTMON	Coupler Test	1
	F2	CSO_MON	Critical Status Override	2
	F3	AVE_NG_MON	AVE No-Go	3
	F4	CPLRNG_MON	Coupler No-Go	4
	F5	COTEST_MON	CO Code Interface Test	5
0-6	G1	RSOUTDATA	R/S Output Data	1
	G2	CSDMSPCSTP	CSD(M) Space and Step	2
	G3	CSDMMRKSTP	CSD(M) Mark and Step	3
	G4	LOCAL_MON	Local Monitor	4
	G5	EN_WRT_MON	Enable Write	5
0-7	H1	CSDM_HOME	CSD(M) Home Monitor	1
	H2	(None)	Spare	2
	H3	CSDMDRV_EN	CSD(M) Drive Enable	3
	H4	CSDM24BTMN	CSD(M) 24th Bit Monitor	4
	H5	CSDMRSTMON	CSD (M) Reset	5
0-8	J1	(None)	Spare	1
	J2	(None)	Spare	2
	J3	(None)	Spare	3
	J4	(None)	Spare	4
	J5	(None)	Spare	5
0-9	K1	(None)	Spare	1
	K2	(None)	Spare	2
	K3	(None)	Spare	3
	K4	(None)	Spare	4
	K5	(None)	Spare	5
0-10	L1	CSDGMARKMN	CSD (G) Mark	1
	L2	CSDGSPACMN	CSD (G) Space	2
	L3	(None)	Spare	3
	L4	(None)	Spare	4
	L5	ACTSUSPSYS	Activate Suspension System	5
0-11	M1	BATACTMON	Battery Activate	1
	M2	ARMORDEVMN	Arm Missile Ordnance Devices	2
	M3	REMLUCHCLM	Remove Launcher Closure	3
	M4	GCUMBRELMN	Critical Leads Disconnect G&C Umbilical Release, and Retract	4
	M5	STG1IGMON	First Stage Ignition	5

Table 3-2. LF Multiplexer Status Inputs (Normal) (Continued)

CHARACTER OUTPUT	STATUS SET AND BIT NO.	MULTIPLEXER STATUS INPUT DESCRIPTION		UIO REGISTER UMBILICAL STATUS NO.
		SYMBOL	NAME [SYSTEM]	
0-12	N1	(None)	Spare	1
	N2	(None)	Spare	2
	N3	(None)	Spare	3
	N4	(None)	Spare	4
	N5	(None)	Spare	5
0-13	P1	STARTUP_MN	Startup Indicator	1
	P2	DISABLEDIS	Disable Discretes	2
	P3	(None)	Spare	3
	P4	(None)	Spare	4
	P5	(None)	Spare	5
0-14	R1	KEYBOARD1	Keyboard Entry 1	1
	R2	KEYBOARD2	Keyboard Entry 2	2
	R3	KEYBOARD4	Keyboard Entry 4	3
	R4	KEYBOARD8	Keyboard Entry 8	4
	R5	(None)	Spare	5
0-15	S1	(None)	Spare	1
	S2	(None)	Spare	2
	S3	(None)	Spare	3
	S4	(None)	Spare	4
	S5	(None)	Spare	5

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Table 3-3. LF Multiplexer Status Inputs (Multiplexer Test Mode)

CHARACTER OUTPUT	SET	MULTIPLEXER TEST PATTERNS UIO REGISTER - UMBILICAL STATUS NO.				
		5	4	3	2	1
0-0	A	1	0	0	0	0
0-1	B	1	0	0	0	1
0-2	C	1	0	0	1	0
0-3	D	1	0	0	1	1
0-4	E	1	0	1	0	0
0-5	F	1	0	1	0	1
0-6	G	1	0	1	1	0
0-7	H	1	0	1	1	1
0-8	J	0	1	0	0	0
0-9	K	0	1	0	0	1
0-10	L	0	1	0	1	0
0-11	M	0	1	0	1	1
0-12	N	0	1	1	0	0
0-13	P	0	1	1	0	1
0-14	R	0	1	1	1	0
0-15	S	0	1	1	1	1

SOURCE: S-133-19251

c. Discrete inputs. The OGP shall interpret discrete input signals as specified in Table 3-4. Data bit 15 is the Least Significant Bit (LSB) and bit 0 is the Most Significant Bit (MSB).

For detailed bit definitions of the discrete input registers listed in Table 3-4, see the Software Requirements Specification for the OGP, S-133-19251, section 3.1.

Table 3-4. Programmed Input/Output (PIO) Read Address Assignments

COMMAND (HEX)	SYMBOL	OPERATION	DESCRIPTION
			CPU XIO -
A008	CPUDO	Read	CPU Discrete Output Register
A009	CPUDISCRIN	Read	CPU Discrete Input Register
			Memory Interface Arbiter (MIA) PIOs -
8080	MIACONFREG	Read	MIA Configuration Register
8081	EWADDRBNDY	Read	Enable Write Address Boundary Register
8082	MIAINPMSK	Read	MIA Interrupt Mask Register
8083	CLDREG	Read	Critical Leads Disconnect Register
8084	MIAERRSTAT	Read	MIA Error/Status Register
8085	NEPTIMEREG	Read	Nuclear Event Protection (NEP) Timer Holding Register
8086	CNRADDCLMP	Read	Circumvention and Recovery (C&R) Address Clamp Register
8087	MISSNTIMER	Read	Mission Timer
8088-80FF	(None)	N/A	not used
			Serial Data Channel (SDC) PIOs -
8100	SDCCHPSTA	Read	SDC Chip Status Register
8101	SDCMSKREG	Read	SDC Interrupt Mask Register
8102	CHAWCLADDR	Read	Channel A Word Count/Address Low Register
8103	CHAHIADDR	Read	Channel A Address High Register
8104	CHACONFREG	Read	Channel A Configuration Register
8105	SDCCHAERR	Read	Channel A Read Error Register
8106	CHAWCLADDC	Read	Channel A Word Count/Address Low Counter
8107	CHAHIADDC	Read	Channel A Address High Counter
8108	CHBWCLADDR	Read	Channel B Word Count/Address Low Register
8109	CHBHIADDR	Read	Channel B Address High Register
810A	CHBCONFREG	Read	Channel B Configuration Register
810B	SDCCHBERR	Read	Channel B Read Error Register

Table 3-4. Programmed Input/Output (PIO) Read Address Assignments (Continued)

COMMAND (HEX)	SYMBOL	OPERATION	DESCRIPTION
810C	CHBWCLADDR	Read	Channel B Word Count/Address Low Counter
810D	CHBHIADDC	Read	Channel B Address High Counter
			Umbilical Input/Output (UIO) PIOs -
8180	CAIOSTATUS	Read	Cable I/O Control Word
8181	CAIOHLDREG	Read	Cable I/O Holding Register
8182	CHAROUT	Read	Character Output Control Word
8183	UIOINPMSK	Read	UIO Interrupt Mask Register
8184	RSDIMON	Read	Reentry System (RS) Discrete Input Monitors
8185	UIODIMON1	Read	UIO Discrete Input Monitors #1
8186	MK21DATA1	Read	MARK 21 RS Data Word #1 Register
8187	MK21DATA2	Read	MARK 21 RS Data Word #2 Register
8188	MK21DATA3	Read	MARK 21 RS Data Word #3 Register
8189	PPLUGREG1	Read	Penetration Plug (P PLUG) Discrete Input Word Register #1
818A	PPLUGREG2	Read	P PLUG Discrete Input Word Register #2
818B	PRECTIME1	Read	Precision Time Register #1 (bit 16 - bit 31)
818C	PRECTIME2	Read	Precision Time Register #2 (bit 0 - bit 15)
818D	UIOPSEREG	Read	UIO Peculiar Support Equipment (PSE) Test Register
818E	UIOPENDINP	Read	UIO Pending Interrupt Register
818F	UIODOREG	Read	UIO Discrete Output Register
8190	RADIOBIT	Read	Radio Input Bit
8191	TIMERC	Read	Timer C Counter
8192	TIMERD	Read	Timer D Counter
8193	CHARINREG	Read	Character Input Register
8194	UIODIMON2	Read	UIO Discrete Input Monitors #2

Table 3-4. Programmed Input/Output (PIO) Read Address Assignments (Continued)

COMMAND (HEX)	SYMBOL	OPERATION	DESCRIPTION
8196	IRTI1CNTR	Read	Inertial Measurement Unit Real Time Interrupt (IRTI) Counter #1 (bits 16 - 31)
8197	IRTI2CNTR	Read	IRTI Counter #2 (bits 0-15)
			Flight Control and Ordnance Input/Output (FOIO) PIOs -
8200	TVCAES1NZ1	Read	Thrust Vector Control (TVC) Actuator Error Signal (AES), Stage 1, Nozzle 1 Command
8201	TVCAES1NZ2	Read	TVC AES, Stage 1, Nozzle 2 Command
8202	TVCAES1NZ3	Read	TVC AES, Stage 1, Nozzle 3 Command
8203	TVCAES1NZ4	Read	TVC AES, Stage 1, Nozzle 4 Command
8204	TVCAES2IJ1	Read	TVC AES, Stage 2, Injector 1 Command
8205	TVCAES2IJ2	Read	TVC AES, Stage 2, Injector 2 Command
8206	TVCAES2IJ3	Read	TVC AES, Stage 2, Injector 3 Command
8207	TVCAES2IJ4	Read	TVC AES, Stage 2, Injector 4 Command
8208	STG2ROLCMR	Read	Stage 2 Roll Command
8209	TVCAES3IJ1	Read	TVC AES, Stage 3, Injector 1 Command
820A	TVCAES3IJ2	Read	TVC AES, Stage 3, Injector 2 Command
820B	TVCAES3IJ3	Read	TVC AES, Stage 3, Injector 3 Command
820C	TVCAES3IJ4	Read	TVC AES, Stage 3, Injector 4 Command
820D	STG3ROLCMR	Read	Stage 3 Roll Command
820E	FCSELEMRB	Read	Flight Control Select/Event Markers
8210	PBPSAESPTH	Read	PBPS AES Pitch
8211	PBPSAESYAW	Read	PBPS AES Yaw
8212	PBPSAXATIT	Read	PBPS Axial/Attitude Command
8213	FOIOPSEREG	Read	FOIO PSE Test Register
8220	ORDENA	Read	Ordnance Enable
8221	ORDCMDS	Read	Ordnance Commands
8230	POSFDBK	Read	Position Feedback

Table 3-4. Programmed Input/Output (PIO) Read Address Assignments (Continued)

COMMAND (HEX)	SYMBOL	OPERATION	DESCRIPTION
8231	STGAUXMON1	Read	Stage Auxiliary Monitor 1
8232	STGAUXMON2	Read	Stage Auxiliary Monitor 2
8233	STGAUXMON3	Read	Stage Auxiliary Monitor 3
8234	STGAUXMON4	Read	Stage Auxiliary Monitor 4
8240	PBPSVALVST	Read	PBPS Valve Status
8241	DNORDSTAT	Read	Downstage Ordnance Status
8242	PBPSORDST	Read	PBPS Ordnance Status
8243	CSDHYDPRST	Read	CSD/Hydraulic Pressure Status
8244	FAULTMON	Read	FOIO Fault Monitor Status

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d. Serial channel input data. The data symbols and descriptions of the MGSC to DCU data are defined in Table 3-5.

(1) The OGP will load, at a 819.5 kHz rate, the MGSC to DCU serial channel data, specified in MGSC to DCU serial channel words 1 through 17 in Table 3-6, into one block of contiguous memory identified as IIW_BLK. (Note: that the highest numbered bit is the LSB.)

(2) A predetermined data validity lag exists for some of the input data. Table 3-5 defines where each input element is computed/valid in the MGSC. The column titled validity time is the time since the last CIRTI. This shows that the largest lag prior to the next CIRTI is one msec. Those parameters not specifically noted in the column are valid at the time of the read.

Table 3-5. MGSC to DCU Serial Channel Input Data

ITEM NO.	SYMBOL	DESCRIPTION	SIZE	LSB	VALIDITY TIME (MSEC)
1	ACINSTRO	AC Instrument On	1	N/A	N/A
2	CLD_MON	Critical Leads Disconnect Monitor Feedback	1	N/A	N/A
3	CMDENAMON	MGSC Command Enable Monitor Feedback	1	N/A	N/A
4	CURGCOVRO	Current GC Overvoltage On	1	N/A	N/A
5	CURGCPWRON	Current GC Power On	1	N/A	N/A
6	CURGCAMOD	Current GCA Mode Controls	1	*	N/A
7	CURPIGAMOD	Current PIGA Mode Controls	1	*	N/A
8	CURPIGPWRO	Current PIGA 800 Hz Power On	1	N/A	N/A
9	CURPLATMOD	Current Platform Mode Controls	1	*	N/A
10	DD_MON	Hardware Disable Discrete Monitor Feedback	1	N/A	N/A
11	G6GT_MON_A	Yaw, Pitch and Roll Gyro Torque Monitor (X, Y and Z) - A	3x1	N/A	N/A
12	G6GT_MON_B	Yaw, Pitch and Roll Gyro Torque Monitor (X, Y and Z) - B	3x1	N/A	N/A
13	GBL_CRT_PH	Yaw, Pitch and Roll Gimbal Current Phase (X, Y and Z)	3x1	N/A	Same as GIBLET
14	GBL_DIREC	Yaw, Pitch and Roll Gimbal Direction (X, Y and Z)	3x1	N/A	Same as GIBLET
15	GBLDEM_PO	Yaw, Pitch and Roll Gimbal Demod Pickoff (X, Y and Z)	3x1	2 arcsec	9.1 (X) 9.2 (Y) 9.0 (Z)
16	GBLINC_SUM	Yaw, Pitch and Roll Gimbal Incremental Sum (X, Y and Z)	3x1	1 gim cnt	Same as GIBLET
17	GC_PO_MON	GC Pickoff Monitor	1	N/A	N/A
18	GCA_CRT_PH	GCA Current Phase	1	*	Same as SELECT_ADC
19	GCA_DIREC	GCA Direction	1	N/A	Same as SELECT_ADC
20	GCA_OR_MON	GCA Overrate Monitor	1	N/A	N/A
21	GCAINC_SUM	GCA Incremental Sum	1	1 oer cnt	Same as SELECT_ADC
22	GCASLCNTLR	GCA Slew Control Readback	1	N/A	N/A
23	GCCURSLCNL	GCA Current Slew Control	1	*	N/A

Table 3-5. MGSC to DCU Serial Channel Input Data (Continued)

ITEM NO.	SYMBOL	DESCRIPTION	SIZE	LSB	VALIDITY TIME (MSEC)
24	GCNULLCTR	GCA Null Counter	1	1 artificial null (see Table 3-7)	N/A
25	GIBLET	X, Y and Z Giblet	3x1	*	9.7 (X) 9.8 (Y) 9.6 (Z)
26	LD_X_MON	Level Detector X-Axis Monitor	1	N/A	N/A
27	LD_Y_MON	Level Detector Y-Axis Monitor	1	N/A	N/A
28	LVLSL1_MON	Monitor Feedback	1	N/A	N/A
29	LVLSL2_MON	Monitor Feedback	1	N/A	N/A
30	MTRVLTMON	Motor Voltage Monitor	1	*	N/A
31	MTRVMONSLT	Motor Voltage Monitor Select	1	*	N/A
32	PG_CRT_PH	X, Y and Z PIGA Current Phase	3x1	*	Same as PIGLET
33	PG_DEM_PO	X, Y and Z PIGA Demod Pickoff	3x1	*	9.2 (X) 9.1 (Y) 9.0 (Z)
34	PG_DIREC	X, Y and Z PIGA Direction	3x1	N/A	Same as PIGLET
35	PGINC_SUM	X, Y and Z PIGA Incremental Sum	3x1	.12 ft/sec	Same as PIGLET
36	PG_TFLP	X, Y and Z PIGA Time From Last Pulse	3x1	31.25 µsec	Same as PIGLET
37	PIGCPL_MON	Inv. 4.8 PIGA Couple	1	N/A	N/A
38	PIGLET	X, Y and Z Piglets	3x1	*	9.5 (X) 9.4 (Y) 9.3 (Z)
39	PLAT_PSMON	Platform Pressure Monitor	1	N/A	N/A
40	SAR_MON	Monitor Feedback	4	N/A	N/A
41	SELECT_ADC	Selectable ADC Data	1	.078125 volts**	9.9
42	SRVOENAMON	MGSC Servo Enable Monitor Feedback	1	N/A	N/A
43	V40ST_MON	40V Gyro Hi-start	1	N/A	N/A

* These parameters are not used by the OGP so the LSB has not been provided.
** This LSB is for the XY and YZ DC Speed Controls, the only SELECT_ADC items used by the OGP.

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Table 3-6. MGSC to DCU Serial Channel Description (IIW_BLK)

BITS	WORD 1	WORD 2	WORD 3	WORD 4	WORD 5
0	PG_TFLP(1)	PG_TFLP(2)	PG_TFLP(3)	GBLDEM_PO(3) or PG_DEM_PO(3)	GBLDEM_PO(2) or PG_DEM_PO(1)
1					
2					
3					
4					
5					
6					
7					
8				GBLDEM_PO(1) or PG_DEM_PO(2)	G6GT_MON_A(1)*
9	CLD_MON	ACINSTRO	PG_DIREC(1)		G6GT_MON_B(1)*
10	GCNULLCTR (see Table 3-7)	V40ST_MON	PG_DIREC(2)		G6GT_MON_A(2)*
11		PLAT_PSMON	PG_DIREC(3)		G6GT_MON_B(2)*
12		LD_X_MON	GCA_DIREC		G6GT_MON_A(3)*
13	GCCURSLCNL	LF_Y_MON	GBL_DIREC(1)		G6GT_MON_B(3)*
14		GC_PO_MON	GBL_DIREC(2)		LVLSL1_MON
15		GCA_OR_MON	GBL_DIREC(3)		LVLSL2_MON

* Indicates items that are not functional

Table 3-6. MGSC to DCU Serial Channel Description (IIW_BLK) (Continued)

BITS	WORD 6	WORD 7	WORD 8	WORD 9
0	PIGLET(3)	PIGLET(2)	PIGLET(1)	GIBLET(3)
1				
2				
3				
4				
5				
6				
7				
8	PGINC_SUM(3)	PGINC_SUM(2)	PGINC_SUM(1)	GBLINC_SUM(3)
9				
10				
11				
12				
13				
14	PG_CRT_PH(3)	PG_CRT_PH(2)	PG_CRT_PH(1)	GBL_CRT_PH(3)
15				

Table 3-6. MGSC to DCU Serial Channel Description (IIW_BLK) (Continued)

BITS	WORD 10	WORD 11	WORD 12	WORD 13
0	GIBLET(1)	GIBLET(2)	SELECT_ADC	MTRVLTMON
1				
2				
3				
4				
5				
6				
7				
8	GBLINC_SUM(1)	GBLINC_SUM(2)	GCAINC_SUM	
9				MTRVMONSLT
10				
11				
12				SAR_MON(8)
13				SAR_MON(9)
14	GBL_CRT_PH(1)	GBL_CRT_PH(2)	GCA_CRT_PH	SAR_MON(10)
15				SAR_MON(11)

Table 3-6. MGSC to DCU Serial Channel Description (IIW_BLK) (Continued)

<table>
<tr><th>BITS</th><th>WORD 14</th><th>WORD 15</th><th>WORD 16</th><th>WORD 17</th></tr>
<tr><td>0</td><td rowspan="14">Echo of Output Word 1</td><td rowspan="8">Echo of Output Word 2, bits 0 - 8</td><td rowspan="8">Echo of Output Word 3, bits 0 - 8</td><td rowspan="2">CURPLATMOD</td></tr>
<tr><td>1</td></tr>
<tr><td>2</td><td rowspan="2">CURGCAMOD</td></tr>
<tr><td>3</td></tr>
<tr><td>4</td><td rowspan="2">CURPIGAMOD</td></tr>
<tr><td>5</td></tr>
<tr><td>6</td><td>CURGCOVRO</td></tr>
<tr><td>7</td><td>CURGCPWRON</td></tr>
<tr><td>8</td><td>CURPIGPWRO</td></tr>
<tr><td>9</td><td rowspan="3">GCASLCNTLR</td><td>DD_MON</td><td>SRVOENAMON</td></tr>
<tr><td>10</td><td>PIGCPL_MON</td><td>CMDENAMON</td></tr>
<tr><td>11</td><td rowspan="2">Echo of Output Word 3, bits 11 - 15</td><td rowspan="2">Echo of Output Word 4, bits 11 - 15</td></tr>
<tr><td>12-15</td><td>Echo of Output Word 2, bits 12 - 15</td></tr>
<tr><td colspan="5">Note: Words 14 - 17 are a complete copy of the last 4 output words, except that bits 0 - 8 of word 17 represent the true state of the MGSC mode, bit 10 of word 16 and bits 9 and 10 of word 17 provide secondary interest indicators and bits 9 - 11 of word 15 will be an echo unless an overrate occurs. If a NEP occurs, the echo bits may be affected if CLD is true (to reflect the reset state).</td></tr>
</table>

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Table 3-7. GC Null Counter Description

GCNULLCTR BITS: 10	11	12	INPUT: +	-
0	0	0	-sin	0
0	0	1	-sin+cos	0
0	1	0	cos	0
0	1	1	cos	-sin
1	0	0	0	-sin
1	0	1	0	-sin+cos
1	1	0	0	cos
1	1	1	-sin	cos

Note: The GC is defined to be at a Moire null when bits 10, 11 and 12 = 0.
An OER count is defined when bit 12 = 0 (4 per Moire null). There are 8 Artificial nulls per Moire null.

Source: S-133-19251

e. Timing inputs. The OGP shall access the precision timing signal from the Operational Ground Equipment (OGE) via the UIO Pending Interrupt Register. The resolution of the precision timing pulse is 0.984615 ± 0.000001 seconds per pulse.

f. Local command inputs. The OGP shall accept commands originated at the Controller/Monitor (C166B) during the Local Communications Mode. These commands appear in the first four bits of Multiplexer Status Set “R” as specified in Table 3-2. Keyboard Output 1 (KEYBOARD1), Keyboard Output 2 (KEYBOARD2), Keyboard Output 3 (KEYBOARD3) and Keyboard Output 4 (KEYBOARD4) inputs correspond to C166B commands 1, 2, 4 and 8, respectively.

g. Character outputs. The OGP interfaces with the Coupler Unit (C604A) by issuing character output code pairs. The OGP issues character output code pairs by executing write PIO instruction 0182_{16}. The two sequential character output codes required by the C604A are specified in Table 3-8. The character output signal timing requirements and the clock signal characteristics are specified in Figure 3-8. Character output codes 2-0 (DATASTART) and 2-15 (DATAEND) are only used by SELECT 880.

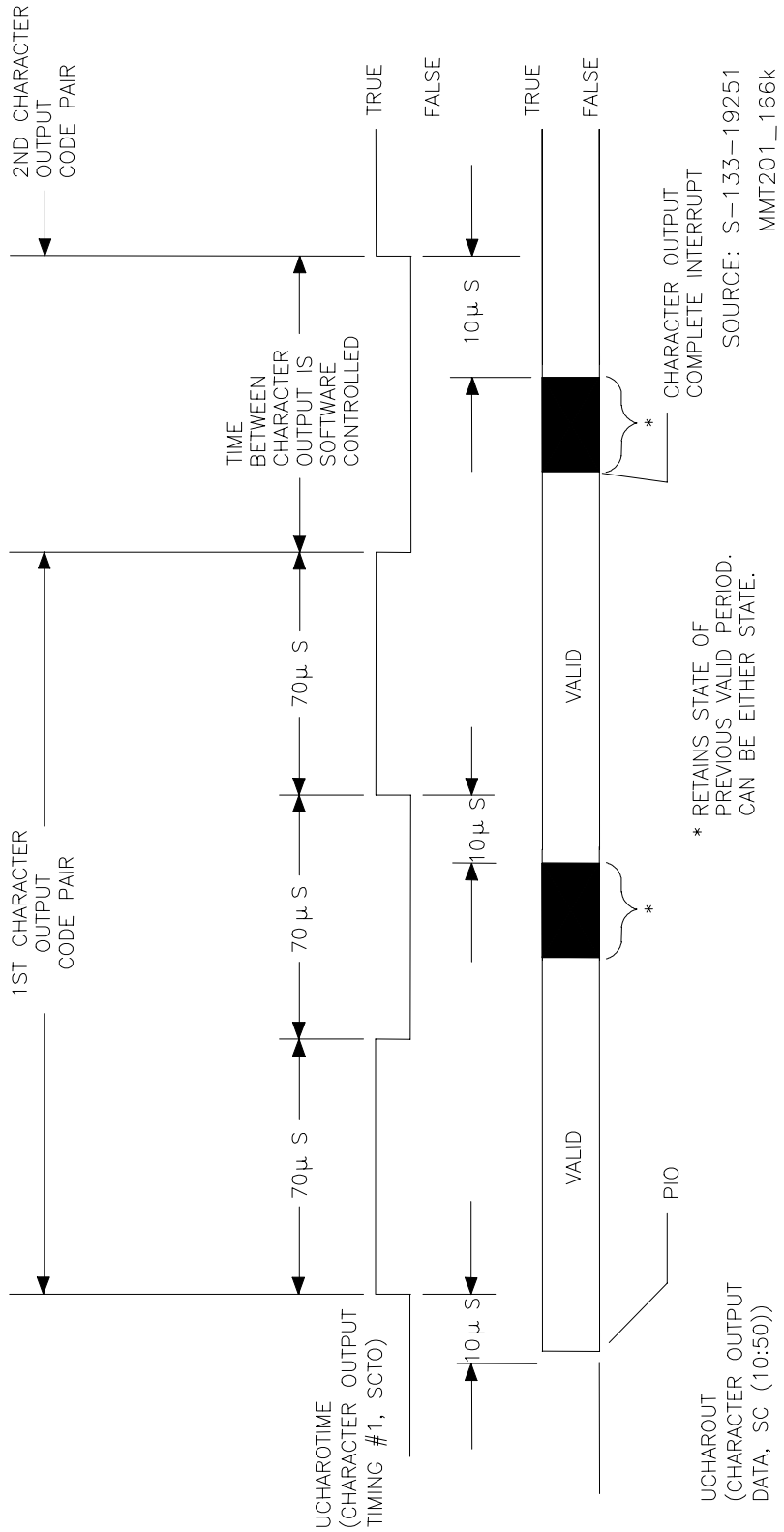

Figure 3-8. Character Output Code Timing

Table 3-8. Character Outputs

CODE NOTE 7	FUNCTION	SYMBOL	USED BY	NOTES
0-0	Select Status Set A	SELECT_A	MX	6
0-01	Select Status Set B	SELECT_B	MX	
0-2	Select Status Set C	SELECT_C	MX	
0-3	Select Status Set D	SELECT_D	MX	
0-4	Select Status Set E	SELECT_E	MX	
0-5	Select Status Set F	SELECT_F	MX	
0-6	Select Status Set G	SELECT_G	MX	
0-7	Select Status Set H	SELECT_H	MX	
0-8	Select Status Set J	SELECT_J	MX	
0-9	Select Status Set K	SELECT_K	MX	
0-10	Select Status Set L	SELECT_L	MX	
0-11	Select Status Set M	SELECT_M	MX	
0-12	Select Status Set N	SELECT_N	MX	
0-13	Select Status Set P	SELECT_P	MX	
0-14	Select Status Set R	SELECT_R	MX	
0-15	Select Status Set S	SELECT_S	MX	
3-0	Clear Text Allowed Reset	CLRTXTRST	A4	6
3-1	Clear Text Allowed Set	CLRTXTSET	A4	
3-2	ALCC Access Allowed Reset	ALC_UHFRST	A4	6
3-3	ALCC Access Allowed Set	ALC_UHFSET	A4	
3-4	Auxiliary Status Enable Reset	ASE_RST	A4	6
3-5	Auxiliary Status Enable Set	ASE_SET	A4	6
3-6	Spare Reset	(None)	–	
3-7	Spare Set	(None)	–	
3-8	Spare Reset	(None)	–	6
3-9	Spare Set	(None)	–	
3-10	Spare Reset	(None)	–	6
3-11	Spare Set	(None)	–	

Table 3-8. Character Outputs (Continued)

CODE NOTE 7	FUNCTION	SYMBOL	USED BY	NOTES
3-12	Spare Reset	(None)	–	6
3-13	Spare Set	(None)	–	
3-14	Spare Reset	(None)	–	6
3-15	Spare Set	(None)	–	
4-0	Data Readout 0	READOUT0	C166B	1
4-1	Data Readout 1	READOUT1	C166B	1
4-2	Data Readout 2	READOUT2	C166B	1
4-3	Data Readout 3	READOUT3	C166B	1
4-4	Data Readout 4/Data Readout Initiate	READ4INIT	C166B	1, 8
4-5	Data Readout 5	READOUT5	C166B	1
4-6	Data Readout 6	READOUT6	C166B	1
4-7	Data Readout 7/Data Readout Blanking	READOUT7	C166B	1, 2, 8
4-8	Data Readout 8	READOUT8	C166B	1
4-9	Data Readout 9	READOUT9	C166B	1
4-10	Data Readout 10	READOUT10	C166B	1
4-11	Data Readout 11	READOUT11	C166B	1
4-12	Data Readout 12	READOUT12	C166B	1
4-13	Data Readout 13	READOUT13	C166B	1
4-14	Data Readout 14	READOUT14	C166B	1
4-15	Data Readout 15	READOUT15	C166B	1
5-0	R/S Input Data Lines Reset	RS_DATARST	ACU	
5-1	R/S Input Data Line 1 Set	RS_DATA1AM	ACU	
5-2	R/S Input Data Line 2 Set	RS_DATA2AM	ACU	3,6
5-3	SCS Test Command Reset	SCS_TC_RST	MSC	
5-4	Coupler No-Go Reset	CPLRNGRST	NGRC	6
5-5	Coupler No-Go Set	CPLRNGST	NGRC	
5-6	Disable Discretes and Startup Indicator Reset	DDSTRUPRST	ACC	4, 6, 9
5-7	C/R Indicator Reset	CRRESET	NGRC	

Table 3-8. Character Outputs (Continued)

CODE NOTE 7	FUNCTION	SYMBOL	USED BY	NOTES
5-8	Critical Status Override Reset	CSORESET	NGRC	
5-9	Critical Status Override Set	CSO_SET	NGRC	6
5-10	AVE No-Go Reset	AVENGRST	NGRC	6
5-11	AVE No-Go Set	AVENGSET	NGRC	
5-12	Enable Write Reset	ENWRTRST	ACU	3, 6
5-13	Enable Write Set	ENWRTST	ACU	
5-14	Keep Alive	KEEPALVE	ACU	6
5-15	Spare	(None)	–	
6-0	Cable Message Enable Reset	CME_RESET	A4	3, 6
6-1	Cable Message Enable Set	CME_SET	A4	
6-2	Start SCNT Reset	SCNT_RST	A4	3, 6
6-3	Start SCNT Set	SCNT_ST	A4	
6-4	Spare Reset	(None)	–	3, 6
6-5	Spare Set	(None)	–	
6-6	SCS Test Enable Reset	SCSTENRST	MSC	3, 6
6-7	SCS Test Enable Set	SCSTENST	MSC	
6-8	Multiplexer Test Reset	MXTESTRST	MX	3, 6
6-9	Multiplexer Test Set	MXTESTST	MX	
6-10	Telemetry Turn-on Reset	TELEMONRST	DB	3, 6
6-11	Telemetry Turn-on Set	TELEMONST	DB	
6-12	Ground Ordnance Interlock 1 Reset	GNORDIN1RT	A6	3, 6
6-13	Ground Ordnance Interlock 1 Set	GNORDIN1ST	A6	
6-14	Coupler Test Reset	COUPTSTRST	NGRC	3, 6
6-15	Coupler Test Set	COUPTSTSET	NGRC	
8-0	C.O. Interface Test Reset (Test 2) (no reset necessary for 8-0)	COITRST	D	6
9-0	Reset Codes 9-1 through 9-7	RST91TO97	D	3, 6
9-1	Set Spare Squib Discrete No. 1	(None)	OC	4
9-2	Set Spare Squib Discrete No. 2	(None)	OC	4, 5

Table 3-8. Character Outputs (Continued)

CODE NOTE 7	FUNCTION	SYMBOL	USED BY	NOTES
9-3	Activate Suspension System	ACTSUSSYS	OC	4
9-4	Battery Activate Command	BATACT	OC	4
9-5	Arm Missile Ordnance Devices	ARMORDEV	SDC	4
9-6	Remove Launcher Closure Command	REMLUCHCL	OC	4
9-7	G&C Umbilical Release Command	GCUMBREL	OC	4
9-8	Resets Codes 9-9 through 9-15	RST99TO915	–	3, 6
9-9	Remove G&C Ground Power Command	RMVGCGDPWR	NGM	
9-10	Spare Set	(None)	–	
9-11	Spare Set	(None)	–	
9-12	Spare Set	(None)	–	
9-13	Spare Set	(None)	–	
9-14	Spare Set	(None)	–	
9-15	C/R Test Initiate	CRTESTINIT	EMPD	
10-0	Ground Ordnance No-Go Reset	GRDORDNGRT	NGM	6
10-1	Ground Ordnance No-Go Set	GRDORDNGST	NGM	
10-2	MOSR Status Reset	MOSRRST	AM	6
10-3	MOSR Status Set	MOSRST	AM	
10-4	Ground Ordnance Alarm Reset	GNDORDALRT	AM	6
10-5	Ground Ordnance Alarm Set	GNDORDALST	AM	
10-6	Spare Reset	(None)	–	6
10-7	Spare Set	(None)	–	
10-8	Spare Reset	(None)	–	6
10-9	Spare Set	(None)	–	
10-10	Spare Reset	(None)	–	6
10-11	Spare Set	(None)	–	
10-12	Spare Reset	(None)	–	6
10-13	Spare Set	(None)	–	
10-14	Spare Reset	(None)	–	6
10-15	Spare Set	(None)	–	

Table 3-8. Character Outputs (Continued)

CODE NOTE 7	FUNCTION	SYMBOL	USED BY	NOTES
12-0	CSD(G) Reset Command Reset	CSDGRCDRST	SDC	3, 6
12-1	CSD(G) Reset Command Set	CSDGRCDSET	SDC	
12-2	CSD(M) Reset Command Reset	CSDMRSTRST	SDC	3, 6
12-3	CSD(M) Reset Command Set	CSDMRST	SDC	
12-4	Spare Reset	(None)	–	3, 6
12-5	Spare Set	(None)	–	
12-6	Ground Ordnance Test Enable Reset	GOTENRST	OC	3, 6
12-7	Ground Ordnance Test Enable Set	GOTENSET	OC	
12-8	R/S Ground Power Reset	GNDPWRRST	NGM	3, 6
12-9	R/S Ground Power Set	GNDPWRSET	NGM	
12-10	SCS Arm Reset	SCSARMRST	SDC	3, 6
12-11	SCS Arm Set (D09A Not Required for SCS Test if SCS Test Command and SCS Test Enable are True)	SCSARMSET	SDC	4
12-12	SCS Safe Reset	SCSSAFERST	SDC	3, 6
12-13	SCS Safe Set	SCSSAFESET	SDC	
12-14	F/C Ground Power Reset	RSTFCNGPON	NGM	3, 6
12-15	F/C Ground Power Set	FCNGPON	NGM	
15-0	Resets Codes 15-1 through 15-7	RST151T157	D	3, 6
15-1	CSD(M) Mark	CSDM_MARK	SDC	
15-2	CSD(M) Space	CSDM_SPACE	SDC	
15-3	Spare Set	(None)	–	
15-4	Spare Set	(None)	–	
15-5	Spare Set	(None)	–	
15-6	Spare Set	(None)	–	
15-7	Spare Set	(None)	–	
15-8	Resets Codes 15-9 through 15-15	RST159TO15	D	3, 6
15-9	CSD(G) Mark	CSDG_MARK	SDC	4
15-10	CSD(G) Space	CSDG_SPACE	SDC	4
15-11	Spare Set	(None)	–	4

Table 3-8. Character Outputs (Continued)

CODE NOTE 7	FUNCTION	SYMBOL	USED BY	NOTES
15-12	Spare Set	(None)	–	
15-13	Spare Set	(None)	–	
15-14	Ground Ordnance Interlock 2 Set	GNORDIN2ST	OC	
15-15	Ground Ordnance Interlock Clear(Test 1)	GNORDINCLR	D&OC	

Abbreviations:

A4	–	Communications Drawer, Programmer Group
A6	–	Ordnance Monitor Drawer, Programmer Group
ACU	–	Activation Control Unit, C604A1
AM	–	Alarm Monitor, Ordnance Monitor Drawer, Programmer Group
C166B	–	Control Monitor
D	–	Decoder, Ordnance Monitor Drawer, Programmer Group
DB	–	Distribution Box
EMPD	–	EMP Detector
MSC	–	Manual Switch Control, C604A1
MX	–	Status Multiplexer, C604A1
NGM	–	No-Go Monitor, Programmer Group
NGRC	–	No-Go and Reset Control, C604A1
OC	–	Ordnance Control, Programmer Group
SDC	–	Safety Device Control, Programmer Group

Note:

1. All Data Readout must be preceded by the 4-4 code. The displayed value will be equal to the last character output issued (i.e., 4-4 4-12 displays a 12).
2. Data Readout Blanking will be executed if this code is not preceded by the 4-4 code.
3. Issued by C604A1/Programmer Group when C604A1 idle/Compute transition occurs or when C604A1 pulses Master Reset following loss of Keep-Alive codes.
4. Require Critical Circuits Enable to be true when code issued.
5. This spare set is active. Inadvertent setting of code 9-2 may result in a true “Any Ground Ordnance Driver On Monitor” signal.
6. Forced by Internal C604A1/Programmer Group logic when Circumvention Reset occurs.
7. Codes not listed are not decoded by the C604A1 or Programmer Group.
8. Two functions are defined but only one is valid at a time.
9. This character output also includes Keep Alive Timer Enable.

h. Discrete outputs. The OGP shall issue commands and discrete output signals as specified in Table 3-9. Data bit 15 is the LSB and bit 0 is the MSB. For detailed bit definitions of the discrete output registers listed in Table 3-9, see the Software Requirements Specifications for the OGP, S-133-19251, Section 3.1.

Table 3-9. Programmed I/O Write Address Assignments

COMMAND (HEX)	SYMBOL	OPERATION	DESCRIPTION	BIT DEFINITIONS
			CPU XIO -	
2008	CPUDO	Write	CPU Discrete Output Register	Table 3-66
			MIA PIOs -	
0080	MIACONFREG	Write	MIA Configuration Register	Table 3-67
0081	EWADDRBNDY	Write	Enable Write Address Boundary Register	Table 3-68
0082	MIAINPMSK	Write	MIA Interrupt Mask Register	Table 3-69
0083	CLDREG	Write	Critical Leads Disconnect Register	Table 3-70
0085	NEPTIMEREG	Write	NEP Timer Holding Register	Table 3-71
0086	CNRADDREG	Write	C&R Address Clamp Register	Table 3-72
0088-00FF	(None)	N/A	not used	N/A
			SDC PIOs -	
0101	SDCMSKREG	Write	SDC Interrupt Mask Register	Table 3-73
0102	CHAWCLADDR	Write	Channel A Word Count/Address Low Register	Table 3-74
0103	CHAHIADDR	Write	Channel A Address High Register	Table 3-75
0104	CHACONFREG	Write	Channel A Configuration Register	Table 3-76
0108	CHBWCLADDR	Write	Channel B Word Count/Address Low Register	Table 3-74
0109	CHBHIADDR	Write	Channel B Address High Register	Table 3-75
010A	CHBCONFREG	Write	Channel B Configuration Register	Table 3-76

Table 3-9. Programmed I/O Write Address Assignments (Continued)

COMMAND (HEX)	SYMBOL	OPERATION	DESCRIPTION	BIT DEFINITIONS
			UIO PIOs -	
0180	CAIOCNTLWD	Write	Cable I/O Control Word	Table 3-77
0181	CAIOHLDREG	Write	Cable I/O Holding Register	Table 3-78
0182	CHAROUT	Write	Character Output Control Word	Table 3-79
0183	UIOINPMSK	Write	UIO Interrupt Mask Register	Table 3-80
0184	RSDOREG	Write	RS Discrete Output Register	Table 3-81
0186	MK21DATA1	Write	MARK 21 RS Data Word #1 Register	N/A
0187	MK21DATA2	Write	MARK 21 RS Data Word #2 Register	N/A
0188	MK21DATA3	Write	MARK 21 RS Data Word #3 Register	N/A
0189	(None)	Start	Start Cable I/O	N/A
018A	HALTCABLE	Halt	Halt Cable I/O	N/A
018B	(None)	Start	MARK 21 RS Fuzing	N/A
018C	(None)	Halt	MARK 21 RS Fuzing	N/A
018D	UIOPSEREG	Write	UIO PSE Test Register	Table 3-88
018E	UIOPENDINP	Clear	UIO Pending Interrupt Register	Table 3-89
018F	UIODOREG	Write	UIO Discrete Output Register	Table 3-90
0190	UIOINPENA	Write	UIO Interrupt Enable/Disable	Table 3-91
0191	TIMERC	Write	Timer C Reset Register	Table 3-92
0192	TIMERD	Write	Timer D Reset Register	Table 3-92
0193	(None)	Set	Set UIO Pending Interrupt Bit	Table 3-89
0194	(None)	Start	Start Timer C	N/A
0195	(None)	Start	Start Timer D	N/A
0196	(None)	Halt	Halt Timer C	N/A
0197	(None)	Halt	Halt Timer D	N/A
			FOIO PIOs -	
0200	TVCAES1NZ1	Write	TVC AES, Stage 1, Nozzle 1 Command	Table 3-93

Table 3-9. Programmed I/O Write Address Assignments (Continued)

COMMAND (HEX)	SYMBOL	OPERATION	DESCRIPTION	BIT DEFINITIONS
0201	TVCAES1NZ2	Write	TVC AES, Stage 1, Nozzle 2 Command	Table 3-93
0202	TVCAES1NZ3	Write	TVC AES, Stage 1, Nozzle 3 Command	Table 3-93
0203	TVCAES1NZ4	Write	TVC AES, Stage 1, Nozzle 4 Command	Table 3-93
0204	TVCAES2IJ1	Write	TVC AES, Stage 2, Injector 1 Command	Table 3-93
0205	TVCAES2IJ2	Write	TVC AES, Stage 2, Injector 2 Command	Table 3-93
0206	TVCAES2IJ3	Write	TVC AES, Stage 2, Injector 3 Command	Table 3-93
0207	TVCAES2IJ4	Write	TVC AES, Stage 2, Injector 4 Command	Table 3-93
0208	STG2ROLCMD	Write	Stage 2 Roll Command	Table 3-94
0209	TVCAES3IJ1	Write	TVC AES, Stage 3, Injector 1 Command	Table 3-93
020A	TVCAES3IJ2	Write	TVC AES, Stage 3, Injector 2 Command	Table 3-93
020B	TVCAES3IJ3	Write	TVC AES, Stage 3, Injector 3 Command	Table 3-93
020C	TVCAES3IJ4	Write	TVC AES, Stage 3, Injector 4 Command	Table 3-93
020D	STG3ROLCMD	Write	Stage 3 Roll Command	Table 3-95
020E	FCSELEM	Write	Flight Control Select/Event Markers	Table 3-96
0210	PBPSAESPTH	Write	PBPS AES Pitch Command	Table 3-93
0211	PBPSAESYAW	Write	PBPS AES Yaw Command	Table 3-93
0212	PBPSAXATT	Write	PBPS Axial/Attitude Command	Table 3-97
0213	FOIOPSEREG	Write	FOIO PSE Test Register	Table 3-98
0220	ORDENA	Write	Ordnance Enable	Table 3-99
0221	ORDCMDS	Write	Ordnance Commands	Table 3-100

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i. Serial channel output data. The data symbols and descriptions of the DCU to MGSC data are defined in Table 3-10. The OGP will load the DCU to MGSC serial channel data, specified in DCU to MGSC serial Channel Words 1 through 4 in Table 3-11, into one block of contiguous memory identified as IOW_BLK, at a 819.5 Khz rate.

Table 3-10. DCU to MGSC Serial Channel Output Data

ITEM NO.	SYMBOL	DESCRIPTION	SIZE	LSB
1	ADCSP_SLCT	ADC Spare Channel Select	1	N/A
2	G6GT_CMD	X, Y and Z Gyro Torque Commands	3x1	N/A
3	GBLSL_CMD	Yaw, Pitch and Roll Gimbal Slew Commands (X, Y and Z)	3x1	.135 volts
4	GC_TRQCMD	GC Torque Command	1	N/A
5	GC_OVRVLT	GC Overvoltage On	1	N/A
6	GCA_MD_CNL	GCA Mode Controls	1	N/A
7	GCASL_CMD	GCA Slew Command	1	*
8	GCASL_CNTL	GCA Slew Controls	1	N/A
9	GCPWRON	GC Power On	1	N/A
10	GIBPH_SLT	Yaw, Pitch and Roll Giblet Phase Select	3x1	N/A
11	LD_SELECTS	Level Detector Selects	1	N/A
12	MTRVMONSLT	Motor Voltage Monitor Select	1	N/A
13	PG_MD_CNL	PIGA Mode Controls	1	N/A
14	PIGAPWRON	PIGA 800 Hz Power On	1	N/A
15	PIGASL_CMD	PIGA Slew Command	3x1	*
16	PIGPH_SLT	X, Y and Z Piglet Phase Select	3x1	N/A
17	PIGDMSLT	ADC PIGA Demod Select	1	N/A
18	PLATMD_CNL	Platform Mode Controls	1	N/A

* These parameters are not used by the OGP so the LSB has not been provided

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Table 3-11. DCU to MGSC Serial Channel Description (IOW_BLK)

BITS	WORD 1	WORD 2	WORD 3	WORD 4
0	GBLSL_CMD(1) or PIGASL_CMD(1) or GCASL_CMD	GBLSL_CMD(2) or PIGASL_CMD(2)	GBLSL_CMD(3) or PIGASL_CMD(3)	PLATMD_CNL (see Table 3-12)
1				
2				GCA_MD_CNL (see Table 3-12)
3				
4				PG_MD_CNL (see Table 3-12)
5				
6				GC_OVRVLT
7				GCPWRON
8				PIGAPWRON
9	PIGDMSLT	GCASL_CNTL (see Table 3-14)	Spare	Spare
10	PIGPH_SLT(1)			
11	PIGPH_SLT(2)		LD_SELECTS (see Table 3-13)	ADCSP_SLCT (see Table 3-16)
12	PIGPH_SLT(3)	GC_TRQCMD		
13	GIBPH_SLT(1)	G6GT_CMD(1)	MTRVMONSLT (see Table 3-15)	
14	GIBPH_SLT(2)	G6GT_CMD(2)		
15	GIBPH_SLT(3)	G6GT_CMD(3)		

Source: S-133-19251

Table 3-12. Mode Control Description

MODE CONTROL BITS:		DESCRIPTION
a	b	
0	0	Stable Operation
0	1	Slew
1	0	Servo Test
1	1	Disable
Note: a < b.		

Source: S-133-19251

Table 3-13. Level Detector Selection Word Description

LD_SELECTS BITS:		DESCRIPTION
11	12	
0	0	Level Detector 1
0	1	Level Detector 2
1	0	MGSC NED Test (was Level Detector 3)
1	1	Level Detector 4

Source: S-133-19251

Table 3-14. GCA Slew Controls Description

GCASL_CNTL BITS:			DESCRIPTION
9	10	11	
x	0	0	Stable Operation
0	0	1	Fast Slew CCW
1	0	1	Fast Slew CW
0	1	0	Slow Slew CCW Mode
1	1	0	Slow Slew CW Mode
x	1	1	Slow Slew Clock
Where x is don't care.			

Source: S-133-19251

Table 3-15. Motor Voltage Monitor Select Description

VALUE	DESCRIPTION
0	X PIGA Motor Voltage Monitor
1	Y PIGA Motor Voltage Monitor
2	Z PIGA Motor Voltage Monitor
3	Yaw Gimbal (X) Motor Voltage Monitor
4	Pitch Gimbal (Y) Motor Voltage Monitor
5	Roll Gimbal (Z) Motor Voltage Monitor
6	GCA Motor Voltage Monitor

Source: S-133-19251

Table 3-16. ADC Spare Channel Select Description

VALUE	DESCRIPTION
0	Roll Gimbal (Z) Demod Pickoff
1	Yaw Gimbal (X) Demod Pickoff
2	Pitch Gimbal (Y) Demod Pickoff
3	Z Piglet -- A Phase
4	Y Piglet -- A Phase
5	X Piglet -- A Phase
6	Roll Giblet (Z) -- A Phase
7	Yaw Giblet (X) -- A Phase
8	Pitch Giblet (Y) -- A Phase
9	GC Demod
10	Pitch Giblet (Y) -- B Phase
11	Z Piglet -- B Phase
12	Y Piglet -- B Phase
13	X Piglet -- B Phase
14	Roll Giblet (Z) -- B Phase
15	Yaw Giblet (X) -- B Phase
16	Z PIGA Demod Pickoff
17	Y PIGA Demod Pickoff
18	X PIGA Demod Pickoff
19	0 v Calibration
20	-7.5 v Calibration
21	XY DC Speed Control
22	YZ DC Speed Control
23	XY-YZ Gyro Caging Pickoff

SOURCE: S-133-19251

3-2.2.9. Dedicated Data Readout. The operational ground program provides a Dedicated Data Readout for local readout of MOSR words, fault data words, the critical no-go word, gyrocompass data words, alignment data words, RS fuzing fault history words, and the IMU Alarm and SBNG No-Go history words (refer to Table 3-17). In addition, local readout of data has been expanded to include other selected address locations of DCU non-write protected SRAM memory locations. Each word, comprised of 16 data bits, is read out 4 bits at a time. At the LF, with the guidance-control system in compute, local data readout is initiated by the control-monitor operator selecting and entering the

appropriate command code via the control-monitor keyboard. DCU acceptance of the command code entry and DCU memory address is indicated by a blanking of the DCU READOUT display and display of the first four bits.

3-2.2.9.1 Missile Operational Status Reply Words. While in the compute mode, the DCU performs continuous monitoring of the operating status of the AVE and a portion of the OGE. If a fault is detected, a flag is set in the DCU memory and a signal transmitted to the control-monitor. The DCU READOUT 8 indicator on the control-monitor illuminates, informing the operator that a change of status has occurred in the guidance-control system. To determine the reason for the status change, the control-monitor operator performs Dedicated Data Readout of the two MOSR words, four bits at a time, via the control-monitor keyboard. Data read out are recorded on the LF fault record and maintained as permanent record of guidance-control system operation.

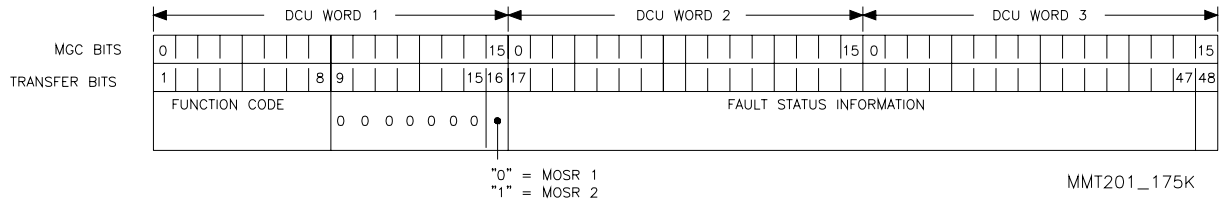


Figure 3-9. MOSR (Missile Operational Status Reply)

3-2.2.9.2 Fault Data Words. The operational ground program provides capability for readout of seven fault data words. Fault data word 1 contains stored fault data for IMU functions and indicates the IMU routine in process at the time of standby no-go detection. The contents of fault data word 1 are stored in SRAM Memory at data location 03. Fault data words 2 through 6 contain stored information, which when read out, enables the maintenance team to determine the reason for an unsuccessful missile test. Data read out of fault data words 2 through 6 following a complete or code change DCU program loading, are invalid until a complete missile test has been performed. Fault data word 7 contains platform servo transient response test failure data. Fault data word 7 is invalid following complete or code change DCU program loading until a Phi calibration has been performed or the LF has entered Standby No-Go for specific faults. During DCU complete program loading, all fault data word locations are set to zero. Stored fault data words 2 through 7 remain valid until another complete or code change DCU program loading is performed. In remote, fault data words 1 through 7 are sent to the LCF automatically during standby no-go. In Local only fault data words 1 through 6 are read out.

Table 3-17. Local Data Readout – Dedicated Data Index

INDEX NUMBER (OCTAL)*	SIZE (BITS)	DATA DESCRIPTION
01	32	MOSR Word No. 1
02	32	MOSR Word No. 2
03	16	Fault Data Word 1
04	32	Fault Data Word 2
05	32	Fault Data Word 3
06	32	Fault Data Word 4
07	32	Fault Data Word 5
10	32	Fault Data Word 6
11	32	Fault Data Word 7
12	16	IMU No-Go History Word 1
13	16	IMU No-Go History Word 2
14	16	IMU No-Go History Word 3
15	16	IMU No-Go History Word 4
16	16	IMU No-Go History Word 5
17	16	IMU No-Go History Word 6
20	16	IMU No-Go History Word 7
21	16	IMU No-Go History Word 8
22	16	IMU No-Go History Word 9
23	16	IMU No-Go History Word 10
24	16	IMU Alarm History Word 1
25	16	IMU Alarm History Word 2
26	16	IMU Alarm History Word 3
27	16	IMU Alarm History Word 4
30	16	IMU Alarm History Word 5
31	16	IMU Alarm History Word 6
32	16	IMU Alarm History Word 7
33	16	IMU Alarm History Word 8
34	16	IMU Alarm History Word 9
35	16	IMU Alarm History Word 10
36	16	IMU Alarm History Word 11
37	16	IMU Alarm History Word 12
40	16	IMU Alarm History Word 13
41	16	IMU Alarm History Word 14
42	16	IMU Alarm History Word 15
43	16	Critical No-Go Identifier
44	48	Estimate of GC IA Azimuth Misalignment Angle (ϕ_N)
45	48	True North to GCA X-axis Azimuth Mis-alignment Angle (ϕ_Z)
46	48	GC Input Axis Misalignment Angle (ϕ_3)
47	16	Missile Roll Attitude Angle (minusϕ_r)
50	16	Platform Slew Correction Angle (minus$\Delta\phi_r$)
51	32	Fault History Word No. 1 Containing R/S Fuzing Attempts Status
52	32	Fault History Word No. 2 Containing R/S Fuzing Attempts Status

* Enter 8 for a zero digit

Table 3-18. MOSR Fault Bit Designation

MOSR NUMBER	TRANSFER BIT	(MOSR Word 1) MISSILE OPERATIONAL STATUS RESPONSE DESIGNATION
-	16	Identifier (0-Set)
11	17	Spare (0-Set)
12	18	Spare (0-Set)
13	19	Spare (0-Set)
14	20	Spare (0-Set)
15	21	Spare (0-Set)
16	22	Spare (0-Set)
17	23	Spare (0-Set)
18	24	Spare (0-Set)
19	25	CSD(G) Test Failure
20	26	Ground Ordnance Discrete Test Failure
21	27	F/C Power Failure
22	28	PSRE Control Failure
23	29	Downstage Discretes Failure
24	30	R/S Discretes Failure
25	31	PSRE Discretes Failure
26	32	Control & Discretes Unit Failure
27	33	Computer Failure
28	34	Downstage Control Failure
29	35	Stage II Roll Control Failure
30	36	Nuclear Event Detector Failure
31	37	Stage III Roll Control Failure
32	38	Spare (0-Set)
33	39	Spare (0-Set)
34	40	Spare (0-Set)
35	41	Spare (0-Set)
36	42	Spare (0-Set)
37	43	Spare (0-Set)
38	44	Spare (0-Set)
39	45	Gyro Speed Control Failure
40	46	Calibrations Inhibited
41	47	Computer Battery Failure/Off

MOSR NUMBER	TRANSFER BIT	(MOSR WORD 2) MISSILE OPERATIONAL STATUS RESPONSE DESIGNATION
-	16	Identifier (1-Set)
42	17	Circumvention Reset Alarm
43	18	LCF Address Time Expired
44	19	CSD(M) Control Failure
45	20	CSD(M) Drive Enable Failure
46	21	Programmer Group Failure
47	22	G&C Coupler Control Monitor Failure
48	23	Low Level Seismic
49	24	UHF Radio Test Failure
50	25	GCA Failure No. 1
51	26	GCA Failure No. 2
52	27	GCA Failure No. 3
53	28	PSAT Calibration Advised
54	29	LAI Check Failure
55	30	Phi Calibration Failure
56	31	Precision Time Failure
57	32	IMU servo Failure
58	33	Coarse Zeta Alignment Failure
59	34	GCA/Platform Indexing Advised
60	35	SCS Armed
61	36	CSD(M) Code Change Mode
62	37	Stage III LITVC Pressure Failure
63	38	Platform Pressure Failure
64	39	Checksum Failure
65	40	Phi Calibration Advised
66	41	R/S Fuzing Failure
67	42	IMU Calibration Failure
68	43	PSRE Pressure Propellant Alarm
69	44	Gyro Bias Shift
70	45	Gravity Residual/PIGA Leveling Failure
71	46	Absolute PIGA Bias Failure
72	47	IMU Calibration Advised

Table 3-19. IMU Fault Data Word 1 and IMU No-Go History Words 1 – 10

NOTES: FAILURE MODE FOR MALFUNCTION INDICATED IS STANDBY NO-GO.

FAULT DATA WORD 1 OR IMU NO-GO HISTORY WORDS 1 - 10 HEXADECIMAL EQUIVALENT OF MINUS ONE (FFFF) AND ZERO, RESPECTIVELY, SIGNIFIES THAT THE RESPECTIVE WORD CONTAINS NO STANDBY NO-GO DATA SINCE TAPE PROGRAM LOADING.

UPON ENTERING STANDBY NO-GO IMU FAILURE DATA ARE STORED IN FAULT DATA WORD 1. PREVIOUSLY STORED IMU FAILURE DATA, IF ANY, IN IMU NO-GO HISTORY WORDS 1 - 9 ARE SHIFTED TO IMU NO-GO HISTORY WORDS 2 - 10 RESPECTIVELY AND THE PREVIOUS FAULT DATA WORD 1, IF ANY, IS STORED IN IMU NO-GO HISTORY WORD 1. THESE LOCATIONS ARE READ OUT USING LOCAL DEDICATED DATA READOUT PROCEDURE AND APPLICABLE COMMAND CODES.

INDIVIDUALLY RECORDED DATA BITS OF FAULT DATA WORD 1 OR IMU NO-GO HISTORY WORDS 1 - 10 ARE NOT SIGNIFICANT. HOWEVER, TOGETHER THE INDIVIDUAL DATA BITS CIRCLED COMPRISE A BIT PATTERN WHICH IS UNIQUE TO A SPECIFIC MALFUNCTION. FOR FAULT DATA WORD 1 AND IMU NO-GO HISTORY WORDS 1 - 10 THE MALFUNCTION INDICATED IS DETERMINED BY CORRELATING RECORDED MOSR BIT SET AND FAULT DATA WORD/IMU NO-GO HISTORY WORD BIT PATTERN.

RECORDED BIT PATTERN	HEX NUMBER	MOSR SET	INDICATED MALFUNCTION
13	0004	50	155-second GCA slew timer expired before completion of GCA slew - not PIGA leveling
13, 15	0005	50	155-second GCA slew timer expired before completion of GCA slew during PIGA leveling (PIGA Leveling exit has been commanded)
11, 12	0018	50	155-second GCA slew timer expired before completion of GCA slew during PIGA leveling (Set at exit from PIGA Leveling)
11, 12, 14, 15	001B	50	Gyrocompass rotor-on test failure
11, 12, 13	001C	50	Q(I) greater than 7400 during second or third bias cycle of autoindexing
11, 12, 13, 15	001D	50	Q(I) greater than 7400 five times in a retarget alignment
11, 12, 13, 14	001E	50	Q(I) greater than 7400 once during initial alignment
10, 14	0022	50	Second Phi(2) failure in autoindexing
10, 11, 12, 13, 14, 15	003F	50	Delta P(n) check failed more than 22 times during initial alignment

Table 3-19. IMU Fault Data Word 1 and IMU No-Go History Words 1 – 10 (Continued)

RECORDED BIT PATTERN	HEX NUMBER	MOSR SET	INDICATED MALFUNCTION
9, 10, 11, 12, 13, 14	007E	50 and 59	GCA detected off reference null during an AOA (2nd time) in autoindexing or east 1 AOA
8	0080	50	155-second GCA slew timer expired while in a null correction GCA slew (not in PIGA Leveling)
14, 15	0003	57	Platform rate dump occurred which was not recoverable
10, 11, 12, 13, 14	003E	57	Platform servo transient response test failed
9, 14	0042	57	6-minute platform leveling timer expired while leveling to level detector No. 4 during coarse ZETA alignment
9, 14, 15	0043	57	6-minute platform leveling timer expired while leveling to level detector No. 2 during coarse ZETA alignment
9, 13	0044	57	25-minute platform slew timer expired during the first slew to level detector No. 1 in initial alignment
9, 13, 15	0045	57	1-minute platform leveling timer expired following GCA 180-degree slew
9, 13, 14	0046	57	25-minute platform leveling timer expired during leveling to level detector No. 1 following the first platform slew in initial alignment
9, 13, 14, 15	0047	57	1-minute platform leveling timer expired on exit from PIGA leveling
9, 12	0048	57	25-minute platform leveling timer expired during leveling following platform slew to Phi calibration reference position
9, 12, 15	0049	57	1-minute platform leveling timer expired during leveling following GCA slew to Phi Calibration position 1
9, 12, 14	004A	57	1-minute platform leveling timer expired during leveling following GCA slew to Phi Calibration position 2
9, 12, 14, 15	004B	57	1-minute platform leveling timer expired during leveling following GCA slew to Phi Calibration position 3
9, 12, 13	004C	57	1-minute platform leveling timer expired during leveling following GCA slew to Phi Calibration position 4

Table 3-19. IMU Fault Data Word 1 and IMU No-Go History Words 1 – 10 (Continued)

RECORDED BIT PATTERN	HEX NUMBER	MOSR SET	INDICATED MALFUNCTION
9, 12, 13, 15	004D	57	1-minute platform leveling timer expired during leveling following GCA slew to Phi Calibration position 5
9, 12, 13, 14	004E	57	1-minute platform leveling timer expired during leveling following GCA slew to Phi Calibration position 6
9, 12, 13, 14, 15	004F	57	1-minute platform leveling timer expired during leveling following GCA slew to Phi Calibration position 7
9, 11	0050	57	1-minute platform leveling timer expired during leveling following GCA slew to Phi Calibration position 8
9, 11, 15	0051	57	1-minute platform leveling timer expired during leveling following GCA slew to Phi Calibration position 9
9, 11, 14	0052	57	25-minute platform slew timer expired during platform slew to Phi calibration reference position
9, 11, 14, 15	0053	57	1-minute platform leveling timer expired following +40 OER count GCA slew in autoindexing
9, 11, 13	0054	57	1-minute platform leveling timer expired following -40 OER count GCA slew during autoindexing
9, 11, 13, 15	0055	57	25-minute platform leveling timer expired during leveling following autoindexing delta Phi R platform slew (coarse alignment)
9, 11, 13, 14	0056	57	25-minute platform slew timer expired during autoindexing delta Phi R platform slew (coarse alignment)
9, 11, 13, 14, 15	0057	57	25-minute platform slew timer expired while slewing during a retarget alignment)
9, 11, 12	0058	57	25-minute platform leveling timer expired while leveling during a retarget alignment
9, 11, 12, 15	0059	57	25-minute platform leveling timer expired during leveling following autoindexing Phi 2 platform slew (fine alignment)
9, 11, 12, 14	005A	57	25-minute platform slew timer expired during autoindexing Phi 2 platform slew (fine alignment)

Table 3-19. IMU Fault Data Word 1 and IMU No-Go History Words 1 – 10 (Continued)

RECORDED BIT PATTERN	HEX NUMBER	MOSR SET	INDICATED MALFUNCTION
9, 11, 12, 14, 15	005B	57	25-minute platform slew timer expired during platform slew following IMU calibration 2 interrupt (position 4 or 6)
9, 11, 12, 13	005C	57	25-minute platform leveling timer expired during leveling following IMU calibration 2 interrupt (position 4 or 6)
9, 11, 12, 13, 15	005D	57	25-minute platform leveling timer expired during leveling following platform slew to IMU calibration 2 position 1
9, 11, 12, 13, 14	005E	57	25-minute platform leveling timer expired during leveling following platform slew to IMU calibration 2 position 2
9, 11, 12, 13, 14, 15	005F	57	25-minute platform leveling timer expired during leveling following platform slew to IMU calibration 2 position 3
13, 14	0006	57	LAI or good IMU read/data check failures occurred during three consecutive data collections
9, 10	0060	57	25-minute platform leveling timer expired during leveling following platform slew to IMU calibration 2 position 4
9, 10, 15	0061	57	25-minute platform leveling timer expired during leveling following platform slew to IMU calibration 2 position 5
9, 10, 14	0062	57	25-minute platform leveling timer expired during leveling following platform slew to IMU calibration 2 position 6
9, 10, 14, 15	0063	57	25-minute platform leveling timer expired during leveling following platform slew to IMU calibration 2 intermediate position
9, 10, 13	0064	57	25-minute platform slew timer expired during platform slew to IMU calibration 2 position 1
9, 10, 13, 15	0065	57	25-minute platform slew timer expired during platform slew to IMU calibration 2 position 2
9, 10, 13, 14	0066	57	25-minute platform slew timer expired during platform slew to IMU calibration 2 position 3
9, 10, 13, 14, 15	0067	57	25-minute platform slew timer expired during platform slew to IMU calibration 2 position 4

Table 3-19. IMU Fault Data Word 1 and IMU No-Go History Words 1 – 10 (Continued)

RECORDED BIT PATTERN	HEX NUMBER	MOSR SET	INDICATED MALFUNCTION
9, 10, 12	0068	57	25-minute platform slew timer expired during platform slew to IMU calibration 2 position 5
9, 10, 12, 15	0069	57	25-minute platform slew timer expired during platform slew to IMU calibration 2 position 6
9, 10, 12, 14	006A	57	25-minute platform slew timer expired during platform slew to IMU calibration 2 intermediate position
9, 10, 12, 14, 15	006B	57	25-minute platform slew timer expired during platform slew to IMU calibration 2 initial position
9, 10, 12, 13	006C	57	25-minute platform leveling timer expired during leveling following platform slew to IMU calibration 2 initial position
9, 10, 12, 13, 15	006D	57	25-minute platform leveling timer expired during leveling following a platform slew to position No. 1 in IMU calibration 1
9, 10, 12, 13, 14	006E	57	25-minute platform leveling timer expired during leveling following a platform slew to position No. 2 in IMU calibration 1
9, 10, 12, 13, 14, 15	006F	57	25-minute platform leveling timer expired during leveling following a platform slew to position No. 3 in IMU calibration 1
9, 10, 11	0070	57	25-minute platform leveling timer expired during leveling following platform slew to intermediate level position prior to initiating IMU calibration 1 position 4
9, 10, 11, 15	0071	57	25-minute platform leveling timer expired during leveling following a platform slew to position No. 4 in IMU calibration 1
9, 10, 11, 14	0072	57	25-minute platform leveling timer expired during leveling to level detector No. 1 following IMU calibration 1
9, 10, 11, 14, 15	0073	57	25-minute platform slew timer expired during platform slew to position No. 1 in IMU calibration 1
9, 10, 11, 13	0074	57	25-minute platform slew timer expired during platform slew to position No. 2 in IMU calibration 1
9, 10, 11, 13, 15	0075	57	25-minute platform slew timer expired during platform slew to position No. 3 in IMU calibration 1

Table 3-19. IMU Fault Data Word 1 and IMU No-Go History Words 1 – 10 (Continued)

RECORDED BIT PATTERN	HEX NUMBER	MOSR SET	INDICATED MALFUNCTION
9, 10, 11, 13, 14	0076	57	25-minute platform slew timer expired during platform slew to intermediate level position prior to initiating IMU calibration 1 position 4
9, 10, 11, 13, 14, 15	0077	57	25-minute platform slew timer expired during platform slew to position No. 4_ in IMU calibration 1
9, 10, 11, 12	0078	57	25-minute platform slew timer expired during slew to level detector No. 1 following IMU calibration 1
9, 10, 11, 12, 15	0079	57	1-minute platform leveling timer expired following +40 OER count GCA slew in PSAT scale factor test
9, 10, 11, 12, 14	007A	57	25-minute platform leveling timer expired during leveling following platform slew to PSAT calibration Alpha (mu) position
9, 10, 11, 12, 14, 15	007B	57	25-minute platform slew timer expired during platform slew to PSAT calibration Alpha (mu) position
9, 10, 11, 12, 13	007C	57	25-minute platform slew timer expired during platform slew to IMU calibration 2 final position
9, 10, 11, 12, 13, 15	007D	57	25-minute platform leveling timer expired during leveling following platform slew to IMU calibration 2 final position
12, 14, 15	000B	58	Delta ZETA check failed three consecutive times during a coarse ZETA alignment
10, 11, 13, 14	0036	67	Failed second IMU calibration 1 delta RL check
10, 11, 12	0038	67	Failed second IMU calibration 2 delta RL check
12, 13	000C	69	G6B4 X-axis gyro bias shift failed gross limit
12, 13, 15	000D	69	G6B4 Y-axis gyro bias shift failed gross limit
12, 13, 14	000E	69	G6B4 Z-axis gyro bias shift failed gross limit
12, 13, 14, 15	000F	69	G6B4 X-axis gyro bias shift failed coarse limit
11	0010	69	G6B4 Y-axis gyro bias shift failed coarse limit
11, 15	0011	69	G6B4 Z-axis gyro bias shift failed coarse limit
14	0002	70	Cumulative LAI check failures/velocity observable data rejections since PIGA leveling entry has reached 60

Table 3-19. IMU Fault Data Word 1 and IMU No-Go History Words 1 – 10 (Continued)

RECORDED BIT PATTERN	HEX NUMBER	MOSR SET	INDICATED MALFUNCTION
12, 14	000A	71	PIGA biases not established prior to strategic alert entry checks
13, 14, 15	0007	71 and 72	X-axis absolute PIGA bias failure
12	0008	71 and 72	Y-axis absolute PIGA bias failure
12, 15	0009	71 and 72	Z-axis absolute PIGA bias failure

Table 3-20. Fault Data Word – Missile Ordnance Discretes Test

NOTE: READOUT DATA FOR FAULT DATA WORDS 2 THROUGH 6 ARE INVALID AFTER CODE CHANGE OR FOLLOWING AN AVE STARTUP UNTIL A COMPLETE MISSILE TEST HAS BEEN PERFORMED. AFTER MISSILE TEST HAS BEEN PERFORMED, THE FAULT DATA WORDS INFORMATION REMAINS VALID UNTIL ANOTHER CODE CHANGE LOAD OR AVE STARTUP IS PERFORMED.

FAULT DATA WORD 2: MISSILE ORDNANCE DISCRETES TEST

NOTES: THE NO FAULT HEXADECIMAL NUMBER FOR FAULT DATA WORD 2 IS 000F, 3F00.

BITS SHOWN UNDERLINED ARE NORMALLY SET.

BIT	BIT IDENTIFIER
0	Unassigned
1	Unassigned
2	Unassigned
3	Unassigned
4	Unassigned
5	Unassigned
6	Unassigned
7	Unassigned
8	Not Used
9	Not Used
10	Not Used
11	Not Used
12	Stage I/II Separation
13	Stage II Ignition
14	Stage II Gas Generator No. 1
15	Stage II Gas Generator No. 2
16	Downstage Ordnance Spare No. 1
17	Downstage Ordnance Spare No. 2
18	Stage II/III Separation
19	Stage III Ignition
20	Stage III Gas Generator No. 3
21	Stage III Gas Generator No. 4
22	Thrust Termination A
23	Thrust Termination B
24	Not Used
25	Not Used
26	Not Used
27	Not Used
28	Not Used
29	Not Used
30	Not Used
31	Not Used

Table 3-21. Fault Data Word 3 - Missile Ordnance Discretes Test

FAULT DATA WORD 3: MISSILE ORDNANCE DISCRETES TEST	
NOTES: THE NO FAULT HEXADECIMAL NUMBER FOR FAULT DATA WORD 3 IS 00CF, DFFF. BITS SHOWN UNDERLINED ARE NORMALLY SET.	
BIT	**BIT IDENTIFIER**
0	Unassigned
1	Unassigned
2	Unassigned
3	Unassigned
4	Unassigned
5	Unassigned
6	Unassigned
7	Unassigned
8	Stage III/PBPS Electrical Separation
9	Stage III/PBPS Mechanical Separation
10	PBPS Ordnance Spare No. 1
11	PBPS Ordnance Spare No. 2
12	PBPS Propellant Outlet
13	PBPS Propellant Pressure
14	Ordnance Hazardous Current Monitor 1
15	Ordnance Hazardous Current Monitor 2
16	RS Hazardous Current Monitor #2
17	RS Hazardous Current Monitor #1
18	RS Prearm Monitor, Warhead Prearm
19	RS Discrete Monitor #12, Chaff Feed Rate Read
20	RS Discrete Monitor #11, Chaff Eject
21	RS Discrete Monitor #10, Chaff Activate
22	RS Discrete Monitor #9
23	RS Discrete Monitor #8
24	RS Discrete Monitor #7
25	RS Discrete Monitor #6
26	RS Discrete Monitor #5
27	RS Discrete Monitor #4
28	RS Discrete Monitor #3
29	RS Discrete Monitor #2B
30	RS Discrete Monitor #2A
31	RS Discrete Monitor #1

Table 3-22. Fault Data Word 4 - Control System Test (Stages I, II, III)

FAULT DATA WORD 4: CONTROL SYSTEM TEST (STAGES I, II, III)		
NOTE: THE NO FAULT HEXADECIMAL NUMBER FOR FAULT DATA WORD 4 IS 0000, 0000.		
BIT	**MISSILE STAGE**	**BIT IDENTIFIER**
0 -7	NA	Unassigned
8	I	Fault monitor check
9	I	Flight control null check
10	I	Flight control rate check
11	I	Flight control extended (steady state) check
12	I	Flight control lag check (V11) (Nozzle 1)
13	I	Flight control lag check (V12) (Nozzle 2)
14	I	Flight control lag check (V13) (Nozzle 3)
15	I	Flight control lag check (V14) (Nozzle 4)
16	II	Fault monitor check
17	II	Flight control null check
18	II	Flight control rate check
19	II	Flight control extended (steady state) check
20	II	Flight control lag check (V24) (Pintle 1)
21	II	Flight control lag check (V23) (Pintle 2)
22	II	Flight control lag check (V22) (Pintle 3)
23	II	Flight control lag check (V21) (Pintle 4)
24	III	Fault monitor check
25	III	Flight control null check
26	III	Flight control rate check
27	III	Flight control extended (steady state) check
28	III	Flight control lag check (V34) (Pintle 1)
29	III	Flight control lag check (V33) (Pintle 2)
30	III	Flight control lag check (V32) (Pintle 3)
31	III	Flight control lag check (V31) (Pintle 4)

Table 3-23. Fault Data Word 5 - PSRE Actuator Response Test

FAULT DATA WORD 5: PSRE ACTUATOR RESPONSE TEST	
NOTES: THE NO FAULT HEXADECIMAL NUMBER FOR FAULT DATA WORD 5 IS 0000, 0000.	
BIT	**BIT IDENTIFIER**
0	Unassigned
1	Unassigned
2	Unassigned
3	Unassigned
4	Unassigned
5	Unassigned
6	Unassigned
7	Unassigned
8	Fault monitor null error
9	Yaw null position error
10	Pitch null position error
11	Fault monitor extended rate error
12	Yaw extend rate position error
13	Pitch extend rate position error
14	Fault monitor deflected error
15	Yaw deflected position error
16	Pitch deflected position error
17	Fault monitor yaw retract rate error
18	Yaw retract rate position error
19	Fault monitor pitch retract rate error
20	Pitch retract rate position error
21	Unassigned
22	Unassigned
23	Unassigned
24	Unassigned
25	Unassigned
26	Unassigned
27	Unassigned
28	Unassigned
29	Unassigned
30	Unassigned
31	Unassigned

Table 3-24. Fault Data Word 6 - PSRE Valve Control Test

FAULT DATA WORD 6: PSRE VALVE CONTROL TEST	
NOTES: THE NO FAULT HEXADECIMAL NUMBER FOR FAULT DATA WORD 6 IS 0000, 0000.	
BIT	**BIT IDENTIFIER**
0	Unassigned
1	Unassigned
2	Unassigned
3	Unassigned
4	Unassigned
5	Unassigned
6	Unassigned
7	Unassigned
8	Unassigned
9	Unassigned
10	Unassigned
11	Unassigned
12	Unassigned
13	Unassigned
14	Unassigned
15	Unassigned
16	Unassigned
17	Unassigned
18	Unassigned
19	Unassigned
20	PBPS valve fault monitor error
21	Axial valve monitor error
22	Yaw No. 1 monitor error
23	Yaw No. 2 monitor error
24	Pitch No. 1 monitor error
25	Pitch No. 2 monitor error
26	Pitch No. 3 monitor error
27	Pitch No. 4 monitor error
28	Roll No. 1 monitor error
29	Roll No. 2 monitor error
30	Roll No. 3 monitor error
31	Roll No. 4 monitor error

3-2.2.9.3. Critical No-Go. A critical no-go identifies an operational condition that is critical to safety or equipment. Monitoring for existence of a critical no-go condition is performed by the DCU and coupler unit (403A5). A critical no-go word (Table 3-25) is maintained by the DCU to indicate the cause of the no-go condition. A critical no-go condition detected by the DCU results in initiation of controlled processing functions to cause system entry to a nonoperational status. MGS primary power will be removed for all critical no-go detected by the DCU except a G&C no-go that occurs in local, which will result in entry to idle mode rather than shutdown. A critical no-go condition detected by the coupler unit, while monitoring input signals, results in system entry to the critical no-go mode (a nonoperational status). The coupler then sets G&C power-on command false resulting in MGS primary power removal; except an AVE no-go mode that occurs in local which will result in system entry to idle instead of shutdown.

3-2.2.9.4. Alarm History Words. Fifteen alarm history words are available for storage of IMU alarm condition data. Alarm history word 1 is located in SRAM memory and provides storage for the value identifying the most recent IMU alarm condition. A subsequent MOSR update, occurring because of a new IMU alarm condition, shifts alarm history word 1 to alarm history word 2, and shifts alarm history word 2 through 14 to alarm history words 3 through 15. Alarm history word 1 is then updated for storage of current alarm condition. Readout of the alarm history words is performed, using the procedures for dedicated data readout and applicable command codes.

3-2.2.9.5. Gyrocompass Data Words. The three gyrocompass data words provide information applicable to operations of the MGS GCA. Data obtained during readout are described as follows:

a. Angle ϕn: This word contains latest calculated value on angle ϕn (azimuth misalignment angle) measured between the astronomic east-west line and the GCA input axis. Angle ϕn is calculated during alignment and is periodically updated during strategic alert. Angle ϕn is read out in arc seconds following data reduction of its binary form.

b. Angle ϕ3: This word contains latest calculated value of angle ϕ3 (GCA input axis misalignment angle) measured between plane normal to GCA level detector No. 2 and GCA input axis. Angle ϕ3 is initially an MGS parameter tape factory value used during initial alignment and initial strategic alert bias cycles. Angle ϕ3 is updated during PSAT calibration. Angle ϕ3 is read out in arc seconds following data reduction of its binary form.

c. Angle ϕz: This word contains latest calculated value of angle ϕz (azimuth misalignment angle, where $\phi z=\phi n-\phi 3$) measured between plane normal to GCA level detector No. 2 and the astronomic east-west line. Angle ϕz is calculated during alignment and is updated during strategic alert. Angle ϕz is read out in arc seconds following data reduction of its binary form.

Table 3-25. Critical No-Go Word

CRITICAL NO-GO WORD		
NOTE: THE INDIVIDUAL BIT PATTERNS, RECORDED ON THE LF FAULT RECORD FOR THE CRITICAL NO-GO WORD, COMPRISE A BIT PATTERN WHICH IS UNIQUE TO A PARTICULAR CRITICAL NO-GO CONDITION.		
RECORD BIT PATTERN	**HEXADECIMAL NUMBER**	**BIT PATTERN SIGNIFICANCE**
15	0001	Ground ordnance power-on failure
14	0002	Any ordnance driver-on failure
13, 15	0005	Periodic checksum failure
13, 14	0006	AC instrument on failure with good IMU read (IMU Power Failure)
13, 14, 15	0007	TCD validity check failure
12	0008	Master Reset in TCD
12, 15	0009	CSD(G) 19th bit monitor failure
12, 14	000A	Five consecutive indications of missing CIRTIs
12, 14, 15	000B	TCD battery test failure
12, 13	000C	Weapon system configuration check failure
12, 13, 15	000D	Acceptance of MCC while overwrite is in process (remote mode only)
12, 13, 14	000E	Master reset while overwrite in process
12, 13, 14, 15	000F	Initial alignment/startup without a complete tape fill following critical no-go during overwrite in process
11	0010	Illegal address detected
11, 15	0011	Miscellaneous machine error faults
11, 14	0012	Secure code checksum failure
11, 14, 15	0013	Acceptance of IMU Cal 1 command while overwrite is in process (local mode only)
11, 13	0014	Acceptance of OWT command when overwrite sum matches factory penetration codes (remote mode only)
11, 13, 15	0015	Illegal instruction detected
11, 13, 14	0016	Five consecutive indications of multiple CIRTIs
11, 13, 14, 15	0017	Executive no-go in terminal countdown

Table 3-26. IMU Alarm History Words 1 - 15

IMU ALARM HISTORY WORDS 1 – 15			
NOTES: THE CURRENT IMU ALARM DATA IS STORED IN IMU ALARM HISTORY WORD 1. PREVIOUS IMU ALARM DATA ARE STORED IN IMU ALARM HISTORY WORDS 2 - 15.			
RECORDED BIT PATTERN	**HEX NUMBER**	**MOSR SET**	**INDICATED MALFUNCTION**
13, 15	0005	50	GCA slew timer expired while in PIGA leveling (No-Go if P/L exit has been commanded)
11, 14	0012	69	Fine delta Gyro bias limit check X-axis
11, 14, 15	0013	69	Fine delta Gyro bias limit check Y-axis
11, 13	0014	69	Fine delta Gyro bias limit check Z-axis
11, 13, 15	0015	70 and 72	Delta PIGA bias check failure X-axis
11, 13, 14	0016	70 and 72	Delta PIGA bias check failure Y-axis
11, 13, 14, 15	0017	70 and 72	Delta PIGA bias check failure Z-axis
11, 12, 14	001A	53 and 57	Good IMU write detected false during PSAT perturbation sequence
11, 12, 13, 14, 15	001F	50	Absolute value of Q(I) is greater than 7400 or Delta P(n) failed more than 22 times during strategic alert-biasing
10	0020	50 and 59	Gyrocompass equivalent angle fails large angle shift test during steady state with the consistency checks passing
10, 15	0021	50	Four consecutive GCA data stability failures during retarget alignment with no hostile environment
10, 14, 15	0023	52	Gyrocompass bias stability failure during steady state
10, 13	0024	-	Azimuth limit cycle check failure
10, 13, 15	0025	50	PSAT GC scale factor test failure
10, 13, 14	0026	51	PSAT Alpha (mu) failure counter reaches 7
10, 13, 14, 15	0027	51	ϕ_3 estimation error in initial sequence (Good IMU Read/Data detected true) (no errors)
10, 12	0028	50	ϕ_3 estimation error in repeat sequence (Good IMU Read/Data detected true) (no errors)

Table 3-26. IMU Alarm History Words 1 - 15 (Continued)

RECORDED BIT PATTERN	HEX NUMBER	MOSR SET	INDICATED MALFUNCTION
10, 12, 15	0029	55 and 65	Phi calibration check failure for best fit check
10, 12, 14	002A	55 and 65	Phi calibration check failure for best fit parameter check
10, 12, 14, 15	002B	55 and 65	Phi calibration check failure for best estimate check - position 1
10, 12, 13	002C	55 and 65	Phi calibration check failure for best estimate check - position 2
10, 12, 13, 15	002D	55 and 65	Phi calibration check failure for best estimate check - position 3
10, 12, 13, 14	002E	55 and 65	Phi calibration check failure for best estimate check - position 4
10, 12, 13, 14, 15	002F	55 and 65	Phi calibration check failure for best estimate check - position 5
10, 11	0030	55 and 65	Phi calibration check failure for best estimate check - position 6
10, 11, 15	0031	55 and 65	Phi calibration check failure for best estimate check - position 7
10, 11, 14	0032	55 and 65	Phi calibration check failure for best estimate check - position 8
10, 11, 14, 15	0033	55 and 65	Phi calibration check failure for best estimate check - position 9
10, 11, 13	0034	55 and 65	Phi calibration check failure for final goodness of fit check - position 1 through 7
10, 11, 13, 15	0035	55 and 65	Phi calibration check failure for final goodness of fit check - position 8 through 9
10, 11, 13, 14, 15	0037	67	First delta RL failure in LD calibration

Table 3-26. IMU Alarm History Words 1 - 15 (Continued)

RECORDED BIT PATTERN	HEX NUMBER	MOSR SET	INDICATED MALFUNCTION
10, 11, 12, 15	0039	67	First delta RL failure in PIGA calibration
10, 11, 12, 14	003A	51	PSAT alpha (mu) failure of Q_190 and alpha (mu) check
10, 11, 12, 14, 15	003B	70	PIGA leveling platform attitude error check failure - North
10, 11, 12, 13	003C	70	PIGA leveling platform attitude error check failure - West
10, 11, 12, 13, 15	003D	70	PIGA leveling platform attitude error check failure - Vertical
9	0040	54	LAI not set during platform slew
9, 15	0041	48	Low level seismic verification criteria exceeded
9, 10, 11, 12, 13, 14	007E	50 and 59	GCA detected off reference null during an AOA (2nd time) except during calibration, (No-Go if an autoindexing or east 1 AOA)
8	0080	50	155-second GCA slew timer expired while in a null correction GCA slew during PIGA leveling
8, 13	0084	50 and 59	GCA detected off reference null in PIGA leveling (4th time since the last control cycle)
8, 13, 15	0085	53	ϕ_3 estimation error in repeat sequence with Good IMU Read/Data detected false in initial sequence only
8, 13, 14	0086	53 and 57	Good IMU Read/Data detected false in repeat ϕ_3 sequence
8, 13, 14, 15	0087	51 and 57	Good IMU Read/Data detected false in initial ϕ_3 sequence
8, 12	0088	55 and 65	Initial Phi calibration check failure for best fit parameter check

3-2.2.9.6. Autoalignment Data Words. The autoalignment data words (Angle ϕr and Angle $\Delta\phi$r) provide data that are relative to the initial emplacement alignment of the missile. Data word descriptions are as follows:

a. Angle ϕr (missile roll attitude angle): Latest calculated value as measured from missile body (positive Zb axis) to north. The ϕr value, measured in gimbal counts, is defined as negative in the counterclockwise direction. Data are read out at discretion of Job Control, after the guidance-control system has attained strategic alert following either an initial startup or restart. Recorded data, read out in gimbal counts in binary form, are

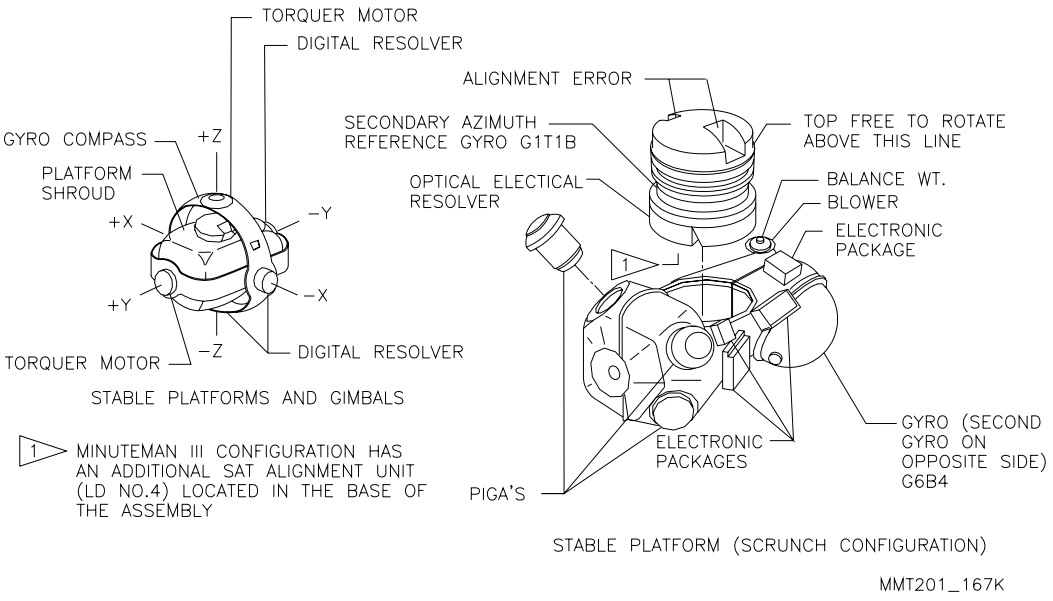
reduced to a degrees value for the purpose of determining missile alignment status and probability of need to reindex the missile.

b. Angle $\Delta\phi r$ (platform slew correction angle): A calculated change to the missile roll attitude angle (ϕr) which, when added to the previous (old) ϕr value results in an updated (new) ϕr value. The $\Delta\phi r$ value, converted to gimbal counts, is defined as positive in the clockwise direction. Data are read out in gimbal counts in binary form at discretion of Job Control, whenever MOSR 50 (GCA failure No. 1) has been set true and system has entered the standby no-go mode.

3-2.2.9.7. Fault History Words. Ten fault history words, 1 through 10, contain a sequential accumulation of fault data word 1 failure data stored in SRAM memory. Upon entry to standby no-go, IMU failure data are stored in fault data word 1. Previously stored IMU failure data in fault history words 1 through 9 are shifted to fault history words 2 through 10, respectively. The fault history word data are initialized to zero during a complete tape loading but remain unaffected by a partial tape loading or by non-IMU failures. Readout of the fault history words is performed using the procedure for dedicated data readout and applicable command codes.

3-2.2.9.8. Expanded Data Words. The operational ground program provides an expansion of the dedicated data readout capability of specific physical regions of DCU SRAM memory that contain fault data and status, and IMU performance data. These data words, read out only upon direction of Job Control or when directed by procedure(s), provide stored data that can be used by personnel to perform further fault analysis. The readout data are also used for comparative purposes following a subsequent fault analysis readout which is performed at a repair facility.

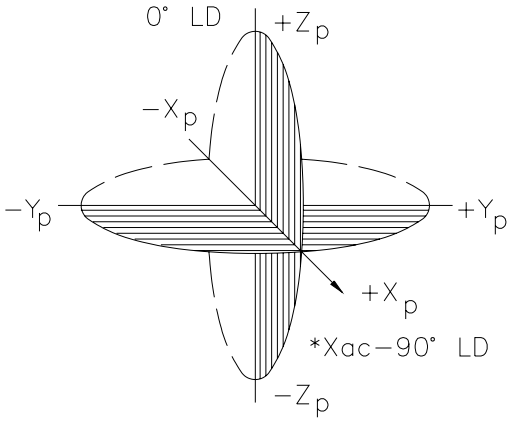
3-2.3. Gyro Stabilized Platform. Figure 3-10 shows the configuration of the stable platform. Two orthogonal gyros provide the stabilizing and relative motion sensing elements of the gyro stabilized platform. These two gyros establish a rectangular coordinate system (3 axes) for platform reference (See Figure 3-11). (One of the sensitive axes of one of the gyros remains caged at all times). Three Pendulous Integrating Gyroscopic Accelerometers (PIGA) arranged in a scrunch configuration on the platform detect platform accelerations. The scrunch configuration offsets the PIGA axes from the platform axes and allows in place calibration and monitoring of PIGA performance. In that position each of the three PIGAs senses a component of gravity acceleration which can be used to measure the continuing performance of each PIGA. Digital resolvers (3) detect angular movement between the platform and the missile. Platform torque motors (3) enable computer control over repositioning information, and includes 4 level detectors used for positioning the platform with reference to the local gravity vector. Figure 3-12 is a flow diagram of the computer directed platform control circuitry.



	DEVICE	FUNCTION	USE OF INFORMATION
1.	PIGAs	Sense missile acceleration and send velocity information to the D37 computer.	DCU uses this information to stage the missile and compute when to generate thrust termination.
2.	Platform Gyros (2) G6B4	Sense angular movements of the stable platform from a fixed reference (established by the collimator and platform level detectors).	Sends an error signal to the platform torque motors.
3.	Platform Torque Motors (3)	Receive error signal from platform gyros causing angular movement of stable platform.	Corrects platform angular position back to reference.
4.	Platform Digital Resolvers (3)	Detect angular movement of the platform relative to the missile.	DCU uses this information as an indication of missile angular attitude for generating nozzle steering commands.
5.	Gyrocompass Assembly G1T1B	Senses azimuth variations and provides an indication to the D37D (ground program only).	DCU uses this information in two ways: a. For positioning stable platform to a target heading. b. As a secondary azimuth reference for platform gyros.
6.	Platform Level Detectors (4)	Detect gravity vertical and sense any movement of the stable platform off the horizontal plane.	DCU uses this information to establish the horizontal reference to the platform gyros.

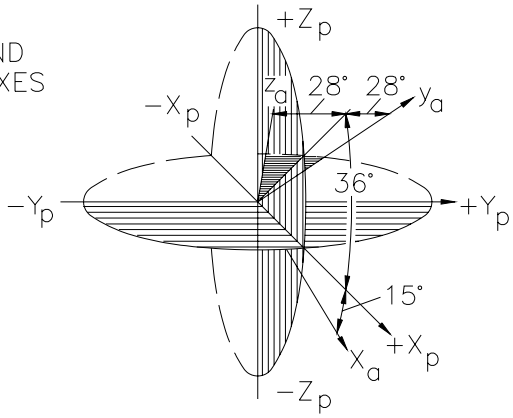
Source: D2-31044-3

Figure 3-10. Stable Platform and Components



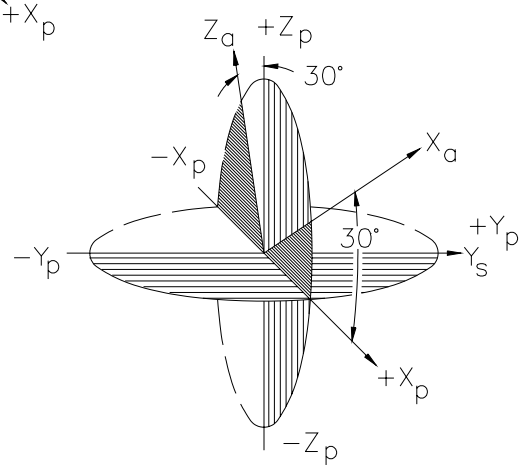
PLATFORM, GCA, AND
LEVEL DETECTOR AXES

*WHEN GCA AND PLATFORM BOTH ORIENTED
NORTH AND 0° LD SELECTED



PIGA INPUT AXES

NOTE: Y−Z PLANE NOT SHOWN



G6B4 GYRO INPUT AXES

SOURCE: C84−309/201

MMT201_168K

Figure 3-11. Platform Functional Axes

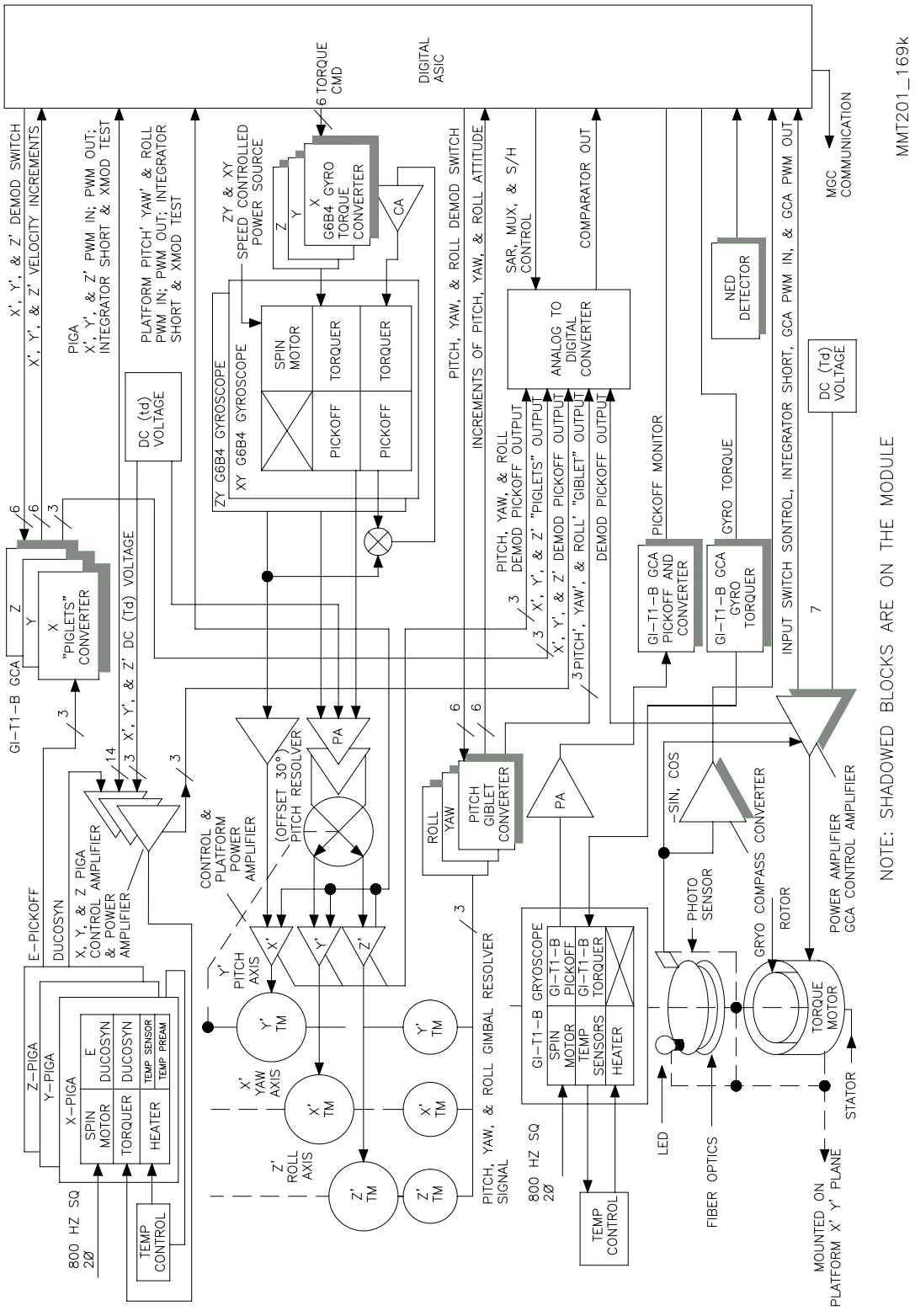


Figure 3-12. Platform Control Functional Diagram

3-2.4. Missile Guidance Set Control (MGSC). The MGSC contains the electronics required for the operation of the GSP, including power supplies, servo amps, gyro torquing circuits, and fan control. A serial communications interface is provided for processing of software commands from the MGC. The MGSC provides the electronics to close the PIGA, G6B4, GCA and platform servo loops. Figure 3-13 shows a block diagram of the MGSC and its interfaces with the GSP.

3-2.5. Permutation (P) Plug. The permutation plug is a fixed wire logic used to store two (2) twenty-four bit codes. The output of the P-plug is sent to the MGC and used to validate the receipt of a correct launch command. The P-plug words are also checked as part of the CMSC routine. During the CMSC the OGP insures the two P-plug words are not in memory at the same time. The P-plug words are overwritten as soon as the computations using them are completed.

3-3. PSRE DESCRIPTION. The propulsion system rocket engine, physically located in the CD2-4A missile body section, adds range and payload to the Minuteman capabilities and is operational above 300,000 feet. See Figure 3-14.

a. The PSRE is a liquid propellant, highly maneuverable fourth stage which will add to the time of controlled flight.

b. The system consists of a fuel tank containing monomethyl hydrazine and an oxidizer tank containing nitrogen tetroxide. The fuel and oxidizer are hypergolic (ignite instantly on contact with each other) so no ignition system is needed. Rather, the fuel and oxidizer are forced through bi-propellant valves into each of the rocket motor chambers under pressure from helium contained in a spherical tank at 3200 psia. Control of the firing period is accomplished with the bi-propellant valves which receive control signals from the MGC.

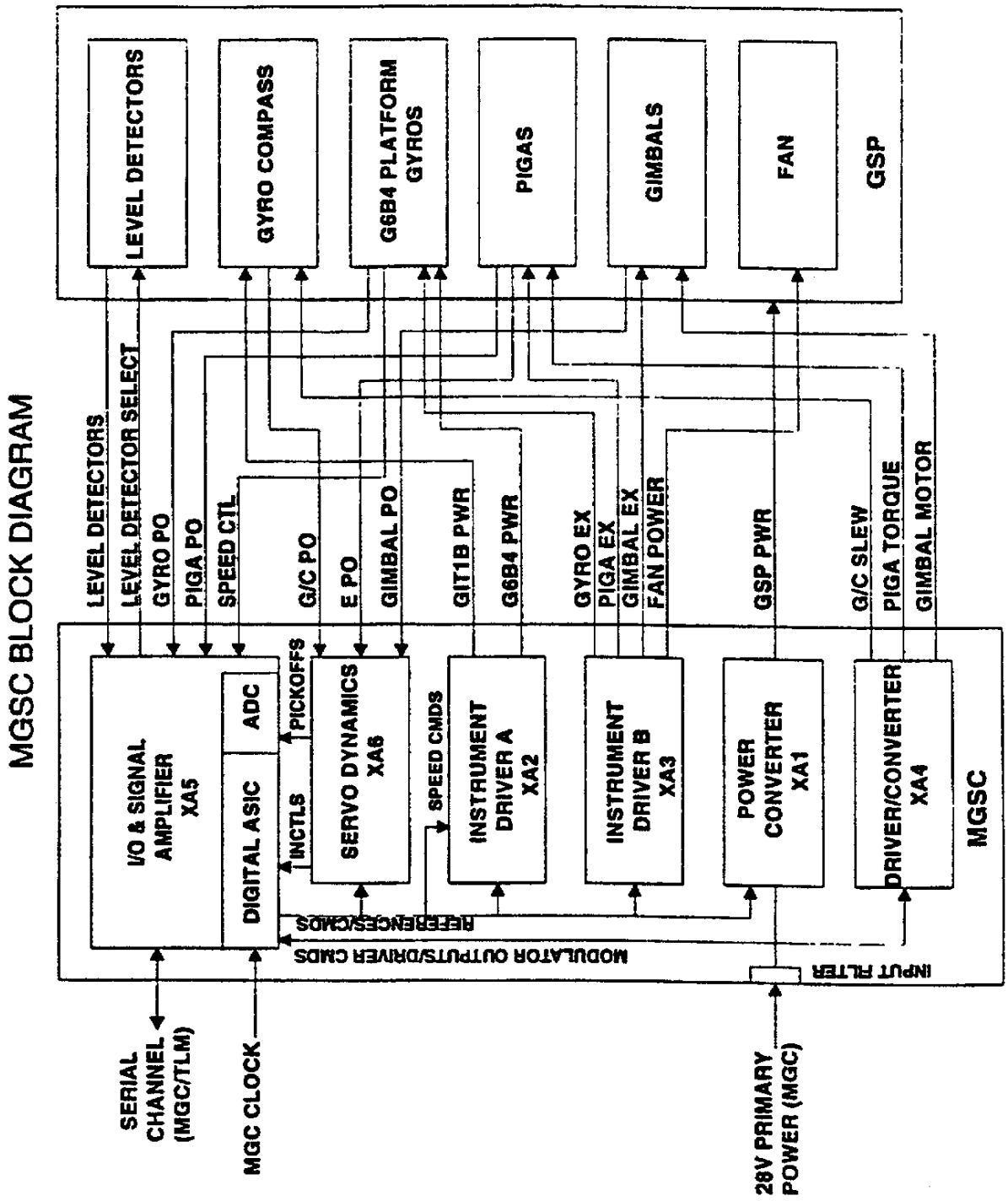


Figure 3-13. MGSC Block Diagram

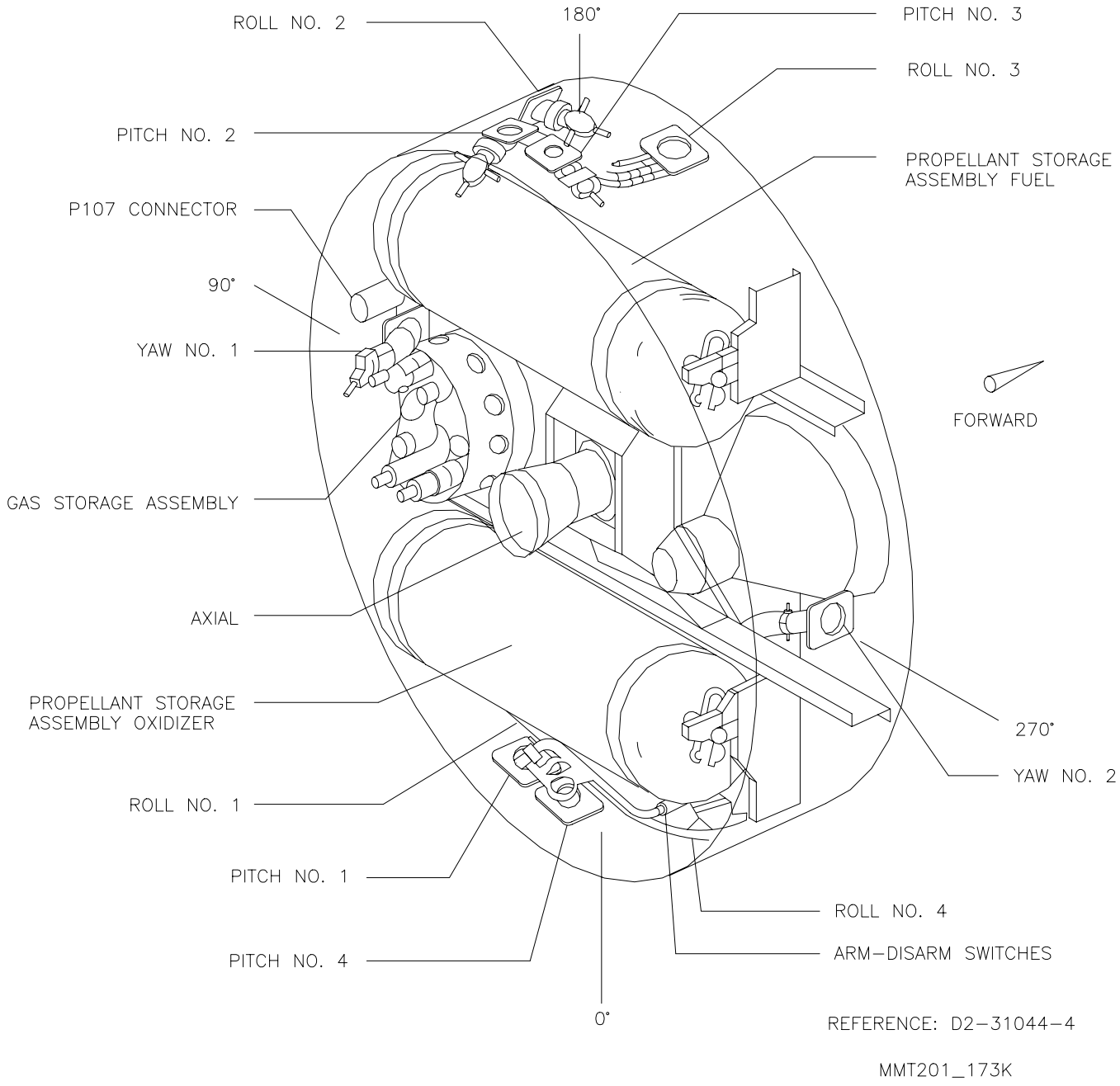


Figure 3-14. Propulsion System Rocket Engine A/A44A-4

c. There are 11 rocket engines in the PSRE. There are four engines for pitch, four for roll, two for yaw, and one axial engine for forward thrust.

d. The system carries approximately 160 pounds by weight of nitrogen tetroxide and approximately 100 pounds by weight of monomethyl hydrazine. There are equal volumes of each, thus the ratio by weight of expulsion of oxidizer to fuel is 1.6 to 1.

e. The fuel, the oxidizer, and the pressurant are physically separate until use by squib activated tank isolation valves. The downstream isolation valves are opened first to allow the fuel and oxidizer to flow into the bi-propellant valves prior to pressure being applied. The helium flows through a regulator set at 240 psia prior to reaching the bellows in the fuel and oxidizer tanks.

3-3.1. PSRE Assemblies. The individual assemblies of which the PSRE is comprised are described as follows:

a. The gas storage assembly contains gaseous helium in a 12.456" dia. titanium spherical tank at storage pressures in the range of 3200 psia at 120°F. The pressurant tank is filled (before shipment) through a manually operated fill and drain valve which is subsequently capped and welded to prevent pressurant leakage. Helium pressure can be monitored by a pressure transducer which is capable of responding to pressures from 0 to 3500 psia. Low pressure indication is provided by a go-no-go pressure switch which is activated at a nominal pressure of 2960 psia. The pressure is isolated from a regulator and propellant storage assemblies by a normally closed squib actuated valve. The regulator provides nominal pressures of 240 psia with a maximum lockup pressure of 247 psia. A filter for contamination control is located downstream from the squib actuated valve (Isolation Valve-Gas) and two test ports, one on each side of the regulator.

b. The propellant storage assembly is designed for a minimum propellant storage life of six years and is capable after system activation, of supplying propellant to the thrust chambers of all engines at any attitude in a zero G environment. The propellant storage assemblies are identical except for a planned difference in the fill and drain valves to prevent incorrect mating of the fill tools to the assemblies.

3-4. OPERATIONAL PROGRAM. The computer program, contained on a magnetic tape cartridge, provides the Digital Computer Unit (DCU) with the software program necessary for ground monitoring, target and launch execution plan change, code processing, and in-flight control. Program information is provided as a number of files containing fixed and variable data recorded on a four-track magnetic type cartridge. Three types of launch facility load cartridges (LFLC) are generated by the Wing Code Processing System (WCPS) using data from the Missile Guidance Set (MGS) parameters tape, the Operational Ground Program/Operational Flight Program (OGP/OFP) tape, the flight program constants tape and the W data. A complete load cartridge is used to completely load the static random access memory (SRAM) in the DCU. A code change LFLC is used for performing code change at the Launch Facility (LF), and a Penetration D LFLC is used for local overwrite at the LF, and may be used to disable the SRAM battery by setting the battery discrete flag to true, purging the SRAM memory for long term system shutdown. See Figure 3-15 for Software Operational Interfaces.

a. The operational programs contained on the LFLC are loaded in the sequence listed below for a compete tape load:

Program	Track	File
Pen D	1	00
DCU Complete Load	1	01
DCU Verify File	2	00

b. The Code Change LFLC contains the Pen D and Code Change files for up to 10 launch facilities and is loaded in the following order:

Program	Track	File
Pen D (1st LF)	1	00
Code Change File (1st LF)	1	01
Pen D (2nd LF)	1	02
Code Change File (2nd LF)	1	03
- - - Continue for up to 10 LFs - - -		

c. Local Overwrite is accomplished by successfully loading a Pen D Cartridge containing only the Pen D file and entering Command Code 8 on the C-MON. As a last resort, memory can also be erased by disconnecting the SRAM Battery, but all maintenance data stored in SRAM will also be lost.

d. W-DATA. The OGP shall provide memory locations and interpret the W-DATA as follows:

(1) One vote launch time (KT) is in 0.18 second increments.

(2) One vote launch time modifier #1 (KA) is non-dimensional.

(3) The ALCC hold off time is in 0.9 second increments.

(4) The LF address is represented in binary XXXXYYY where XXXX = 0100 through 1101 (LFs 2-11 in backward binary), YYY = 100 through 101 (flights 1-5 in backward binary).

(5) The launch point gravity term is the value of gravity that exists at the window of the G&C section of the missile in ft/sec^2.

(6) The astronomic latitude measured at the center of the launch tube (rad), pre-multiplied by $2/\pi$, plus the sine and cosine of the astronomic latitude of the launch point (non-dimensional).

(7) A variable to define the weapon system configuration (WS-133AM=0) WS-133B=$FFFF_{16}$.

(8) A checksum such that the sum of all the data listed above loaded by this file equals $BBBBBBBB_{16.}$

(9) Secure Code Data, to include ten R-Code words, two Inhibit Command Secure Code words, the SELECTIVE ENABLE B-Code, and a checksum such that the sum of all the Secure Data equals $CCCCCCCC_{16}$.

(10) Penetration Change Data consists of new secure penetration codes. A 32-bit linear checksum of the Penetration Codes is included in the W-Data so the sum of the Penetration Codes and the checksum balancing value equals $DDDDDDDD_{16}$.

(11) The W-Data provides two screen and two control words for use during the CMSC computation.

(a) Screen Word - $S_{(S)}$ (SS)

(b) Screen Word - $S_{(f)}$ (SF)

(c) C(a) Control Word - C_a

(d) C(b) Control Word - C_b

3-4.1. LF Unique Data.

a. Penetration Data File. The CTU transfers a 4-bit Record ID, six 16-bit penetration code words, and a 16-bit checksum value from the LFLC penetration data file to DCU memory in 4-bit "nibbles". If all of these values match the values currently stored in DCU dedicated memory, the DCU enters the Load Mode and the factory penetration code is loaded from the LFLC (0539_{16}, 7705_{16}, 3977_{16}, 0539_{16}, 7705_{16}, 3977_{16}). The factory penetration code exists on all files to facilitate memory loading, having once penetrated with a secure code.

b. Missile Guidance Set Parameters Tape. The Missile Guidance Set Parameters are loaded into a section of contiguous memory by the DCU complete load file. This data includes factory calibrated parameters for the gyros, the PIGAs, the platform level detectors, and other physical parameters, bias values, and scale factors unique to the individual guidance set. The serial number for the MGS, MGSC, MGC, and GSP are also included. A checksum is included such that the sum of all the locations filled by this file equals $AAAAAAAA_{16}$.

c. Flight Program Constants Tape. This tape provides configuration dependent constants used by both the Flight Program and the Ground Program. Data includes the number of RVs to be fused, the RS configuration ID (MK12 or MK12A) Earth Rate, NEP timer value, and various flight control and reentry system mission parameters. A checksum is included such that the sum of all the locations filled by this file equals $EEEEEEEE_{16}$.

3-4.2. LF Common Data.

a. Operational Ground Program (OGP). The OGP provides ground program routines for control and status monitoring of AVE and OGE operations. The OGP includes a CMSC routine in MGC ROM for verifying that untampered file data were properly loaded into the SRAM memory and initiates the CMSC computation sequence. The OGP performs the following functions:

(1) Maintains the guidance system level and aligned in azimuth through the pre-launch phase.

(2) Decodes and processes command, data, and interrogation-type messages received from the Programmer Group (P/G), C-MON, C604, or C631AA.

(3) Conducts and processes AVE and AGE tests and reports status.

(4) Monitors, processes, and reports AVE and AGE status.

(5) Sequences the AVE and AGE through the initial portion of a terminal countdown (TCD) sequence.

(6) Performs a CMSC after any tape set fill sequence.

b. Operational Flight Program. The Operational Flight Program provides routines to control AVE operations from approximately 21 seconds prior to stage 1 ignition through initiation of the Reentry System (R/S) electrical disconnect command.

3-4.3. DCU Tape Load and Verify Sequence. DCU Tape Load and Verify begins when the DCU enters load mode processing and penetration codes are loaded into memory. A complete load cartridge is required to complete DCU tape load and verify operations. When tape loading begins, penetration codes are read from the tape and compared to the penetration codes stored in dedicated memory. A match opens the DCU Random Access Memory (RAM) to tape fill and verify operations. Upon completion of tape fill and verify operations, factory penetration codes are replaced with secure penetration codes and CMSC processing is performed. During the tape load, the SRAM battery is disconnected via a software switch during fill and verify operations and reconnected prior to CMSC processing. This is a result of the scheme implemented to disconnect the SRAM battery when AVE power will be shut down for an extended time.

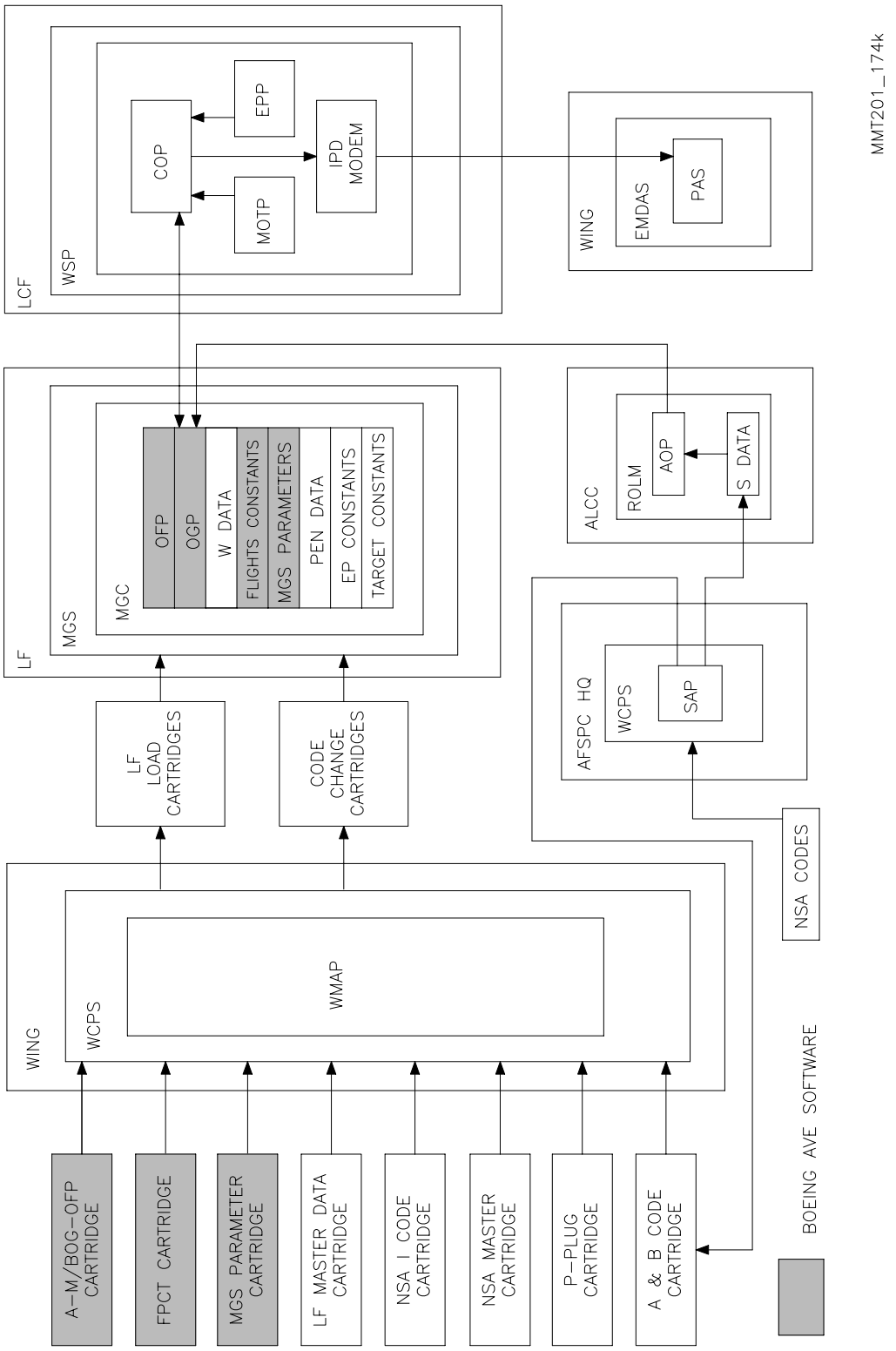
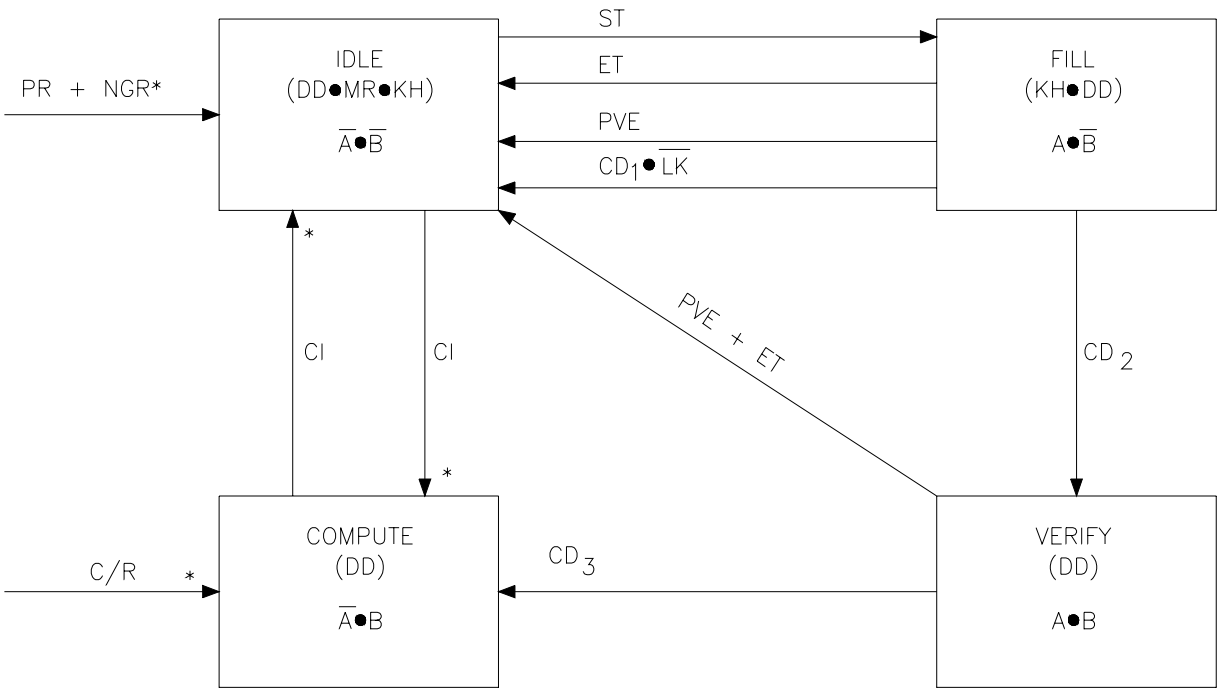


Figure 3-15. GRP Operational Software Interfaces

3-5. C604 GUIDANCE AND CONTROL COUPLER. The guidance and control coupler (C604A) resides in the A5 position of the LF Figure A 1201 programmer group and is the prime electronic interface between the MGS and the EGS. The multiplexer section of the C604 receives 80 status items from the LF. This status is divided into 16 groups (A through S) of 5 items (1 through 5) per group. The DCU monitors each status group by issuing the appropriate character output code for that status which is then monitored by the DCU on the X1-X5 lines. The decoder section of the coupler receives the character output from the DCU and converts it to perform the action requested by the DCU. The G&C coupler monitors and controls the MGS during startup, test, and prelaunch alert readiness, and responds to DCU character output commands to support test and launch sequences. It also acts as a buffer for DCU character output commands routed to the programmer group ordnance monitor (A6). Figure 3-16 is an activation and control sequencing diagram of the G&C coupler. Table 3-8 defines the DCU character output commands to the C604 coupler and the ordnance monitor drawer. As can be seen in Table 3-8, the data readout character output codes are intended for the C-MON. Table 3-2 is a listing of the C604/DCU multiplexer status bit/set assignments.



*ENABLE FOR LOCAL OR REMOTE MODES
ALL OTHERS LOCAL MODE ONLY

A – MODE MEMORY F–F
B – MODE MEMORY F–F
CD_1 – FILL STEERING COMMAND
CD_2 – VERIFY STEERING COMMAND
CD_3 – COMPUTE STEERING COMMAND
CI – COMPUTE/IDLE COMMAND

C/R – CIRCUMVENTION RESET
DD – DISABLE DISCRETES
ET – END OF TAPE
KCC – COMPUTE MODE INDICTOR
KH – HALT

LK – LOAD MODE INDICATOR
MR – MASTER RESET
NGR – NO–GO RESET
PR – POWER ON RESET
PVE – PARITY/VERIFY ERROR
ST – START TAPE

MMT201_180k

SOURCE: D2–31044–3

Figure 3-16. Mode Control Memory Sequencing, G&C Activation and Control - G&C Coupler (C604A)

3-6. LOCAL COMMUNICATIONS. The C-MON provides capability for local communications between the DCU and a maintenance team at the LF. The C-MON is used to support startup, program loading, command/interrogation initiations, and status monitoring. Continuous status monitoring is available at anytime with the C-MON. Commands and interrogations can only be initiated when the C-MON and the DCU are in the local mode (controlled by the local/remote switch on the C-MON). The DCU provides system status to the C-MON via the character output lines once every 250 ms except that missile test status is provided at least once during the first part of the test. Table 3-27 defines the C-MON DCU readout status lights corresponding to system status and the character output codes that provide them. Table 3-28 defines the C-MON command codes which (in local) direct the MGS into various operating modes. The DCU monitors the C-MON keyboard inputs every 250 milliseconds and if the command is received during a valid operating mode, will execute the command. Table 3-29 defines the meaning of the LF status sets monitored by the C-MON.

3-6.1. C-MON Keyboard Control/Readout. Control/readout functions of the C-MON keyboard are described as follows:

a. Command and readout functions associated with the missile computer (DCU) and C-MON are enabled only under the local mode of launch facility operation as selected by the C-MON operator. These functions are therefore classified as local communications to distinguish them from the normal DCU/launch control center (LCC) command and status link referred to as remote communications. Under local mode the DCU is required to receive, interpret and act upon commands and interrogations from the C-MON in lieu of those from the LCC. The local mode is entered upon the DCU detecting a local signal originated by the C-MON and routed via the G&C coupler to the DCU.

b. Commands or interrogations are routed from the C-MON to the DCU via the G&C Coupler multiplexer. The DCU response to a command may be mode change or a test. Responses to an interrogation take a form of data presented to the operator on the C-MON readout lights. The R multiplexer is sampled for commands once each 250 milliseconds. For a command to be recognized, the computer must detect at least two consecutive, identical samples. The zero character is used as a separator between input characters.

c. Data can be manually retrieved from the DCU memory in local operations by reading out Dedicated Data (MOSRs, FDWs, etc.) (refer to 3-2.2.9 and Table 3-17), a single memory location, a block of up to 63 consecutive memory locations, or a dump of all DCU Maintenance Data (SELECT 880 data dump). In addition, system status (see Table 3-27) is displayed on the C-MON readout lights whenever the system is in the local mode.

d. Whether in the local or remote mode of operation, LF status can be obtained directly from the C604A via the status group select switch on the C-MON. The status in Table 3-27 is displayed on the C-MON LF status lights.

Table 3-27. Controller Monitor System Status Display

ITEM NO.	INDICATION	CHARACTER OUTPUT ISSUED (NOTE)	CONTROLLER MONITOR DISPLAY
1	Standby No-Go	READOUT0	0
2	Restart	READOUT1	1
3	PSAT Calibration	READOUT2	2
4	Strategic Alert PIGA Leveling	READOUT3	2-1
5	Strategic Alert Biasing	READ4INIT	4
6	Alignment	READOUT5	4-1
7	IMU Calibration 1	READOUT6	4-2
8	IMU Calibration 2	READOUT6	4-2
9	Phi Calibration	READOUT6	4-2
10	Missile Test	READOUT7	4-2-1
11	Fault Data Changed and Standby No-Go	READOUT8	8
12	Fault Data Changed and Restart	READOUT9	8-1
13	Fault Data Changed and PSAT Calibration	READOUT10	8-2
14	Fault Data Changed and Strategic Alert PIGA Leveling	READOUT11	8-2-1
15	Fault Data Changed and Strategic Alert Biasing	READOUT12	8-4
16	Fault Data Changed and Alignment	READOUT13	8-4-1
17	Fault Data Changed and IMU Calibration 1	READOUT14	8-4-2
18	Fault Data Changed and IMU Calibration 2	READOUT14	8-4-2
19	Fault Data Changed and Phi Calibration	READOUT14	8-4-2
20	Standby No-Go and Overwrite in Process	READOUT15	8-4-2-1

Note: READ4INIT must be issued before every character output specified in the table to display system status.

Table 3-28. C-MON Local Keyboard Commands

ITEM NO.	COMMANDS	CONTROLLER MONITOR KEYBOARD COMMAND	COMMAND NUMBER
1	Advance	1	1
2	Individual Data Readout (single memory location)	2	2
3	IMU Calibration 1	2-1	3
4	IMU Calibration 2	4	4
5	Phi Calibration	4-1	5
6	Fault Data Change Unlatch	4-2	6
7	Missile Test	4-2-1	7
8	Overwrite	8	8
9	PSAT Calibration	8-1	9
10	Exit Data Readout	8-2	10
11	Select 880 Data Dump	8-2-1	11
12	Block Data Readout	8-4	12
13	Standby No-Go	8-4-1	13
14	IMU Performance Data Halt	8-4-2	14
15	Dedicated Data Readout	8-4-2-1	15
16	Idle	0	0

Table 3-29. C-MON LF Status Groups

STATUS	FUNCTION
A1	Multiplexer Control - MA
A2	Multiplexer Control - MB
A3	Multiplexer Control - MC
A4	Multiplexer Control - MD
A5	Multiplexer Test
B1	Multiplexer Output
B2	Multiplexer Output
B3	Multiplexer Output
B4	Multiplexer Output
B5	Multiplexer Output
C1	P/G Monitor Fault
C2	Coupler Test
C3	Critical Status Override
C4	Loss of Keep Alive (SD_6)
C5	1st/2nd Character
D1	Mode Control A_M
D2	Mode Control B_M
D3	Startup Indicator
D4	Disable Discretes
D5	Enable Write
E1	CSD(M) Drive Enable
E2	CSD(M) Mark & Step
E3	CSD(M) Space and Step
E4	CSD(M) 24th Bit Monitor
E5	CSD(M) Home Monitor
F1	Any Ordnance Driver On
F2	CSD(M) Reset
F3	CSD(G) Mark
F4	CSD(G) Space
F5	R/S Ground Power

3-6.2. SELECT 880 Data Dump. The SELECT 880 Data Dump shall allow retrieval of all DCU Mainenance Data from the DCU when operating in the Local Mode. Keyboard Command 11 from the C-MON shall initiate the data dump sequence. The data is output to the SELECT 880 via character output in hexadecimal format. The memory addresses of the first and last buffer location are also output in hexadecimal format. The data dump may be terminated by issuing Keyboard Command 10 from the C-MON.

SECTION IV - LCC: WEAPON SYSTEM PROCESSOR

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LIST OF TABLES

4-1. SCOPE. This section contains a detailed description of the Weapon System Processor (WSP), including its major components, internal and external interfaces, software, and self tests. Cabling internal to the WSP is shown in this section; cabling external to the WSP is contained in Section 9. The WSP is located within the Weapon System Control Console.

4-2. WSP GENERAL DESCRIPTION. The Weapon System Processor is a general purpose processor whose components and interfaces are shown in Figure 4-1. The organization of the WSP is described in the subparagraphs that follow. Characteristics of each component, and direct-interface characteristics for each component, are described in paragraph 4-3.

4-2.1. Central Processor. The central processor for the WSP is the Raytheon Single Module Computer (SMC810). This is a VAX-type computer that executes the VAX instruction set. It accesses Random Access Memory (RAM) modules over a private memory bus (MEbus), and communicates with input/output (I/O) modules over a modified VAX Bus Interface (VAXBI-M). The termination for the VAXBI-M is the VAX Expansion System Support (VESS) module.

4-2.2. Main Memory. Main memory for the WSP is the Embedded Modular Array Dynamic (EMAD). There is one board with 4 MBytes of memory installed in the system, and an expansion capability of one additional board. Note: 1 MByte = 1024 x 1024 Bytes = 1,048,576 Bytes. There is also local memory on the SMC810 and on some of the I/O modules.

4-2.3. Input/Output. I/O modules for the WSP consist of two Raytheon RMB32 modules, a Raytheon Small Computer System Interface (RSCSI) module, a Loral CDA/IPD interface card, two GTE controller modules for the Visual Display Units (VDUs), a Loral Launch Control Panel (LCP) interface module, a Loral Launch Enable Panel (LEP) interface module, a Loral Communications Message Processing Group (CMPG) interface module, and a Loral Black Discrete Interface (BDI) module. Although the activities of these modules may be commanded by the central processor, each of them acts asynchronously to the central processor, and carries out its interface protocol independent of the central processor.

4-2.4. Power Supply. The Red Power Supply provides all power required by the WSP. It is distributed directly to the Red section of the WSP, and through filters to the Black section.

4-2.5. Red and Black Sections. The WSP is divided into two sections, Red and Black, shown functionally in Figure 4-1 and physically in Figure 4-2.

4-2.5.1. 9-slot Backplane. The Raytheon 9-slot backplane (slots A1-A9) is in the Red section and provides the VAXBI, Memory Expansion Bus, and I/O interconnection facilities for the SMC810, EMAD, RMB32, RSCSI, VESS, Power Supply and CDA/IPD modules. The 9 slot backplane has spare slots for an additional EMAD module and an I/O module. The backplane provides keyed connectors to prevent insertion of incorrect modules into each slot.

4-2.5.2. Red Backplane. The Loral-developed Red Backplane (slots A10-A13) is in the Red sections and accommodates the VDU Controllers and the NED/Printer Switch. It has one spare slot which is wired to a connector. The Red Backplane also provides a transition from the 9-slot backplane to the rear panel WSP connectors and to the Black section.

4-2.5.3. Black Backplane. The Black Backplane is in the black section and provides 6 slots (A14-A19) for the LEP Interface, LCP Interface, Black Discrete Interface, and CMPG Interface modules (CMPG A and B). The backplane routes the I/O signals from these cards to connectors which are then wired to the rear WSP connectors and the Red section. There is one spare slot in this backplane which is wired to a connector on the backplane.

4-2.5.4. Red/Black Isolation Filters. The Red/Black Isolation Filters (there are four types, shown in Figure 4-3) provide the electrical connection between the Red and Black sections. The purpose of the filters is to allow the desired signal to pass between the sections but to block any high frequency signals that may have coupled onto the line. The filters are due to TEMPEST requirements.

4-2.6. Internal Cabling. Figure 4-3 shows the internal cabling for the WSP. Connectors P1-P5 are at the boundary of the WSP and provide the interfaces to the devices listed under each. Table 4-1 traces the connector and pin number from each component of the WSP to the boundary of the WSP. Tables 4-1, 4-2, 4-3, etc., are used in conjunction with Figure 4-3.) Cabling external to the WSP is contained in Section 9.

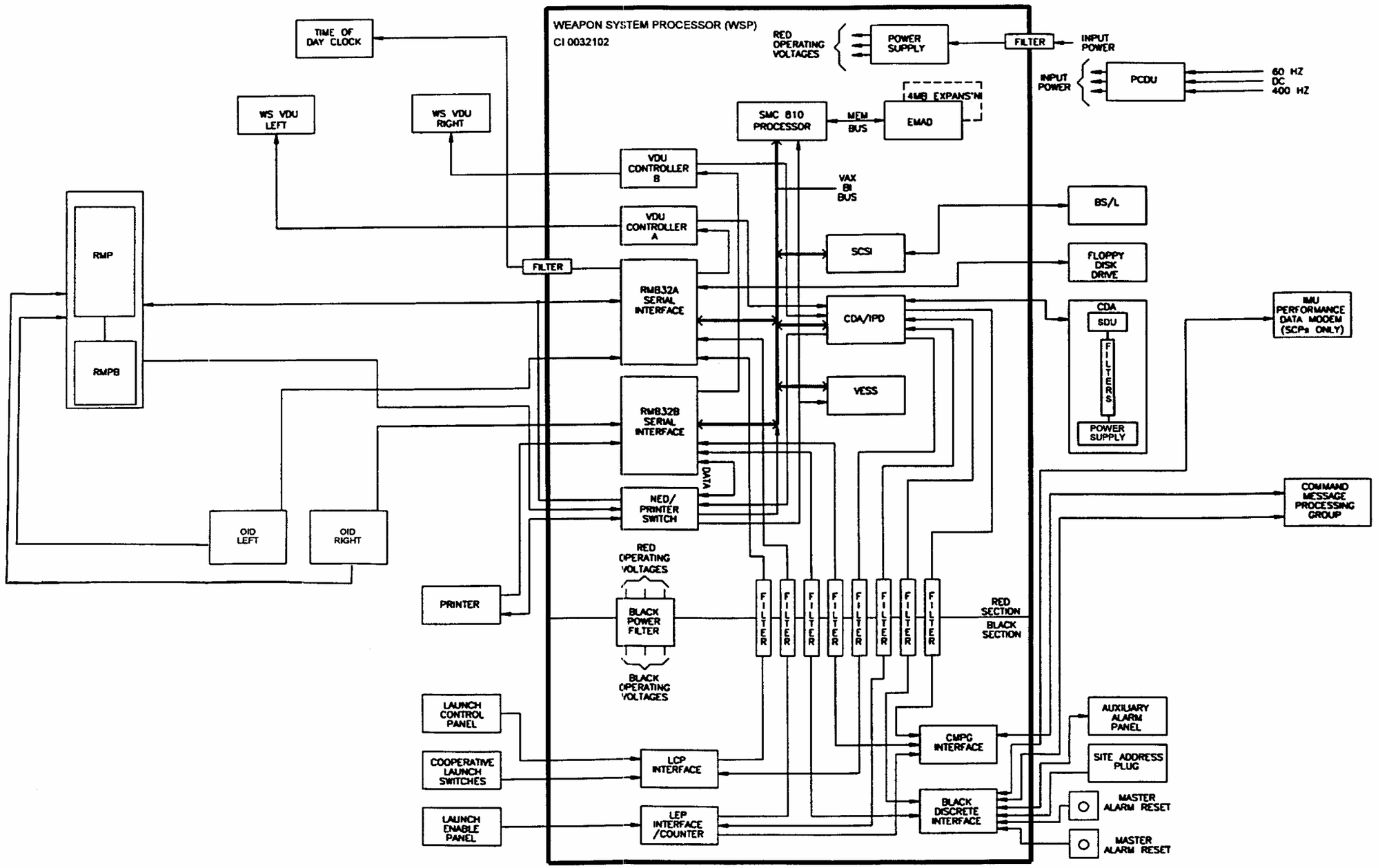


Figure 4-1. WSP CI Interface Block Diagram

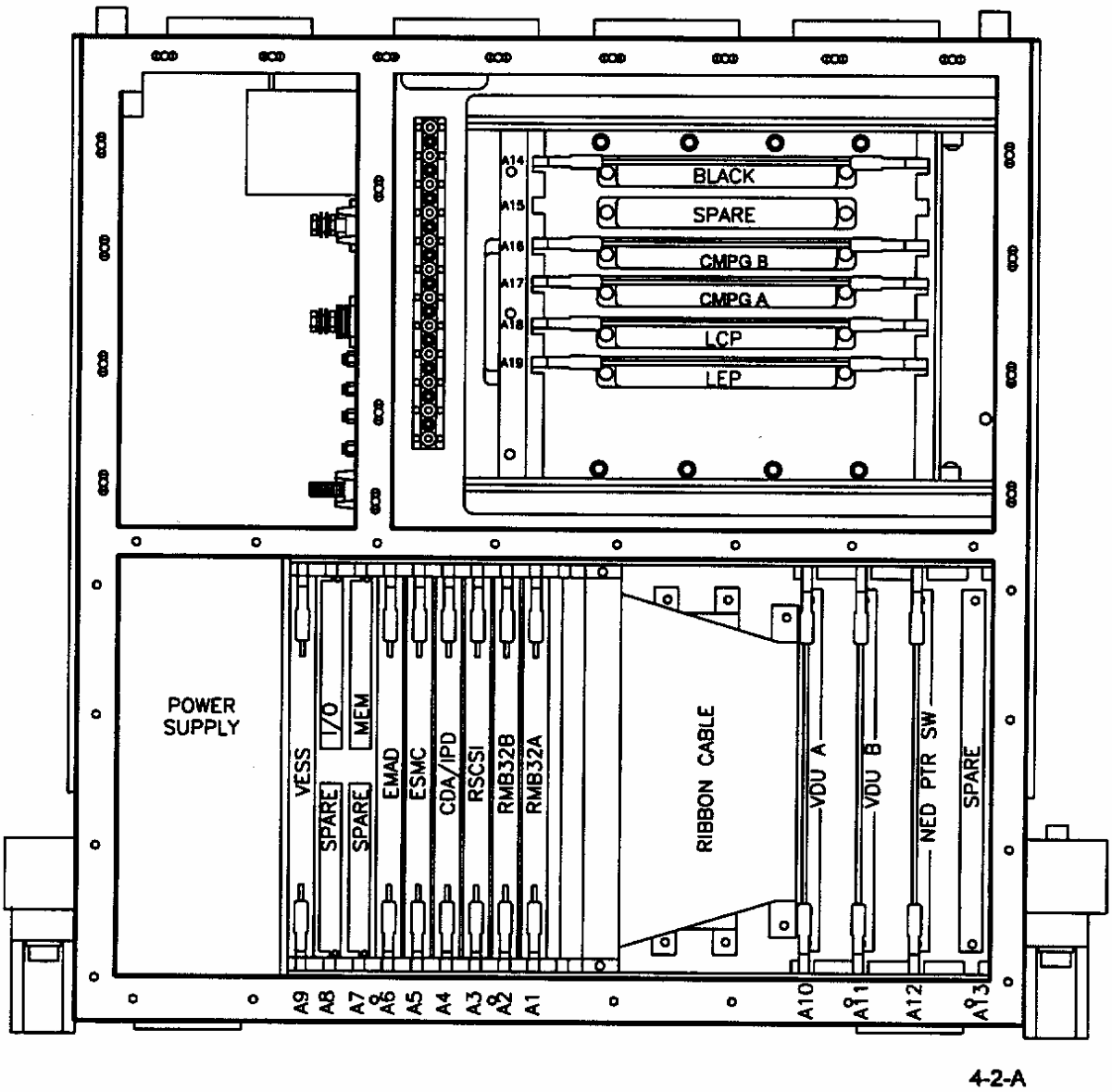


Figure 4-2. Physical Layout of WSP Chassis

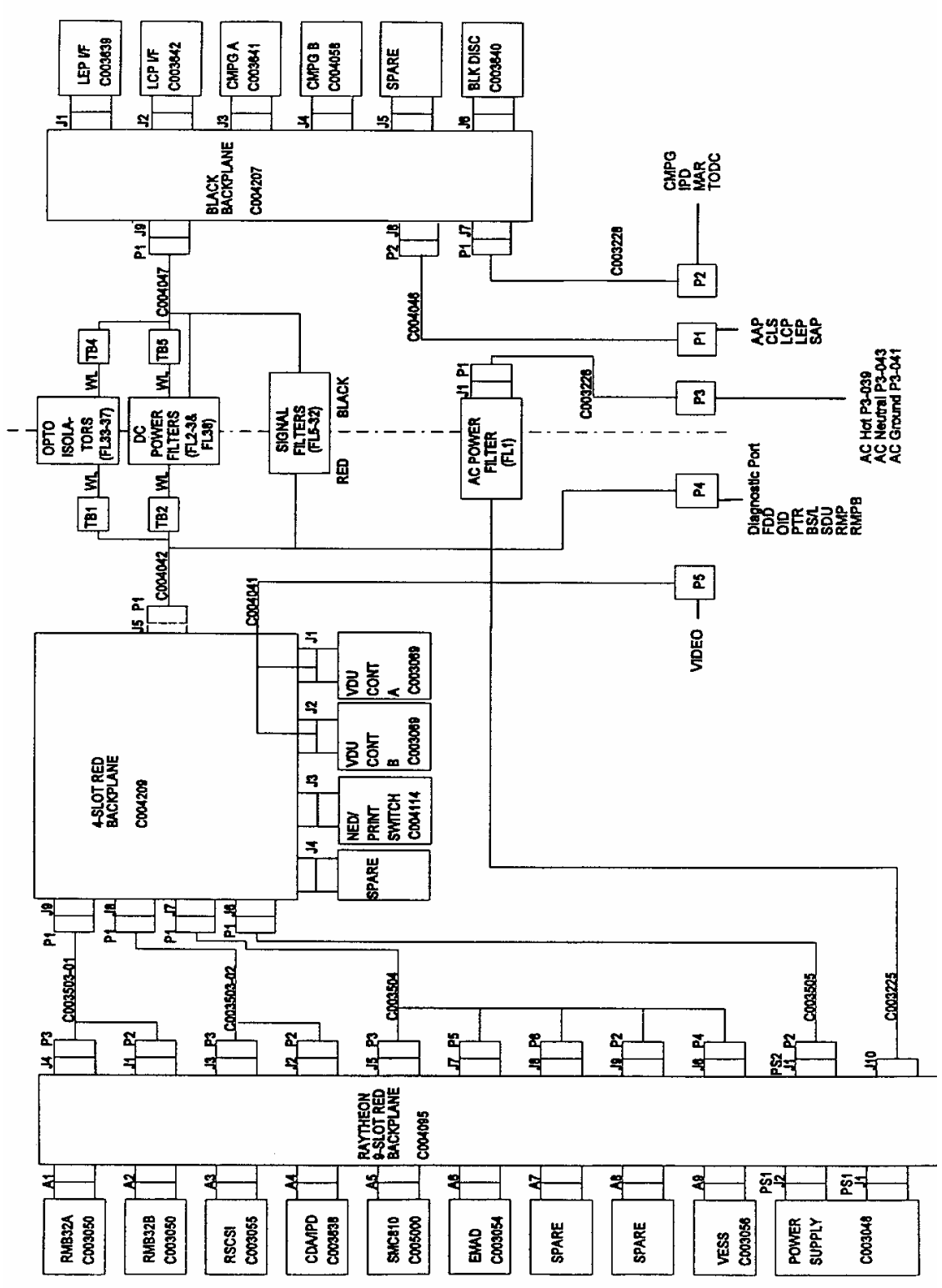


Figure 4-3. Cabling Inside WSP Chassis

Table 4-1. Cabling for SMC810 Interfaces

Signals between the SMC810 and the WSP External Plug P4 (Diagnostic Port)

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 & PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
CONSOLE PORT RETURN	A5-A38	J08-B04	J7-D08	-------	J5-A66	--------	--------	--------	--------	P4-171	-------	-------
CONSOLE PORT RXD H	A5-A40	J08-B02	J7-B09	-------	J5-A67	--------	--------	--------	--------	P4-157	-------	-------
CONSOLE PORT RXD L	A5-B39	J08-A02	J7-A09	-------	J5-A65	--------	--------	--------	--------	P4-158	-------	-------
CONSOLE PORT TXD	A5-B38	J08-A04	J7-C08	-------	J5-A68	--------	--------	--------	--------	P4-172	-------	-------

Table 4-1. Cabling for Interfaces, subtables A through I, are to be used in conjunction with Figure 4-3.

Table 4-2. Cabling for RMB32-A Interfaces

Signals between the RMB32A and the VDU Controller A

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 & PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
VDU CONTROL DATA A	A1-B17	J04-A19	J9-A14	J1-B56	-------	--------	--------	--------	--------	-------	-------	-------
VDU CONTROL DATA A RTN	A1-C16	J04-B19	J9-B14	J1-A56	-------	--------	--------	--------	--------	-------	-------	-------

Signals between the RMB32-A and the NED/Printer Switch Card

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 & PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
BI RESET L	A1-E39	PS2J1-C30	J6-B05	J3-A44	-------	--------	--------	--------	--------	-------	-------	-------
PRINTER SWITCH STATUS	A1-A31	J04-B06	J9-B27	J3-B27	-------	--------	--------	--------	--------	-------	-------	-------

Table 4-2. Cabling for RMB32-A Interfaces (Continued)

Signals between the RMB32-A and the LEP I/F Card

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 & PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
LEP CODE DISSIPATED INTERRUPT	A1-A27	J04-A08	J9-A25	-------	J5-B03	--------	FL12-02	FL12-01	--------	-------	J9-C05	J1-D07
LEP OUTPUT DATA (H)	A1-B25	J04-B10	J9-B23	-------	J5-B06	--------	FL15-02	FL15-01	--------	-------	J9-C08	J1-D08

Signals between the RMB32A and the LCP I/F Card

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 & PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
LCP INTERRUPT	A1-C06	J04-B29	J9-B04	-------	J5-D08	--------	FL08-02	FL08-01	--------	-------	J9-D11	J2-C14
LCP OUTPUT DATA (H)	A1-A04	J04-A31	J9-A02	-------	J5-A19	--------	FL11-02	FL11-01	--------	-------	J9-D12	J2-C13

Signals between the RMB32-A and the WSP External Plug P2 (TODC)

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9)	9 SLOT RED BACKPLANE (J1-J10)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1)	RED TERMINAL BLOCKS (TB1)	ISOLATOR CONNEC-TION (RED Side)	(Signal Inverted)	ISOLATOR CONNEC-TION (BLACK Side)	BLACK TERMINAL BLOCKS	BLACK BACKPLANE (J9)	BLACK BACKPLANE (J7)	WSP EXTER-NAL I/O
A	B	C	D	E	F	G	H	I	J	K	L	M	N
TODC (H) (Internal)	A1-B15	J04-A20	J9-A13	J5-A09	TB01-06	TB01-J5	FL35-A	↘					
TODC (L) (External)									FL35-V0	TB04-06	J9-C10	J7-A41	P2-041
TODC (L) (Internal)	A1-B16	J04-B20	J9-B13	J5-C08	TB01-04	TB01-J3	FL34-A	↘					
TODC (H) (External)									FL34-VO	TB04-04	J9-C11	J7-A42	P2-042

Table 4-2. Cabling for RMB32-A Interfaces (Continued)

Signals between the RMB32-A and the WSP External Plug P4 (FDD, RMP, OID-L)

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 & PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
FLOPPY DISC DRIVE CLOCK IN H	A1-B62	J04-D22	J9-D11	-------	J5-C37	--------	--------	--------	--------	P4-001	-------	-------
FLOPPY DISC DRIVE CLOCK IN L	A1-A62	J04-C22	J9-C11	-------	J5-C36	--------	--------	--------	--------	P4-002	-------	-------
FLOPPY DISC DRIVE CLOCK OUT H	A1-C68	J04-D28	J9-D05	-------	J5-B50	--------	--------	--------	--------	P4-004	-------	-------
FLOPPY DISC DRIVE CLOCK OUT L	A1-B68	J04-C28	J9-C05	-------	J5-B51	--------	--------	--------	--------	P4-003	-------	-------
FLOPPY DISC DRIVE IN 1 {RXD+}	A1-C66	J04-D27	J9-D06	-------	J5-B57	--------	--------	--------	--------	P4-038	-------	-------
FLOPPY DISC DRIVE IN 2 {RXD-}	A1-A67	J04-C27	J9-C06	-------	J5-B56	--------	--------	--------	--------	P4-039	-------	-------
FLOPPY DISC DRIVE OUT 1 {TXD+}	A1-B71	J04-D31	J9-D02	-------	J5-B55	--------	--------	--------	--------	P4-041	-------	-------
FLOPPY DISC DRIVE OUT 2 {TXD-}	A1-A71	J04-C31	J9-C02	-------	J5-B54	--------	--------	--------	--------	P4-042	-------	-------
HAC ACK DISCRETE	A1-A33	J04-A04	J9-A29	-------	J5-A30	--------	--------	--------	--------	P4-009	-------	-------
HAC CLEAR TO SEND	A1-B13	J04-B23	J9-B10	-------	J5-A52	--------	--------	--------	--------	P4-024	-------	-------
HAC CLOCK SYNC	A1-B12	J04-A23	J9-A10	-------	J5-A50	--------	--------	--------	--------	P4-022	-------	-------
HAC COMMON (CLEAR TO SEND)	A1-C58	J04-D17	J9-D16	-------	J5-A43	--------	--------	--------	--------	P4-025	-------	-------
HAC EAM ALARM RESET DISCRETE	A1-A57	J04-D16	J9-D17	-------	J5-A41	--------	--------	--------	--------	P4-013	-------	-------
HAC EAM DATA RELEASE DISCRETE	A1-C56	J04-C16	J9-C17	-------	J5-A40	--------	--------	--------	--------	P4-005	-------	-------
HAC LCC TEST DISCRETE	A1-B11	J04-A24	J9-A09	-------	J5-A56	--------	--------	--------	--------	P4-018	-------	-------
HAC NAK DISCRETE	A1-B32	J04-A05	J9-A28	-------	J5-A29	--------	--------	--------	--------	P4-011	-------	-------

Table 4-2. Cabling for RMB32-A Interfaces (Continued)

Signals between the RMB32-A and the WSP External Plug P4 (FDD, RMP, OID-L)

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 & PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
HAC NON EAM ALARM RESET DISC	A1-C32	J04-B05	J9-B28	-------	J5-A32	--------	--------	--------	--------	P4-014	-------	-------
HAC ROUTINE ALRM RSET DISC	A1-B34	J04-B04	J9-B29	-------	J5-A31	--------	--------	--------	--------	P4-016	-------	-------
HAC/RMPE PRINTER DATA (H)	A1-A58	J04-D18	J9-D15	-------	J5-A46	--------	--------	--------	--------	P4-020	-------	-------
HAC/RMPE PRINTER DATA (L)	A1-B58	J04-C18	J9-C15	-------	J5-A44	--------	--------	--------	--------	P4-021	-------	-------
HAC/RMPE WSP DATA (H)	A1-C42	J04-C05	J9-C28	-------	J5-A33	--------	--------	--------	--------	P4-007	-------	-------
HAC/RMPE WSP DATA (L)	A1-B43	J04-D05	J9-D28	-------	J5-A34	--------	--------	--------	--------	P4-008	-------	-------
OID 1 RXD (H)	A1-B03	J04-B32	J9-B01	-------	J5-C41	--------	--------	--------	--------	P4-090	-------	-------
OID 1 RXD (L)	A1-A03	J04-A32	J9-A01	-------	J5-B41	--------	--------	--------	--------	P4-091	-------	-------
OID 1 SWITCHED TO WSCE H	A1-C08	J04-B26	J9-B07	-------	J5-A62	--------	--------	--------	--------	P4-092	-------	-------
OID 1 SWITCHED TO WSCE L	A1-A05	J04-A30	J9-A03	-------	J5-A64	--------	--------	--------	--------	P4-093	-------	-------

Table 4-3. Cabling for RMB32-B Interfaces

Signals between the RMB32-B and the VDU Controller B

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 & PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
VDU CONTROL DATA B	A2-B17	J01-A14	J9-A51	J2-B56	-------	--------	--------	--------	--------	-------	-------	-------
VDU CONTROL DATA B RTN	A2-C16	J01-B14	J9-B51	J2-A56	-------	--------	--------	--------	--------	-------	-------	-------

Table 4-3. Cabling for RMB32-B Interfaces (Continued)

Signals between the RMB32-B and the Black Discrete Card

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 & PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
BLACK DISCRETE COMMAND	A2-A51	J01-D22	J9-D43	-------	J5-D03	--------	FL05-02	FL05-01	--------	-------	J9-A04	J6-C45
BLACK DISCRETE DATA	A2-C60	J01-D14	J9-D51	-------	J5-C01	--------	FL06-02	FL06-01	--------	-------	J9-A08	J6-D31

Signals between the RMB32-B and the CMPG-A

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 & PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
CMPG INPUT DATA	A2-B25	J01-B23	J9-B42	-------	J5-D04	--------	FL17-02	FL17-01	--------	-------	J9-C12	J3-B11
CMPG OUTPUT DATA	A2-B22	J01-B19	J9-B46	-------	J5-C02	--------	FL24-02	FL24-01	--------	-------	J9-B09	J3-D06
CMPG STATUS	A2-B43	J01-D28	J9-D37	-------	J5-D02	--------	FL25-02	FL25-01	--------	-------	J9-B10	J3-D11

Signals between the RMB32-B and the WSP External Plug P4 (RMPB, OID-R, PTR)

ALARM INHBT, SWITCH TO BACKUP	A2-A57	J01-D17	-------	J3-A04	J5-B65	--------	--------	--------	--------	P4-030	-------	-------
BACKUP COMMON (ALRM INHBT RTN)	A2-C58	J01-D16	J9-D49	J3-B54	J5-B64	--------	--------	--------	--------	P4-031	-------	-------
BACKUP EAM ALARM (H)	A2-A66	J01-C07	J9-C58	-------	J5-B61	--------	--------	--------	--------	P4-034	-------	-------
BACKUP EAM ALARM (L)	A2-B66	J01-D07	J9-D58	-------	J5-B60	--------	--------	--------	--------	P4-035	-------	-------
BACKUP ROUTINE ALARM (H)	A2-A61	J01-C12	J9-C53	-------	J5-B63	--------	--------	--------	--------	P4-032	-------	-------
BACKUP ROUTINE ALARM (L)	A2-B61	J01-D12	J9-D53	-------	J5-B62	--------	--------	--------	--------	P4-033	-------	-------

Table 4-3. Cabling for RMB32-B Interfaces (Continued)

Signals between the RMB32-B and the WSP External Plug P4 (RMPB, OID-R, PTR)

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 & PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
OID 2 RXD (H)	A2-B03	J01-B01	J9-B64	-------	J5-D46	--------	--------	--------	--------	P4-082	-------	-------
OID 2 RXD (L)	A2-A03	J01-A01	J9-A64	-------	J5-D47	--------	--------	--------	--------	P4-083	-------	-------
OID 2 SWITCHED TO WSCE H	A2-C08	J01-B07	J9-B58	-------	J5-D45	--------	--------	--------	--------	P4-084	-------	-------
OID 2 SWITCHED TO WSCE L	A2-A05	J01-A03	J9-A62	-------	J5-D44	--------	--------	--------	--------	P4-085	-------	-------
PRINTER STATUS H	A2-B24	J01-A22	J9-A43	-------	J5-D43	--------	--------	--------	--------	P4-080	-------	-------
PRINTER STATUS L	A2-C24	J01-B22	J9-B43	-------	J5-D42	--------	--------	--------	--------	P4-081	-------	-------

Table 4-4. Cabling for RSCSI Interfaces

Signals between the RSCSI and the WSP External Plug P4 (BS/L)

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 &PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
SCSI ACK GND H	A3-B47	J03-D08	J8-D25	-------	J5-D66	--------	--------	--------	--------	P4-078	-------	-------
SCSI ACK L	A3-A47	J03-C08	J8-C25	-------	J5-D67	--------	--------	--------	--------	P4-079	-------	-------
SCSI ATN GND H	A3-C56	J03-C16	J8-C17	-------	J5-D62	--------	--------	--------	--------	P4-072	-------	-------
SCSI ATN L	A3-A57	J03-D16	J8-D17	-------	J5-D63	--------	--------	--------	--------	P4-073	-------	-------
SCSI BSY GND H	A3-B42	J03-D04	J8-D29	-------	J5-D68	--------	--------	--------	--------	P4-074	-------	-------
SCSI BSY L	A3-A42	J03-C04	J8-C29	-------	J5-C42	--------	--------	--------	--------	P4-075	-------	-------
SCSI C/D GND H	A3-C52	J03-D12	J8-D21	-------	J5-D54	--------	--------	--------	--------	P4-076	-------	-------
SCSI C/D L	A3-B52	J03-C12	J8-C21	-------	J5-D55	--------	--------	--------	--------	P4-077	-------	-------
SCSI DB0 GND H	A3-B34	J03-B04	J8-B29	-------	J5-C43	--------	--------	--------	--------	P4-043	-------	-------
SCSI DB0 L	A3-A33	J03-A04	J8-A29	-------	J5-C44	--------	--------	--------	--------	P4-044	-------	-------
SCSI DB1 GND H	A3-A31	J03-B06	J8-B27	-------	J5-C45	--------	--------	--------	--------	P4-045	-------	-------
SCSI DB1 L	A3-A29	J03-A06	J8-A27	-------	J5-C46	--------	--------	--------	--------	P4-046	-------	-------

Table 4-4. Cabling for RSCSI Interfaces (Continued)

Signals between the RSCSI and the WSP External Plug P4 (BS/L)

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 &PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
SCSI DB2 GND H	A3-C26	J03-B08	J8-B25	-------	J5-C47	--------	--------	--------	--------	P4-047	-------	-------
SCSI DB2 L	A3-A27	J03-A08	J8-A25	-------	J5-C48	--------	--------	--------	--------	P4-048	-------	-------
SCSI DB3 GND H	A3-B25	J03-B10	J8-B23	-------	J5-C53	--------	--------	--------	--------	P4-049	-------	-------
SCSI DB3 L	A3-A25	J03-A10	J8-A23	-------	J5-C49	--------	--------	--------	--------	P4-050	-------	-------
SCSI DB4 GND H	A3-A24	J03-B12	J8-B21	-------	J5-C50	--------	--------	--------	--------	P4-051	-------	-------
SCSI DB4 L	A3-A23	J03-A12	J8-A21	-------	J5-C52	--------	--------	--------	--------	P4-052	-------	-------
SCSI DB5 GND H	A3-B22	J03-B14	J8-B19	-------	J5-C54	--------	--------	--------	--------	P4-053	-------	-------
SCSI DB5 L	A3-A22	J03-A14	J8-A19	-------	J5-C51	--------	--------	--------	--------	P4-054	-------	-------
SCSI DB6 GND H	A3-B20	J03-B16	J8-B17	-------	J5-C56	--------	--------	--------	--------	P4-055	-------	-------
SCSI DB6 L	A3-A20	J03-A16	J8-A17	-------	J5-C55	--------	--------	--------	--------	P4-056	-------	-------
SCSI DB7 GND H	A3-B18	J03-B18	J8-B15	-------	J5-C58	--------	--------	--------	--------	P4-057	-------	-------
SCSI DB7 L	A3-A18	J03-A18	J8-A15	-------	J5-C57	--------	--------	--------	--------	P4-058	-------	-------
SCSI DBP GND H	A3-B16	J03-B20	J8-B13	-------	J5-D60	--------	--------	--------	--------	P4-059	-------	-------
SCSI DBP L	A3-B15	J03-A20	J8-A13	-------	J5-D61	--------	--------	--------	--------	P4-060	-------	-------
SCSI GND H	A3-C32	J03-B05	J8-B28	-------	J5-D51	--------	--------	--------	--------	P4-069	-------	-------
SCSI I/O GND H	A3-B55	J03-D14	J8-D19	-------	J5-D52	--------	--------	--------	--------	P4-061	-------	-------
SCSI I/O L	A3-B54	J03-C14	J8-C19	-------	J5-D53	--------	--------	--------	--------	P4-062	-------	-------
SCSI MSG GND H	A3-B50	J03-D10	J8-D23	-------	J5-D64	--------	--------	--------	--------	P4-063	-------	-------
SCSI MSG L	A3-A50	J03-C10	J8-C23	-------	J5-D65	--------	--------	--------	--------	P4-064	-------	-------
SCSI REQ GND H	A3-C44	J03-D06	J8-D27	-------	J5-D56	--------	--------	--------	--------	P4-065	-------	-------
SCSI REQ L	A3-B44	J03-C06	J8-C27	-------	J5-D57	--------	--------	--------	--------	P4-066	-------	-------
SCSI RST GND H	A3-B58	J03-C18	J8-C15	-------	J5-C60	--------	--------	--------	--------	P4-067	-------	-------
SCSI RST L	A3-A58	J03-D18	J8-D15	-------	J5-C59	--------	--------	--------	--------	P4-068	-------	-------
SCSI SEL GND H	A3-C40	J03-D02	J8-D31	-------	J5-D58	--------	--------	--------	--------	P4-070	-------	-------
SCSI SEL L	A3-B40	J03-C02	J8-C31	-------	J5-D59	--------	--------	--------	--------	P4-071	-------	-------

Table 4-5. Cabling for CDA/IPD Card Interfaces

Signals between the CDA/IPD Card and the LEP Card

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 & PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
LEP DIAGNOSTICS REQUEST	A4-C64	J02-D09	J8-D56	-------	J5-B10	--------	FL13-02	FL13-01	--------	-------	J9-C06	J1-D06
LEP READ	A4-B62	J02-D11	J8-D54	-------	J5-A12	--------	FL14-02	FL14-01	--------	-------	J9-C07	J1-D05

Signals between the CDA/IPD Card and the LCP Card

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 & PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
LCP DIAGNOSTICS REQUEST	A4-C66	J02-D06	J8-D59	-------	J5-A08	--------	FL07-02	FL07-01	--------	-------	J9-D10	J2-C10
LCP MCU READ-ALL	A4-B65	J02-D08	J8-D57	-------	J5-A10	--------	FL09-02	FL09-01	--------	-------	J9-D14	J2-C11
LCP READ-SWITCH	A4-C58	J02-D16	J8-D49	-------	J5-D14	--------	FL10-02	FL10-01	--------	-------	J9-D13	J2-C12

Signals between the CDA/IPD Card and the CMPG-A Card

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 & PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
CMPG RESET	A4-C70	J02-D03	J8-D62	-------	J5-A05	--------	FL18-02	FL18-01	--------	-------	J9-C13	J3-C08

Table 4-5. Cabling for CDA/IPD Card Interfaces (Continued)

Signals between the CDA/IPD and the BDI Card

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 & PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
BLACK DISCRETE RESET	A4-C68	J02-D05	J8-D60	-------	J5-D06	--------	FL19-02	FL19-01	--------	-------	J9-C02	J6-B04
IPD DATA, INTERNAL	A4-A18	J02-A15	J8-A50	-------	J5-A11	TB01-07	FL36-A	FL36-VO	TB04-09	-------	J9-A09	J6-D30
IPD TRANSFER TIMING, INTERNAL	A4-B08	J02-B06	J8-B59	-------	J5-B05	TB01-01	FL33-A	FL33-VO	TB04-02	-------	J9-D09	J6-C31
IPD TRANSMIT CLOCK, INTERNAL	A4-B09	J02-A07	J8-A58	-------	J5-C03	TB01-10	FL37-VO	FL37-A	TB04-10	-------	J9-A07	J6-D35

Signals between the CDA/IPD Card and the WSP External Plug P4 (SDU)

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 & PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
SDU ALARM	A4-C14	J02-B11	J8-B54	-------	J5-C62	--------	--------	--------	--------	P4-184	-------	-------
SDU ALARM RETURN	A4-B14	J02-A11	J8-A54	-------	J5-C61	--------	--------	--------	--------	P4-185	-------	-------
SDU DATA IN	A4-A04	J02-A02	J8-A63	-------	J5-B49	--------	--------	--------	--------	P4-169	-------	-------
SDU DATA IN RETURN	A4-B04	J02-B02	J8-B63	-------	J5-B48	--------	--------	--------	--------	P4-170	-------	-------
SDU DATA OUT	A4-B11	J02-A09	J8-A56	-------	J5-B45	--------	--------	--------	--------	P4-183	-------	-------
SDU DATA OUT RETURN	A4-C12	J02-B09	J8-B56	-------	J5-B44	--------	--------	--------	--------	P4-182	-------	-------
SDU DATA READY	A4-A05	J02-A03	J8-A62	-------	J5-C64	--------	--------	--------	--------	P4-168	-------	-------
SDU DATA READY RETURN	A4-B05	J02-B03	J8-B62	-------	J5-C63	--------	--------	--------	--------	P4-167	-------	-------
SDU DATA SHIFT PULSE	A4-B06	J02-A04	J8-A61	-------	J5-B47	--------	--------	--------	--------	P4-180	-------	-------
SDU DATA SHIFT PULSE RETURN	A4-C06	J02-B04	J8-B61	-------	J5-B46	--------	--------	--------	--------	P4-181	-------	-------
SDU MODE 1 (ENCRYPT)	A4-C10	J02-B08	J8-B57	-------	J5-B43	--------	--------	--------	--------	P4-165	-------	-------
SDU MODE 1 (ENCRYPT) RETURN	A4-B10	J02-A08	J8-A57	-------	J5-B42	--------	--------	--------	--------	P4-166	-------	-------
SDU MODE 2 (DECRYPT)	A4-A07	J02-A05	J8-A60	-------	J5-C68	--------	--------	--------	--------	P4-179	-------	-------
SDU MODE 2 (DECRYPT) RETURN	A4-B07	J02-B05	J8-B60	-------	J5-C67	--------	--------	--------	--------	P4-178	-------	-------
SDU READ MODE	A4-A03	J02-A01	J8-A64	-------	J5-C65	--------	--------	--------	--------	P4-163	-------	-------
SDU READ MODE	A4-B03	J02-B01	J8-B64	-------	J5-C66	--------	--------	--------	--------	P4-164	-------	-------

Table 4-6 Cabling for Black Discrete I/F Card Interfaces

Signals between the BDI Card and the WSP External Plug P1 (AAP, SAP)

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 & PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
AUDIO ALARM CODE BIT-01 NOT	---	---	---	---	---	---	---	---	---	P1-181	J8-D03	J6-D05
AUDIO ALARM CODE BIT-01 {LSB}	---	---	---	---	---	---	---	---	---	P1-152	J8-C43	J6-C13
AUDIO ALARM CODE BIT-02	---	---	---	---	---	---	---	---	---	P1-108	J8-C39	J6-C06
AUDIO ALARM CODE BIT-02 NOT	---	---	---	---	---	---	---	---	---	P1-137	J8-D04	J6-C04
AUDIO ALARM CODE BIT-03	---	---	---	---	---	---	---	---	---	P1-093	J8-C44	J6-C14
AUDIO ALARM CODE BIT-03 NOT	---	---	---	---	---	---	---	---	---	P1-122	J8-D06	J6-D04
AUDIO ALARM CODE BIT-04 NOT	---	---	---	---	---	---	---	---	---	P1-107	J8-D05	J6-C05
AUDIO ALARM CODE BIT-04 {MSB}	---	---	---	---	---	---	---	---	---	P1-092	J8-C35	J6-D07
FACILITY ALARM SUMMARY	---	---	---	---	---	---	---	---	---	P1-106	J8-C27	J6-C03
FACILITY ALARM SUMMARY NOT	---	---	---	---	---	---	---	---	---	P1-091	J8-D01	J6-A05
LCEB FIRE ALARM	---	---	---	---	---	---	---	---	---	P1-090	J8-C45	J6-D19
LCEB FIRE ALARM NOT	---	---	---	---	---	---	---	---	---	P1-105	J8-C40	J6-A04
SITE ADDRESS PLUG GROUND	---	---	---	---	---	---	---	---	---	P1-182	J8-C37	J6-C44
SITE ADDRESS PLUG LCC BIT-01	---	---	---	---	---	---	---	---	---	P1-168	J8-C28	J6-D11
SITE ADDRESS PLUG LCC BIT-02	---	---	---	---	---	---	---	---	---	P1-167	J8-C30	J6-D10
SITE ADDRESS PLUG LCC BIT-03	---	---	---	---	---	---	---	---	---	P1-153	J8-C34	J6-D08
SITE ADDRESS PLUG PULLUP	---	---	---	---	---	---	---	---	---	P1-094	J8-C36	J6-C28
SITE ADDRESS PLUG SQUAD BIT-01	---	---	---	---	---	---	---	---	---	P1-139	J8-C38	J6-D06

Table 4-6 Cabling for Black Discrete I/F Card Interfaces (Continued)

Signals between the BDI Card and the WSP External Plug P1 (AAP, SAP)

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 & PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
SITE ADDRESS PLUG SQUAD BIT-02	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-138	J8-C29	J6-C10
SITE ADDRESS PLUG WING BIT-01	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-124	J8-C32	J6-D09
SITE ADDRESS PLUG WING BIT-02	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-123	J8-C33	J6-C08
SITE ADDRESS PLUG WING BIT-03	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-109	J8-C31	J6-C09
WSP ACKNOWLEDGE	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-118	J8-D02	J6-C07
WSP ACKNOWLEDGE NOT	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-104	J8-D07	J6-B02
Signals between the BDI Card and the WSP External Plug P2 (IPD, CMPG, MAR)												
IPD DATA	---------	---------	-------	-------	-------	---------	---------	---------	---------	P2-039	J7-A40	J6-D26
IPD DATA RETURN	---------	---------	-------	-------	-------	---------	---------	---------	---------	P2-040	J7-A39	J6-D27
IPD TRANSFER TIMING	---------	---------	-------	-------	-------	---------	---------	---------	---------	P2-035	J7-A34	J6-D32
IPD TRANSFER TIMING RETURN	---------	---------	-------	-------	-------	---------	---------	---------	---------	P2-036	J7-A35	J6-D36
IPD TRANSMIT CLOCK	---------	---------	-------	-------	-------	---------	---------	---------	---------	P2-037	J7-A37	J6-D43
IPD TRANSMIT CLOCK RETURN	---------	---------	-------	-------	-------	---------	---------	---------	---------	P2-038	J7-A36	J6-D42
J6-J7-N09	---------	---------	-------	-------	-------	---------	---------	---------	---------	P2-005	J7-A06	J6-A40
J6-J7-N10	---------	---------	-------	-------	-------	---------	---------	---------	---------	P2-006	J7-A05	J6-A39
MISSILE AWAY LF 02	---------	---------	-------	-------	-------	---------	---------	---------	---------	P2-015	J7-A15	J6-C24
MISSILE AWAY LF 03	---------	---------	-------	-------	-------	---------	---------	---------	---------	P2-017	J7-A17	J6-D24
MISSILE AWAY LF 04	---------	---------	-------	-------	-------	---------	---------	---------	---------	P2-019	J7-A19	J6-C25
MISSILE AWAY LF 05	---------	---------	-------	-------	-------	---------	---------	---------	---------	P2-021	J7-A21	J6-C26
MISSILE AWAY LF 06	---------	---------	-------	-------	-------	---------	---------	---------	---------	P2-023	J7-A23	J6-C27
MISSILE AWAY LF 07	---------	---------	-------	-------	-------	---------	---------	---------	---------	P2-025	J7-A25	J6-D23
MISSILE AWAY LF 08	---------	---------	-------	-------	-------	---------	---------	---------	---------	P2-027	J7-A27	J6-D22
MISSILE AWAY LF 09	---------	---------	-------	-------	-------	---------	---------	---------	---------	P2-029	J7-A30	J6-D16

Table 4-6 Cabling for Black Discrete I/F Card Interfaces (Continued)

Signals between the BDI Card and the WSP External Plug P2 (IPD, CMPG, MAR)

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 & PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
MISSILE AWAY LF 10	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-031	J7-A32	J6-D29
MISSILE AWAY LF 11	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-033	J7-A33	J6-C29
MISSILE AWAY LF RETURN	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-034	J7-A38	J6-A43
MSTR ALARM RESET SWITCH LEFT	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-003	J7-A03	J6-C02
MSTR ALRM RSET SW LEFT RETURN	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-004	J7-A04	J6-B44
MSTR ALRM RSET SW RIGHT	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-001	J7-A01	J6-B03
MSTR ALRM RSET SW RIGHT RETURN	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-002	J7-A02	J6-B43

Table 4-7. Cabling for CMPG Card Interfaces

Signals between the CMPG-A and the WSP External Plug P2 (CMPG)

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 & PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
CMPG CBL RCV DATA XFER TIMING	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-097	J7-C06	J3-B12
CMPG CBL RCV DATA XFER TMNG R	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-098	J7-C07	J3-A12
CMPG COMM XMIT CLOCK	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-095	J7-C04	J3-D43
CMPG COMM XMIT CLOCK RTN	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-096	J7-C05	J3-C44
CMPG COMPUTER CLOCK	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-067	J7-B21	J3-D15

Table 4-7. Cabling for CMPG Card Interfaces (Continued)

Signals between the CMPG-A and the WSP External Plug P2 (CMPG)

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 & PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
CMPG COMPUTER CLOCK RTN	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-068	J7-B22	J3-C15
CMPG NO DATA	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-093	J7-C02	J3-B38
CMPG NO DATA RTN	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-094	J7-C03	J3-B39
CMPG RCV DATA	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-089	J7-B43	J3-C34
CMPG RCV DATA RTN	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-090	J7-B44	J3-D34
CMPG RCV DATA TIMING	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-091	J7-B45	J3-B43
CMPG RCV DATA TIMING RTN	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-092	J7-C01	J3-B44
CMPG SELECT LINE 01	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-043	J7-A44	J3-D24
CMPG SELECT LINE 01 RTN	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-044	J7-A43	J3-C24
CMPG SELECT LINE 02	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-045	J7-A45	J3-D23
CMPG SELECT LINE 02 RTN	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-046	J7-C45	J3-C23
CMPG SELECT LINE 03	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-047	J7-B14	J3-D22
CMPG SELECT LINE 03 RTN	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-048	J7-B12	J3-C22
CMPG SELECT LINE 04	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-049	J7-B13	J3-D21
CMPG SELECT LINE 04 RTN	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-050	J7-B11	J3-C21
CMPG SELECT LINE 05	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-051	J7-B09	J3-D20
CMPG SELECT LINE 05 RTN	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-052	J7-B10	J3-C20
CMPG SELECT LINE 06	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-053	J7-B07	J3-D18
CMPG SELECT LINE 06 RTN	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-054	J7-B08	J3-C18
CMPG SELECT LINE 07	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-055	J7-B03	J3-D14
CMPG SELECT LINE 07 RTN	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-056	J7-B04	J3-C14
CMPG SELECT LINE 08	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-057	J7-B06	J3-B15
CMPG SELECT LINE 08 RTN	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-058	J7-B05	J3-A15

Table 4-7. Cabling for CMPG Card Interfaces (Continued)

Signals between the CMPG-A and the WSP External Plug P2 (CMPG)

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 & PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
CMPG SELECT LINE 09	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-059	J7-B01	J3-D13
CMPG SELECT LINE 09 RTN	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-060	J7-B02	J3-C13
CMPG SELECT LINE 10	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-061	J7-B15	J3-B14
CMPG SELECT LINE 10 RTN	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-062	J7-B16	J3-A14
CMPG TONE ON LINE 01	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-069	J7-B23	J3-B22
CMPG TONE ON LINE 01 RTN	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-070	J7-B24	J3-A22
CMPG TONE ON LINE 02	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-071	J7-B28	J3-B28
CMPG TONE ON LINE 02 RTN	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-072	J7-B29	J3-C28
CMPG TONE ON LINE 03	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-073	J7-B25	J3-C31
CMPG TONE ON LINE 03 RTN	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-074	J7-B26	J3-D31
CMPG TONE ON LINE 04	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-075	J7-B33	J3-C26
CMPG TONE ON LINE 04 RTN	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-076	J7-B30	J3-D26
CMPG TONE ON LINE 05	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-077	J7-B31	J3-C27
CMPG TONE ON LINE 05 RTN	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-078	J7-B32	J3-D27
CMPG TONE ON LINE 06	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-079	J7-B27	J3-B30
CMPG TONE ON LINE 06 RTN	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-080	J7-B34	J3-C30
CMPG TONE ON LINE 07	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-081	J7-B35	J3-B29
CMPG TONE ON LINE 07 RTN	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-082	J7-B36	J3-C29
CMPG TONE ON LINE 08	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-083	J7-B37	J3-B23
CMPG TONE ON LINE 08 RTN	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-084	J7-B38	J3-A23
CMPG TONE ON LINE 09	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-085	J7-B40	J3-B36
CMPG TONE ON LINE 09 RTN	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-086	J7-B39	J3-B37
CMPG TONE ON LINE 10	---------	---------	-------	-------	-------	--------	--------	--------	--------	P2-087	J7-B41	J3-D35

Table 4-7. Cabling for CMPG Card Interfaces (Continued)

Signals between the CMPG-A and the WSP External Plug P2 (CMPG)

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 & PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
CMPG TONE ON LINE 10 RTN	---------	---------	-------	-------	-------	---------	---------	---------	---------	P2-088	J7-B42	J3-C35
CMPG TONE PRESENT ANY LINE	---------	---------	-------	-------	-------	---------	---------	---------	---------	P2-065	J7-B19	J3-D42
CMPG TONE PRESENT ANY LINE RTN	---------	---------	-------	-------	-------	---------	---------	---------	---------	P2-066	J7-B17	J3-C42
CMPG TRANSMIT DATA	---------	---------	-------	-------	-------	---------	---------	---------	---------	P2-099	J7-C11	J3-D17
CMPG TRANSMIT DATA RTN	---------	---------	-------	-------	-------	---------	---------	---------	---------	P2-100	J7-C10	J3-C17
CMPG TRANSMIT DATA XFER TIMING	---------	---------	-------	-------	-------	---------	---------	---------	---------	P2-101	J7-C09	J3-D19
CMPG XMIT DATA XFER TIMING RTN	---------	---------	-------	-------	-------	---------	---------	---------	---------	P2-102	J7-C08	J3-C19
CMPG XMIT TONE LOST ANY LINE	---------	---------	-------	-------	-------	---------	---------	---------	---------	P2-063	J7-B20	J3-D41
CMPG XMIT TONE LOST ANY LN RTN	---------	---------	-------	-------	-------	---------	---------	---------	---------	P2-064	J7-B18	J3-C41

Table 4-8. Cabling for LCP Card Interfaces

Signals between the LCP Card and the WSP External Plug P1 (LCP)

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 & PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
CLS1	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-177	J8-C16	J2-B07
CLS1 CONTINUITY A	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-149	J8-C23	J2-B04
CLS1 RTN	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-180	J8-C20	J2-C33
CLS2	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-162	J8-C19	J2-B06

Table 4-8. Cabling for LCP Card Interfaces (Continued)

Signals between the LCP Card and the WSP External Plug P1 (LCP)

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 & PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
CLS2 RTN	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-165	J8-C26	J2-C34
CLS3	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-176	J8-C21	J2-B05
CLS3 CONTINUITY B	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-148	J8-C24	J2-C36
CLS3 RTN	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-150	J8-C22	J2-C35
LCP BIT-01 RETURN	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-011	J8-C02	J2-D08
LCP BIT-02 RETURN	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-010	J8-C03	J2-D07
LCP BIT-03 RETURN	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-009	J8-C04	J2-D06
LCP BIT-04 RETURN	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-008	J8-C05	J2-D05
LCP BIT-05 RETURN	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-007	J8-C06	J2-D04
LCP BIT-06 RETURN	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-006	J8-C07	J2-C08
LCP BIT-08 RETURN	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-019	J8-C08	J2-C07
LCP BIT-09 RETURN	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-020	J8-C09	J2-C06
LCP BIT-10 RETURN	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-021	J8-C10	J2-C05
LCP BIT-11 RETURN	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-022	J8-C11	J2-C04
LCP BIT-12 RETURN	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-023	J8-C12	J2-C03
LCP BIT-13 RETURN	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-024	J8-C13	J2-C02
LCP BIT-14 RETURN	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-025	J8-C14	J2-B09
LCP BIT-15 RETURN	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-038	J8-C15	J2-B08
LCP CODE DISSIPATED	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-037	J8-C25	J2-B03
LCP CODE DISSIPATED RETURN	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-081	J8-C01	J2-C32
LCP COH/CE	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-036	J8-A32	J2-C40
LCP INJ/CE	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-035	J8-A33	J2-C39
LCP MCU BIT-01	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-001	J8-B45	J2-C43
LCP MCU BIT-08	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-002	J8-A36	J2-D43

Table 4-8. Cabling for LCP Card Interfaces (Continued)

Signals between the LCP Card and the WSP External Plug P1 (LCP)

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 & PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
LCP MCU BIT-09	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-003	J8-A37	J2-D42
LCP MCU BIT-10	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-014	J8-A38	J2-D41
LCP MCU BIT-11	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-015	J8-A39	J2-D40
LCP MCU BIT-12	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-016	J8-A40	J2-B40
LCP MCU BIT-13	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-017	J8-A41	J2-D38
LCP MCU BIT-14	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-028	J8-A42	J2-D37
LCP MCU BIT-15	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-029	J8-A43	J2-D36
LCP MCU BIT-16	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-030	J8-A44	J2-D35
LCP MCU BIT-17	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-041	J8-A45	J2-D34
LCP MCU BIT-18	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-042	J8-B01	J2-D33
LCP MCU BIT-19	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-043	J8-B02	J2-D32
LCP MCU BIT-20	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-044	J8-B03	J2-D31
LCP MCU BIT-21	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-055	J8-B04	J2-D30
LCP MCU BIT-22	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-056	J8-B05	J2-D29
LCP MCU BIT-23	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-057	J8-B06	J2-D28
LCP MCU BIT-24	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-058	J8-B07	J2-D27
LCP MCU BIT-25	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-070	J8-B08	J2-D26
LCP MCU BIT-26	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-071	J8-B09	J2-D25
LCP MCU BIT-27	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-072	J8-B10	J2-D24
LCP MCU BIT-28	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-073	J8-B11	J2-D23
LCP MCU BIT-29	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-084	J8-B12	J2-D22
LCP MCU BIT-30	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-085	J8-B13	J2-D21
LCP MCU BIT-31	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-086	J8-B14	J2-D20
LCP MCU BIT-32	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-087	J8-B15	J2-D19
LCP MCU BIT-33	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-099	J8-B16	J2-D18
LCP MCU BIT-34	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-100	J8-B17	J2-D17

Table 4-8. Cabling for LCP Card Interfaces (Continued)

Signals between the LCP Card and the WSP External Plug P1 (LCP)

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 & PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
LCP MCU BIT-35	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-101	J8-B18	J2-D16
LCP MCU BIT-36	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-102	J8-B19	J2-D15
LCP MCU BIT-37	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-113	J8-B20	J2-D14
LCP MCU BIT-38	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-114	J8-B21	J2-D13
LCP MCU BIT-39	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-115	J8-B22	J2-D12
LCP MCU BIT-40	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-116	J8-B23	J2-D11
LCP MCU BIT-41	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-128	J8-B24	J2-D10
LCP MCU BIT-42	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-129	J8-B38	J2-C31
LCP MCU BIT-43	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-130	J8-B37	J2-C30
LCP MCU BIT-44	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-131	J8-B36	J2-C29
LCP MCU BIT-45	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-142	J8-B35	J2-C28
LCP MCU BIT-46	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-143	J8-B34	J2-C27
LCP MCU BIT-47	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-144	J8-B33	J2-C26
LCP MCU BIT-48	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-145	J8-B32	J2-C25
LCP MCU BIT-49	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-157	J8-B31	J2-C24
LCP MCU BIT-50	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-158	J8-B30	J2-C23
LCP MCU BIT-51	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-159	J8-B29	J2-C22
LCP MCU BIT-52	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-160	J8-B28	J2-C21
LCP MCU BIT-53	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-171	J8-B27	J2-C20
LCP MCU BIT-54	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-172	J8-B26	J2-C19
LCP MCU BIT-55	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-173	J8-B25	J2-C18
LCP MCU BIT-56	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-174	J8-C17	J2-C44
LCP SIGNAL COMMON	---------	---------	-------	-------	-------	--------	--------	--------	--------	P1-033	J8-C18	J2-B02

Table 4-9. Cabling for LEP Card Interfaces

Signals between the LEP Card and the WSP External Plug P1 (LEP)

SIGNAL_NAME (AM)	9 SLOT RED BACKPLANE (A1-A9 & PS1)	9 SLOT RED BACKPLANE (J1-J10 & PS2J1)	4 SLOT RED BACKPLANE (J6-J9)	4 SLOT RED BACKPLANE (J1-J4)	4 SLOT RED BACKPLANE (J5)	RED TERMINAL BLOCKS (TB1,TB2)	ISOLATOR CONNEC-TION (RED)	ISOLATOR CONNEC-TION (BLACK)	BLACK TERMINAL BLOCKS (TB4,TB5)	WSP EXTERNAL I/O (P1-P5)	BLACK BACKPLANE (J7-J9)	BLACK BACKPLANE (J1-J6)
A	C	D	E	F	G	H	I	J	K	L	M	N
LEP CODE DISSIPATED	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-005	J8-A02	J1-D42
LEP CODE DISSIPATED RTN	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-060	J8-A28	J1-D10
LEP MCU BIT-01	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-013	J8-A27	J1-D11
LEP MCU BIT-02	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-026	J8-A26	J1-D12
LEP MCU BIT-03	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-027	J8-A25	J1-D13
LEP MCU BIT-04	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-040	J8-A24	J1-D14
LEP MCU BIT-05	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-053	J8-A23	J1-D15
LEP MCU BIT-06	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-054	J8-A22	J1-D16
LEP MCU BIT-07	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-068	J8-A21	J1-D17
LEP MCU BIT-08	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-069	J8-A20	J1-D18
LEP MCU BIT-09	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-082	J8-A19	J1-D19
LEP MCU BIT-10	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-083	J8-A18	J1-D20
LEP MCU BIT-11	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-097	J8-A17	J1-D21
LEP MCU BIT-12	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-098	J8-A16	J1-D22
LEP MCU BIT-13	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-111	J8-A15	J1-D23
LEP MCU BIT-14	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-112	J8-A14	J1-D24
LEP MCU BIT-15	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-126	J8-A13	J1-D25
LEP MCU BIT-16	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-127	J8-A12	J1-D26
LEP MCU BIT-17	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-140	J8-A11	J1-D27
LEP MCU BIT-18	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-141	J8-A10	J1-D28
LEP MCU BIT-19	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-155	J8-A09	J1-D29
LEP MCU BIT-20	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-156	J8-A08	J1-D30
LEP MCU BIT-21	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-169	J8-A07	J1-D31
LEP MCU BIT-22	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-170	J8-A06	J1-D32
LEP MCU BIT-23	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-184	J8-A05	J1-D33
LEP MCU BIT-24	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-185	J8-A04	J1-D34
LEP SIGNAL COMMON	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-074	J8-A01	J1-D43
LEP SWITCH	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-018	J8-A03	J1-D41
LEP SWITCH RTN	---------	---------	-------	-------	-------	---------	---------	---------	---------	P1-046	J8-A29	J1-D09

4-3. WSP COMPONENTS. A brief functional description of each WSP component is given in the paragraphs below. Block diagrams of the component's architecture are provided in Figures 4-4 through 4-15. Characteristics and interfaces of each component are given in Tables 4-10, 4-11, etc., one for each WSP component. In the interface sections of these tables, the following conventions are used:

a. DI-n = Discrete Input, n lines

b. DO-n = Discrete Output, n lines

c. SI = Serial Input

d. SO = Serial Output

e. PIO-n = Parallel Input/Output, n data bits wide

f. CLK-I-n = Clock Input, n lines

g. CLK-O-n = Clock Output, n lines

h. PWR-I = Power Input

i. PWR-O = Power Output

j. 1/1/E = 1 start bit, 1 stop bit, even parity

k. 1/1/N = 1 start bit, 1 stop bit, no parity

4-3.1. Central Processor (SMC810). The SMC810 processor (also called an Embedded Single Module Computer (ESMC)) is a single module, Bus Interconnect (BI) based computer. It executes the WSP software and communicates directly with I/O modules on the VAXBI-M bus. Through those modules, and through secondary I/O modules connected to them, the WSP interfaces to the external devices shown in Figure 4-1. The WSP software consists of the Console Operations Program (COP), the Minuteman III Operational Targeting Program (MOTP-III), and the Execution Plan Program (EPP). The SMC810 executes a subset of the DEC VAX instruction set.

a. Block Diagram: See Figure 4-4, SMC810 Block Diagram.

b. Characteristics and Interfaces: See Table 4-10, SMC810 Characteristics and Interfaces.

4-3.2. Main Memory. The main memory for the WSP is a four Megabyte (1Mbyte = 1024x1024 bytes) dynamic RAM (DRAM) module, which resides on the 810 private memory expansion bus (MEbus). This memory is called Embedded Memory Array - Dynamic (EMAD).

a. Block Diagram: See Figure 4-5, EMAD Block Diagram.

b. Characteristics and Interfaces: See Table 4-11, EMAD Characteristics and Interfaces.

4-3.3. VAXBI-M Bus. The VAXBI-M bus is the communications medium between the SMC810 processor and the I/O cards connected to the bus. The VAXBI protocol has a three-cycle structure: command/address, imbedded arbitration, and data. All transfers are between the SMC810 and the first-level I/O cards (i.e., those attached to the VAXBI-M bus).

Characteristics and Interfaces: See Table 4-12, VAXBI-M Characteristics and Interfaces.

4-3.4. VESS Bus Controller Module. The Raytheon VESS terminates the VAXBI and provides VAXBI related reset functions. The VESS also receives the nuclear event flag directly from the NED/Printer Switch card. This terminates all bus activity immediately.

a. Block Diagram: See Figure 4-6, VESS Block Diagram.

b. Characteristics and Interfaces: See Table 4-13, VESS Characteristics and Interfaces.

4-3.5. RMB32 I/O Cards. The primary function of the RMB32 modules is to transfer data between their communications ports and the VAXBI-M bus. With the exception of the Bulk Storage/Loader (BS/L) and the Secure Data Unit (SDU), all WSP external interfaces pass through one of the RMB32 cards.

a. Block Diagram: See Figure 4-7, RMB32 Interface Card Block Diagram.

b. Characteristics and Interfaces: See Table 4-14, RMB32 Characteristics and Interfaces.

4-3.6. RSCSI Interface Card. The Raytheon Small Computer System Interface (RSCSI) module is a microprocessor based module that interfaces the SCSI bus to the VAXBI-M bus. It serves to transfer data between the SMC810 processor and the BS/L.

a. Block Diagram: See Figure 4-8. RSCSI Interface Block Diagram.

b. Characteristics and Interfaces: See Table 4-15, RSCSI Characteristics and Interfaces.

4-3.7. CDA/IPD Interface Card. The main function of the CDA/IPD module is to provide encryption and decryption services by transferring data between the VAXBI bus and the Secure Data Unit (SDU) device, which resides in the Coder-Decoder Assembly (CDA). The CDA/IPD module sends discrete signals to other cards. These discretes are used to cause card resets or to trigger diagnostics on those cards. Finally, the CDA/IPD module transfers encrypted data being sent to the IPD modem to the Black Discrete Interface card for transmission to the IPD modem.

a. Block Diagram: See Figure 4-9. CDA/IPD Interface Block Diagram.

b. Characteristics and Interfaces: See Table 4-16, CDA/IPD Interface Card Characteristics and Interfaces.

4-3.8. NED/Printer Switch Card. The purpose of this card is to detect a nuclear event, halt the WSP processor, and switch the Printer to direct access by the RMP Backup (RMPB) processor.

a. Block Diagram: See Figure 4-10, NED/Printer Switch Card Block Diagram.

b. Characteristics and Interfaces: See Table 4-17, NED/Printer Switch Card Characteristics and Interfaces.

4-3.9. VDU Controller Card. The GTE VDU Controller is used to transform ASCII data from an RMB32 module into video Red-Green-Blue (RGB) bit streams which are sent to a VDU. The VDU Controller supports text and character graphics as well as 8 colors, underlining, inverse video and flash. There are two VDU Controllers in each WSP: one for each Weapon System (WS) VDU.

a. Block Diagram: See Figure 4-11, VDU Controller Block Diagram.

b. Characteristics and Interfaces: See Table 4-18, VDU Controller Card Characteristics and Interfaces.

4-3.10. Black Discrete Interface (BDI) Card. The Black Discrete card communicates with COP via the RMB32-B card, and provides interfaces to the Auxiliary Alarm Panel (AAP), Master Alarm Reset (MAR), Missile Away lines, and Site Address Plug (SAP). It also interfaces to the IPD modem, to which it transmits data received from COP via the CDA/IPD card. Finally, the BDI card provides buffered power for the optoisolators between the Red and Black sections of the WSP.

a. Block Diagram: See Figure 4-12, Black Discrete Block Diagram.

b. Characteristics and Interfaces: See Table 4-19, Black Discrete Interface Card Characteristics and Interfaces.

4-3.11. CMPG Interface Module. The CMPG Interface Module is a two-card set that provides the interface to the Command Message Processing Group (CMPG). The CMPG Interface module exchanges data with the SMC810 via the RMB32-B module. The CMPG interface module is responsible for handling the timing and sequencing aspects of the interface to the CMPG.

a. Block Diagram: See Figure 4-13, CMPG Interface Module Block Diagram.

b. Characteristics and Interfaces: See Table 4-20, CMPG Interface Module Characteristics and Interfaces.

4-3.12. LCP Interface Card. The LCP Interface card provides the interface to the Launch Control Panel. This interface consists of 48 parallel Mechanical Code Unit (MCU) bits and other LCP control bits. Additionally, the LCP Interface Card provides an interface to each of the three Cooperative Launch Switches (CLSs). The LCP Interface card converts this parallel data into a serial bit stream which it sends to an RMB32 card in the Red section. The SMC 810 commands the LCP interface card to send the serial data by setting one of the CDA/IPD discrete lines.

a. Block Diagram: See Figure 4-14, LCP Interface Card Diagram.

b. Characteristics and Interfaces: See Table 4-21, LCP Interface Module Characteristics and Interfaces.

4-3.13. LEP Interface Card. The LEP Interface card provides the interface to the Launch Enable Panel (LEP). This interface consists of 24 parallel Mechanical Code Unit (MCU) bits, Code Dissipated and LEP Switch bits. The LEP Interface card converts this parallel data into a serial bit stream which it sends to an RMB32 card in the Red section. The SMC 810 commands the LEP interface card to send the serial data by setting one of the CDA/IPD discrete lines. The LEP also contains the (hardened) Time of Day Counter. This counter sends an interrupt to the SMC 810 via the CDA/IPD every 10 ms and can be read by software at any time.

a. Block Diagram: See Figure 4-15, LEP Interface Block Diagram.

b. Characteristics and Interfaces: See Table 4-22, LEP Interface Module Characteristics and Interfaces.

4-3.14. Red Power Supply. The (Raytheon) Red Power Supply produces +5, -5, -5.2, +12, and -12 volt outputs. This DC power is used by every card within the WSP and is also routed to the Operator Input Devices (OIDs).

Characteristics and Interfaces: See Table 4-23, Red Power Supply Characteristics and Interfaces.

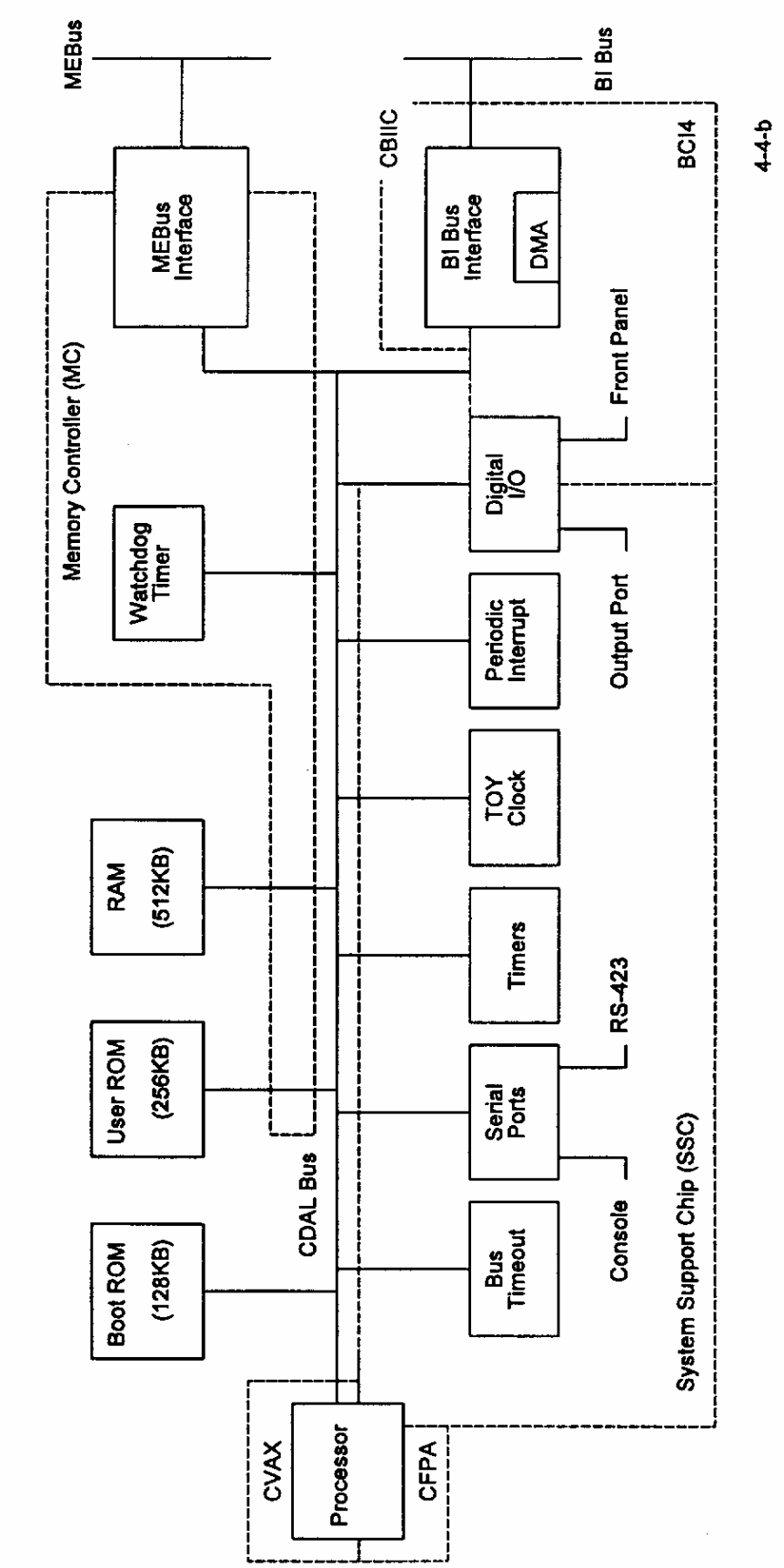


Figure 4-4. SMC810 Block Diagram

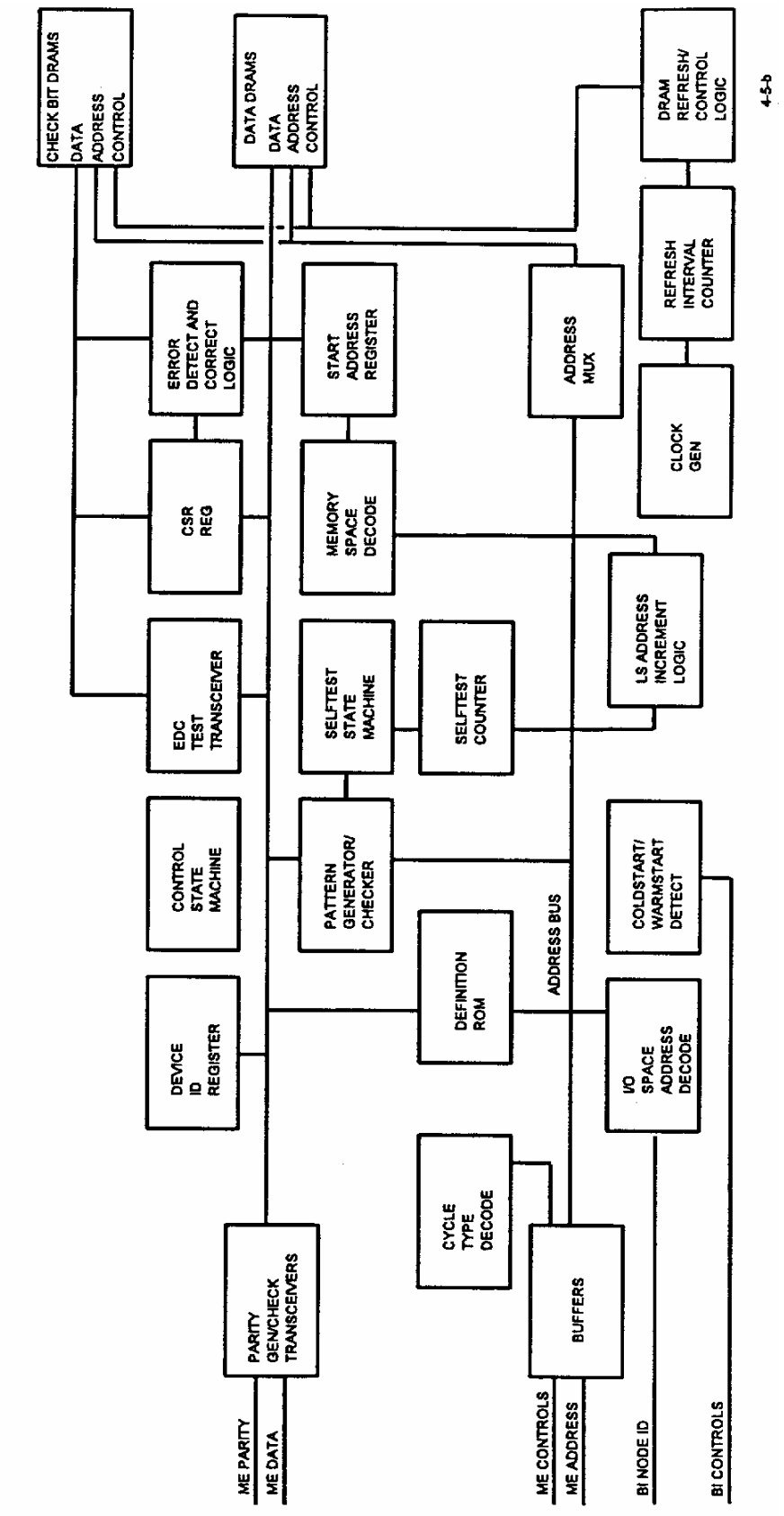


Figure 4-5. EMAD Block Diagram

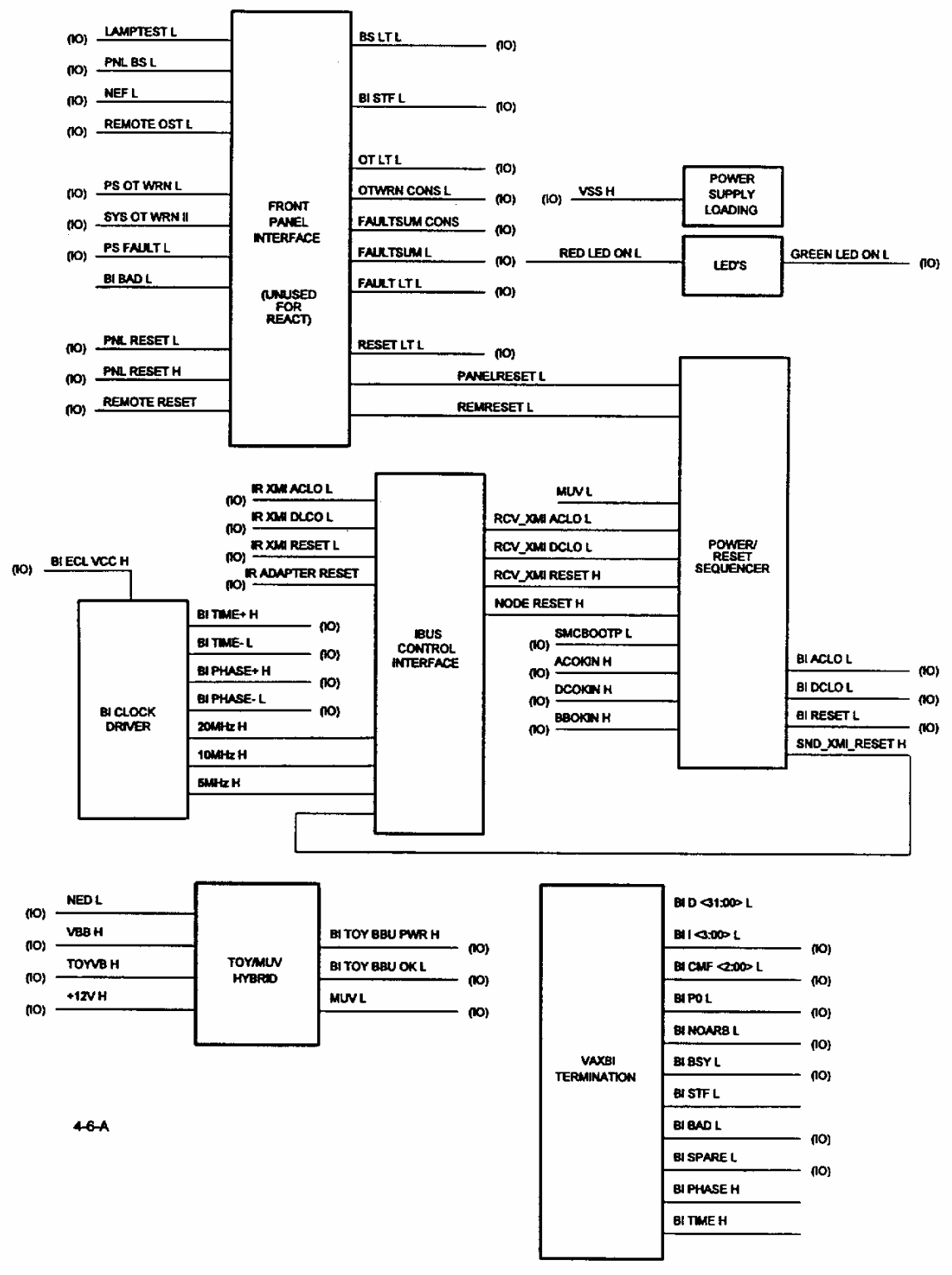


Figure 4-6. VESS Block Diagram

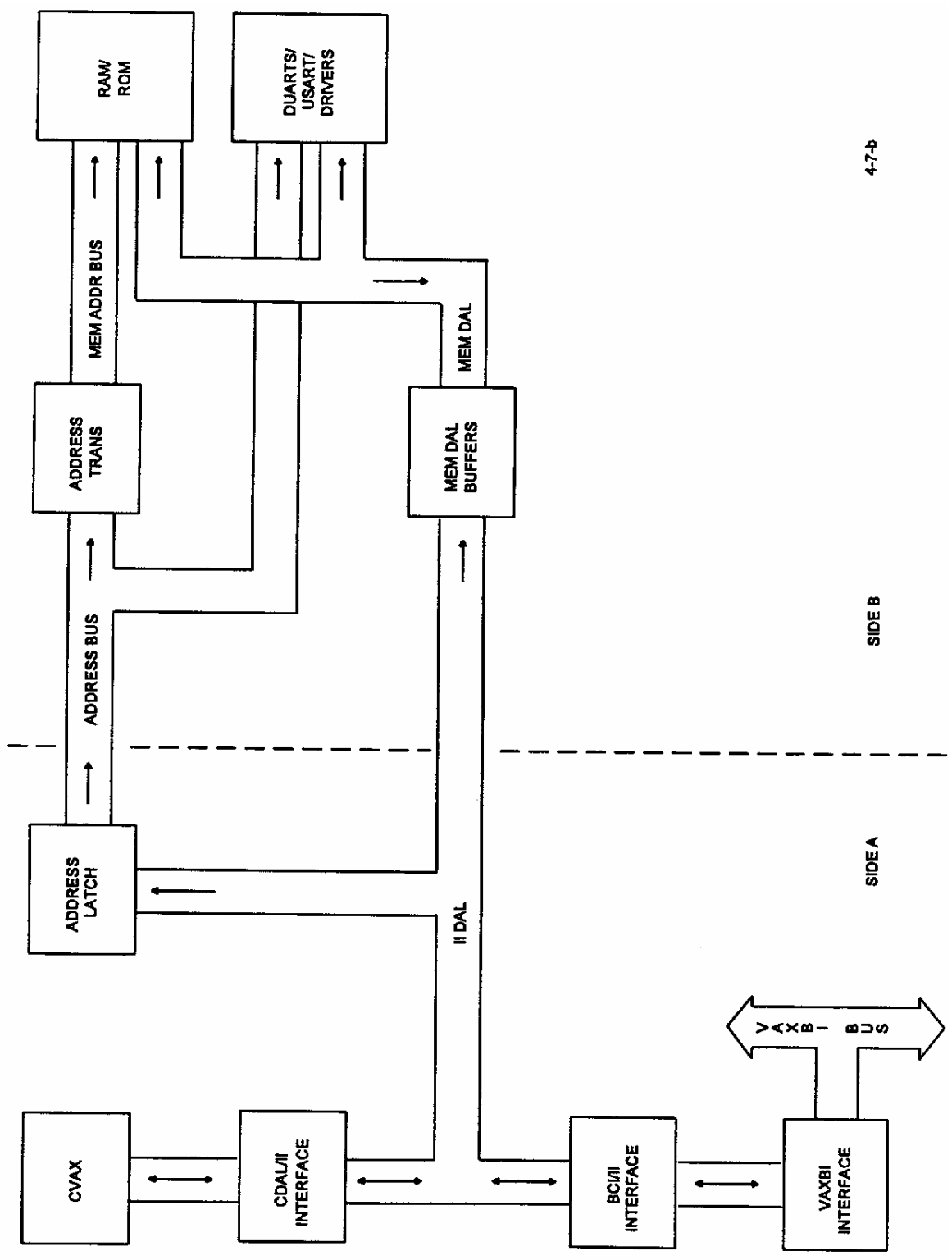


Figure 4-7. RMB32 Interface Card Block Diagram

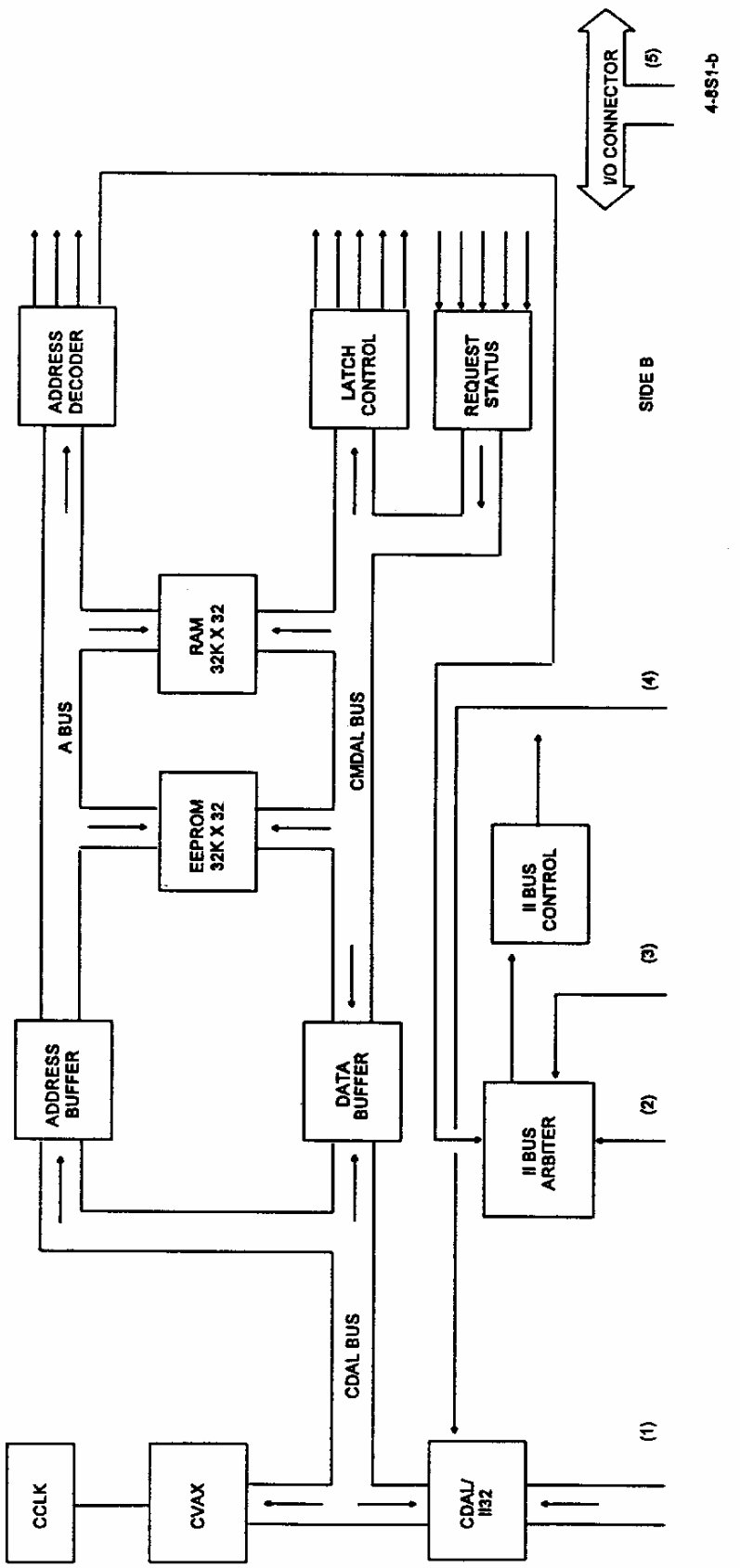


Figure 4-8. RSCSI Interface Block Diagram (Sheet 1 of 2)

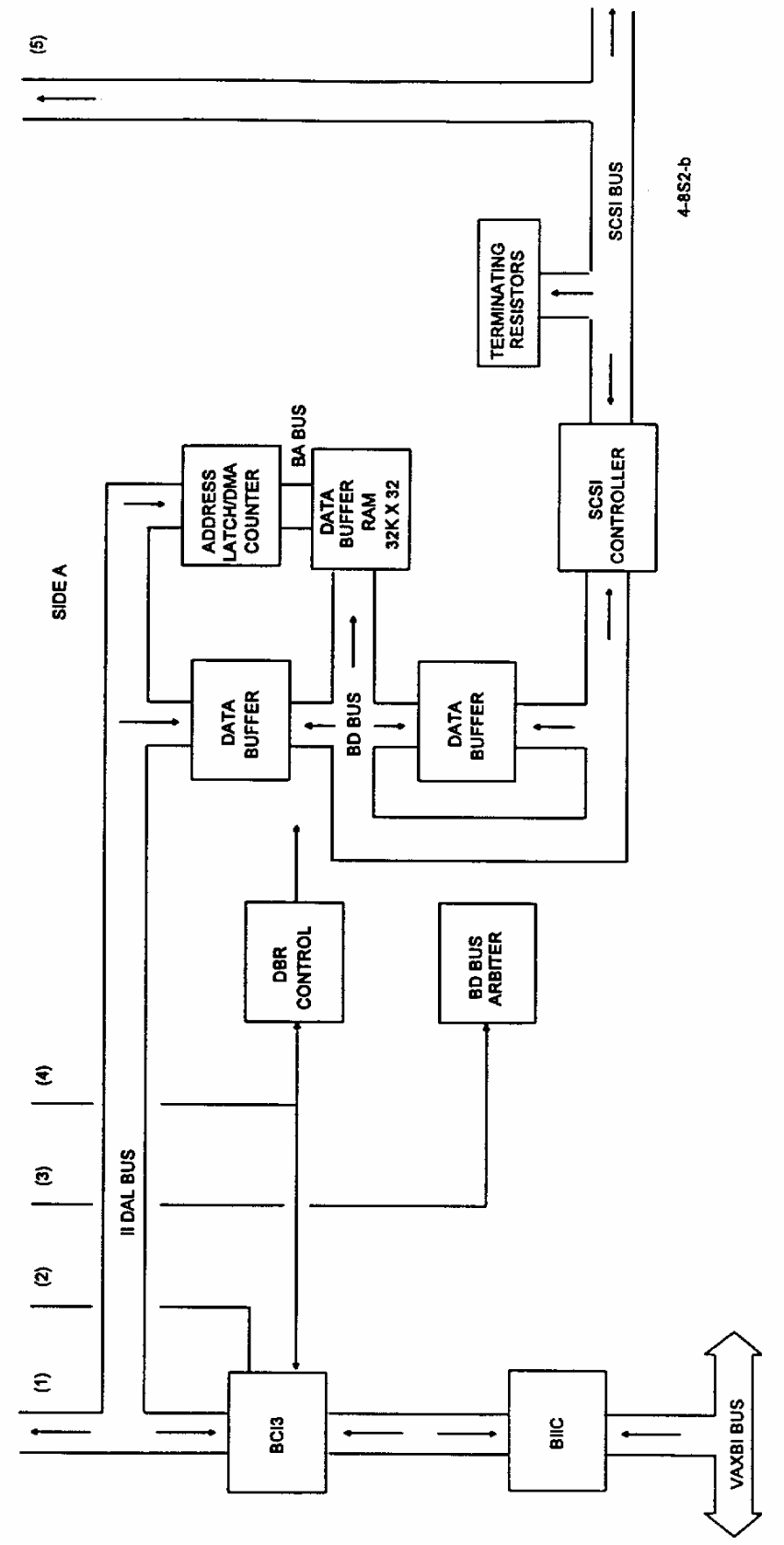


Figure 4-8. RSCSI Interface Block Diagram (Sheet 2 of 2)

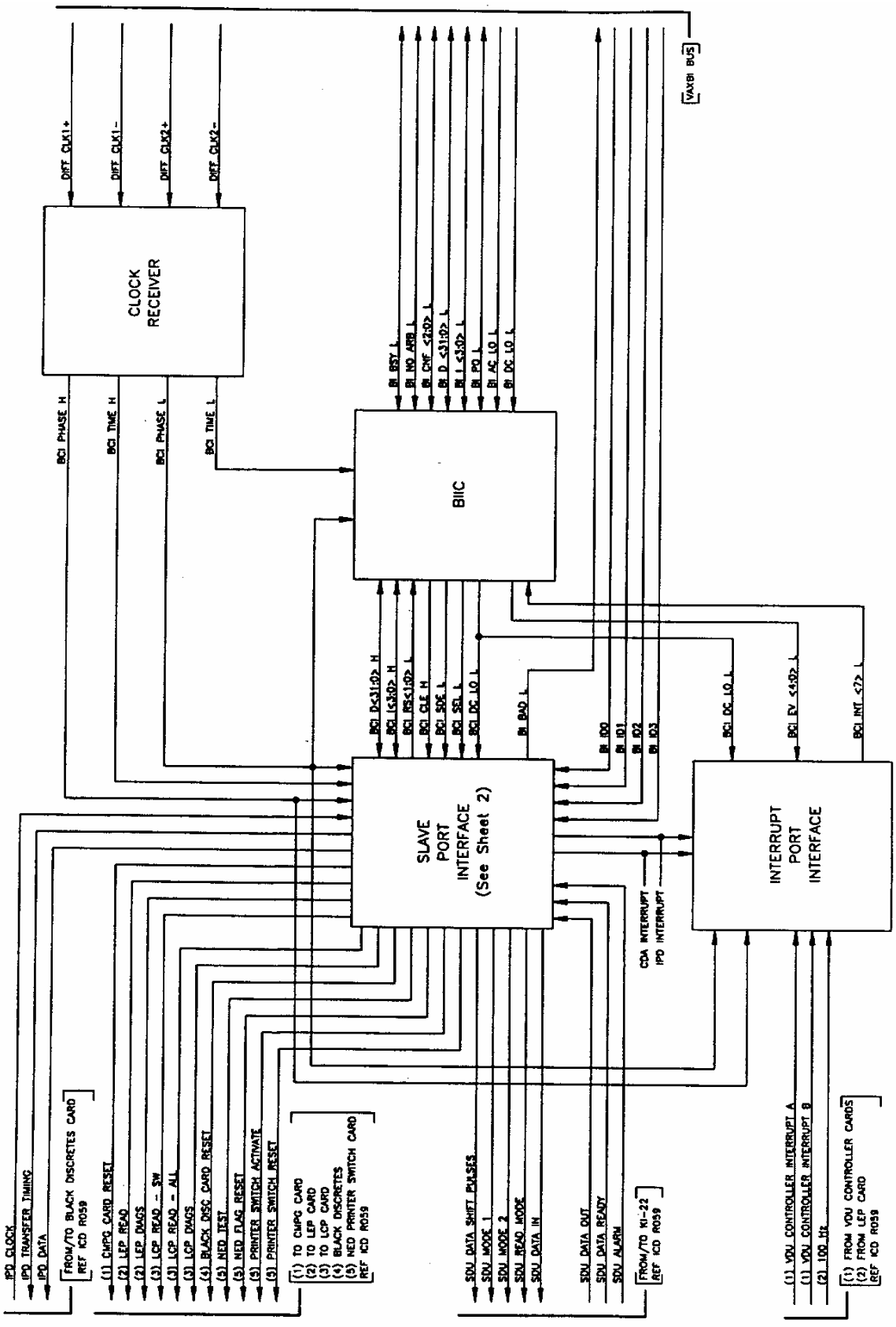


Figure 4-9. CDA/IPD Interface Block Diagram (Sheet 1 of 2)

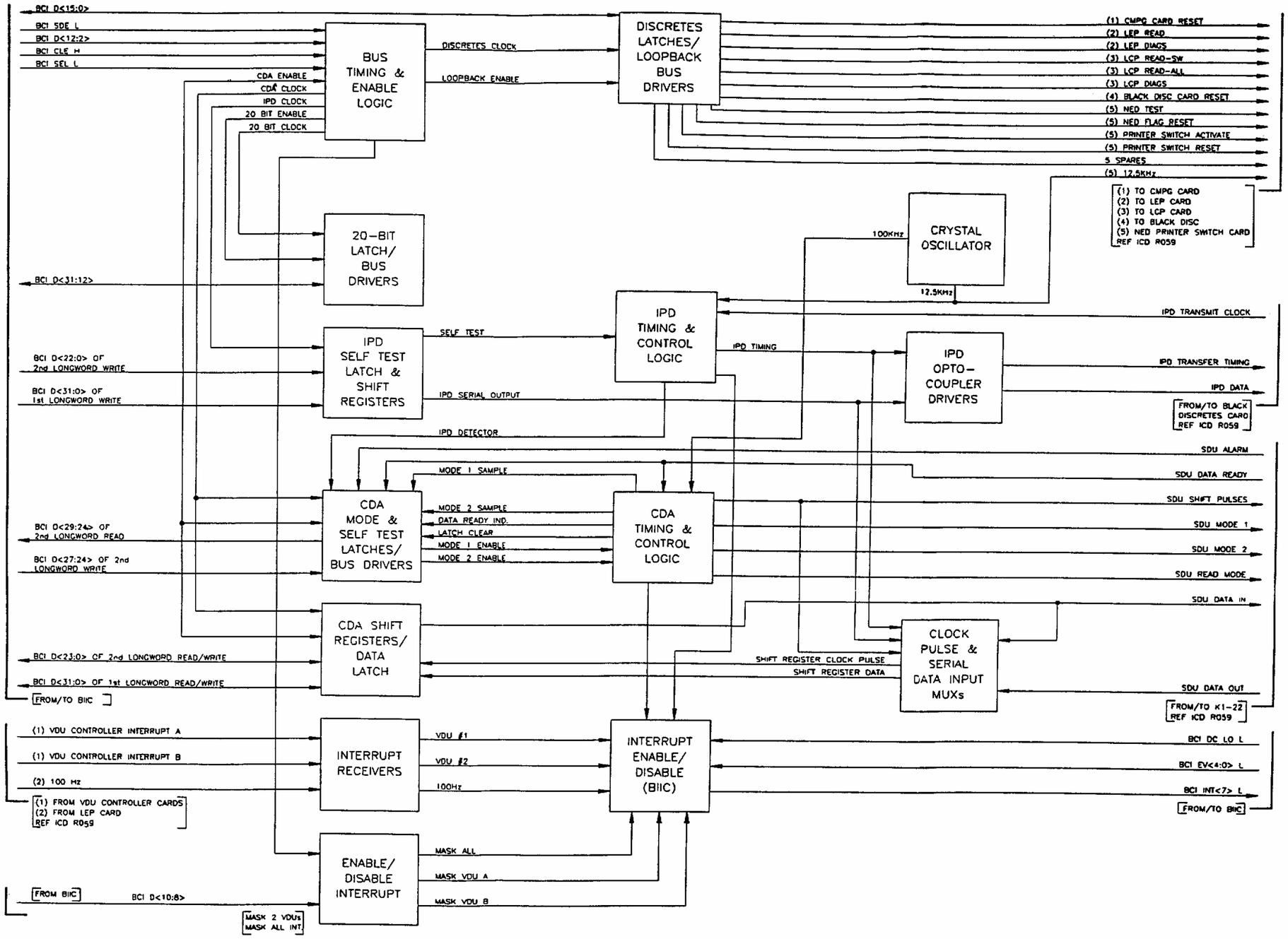


Figure 4-9. CDA/IPD Interface Block Diagram (Sheet 2 of 2)

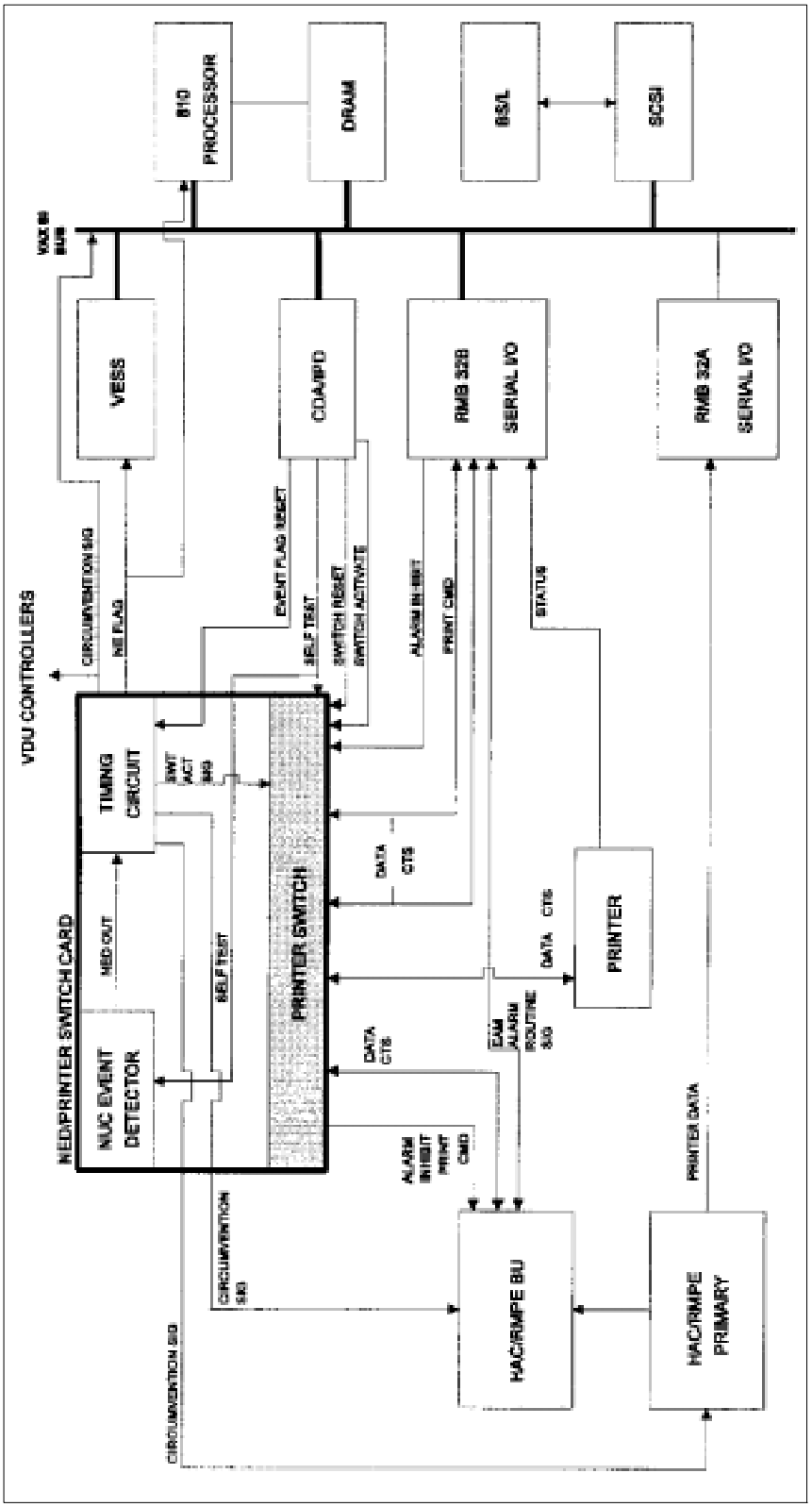


Figure 4-10. NED Printer Switch

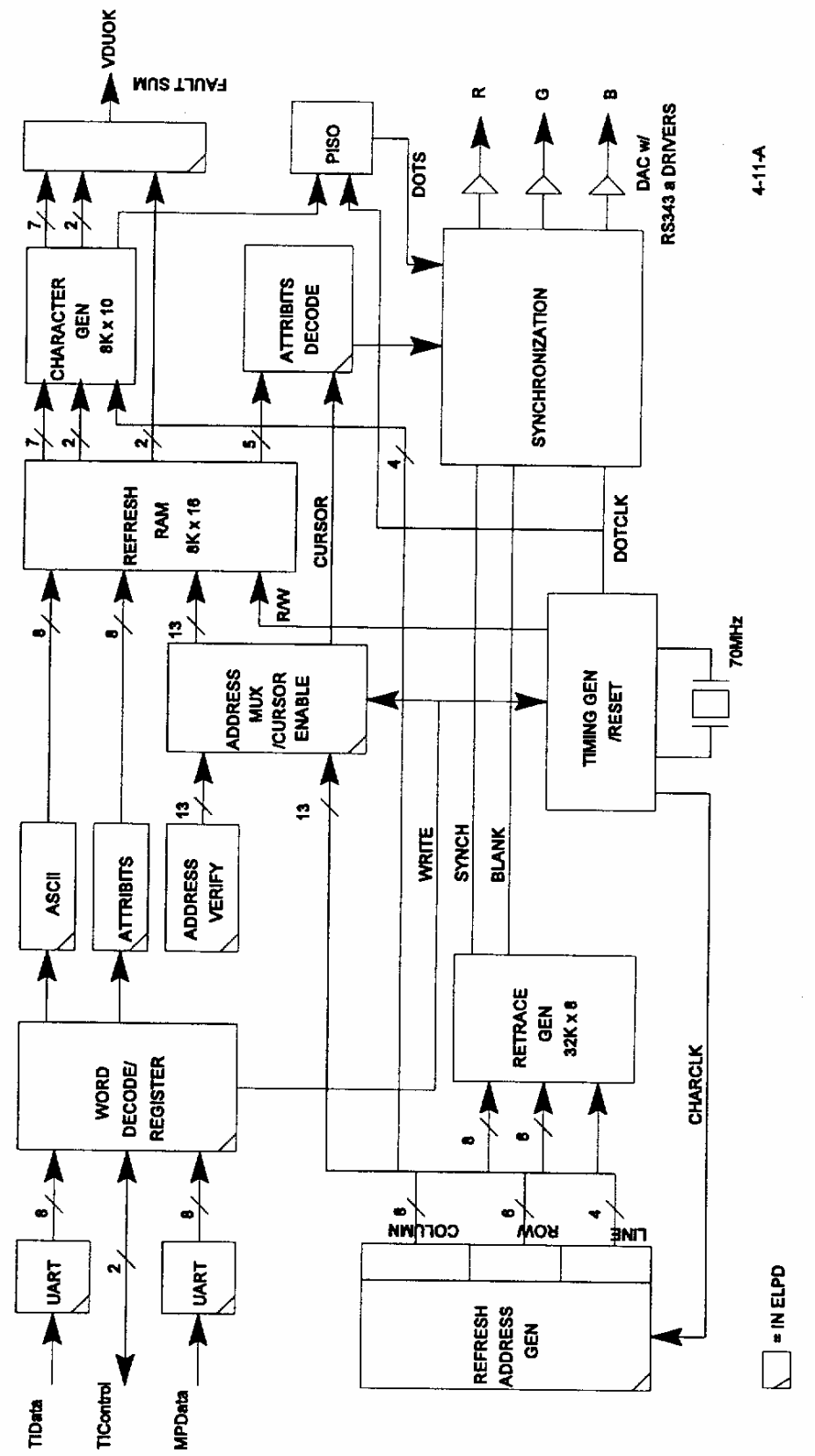


Figure 4-11. VDU Controller Block Diagram

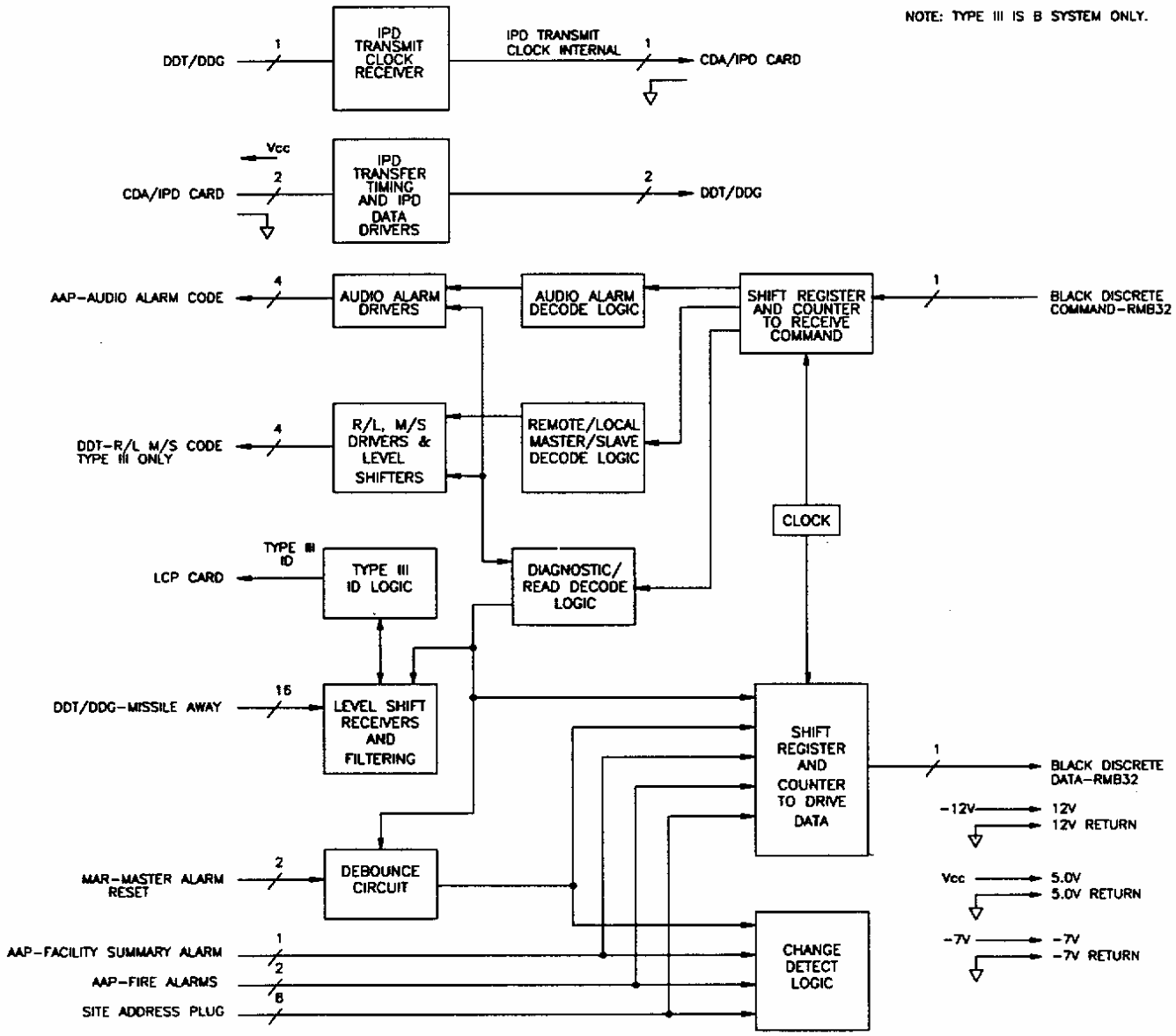


Figure 4-12. Black Discrete Block Diagram

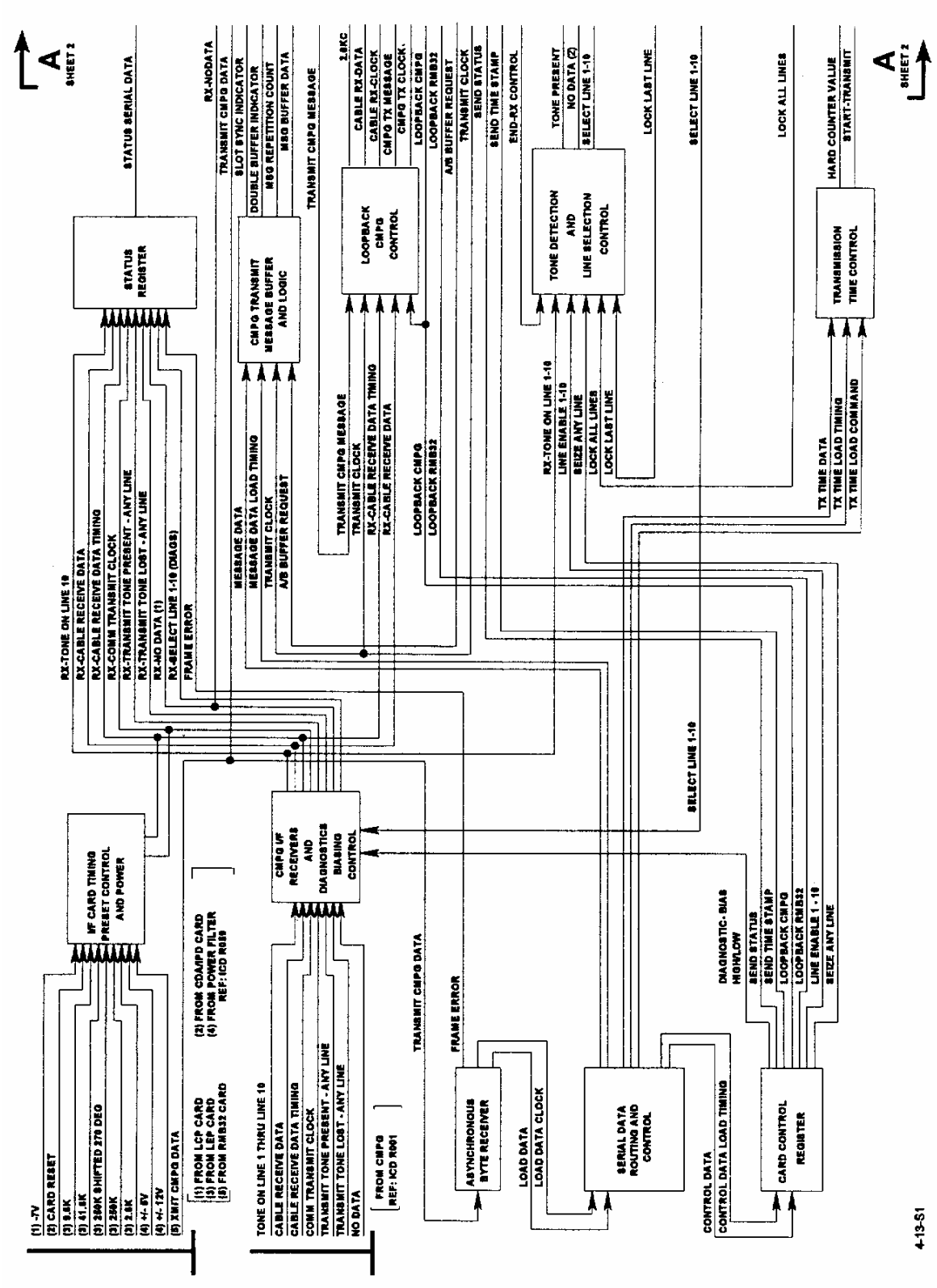


Figure 4-13. CMPG Interface Block Diagram (Sheet 1 of 2)

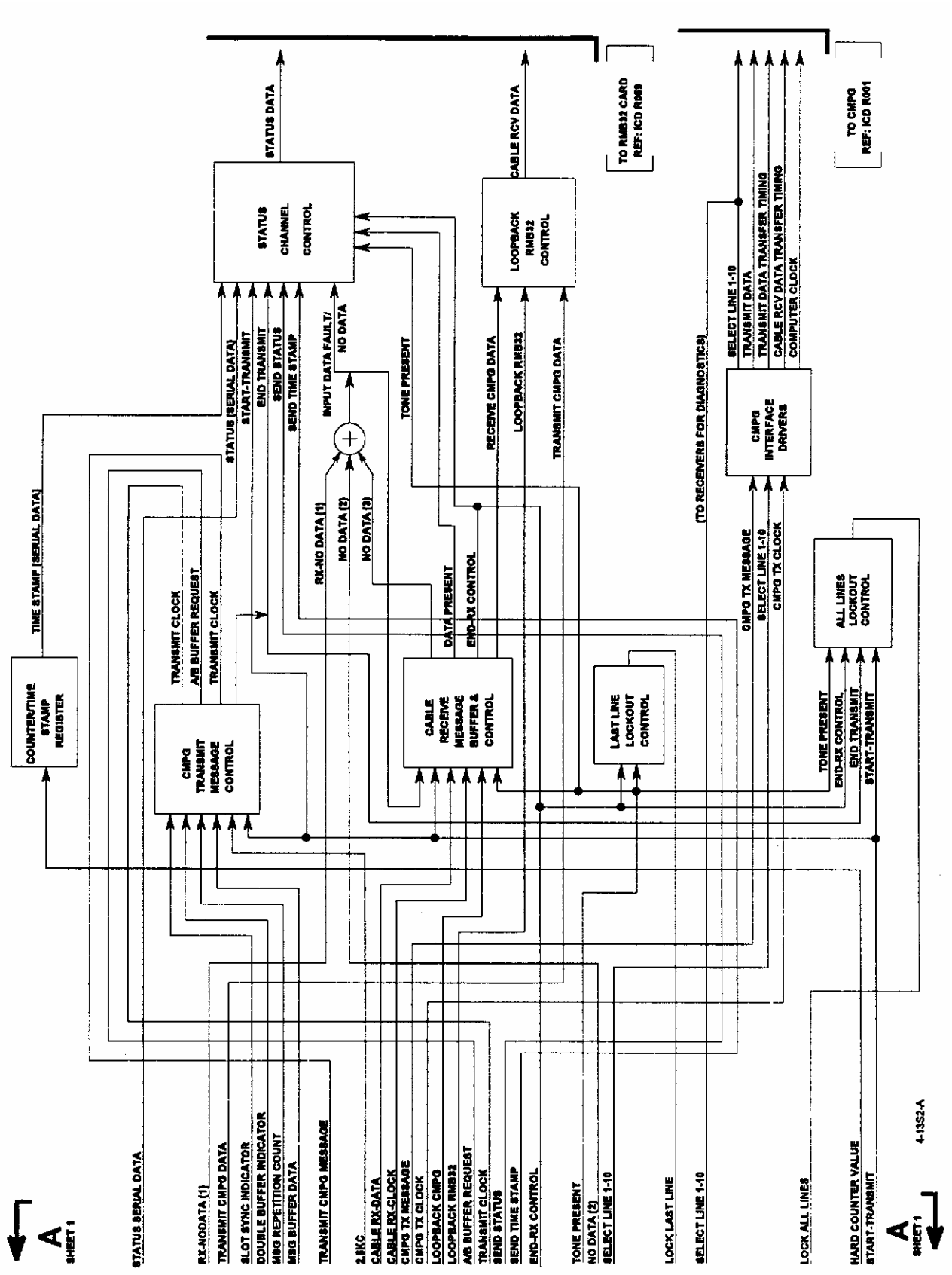


Figure 4-13. CMPG Interface Block Diagram (Sheet 2 of 2)

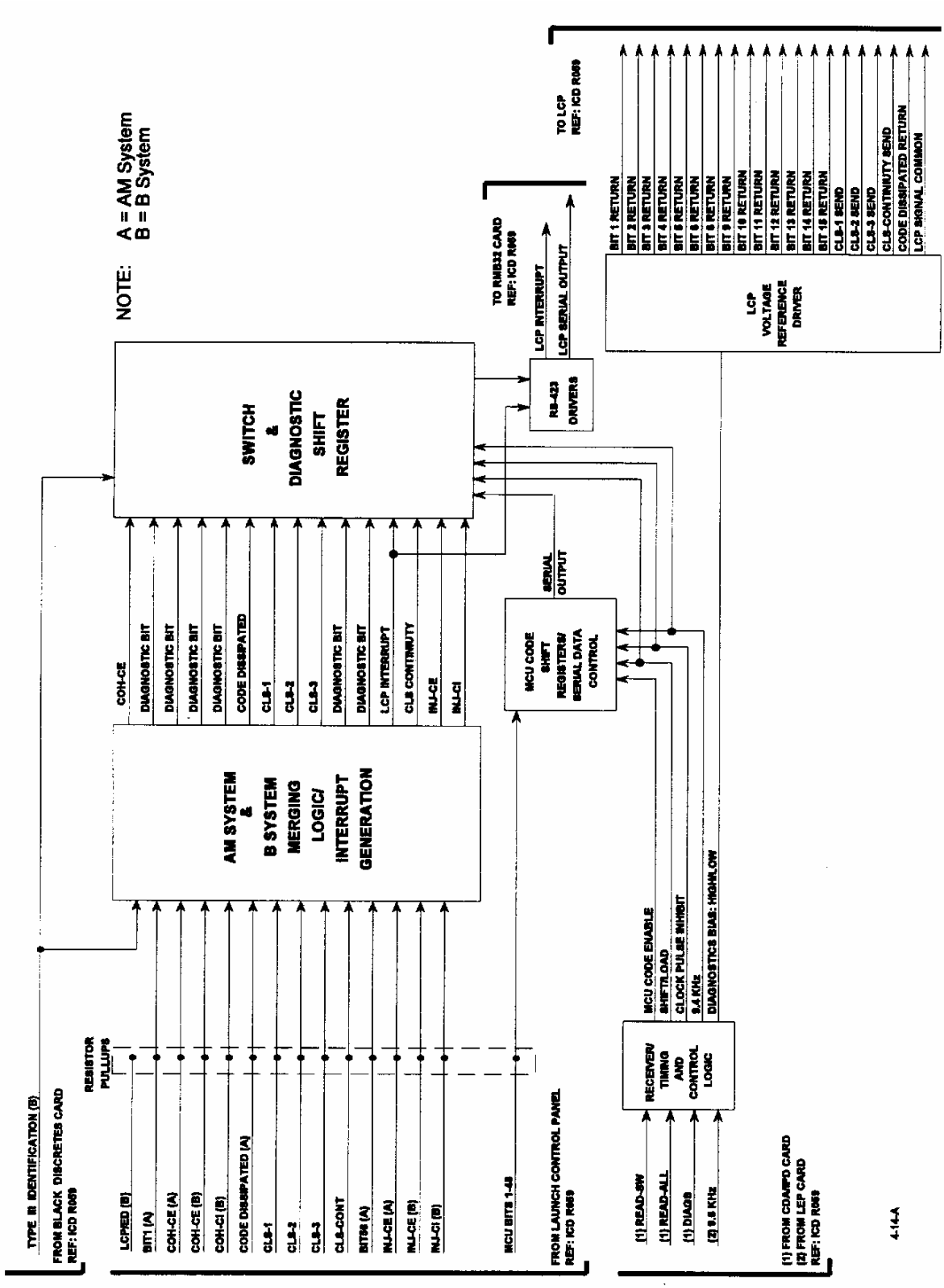


Figure 4-14. LCP Interface Block Diagram

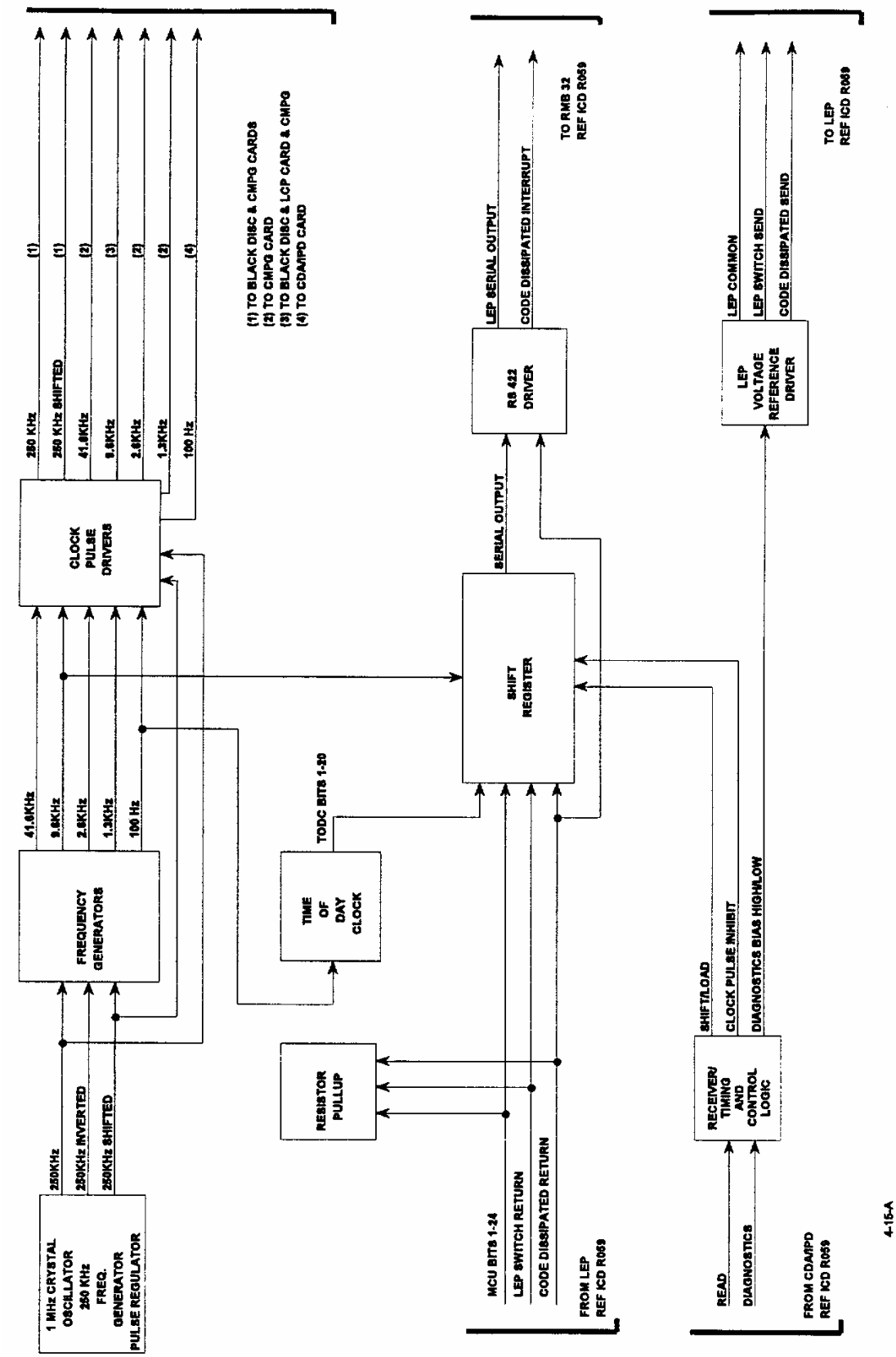


Figure 4-15. LEP Interface Block Diagram

Table 4-10. WSP Characteristics and Interfaces
Central Processor SMC810 (or ESMC)

SMC810 CHARACTERISTICS	
Power	· Three +5 Vdc, one -5 Vdc required · 18 Watts nominal · Startup order of power application: - Memory (+5 Vdc) - Time of Year Clock (+5 Vdc) - Computer Logic (+5 Vdc) - Serial Buffer Ports (-5 Vdc)
Location	· Slot A5 of the 9-slot backplane
CPU	· 32 bit CPU, 32 bit word size · CMOS Micro VAX family · CMOS Floating Point Accelerator (CFPA) coprocessor · Bus Interconnect architecture · VAXELN operating system · Interrupt driven · Run, halt modes
Instructions	· DEC VAX Instruction Set · 32-bit instruction words · Arithmetic operations on 32-bit words; double precision on 64-bit words
Timing	· 40 MHz clock · 1.7 MIPS for typical instruction mix · 0.6 μsec typical arithmetic instruction
Memory	· Boot ROM - 128 Kbytes of UVEPROM - Raytheon firmware - Startup/Restart routines, including self-tests - Diagnostic port user interface - ROM-based diagnostics (RBDs) commandable in halt mode · User ROM - 256 Kbytes of UVEPROM - COP firmware (SUR = System User ROM) - Startup routines - Tests of I/O cards - Memory overwrite routines · RAM - 512 Kbytes - Byte parity protection
Interval Timers (2)	· Resolution of 1 microsecond (μs) · Setable & readable under software control from 1 μs to 60 min · Stability no worse than 80 parts per million (ppm)
Time-of-Year Timer	· Setable & readable under software control · Provides day-of-year, hours, minutes, seconds, and msec · Resolution: 10 msec · Stability no worse than 80 ppm
Watchdog Timer	· Setable from 100 ns to 429 sec · Set by COP to 10 sec
Self-Tests	· ROM-based diagnostics (RBDs) · Run at startup and at restarts · Commandable via diagnostic port

Table 4-10. WSP Characteristics and Interfaces Central Processor SMC810 (or ESMC) (Continued)

SMC810 INTERFACES		
Main Memory (EMAD)	PIO-32	DATA transfers via MEbus - 32bit, 20 MHz
I/O Modules (RMB32s, RSCSI, CDA/IPD)	PIO-32	MESSAGE transfers via VAXBI-M - 32bit, 20 Mhz Note: this interface is only repeated for each of the I/O modules on the VAXBI-M bus if there is some special characteristic to mention.
Diagnostic Port (also called Console Port)	SIO	OFF-LINE COMMANDS/DATA - Async (1/1/N), 2.4 kbps, RS-423
Front panel port	SIO	(not used)
NED/Printer Switch Card	DI	NED FLAG

Table 4-11. WSP Characteristics and Interfaces Memory (EMAD)

EMAD CHARACTERISTICS	
Power	· +5 Vdc · 18.2 Watts typical · 21.5 Watts maximum
Location	· Slot A6 of the 9-slot backplane
Type	· Dynamic Random Access Memory (DRAM)
Size	· 4 Mbyte = 4,194,304 bytes (1M = 1024 x 1024 = 1,048,576) · 32-bit words (called long-word)
Speed	· 10 Mhz ME clock · 600-1800 ns Read/Write transactions (byte to octaword range)
Refresh	· Required every 15.47 μs average · Duration 385 ns average; 500 ns worst case
Modules	· 1 4-MByte board installed · Expansion capability for 1 board
Error Detection and Correction	· 7-bit code attached to each long-word · Corrects 1-bit errors · Detects and faults multiple bit errors
Organization	· Data stored in 32 1Mbit by 1-bit DRAM logic devices, organized in 1 bank of 1M addresses by 32 bits wide · Check code stored in 7 1Mbit by 1-bit DRAM logic devices, organized in 1 bank of 1M addresses by 7 bits wide

Table 4-11. WSP Characteristics and Interfaces Memory (EMAD) (Continued)

EMAD CHARACTERISTICS		
Firmware	· In 32 KByte EEPROM (Electrically Erasable) · Contains RBDs	
Self-Tests	· RBDs run at startup - All locations tested for 1s and 0s · RBDs commandable via diagnostic port - Three-pass memory test · On-line self-test via error detection and correction (EDAC)	
EMAD INTERFACES		
MEbus	PIO-32	DATA via MEbus - 32 bit, 20 MHz

Table 4-12. WSP Characteristics and Interfaces Input/Output (I/O) - VAXBI-M

VAXBI BUS CHARACTERISTICS	
Power	· N/A
Location	· Part of 9-slot backplane
Functions	· Connects SMC810 to RMB32s, RSCSI, and CDA/IPD modules.
Architecture	· 32 data lines · Bus terminator is VESS module · Node ID on bus comes from plug on backplane slot: range 1-15 · Address space (in Hex): - Memory 0000 0000 to 1FFF FFFF - I/O 2000 0000 to 3FFF FFFF
Protocol	· 3-cycles: - address/command - imbedded arbitration - data · 32-bit data word - 4 instruction bits - 1 parity bit · Direct Memory Access (DMA) from SMC810 to I/O cards · Byte, Word (16-bits), Longword (2 words, 32-bits) or Octaword (8 words) transfers from I/O cards to SMC810

Table 4-12. WSP Characteristics and Interfaces Input/Output (I/O) – VAXBI-M (Continued)

VAXBI BUS CHARACTERISTICS	
Speed	· 13.3 MBytes per second (Octaword) · 10.0 MBytes per second (Quadword) · 6.67 MBytes per second (Longword)
VAXBI-M BUS INTERFACES	
SMC810	· Addressed card latches command, e.g., WRITE, READ · At data cycle, WRITE latches data from SMC810 into addressed card registers; READ enables addressed card to drive data onto bus
VESS	· Provides bus termination · Provides bus reset signals
RMB32, RSCSI, CDA/IPD	· Data exchanged between these I/O cards and SMC810

Table 4-13. WSP Characteristics and Interfaces Input/Output (I/O) - VESS: Bus Controller Card

VESS MODULE CHARACTERISTICS		
Power	· +5 Vdc, 11.0 Watts maximum · +12 Vdc, 1.3 Watts maximum · -12 Vdc, 0.1 Watts maximum	
Location	· Slot A9 of 9-slot backplane	
Functions	· Terminates VAXBI bus · Sequences power at startup · Provides VAXBI reset functions · Generates Time and Phase clocks for VAXBI bus · Senses Time of Year clock power out of spec · Receives status signals to generate fault and warning signals · Halts bus activity at NED signal	
Components	· Pull-up resistors for termination · Sensing circuitry for functions above	
Processor	· No processor or software	
Memory	· No ROM or RAM	
Resets	· Initiated from power supply, VAXBI-M interfaces · Initiated from NED module	
Diagnostics	· Reports faults sensed by power supply, VAXBI bus, sensors in chassis	
VESS CARD INTERFACES		
· VAXBI-M bus	CLK-O DO	20 MHz RESET BUS control line
· NED/Printer Switch card	DI	NED RESET

Table 4-14. WSP Characteristics and Interfaces Input/Output (I/O) - RMB32

RMB32 CHARACTERISTICS	
Power	· 15-30.5 Watts (nominal). ± 5 Vdc
Location	· RMB32A: slot A1 of 9-slot backplane · RMB32B: slot A2 of 9-slot backplane
Functions	· Transfer data between comm ports and the VAXBI-M bus
Components	· Microprocessor, ROM, RAM, comm ports
Processor	· 32-bit μproc · Runs on-board firmware and diagnostics
Memory	· 128 KByte EEPROM - Contains operational firmware - RBDs commandable from diagnostic port · 128 KByte RAM for data transfers - Control and status registers - FIFOs for async channels - DMA files and scratchpad registers
Async Ports	· 8 asynchronous RS422/RS423 channels - 4 with full modem controls - Data rates to 38.4 Kbps
Sync Port	· 1 synchronous RS422/RS423 channel - SDLC protocol - Data rates to 64.0 Kbps
Throughput	· Max throughput 21,000 char per sec (includes all input and output, all channels) · Modified protocol gives priority to port 0 (used for VDUs)
Bus Interface	· VAXBI-M bus interface - DMA transfers from SMC810, in octawords - DMA transfers into SMC810 only for sync port - Byte, Word, Longword, Octaword transfers into SMC810
Self-Tests	· RBDs, run at startup and restarts - Check ROM, RAM, internal functions, VAXBI interface · Commandable RBDs, via diagnostic port (in HALT mode) - Additional RBDs do external loopback

Table 4-14. WSP Characteristics and Interfaces Input/Output (I/O) - RMB32 (Continued)

RMB32-A INTERFACES		
Left OID	SI DI-pair	OID 1 CONTROL/DATA (Port 0 RxD) - Async (1/1/E), 2400 baud, RS-422A OID 1 CONNECTED INDICATOR (Port 0 CTS(H), RC(L)) - Switched to WSCE if set
Left VDU controller card	SO	VDU DATA (Port 0 TxD) - Async (1/1/E), 38.4 kbaud, RS-423
HAC/RMPE Primary (RMP)	SI SI DO-9	WSP DATA (R030)/HAC DATA (R059) (Port 4 RxD) - Async (1/1/N), 9600 baud, RS-422A PRINTER DATA/HAC PRINT DATA Port 6 RxD) - Async (1/1/N), 9600 baud, RS-422A HAC ACK (Port 3 RTS) HAC CLEAR TO SEND (Port 0 RTS) HAC CLOCK SYNC (Port 1 RTS) HAC EAM ALARM RESET (Port S RTS) HAC EAM RELEASE (Port S DTR) HAC LCC TEST (Port 1 DTR) HAC NAK (Port 3 DTR) HAC NON-EAM ALARM RESET (Port 2 DTR) ROUTINE ALARM RESET (Port 2 RTS) - all are RS-423
Time of Day Clock (TODC)	SO	TIME OF DAY DATA (Port 1 TxD) - Async (1/1/N), 1200 baud, RS-422A
Floppy Disk Drive (FDD)	SI SO	FDD STATUS/DATA (Port S RxD) - Sync, 38.4 Kbps, RS-422A, SDLC protocol FDD CONTROL/DATA (Port S TxD) - Sync, 38.4 Kbps, RS-422A, SDLC protocol
NED/Printer Switch Card	DI	PRINTER SWITCH STATUS (Port 3 CTS)
LCP I/F card	SI DI	LCP OUTPUT DATA (Port 1 RxD) - SECURE CODE DATA - LAUNCH DIAGNOSTIC DATA - READ SWITCHES DATA - Async (1/1/N), 9600 baud, RS-423 INITIATE INDICATION (Port 1 DSR) - Indicates LCP and/or CLS switch thrown

Table 4-14. WSP Characteristics and Interfaces Input/Output (I/O) - RMB32 (Continued)

RMB32-A INTERFACES		
LEP I/F card	SI DI	LEP OUTPUT DATA (Port 3 RxD) - ENABLE DIAGNOSTIC DATA - ENABLE SECURE CODE DATA - Async (1/1/N), 9600 baud, RS-423 CODE DISSIPATED INDICATION (Port 3 DSR) - Indicates code dissipated when set
RMB32-B INTERFACES		
Right OID	SI DI-pair	OID 2 DATA (Port 0 RxD) - Async (1/1/E), 2400 baud, RS-422A OID 2 CONNECTED INDICATOR (Port 0 CTS(H), RC(L)) - Switched to WSCE if set
Right VDU controller card	SO	VDU CONTROL/DATA (Port 0 TxD) - Async (1/1/E), 38.4 kbaud, RS-423
HAC/RMPE Backup	SI DI-2 DO-3	RMPB PRINTER DATA (Port 6 RxD) - Async (1/1/N), 9600 bps, RS-422A RMPB EAM ALARM (Port S DSR) RMPB ROUTINE ALARM (Port S CTS) RMPB CTS (Port 0 RTS) RMPB PRINT CMMD (Port S RL) RMPB ALARM INHIBIT (Port S LL)
Printer	SI DI-pair SO	PRINTER STATUS (Port 2 RxD) - Async (1/1/E), 9600 bps, RS-422A PRINTER CTS (via NED/PS) (Port 2 CTS(H), RC(L)) PRINTER DATA (via NED/PS) (Port 2 TxD) - Async (1/1/E), 9600 bps, RS-422A
CMPG I/F module	SI SO SI	CMPG INPUT DATA (Port 3 RxD) - Async (1/1/N), 9600 bps, RS-423A CMPG OUTPUT DATA (Port 3 TxD) - Async (1/1/N), 9600 bps, RS-423A CMPG STATUS (Port 4 RxD) - Async (1/1/N), 9600 bps, RS-423A
Black Discrete I/F card	SI SO	BLACK DISCRETE DATA (Port 7 RxD) - Async (1/1/N), 9600 bps, RS-423 BLACK DISCRETE CMMD (Port 7 TxD) - Async (1/1/N), 9600 bps, RS-422A

Table 4-15. WSP Characteristics and Interfaces Input/Output (I/O) - RSCSI

RSCSI CHARACTERISTICS		
Power	· +/- 5 Vdc · 18 watts max	
Location	· Slot A3 of 9-slot backplane	
Functions	· Transfer data between VAXBI-M bus (SMC810) and SCSI bus (BS/L) · Conforms to ANSI X3.131, 1986	
Components	· Microprocessor, ROM, RAM, bus interfaces	
Processor	· CVAX Microprocessor · Executes ANSI Common Command Set (CCS) (ANSI X3T9.2)	
Memory	· Programmable Array Logic (PAL) for address code and decode · 128 KByte ROM - Initialization routines - Control routines - Diagnostics · 128 KByte RAM for data transfers - Command and status registers - Data transfer buffers	
Transfers on SCSI bus	· 1.5 MByte/sec asynchronous transfer · 4.0 MByte/sec synchronous transfer · Transfers protected by Fire Code and byte parity · Transfers use REQ/ACK handshake protocol · One byte transferred per handshake	
VAXBI Bus Interface	· VAXBI-M bus interface - Octaword DMA transfers from SMC810 - Byte transfers into SMC810	
Self-Tests	· RBDs at power-up - Check ROM, RAM, internal functions, VAXBI interface · Commandable RBDs, via diagnostic port - Check disk (BS/L) formatting - Perform destructive disk tests	
RSCSI INTERFACES		
· Bulk Storage/Loader (BS/L)	PIO-8+1	BS/L STATUS and (READ/WRITE) DATA - 8-bit parallel plus parity bit - 1.5 MByte/sec, asynchronous
	DIO-2	Control signals: BSY, RST
	DO-3	Control signals: ACK, SEL, ATN
	DI-4	Control signals: MSG, REQ, C/D, I/O

Table 4-16. WSP Characteristics and Interfaces Input/Output (I/O) - CDA/IPD Card

CDA/IPD CARD CHARACTERISTICS	
Power	· + 5 Vdc · 11.4 watts nominal
Location	· Slot A4 of 9-slot backplane
Functions	· Transfer data between VAXBI-M bus (SMC810) and SDU device (KI-22) - ENCRYPT, DECRYPT, HALF-ADD and ENCRYPT, ALARM TEST operations · Send discrete commands to CMPG, LEP, LCP, Black Discrete interface modules, and the NED Card · Prepare data for transfer to IPD modem
Components	· Hardened register · Interrupt port (5 interrupts) · 16 discrete lines - Discrete asserted for 140 - 160 μsec min
Processor	· No processor
Memory	· No ROM or RAM · Shift registers for data transfer · Latched registers for storing TOD Counter data (from LEP Card)
Interrupt Port	· 5 external interrupts, 2 maskable - 100 Hz clock pulse from LEP card - VDU error interrupt A, maskable - VDU error interrupt B, maskable · 2 internal interrupts - CDA transaction complete - IPD transaction complete
Hardened register	· Set and read from SMC810 · Stores frame start time · Used after NED circumvention
Diagnostics	· CDA loopback: moves data from SMC810 through CDA shift registers on card · IPD loopback: Moves data from SMC810 through IPD shift registers on card, and into CDA registers · Discretes loopback (SMC810 can read discretes and interrupt port within 140 μsec after discrete write)

Table 4-16. WSP Characteristics and Interfaces Input/Output (I/O) - CDA/IPD Card (Continued)

CDA/IPD CARD INTERFACES		
· VAXBI-M bus	PIO-32	MESSAGE transfers via VAXBI-M · DMA transfers from SMC810 · Longword transfers into SMC810 · Interrupt to SMC810 for: - external interrupt - transaction complete
· SDU (KI-22)	SO SI DO-3 CLK-O DI-2	SDU DATA IN SDU DATA OUT - Sync, 100 kHz Control lines - SDU MODE 1, SDU MODE 2, SDU READ MODE SDU DATA SHIFT PULSE: 100 kHz Control lines - SDU DATA READY, SDU ALARM
· IPD Modem, via Black Discrete Card	SO	IPD DATA - Sync, 50 kHz, 54-bit transfers - Clock supplied by IPD, passed through by Black Discrete Interface card
· CMPG I/F Card	DO	CMPG CARD RESET
· LEP I/F Card	DO-2 CLK-I	LEP READ LEP DIAGS 100 Hz
· LCP I/F Card	DO-3	LCP READ-SWITCHES LCP READ-ALL LCP DIAGNOSTICS
· Black Discrete I/F Card	DO	BLACK DISCRETE CARD RESET
· NED/Printer Switch Card	DO-4	NED TEST NED FLAG RESET PRINTER SWITCH RESET PRINTER SWITCH ACTIVATE
· Opto Isolators	PWR	+5 Vdc, GND

Table 4-17. WSP Characteristics and Interfaces Input/Output (I/O) - NED/Printer Switch Card

NED/PRINTER SWITCH MODULE CHARACTERISTICS		
Power	· ± 5 Vdc, ± 12 Vdc · 5 Watts maximum	
Location	· Slot A12 of the Red Backplane	
Functions	· Detect gamma dose-rate radiation · Detect multiple events separated in time · Output a reset signal to the WSP when the detection threshold is exceeded - Within 150 nanoseconds - Pulse width of 0.5 sec ± 0.1 sec. · Supply a status indication, readable by COP · Operate without upset · Simulate NED activation upon COP request · Perform printer switch function upon COP request · Test switch function upon COP request	
Components	· NED circuitry · Multiplexers (for switching) · Timing circuitry	
Processor	· No processor	
Memory	· No ROM or RAM	
Diagnostics	· Test printer switch function	
NED/PRINTER SWITCH CARD INTERFACES		
SMC810	DO	NED FLAG
VESS	DO	CIRCUMVENTION FLAG
VAXBI-M	DO	NED PULSE
CDA/IPD I/F card	DI-4	NED TEST request NED FLAG RESET PRINTER SWITCH RESET PRINTER SWITCH ACTIVATE
RMB32-A	DI SO	PRINTER CTS PRINTER DATA
RMP	DO	NED PULSE
RMPB	DO-2 DO SI	ALARM INHIBIT PRINT COMMAND PRINTER CTS PRINTER DATA

Table 4-18. WSP Characteristics and Interfaces Input/Output (I/O) - VDU Controller Cards

VDU CONTROLLER CHARACTERISTICS	
Power	· +5 Vdc, -5.2 Vdc · 19.9 Watts maximum
Location	· VDUC-A: slot A-10 of Red Backplane · VDUC-B: slot A-11 of Red Backplane
Functions	· Transform data from COP (via RMB32) into video Red/Green/Blue (RGB) signals - 8 colors, inverse video, flash - Text and character graphics - Standard, bold, underline fonts - Trackball display · Report error conditions
Components	· ROM, RAM, 70 MHz crystal oscillator, 343-A drivers · Cell pointers: - 48 rows x 102 chars - Cell = 10 horiz x 16 vert pixels
Memory	· Retrace Timing Generator ROM - 1 32K x 8 bit EPROM · Character Generator ROM - 2 32K x 8 bit EPROMs · Refresh RAM - 7 ASCII + 1 parity bits - 7 attribute + 1 parity bits - 2 32K x 8 bit CMOS RAMs
Diagnostics	· Detected on-line: - Serial input parity error - Serial input framing error - Refresh RAM ASCII parity error - Refresh RAM attribute parity error - Character EPROM High byte parity error - Character EPROM Low byte parity error - Timing EPROM parity error

Table 4-18. WSP Characteristics and Interfaces Input/Output (I/O) - VDU Controller Cards (Continued)

VDU CONTROLLER INTERFACES		
RMB32A or B	SI	SCREEN DATA - 38.4 Kbps, async, 1/1/E
CDA/IPD I/F card	DO	ERROR INTERRUPT
VDU Left or Right	SO-3	Video signals, RGB - Coaxial cable, RS-343-A - Sync signal on Green - Horizontal timing 48 kHz - Vertical synchronization 60 Hz

Table 4-19. WSP Characteristics and Interfaces Input/Output (I/O) - Black Discrete Interface Card

BLACK DISCRETE INTERFACE CARD CHARACTERISTICS	
Power	· +5 Vdc, -7 Vdc, -12 Vdc · 6.5 watts nominal
Location	· Slot A14 of the Black Backplane
Functions	· Receive discrete data from CMPG, AAP, SAP and MAR; send data serially to COP (via RMB32-B) · Receive serial data from COP (via RMB32-B); send discretes to AAP with loop back capability · Provide drivers and receivers for CDA/IPD to IPD interface · Provide power to optoisolators and SAP · Provide self-diagnostics capability
Components	· Shift registers, change detect logic, drivers, receivers
Processor	· No processor
Memory	· No ROM or RAM · Shift registers to move data
Diagnostics	· Capability for COP to read (via RMB32-B card) status of discretes · High and Low diagnostics commandable by COP (via CDA/IPD card: sets lines high or low, respectively)

Table 4-19. WSP Characteristics and Interfaces Input/Output (I/O) - Black Discrete Interface Card (Continued)

BLACK DISCRETE CARD INTERFACES		
· RMB32-B card	SI	BLACK DISCRETE COMMAND - Async, 9600 bps, 1/1/N; unbalanced, ±5 V - byte error detected if first 4 bits of command are not 0
	SO	BLACK DISCRETE DATA - Async, 9600 bps, 1/1/N; unbalanced, ±5 V
· LEP card	CLK-I-3	9.6 kHz, 250 kHz, and 250 kHz shifted 270 deg
· CDA/IPD card	DI SI CLK-I CLK-O	BLACK DISCRETE RESET IPD DATA IPD TRANSFER TIMING INTERNAL IPD TRANSMIT CLOCK INTERNAL
· IPD Modem	SO CLK-O CLK-I	IPD DATA FOR TRANSMISSION TO IPD MODEM IPD TRANSFER TIMING, -6 V driver IPD TRANSMIT CLOCK, -6 V receiver
· Auxiliary Alarm Panel (AAP)	DI-2	FACILITY SUMMARY ALARM FIRE ALARM - Notify COP upon change - balanced TTL input lines
	DO-4 DO	AUDIO ALARM CODE (4-bit code) ALARM ACKNOWLEDGE
· CMPG (Missile Away lines)	DI-10	MISSILE AWAY lines (Contact closure) - notify COP upon change
· Master Alarm Reset (MAR)	DI-2	MASTER ALARM RESET (Contact closure) - notify COP upon change
· Site Address Plug (SAP)	DI-8 PWR GRND	SITE ADDRESS - send to COP upon READ command - provide power and ground - pullup resistor to +5V
· Optoisolators	PWR	+5 Vdc, GND

Table 4-20. WSP Characteristics and Interfaces Input/Output (I/O) - CMPG Interface Module

CMPG INTERFACE MODULE CHARACTERISTICS	
Power	· 14.5 watts nominal, +5 Vdc, -7 Vdc
Location	· Slots A16 and A17 of Black Backplane
Functions	· Transfer messages to CMPG - Store message and start time - Start xmsn at requested time - Generate message preamble - Generate unique message sync - Slot sync bit control - Perform diphase encoding - Provide gated 2.6 kHz timing - Provide message repetition - Handle PLCA1/PLCA2 dual message · Receive messages from CMPG - Detect tone present - Send select line signal (to CMPG) - Control line lockout - Send received bytes to RMB32-B · Provide status to COP - Line check status, card status, tone present, data present, no-data indicator · Provide 41.6 kHz clock to CMPG · Radiation hardened interval timer (operates through a nuclear environment) · Perform loopback and receiver diagnostics
Components	· Time comparator, shift registers, static RAM, rad-hard interval timer, EPROM
Processor	· No processor
Memory	· UVEPROM (transmission and status control state machines) · Static RAM for message buffer from COP (15 bytes) · Shift registers for message buffering and transfer
Diagnostics	· Receiver tests - Rcvrs forced to requested state (1 or 0), then read back and reported · RMB32 loopback test - Routes bytes from Transmit Data channel to input of the RS-423 driver to CMPG Receive Data channel and back to COP (via RMB32) · CMPG loopback test - Routes transmission message (including preamble, sync, repetitions) into receive message buffers of CMPG Receive Data channel and back to COP (via RMB32)

Table 4-20. WSP Characteristics and Interfaces Input/Output (I/O) - CMPG Interface Module (Continued)

CMPG INTERFACE MODULE INTERFACES		
RMB32-B card	SI SO SO	CMPG OUTPUT DATA CMPG INPUT DATA CMPG STATUS - All above Async (1/1/N), 9600 bps, RS-423A
CDA/IPD card	DI	· CMPG CARD RESET INDICATION
LEP card	CLK-I-6	· 1.3, 2.6, 9.6, 41.6, 250 kHz and 250 kHz shifted 270 deg
CMPG	DO-10 SO CLK-O CLK-O CLK-O DI-10 SI DI DI DI CLK-I CLK-I	· Select Line · Transmit Data · 2.6 kHz Transmit Data Timing · 1.3 kHz Receive Data Xfer Timing · 41.6 kHz clock to CMPG · Tone-on-Line · Receive Data · Transmit Tone Lost (any line) · Transmit Tone Present (any line) · No-Data · 2.6 kHz Comm Transmit clock (from CMPG) · 1.3 kHz Receive Data Timing

Table 4-21. WSP Characteristics and Interfaces Input/Output (I/O) - LCP Interface Module

LCP INTERFACE MODULE CHARACTERISTICS		
Power	· +5 Vdc, -12 Vdc · 2.7 Watts nominal	
Location	· Slot A18 of the Black Backplane	
Functions	· Pass codes and signals received from Launch Control Panel (LCP) to SMC810 · Provide -7 Vdc to BDI, CMPG, and LEP interface cards	
Components	· Shift registers, voltage reference driver, voltage converter, RS-423 drivers	
Processor	· No processor	
Memory	· No ROM or RAM	
Diagnostics	· Breakwire test: [1]. Read Switch (LCP, Launch, Inhibit, CLS) [2]. Read All (Reads [1] above plus MCU code) [3]. Diagnostic (Opens LCP Common and CLS grounds plus reads [2] above)	
LCP INTERFACE MODULE INTERFACES		
RMB32-A	SO DO	· LCP OUTPUT DATA - RS-423, 9.6 kHz · INITIATE INDICATION - RS-423 - Send for Launch or Inhibit switch thrown, any CLS thrown, code dissipated indication, CLS_CONT opened
CDA/IPD I/F card	DI DI DI	· READ SWITCHES COMMAND · READ ALL COMMAND · DIAGNOSTICS COMMAND
BDI	PWR-O	· -7 Vdc
CMPG	PWR-O	· -7 Vdc
LEP	PWR-O CLK-I	· -7 Vdc · 9.6 kHz clock
LCP: MCU	DI-48 DI-4 DI DO-6 DO-8 DO	· Launch/Inhibit code (MCU code, BITs 8-55) · COH-CE, INJ-CE, BIT1, BIT56 · Code Dissipated · MCU BITs 1-6 RETURN · MCU BITs 8-15 RETURN · LCP Signal Common (MCU BITs 7, 16-56)
LCP: CLS	DO-3 DO DI-3 DI	· CLS-1, -2, -3 Send · CLS Continuity Send · CLS-1, -2, -3 · CLS Continuity

Table 4-22. WSP Characteristics and Interfaces Input/Output (I/O) - LEP Interface Module

LEP INTERFACE MODULE CHARACTERISTICS		
Power	· +5 Vdc, -7 Vdc · 4.5 Watts nominal	
Location	· Slot A19 of the Black Backplane	
Functions	· Pass codes and signals received from Launch Enable Panel (LEP) to SMC810 · Provide clock to BDI, CMPG, LCP, and CDA/IPD interface modules	
Components	· Shift registers, voltage reference driver, RS-423 drivers, 1 MHz crystal oscillator, clock frequency generators, time of day counter	
Processor	· No processor	
Memory	· No ROM or RAM · Shift registers for data transfer	
Diagnostics	· High & Low · TODC	
LEP INTERFACE MODULE INTERFACES		
RMB32-A	SO DO	· LEP OUTPUT DATA (code/diag data) - RS-423, 9.6 kHz · LEP CODE DISSIPATED INDICATION - RS-423 interrupt
CDA/IPD I/F card	CLK-O	· 100 Hz
BDI I/F module	CLK-O-6	· 250 and 250 shifted 270 deg, 41.6, 9.6, 2.6, 1.3 kHz
CMPG I/F module	CLK-O-6	· 250 and 250 shifted 270 deg, 41.6, 9.6, 2.6, 1.3 kHz
LCP I/F module	CLK-O	· 9.6 kHz
Launch Enable Panel	DI-24 DI DI DO-2 DO	· LEP MCU Bits 1 through 24 · LEP SWITCH · LEP CODE DISSIPATED · LEP switch send, Code dissipated send · LEP signal common

Table 4-23. WSP Characteristics and Interfaces Red Power Supply

RED POWER SUPPLY CHARACTERISTICS	
Location	· Slot PS1 of the 9-slot backplane
Input Power Requirements	· 120 +/- 2.4 Vac, single phase · 60 Hz nominal, [54-62 Hz] · 400 Hz nominal, [380-435 Hz]
Input Power Characteristics	· 120 vac nominal, 50/60/400 Hz.
Red Operating Voltage Characteristics	· + 5.0 vdc +0% -5% at a max of 50 amps · - 5.0 vdc +10% -5% at a max of 1.5 amps · - 5.2 vdc +20% -5% at a max of 4 amps · +12.0 vdc +10% -5% at a max of 5 amps · -12.0 vdc +10% -5% at a max of 1 amp · Combined power supplied by the above voltages not over 320 watts.
Protection Features	· Surge protection - Normal performance: 103-132 VRMS - Normal performance during 2 second surge: 80-156 VRMS - Will survive during 2 second surge: 0-180 VRMS · Power on/off protection - Overshoot and undershoot protection, no-load and full-load · No single points of failure · Electronic overload protection · Withstands direct short to ground · Over-voltage protection on each voltage - Shuts down all output voltages · Operates without upset

4-4. WSP EXTERNAL INTERFACES. The interfaces between the WSP and external devices are described in the paragraphs that follow. See Figure 4-1 for the paths between the SMC810 (and hence also the Console Operations Program (COP)) and the devices.

4-4.1. Auxiliary Alarm Panel (AAP).

4-4.1.1. Functions. The COP and WSP interface with the auxiliary alarm panel for summary alarm indications from the panel, alarm acknowledgment to the panel, and the generation and reset of audio alarms at the panel.

4-4.1.2. Interface Definition. The interface consists of three discrete inputs to the WSP and 5 discrete outputs from the WSP. The input discretes are the LCEB Fire Alarm, the LCSB Fire Alarm, and the Facility Alarm Summary (i.e., any other alarm activates this input). The output discretes consist of a set of four that defines the Audio Alarm tone, and an Alarm Acknowledgment.

4-4.1.3. Audio Alarms. The commands for audio alarms correspond to 0 for Reset, 1 for Operator Notification, 2 for Yellow Routine, 3 for Green Routine, 4 for EAM, 5 for Critical, 6 for Fire, and 15 for Silence Audio.

4-4.1.4. Audio Alarm Protocol. To sound an alarm, COP sends first a Reset command, then the code for the desired alarm. COP sends the Silence Audio command to terminate the alarm sound. The Operator Notification is a "beep" type alarm; COP silences it within 200 ms after commanding it. The Green Routine is also a short-duration alarm that silences itself without operator intervention; COP sends the Silence Audio command within 800 ms of the Green Routine command.

4-4.1.5. Alarm Acknowledgment. The Alarm Acknowledgment discrete output from the COP and WSP provides the acknowledgment of alarms. The Alarm Acknowledgment discrete is normally 0 and becomes 1 upon acknowledgment by the COP and WSP that a facility and/or fire alarm was received. This acknowledgment occurs as an automatic response from COP when a facility and/or fire alarm is received. It inhibits the transmission of further facility or fire alarms until the operator has pushed the ACK pushbutton (see Figure 5-11) on the AAP.

4-4.2. Bulk Storage/Loader (BS/L).

4-4.2.1. Functions. The main functions performed by the WSP/BSL interface are those of writing information on and reading information from the BS/L. This transfer of information is accomplished by means of an 8-bit (plus parity) data bus, using the Small Computer System Interface (SCSI) request/acknowledge protocol. This protocol is performed by the RSCSI card, and is transparent to COP unless an error is detected, persists (the card retries twice), and is reported. The device drivers report only the existence of an error, not its type.

4-4.2.2. Electrical Interface. In addition to the 8-bit data bus, plus a parity bit, the following discrete signals are used:

a. ACK - Signal driven by the WSP to indicate acknowledgment for a REQ data transfer handshake.

b. BSY - Signal that indicates the data bus is being used.

c. MSG - Signal from the BS/L indicating that messages are being transferred either in or out of the BS/L.

d. SEL - Signal used by the WSP to select the BS/L as the output/input device.

e. REQ - Signal driven by the BS/L to indicate a request for a REQ/ACK handshake with data to follow.

f. C/D - Signal driven by the BS/L that indicates whether control or data information is on the data bus. True indicates control.

g. I/O - Signal driven by the BS/L that controls the direction of data movement on the data bus with respect to the WSP. True indicates input to the WSP.

h. ATN - Signal driven by the WSP to indicate an "attention" condition: the REACT application is to request a message out of phase.

i. RST - An "OR-tied" signal that indicates the RESET condition; it clears all bus activity.

4-4.2.3. Contents of BS/L. The data storage medium of the BS/L is the Head Drive Assembly (HDA). The HDA is a self-contained, environmentally sealed, removable, transportable hard disk assembly. The maximum usable HDA storage capacity is 104.8 Megabytes (512 bytes/sector, 33 sectors/track, 776 tracks/surface, 8 surfaces). The Wing Code Processing System (WCPS) writes and verifies the operational system programs and files to the BS/L as specified in Table 4-24. It writes and verifies additional Console Operations Program (COP) database files to the BS/L as specified by the FILE_LIST.DAT file on the COP Database input tape. These files are listed in Table 4-25. The files listed in Table 4-26 are protected by a Computer Memory Security Check, which is computed by the WCPS and stored in the CMSC.DAT file.

4-4.3. Command Message Processing Group (CMPG).

4-4.3.1. Functions. The WSP/CMPG interface is used to pass messages from COP and the WSP to the CMPG for transmission to the rest of the squadron; and to receive messages from the rest of the squadron via the CMPG. The received messages are passed to COP for processing.

4-4.3.2. Interface Definition. The WSP interface with the CMPG consists of one external indication, one serial input channel, one serial output channel, 22 discrete inputs, 10 discrete outputs, and five clock signals. The WSP controls all protocol and timing with the CMPG.

a. No Data - The external indication is a No Data interrupt from the CMPG to the WSP. The indication occurs when the CMPG detects the loss of diphase during the cable message receive function. The WSP responds to this interrupt by dropping the selected line and performing line lockout functions. The WSP will send a notification to COP that a No Data indication has occurred. A No Data indication is also sent to COP when tone on a selected line disappears prior to receipt of the last intelligence bit of the message.

b. Cable Receive Data - The one serial input channel transfers digital data received by the CMPG to the WSP, which then transfers it to COP. The timing for this channel is derived from the incoming data by the CMPG, and the message transfer is controlled by the WSP. Data transfer rate for this channel is 1,300 bits per second (bps).

c. Transmit Data - The one serial output channel transfers digital data from the WSP to the CMPG for transmission to the remainder of the squadron. The timing for this channel is supplied by the CMPG. Data transfer rate for this channel is 2,600 bps.

d. Tone on Line - The ten Tone on Line discrete inputs are used by the WSP to determine if a Tone Present state exists. If tone on line is detected for any or all lines enabled by COP, then the WSP begins line selection processing on all lines enabled by COP. The states of these lines are sampled by the WSP at various points during message reception. This status is sent to COP, which uses it to identify lines that have lost tone, lines that have a tone after a No Data interrupt, or lines that have continuous tones. Sampling is also performed during transmission. The ten Tone on Line discrete inputs are set to 1 to indicate tone present and 0 to indicate the absence of tone.

e. Transmit Tone Lost (any line) - This line is sampled by the WSP and sent to COP at various points during message reception and transmission. The Transmit Tone Lost discrete input from the CMPG indicates that one or more of the ten cable transmitter output lines have no signal. This discrete is set to 0 if all transmit lines have tones present. If any line does not have a tone, the discrete remains a 1.

Table 4-24. BS/L Fixed Files and Sources

File Description	File Name	Source Tape Number (Note 1)	Size (K=1024 bytes)
Disk Index	INDEXF.SYS	2	1.0 K
Main Directory	000000.DIR	2	8.0 K
Disk Bitmap	BITMAP.SYS	2	26.0 K
Text List of Disk Contents	FILE_LIST.DAT	2	21.5 K
Ca, Cb, Normalizing Words	CMSC.DAT	0	0.5 K
System Configuration Data	CONFIG.DAT	0	0.5 K
Target Case Input Database	CASE_OTP.TXT	8	387.0 K
Execution Plan Case Input Database	CASE_EPP.TXT	8	31.0 K
MA Database	MADB.DAT	5	67.0 K
EPP Database	EPPDB.DAT	5	78.0 K
Trajectory and Missile Parameters Data	TAMP.DAT	7	128.0 K
Launch Site Data	SITE.DAT	10	8.0 K
Launch Region Gravity Model Data	LRGM.DAT	10	31.5 K
Climatology Data	CLIM.DAT	10	140.0 K
Climatology Data Index	CLMNDX.DAT	10	6.0 K
Generalized Error IMU Compensation Model Data	GENERIC.DAT	10	0.5 K
Minimum Case Input Selection Data	MINSEL.TXT	10	1.0 K
COP Executable	COP.SYS (Note 2)	1	3096.0 K
EPP Executable	EPP.EXE	4	73.5 K
EPP Case Validation Table	FORM_EPP.TXT	4	14.5 K
EPP Error Message Table	ERR_EPP.TXT	4	8.0 K
OTP Executable	OTP.EXE	6	332.5 K
OTP Case Validation Table	FORM_OTP.TXT	6	27.5 K
OTP Error Message Table	ERR_OTP.TXT	6	23.5 K
FDM Format Database	FDM_FMT.DAT	9	1.5 K
LF Offload Programs	OFFLOAD.DAT	12	38.0 K
WCPS Disk Information	WCPS.DAT	0	6.5 K

Source: ICD 25-R060

NOTE 1: Source tapes are numbered as follows:

0. Data generated by WCPS
1. COP
2. COP Database
3. COP Firmware Image (N/A to table)
4. EPP
5. EPP/MA Database
6. OTPD
7. TAMP
8. TCI/DGZ/EPCI or TCI/EPCI
9. FDM Format Database
10. OTP Database
11. COP BootROM Image (N/A to table)
12. LF Offload

NOTE 2: COP.SYS is a variable file as defined in ICD 25-R050.

Table 4-25. COP Database Files

FILES	FILENAME	(BYTES)
DISK INDEX	INDEXF.SYS	1024
MAIN DIRECTORY	000000.DIR	8192
DISK BITMAP	BITMAP.SYS	26624
TEXT LIST OF DISK CONTENTS	FILE_LIST.DAT	22016
DISK INDEX	INDEXF.SYS	512
DISK INDEX	INDEXF.SYS	125512
DISK INDEX	INDEXF.SYS	512
ACTIVE STACK	ACTIVE_STACK.DAT	1536
MENU DATABASE	HMI_MENU1.DAT HMI_MENU2.DAT HMI_MENU3.DAT HMI_MENU4.DAT HMI_TEXT1.DAT HMI_TEXT2.DAT HMI_TEXT3.DAT HMI_TEXT4.DAT	140000 140000 140000 140000 125000 125000 125000 125000
DEFAULTS DATABASE	DEFAULTS_DB.DAT	135000
DISPLAY TEMPLATES	TEMPLATES_FIELDS.DAT	200000
DISPLAY TEMPLATES	TEMPLATES_DEF.DAT	824000
HMI TEXT DATABASE	HMI_TEXT.DAT	10240
COMMAND DEFINITIONS	WSC_CMD_DEF.DAT	117512
COMMAND DEFINITION INDICES	WSC_CMD_INDEX.DAT WSC_OES_INDEX.DAT	512 2000
AFI TAKEOVER RULES	AFI_TAKEOVER.DAT AFI_AJ_TAKEOVER.DAT	512 512
PLC-B STACK	PLC_B_STACK.DAT	1536
EAM DEFAULTS	EAM_TO_DEFAULT.DAT	9216
PSO RULES	LF_ACTION_PSO.DAT	512
LF ALARM & GRID DATABASE	LF_ACTION.DAT	2560
SQUADRON ALIGNMENT DATABASE	SQD_ALIGN.DAT	4000
FILE ATTRIBUTES DATABASE	FILE_ATTRIBUTES.DAT	21512

Source: ICD 25-R060

Table 4-26. Files Requiring CMSC

Data Set	File Name	Notes
COP LOAD IMAGE	BOOTROM.EXE COP_FIRM.EXE COP.SYS	
OTP EXECUTABLE	OTP.EXE	
EPP EXECUTABLE	EPP.EXE	
COP DISK IMAGE	COP.SYS FILE_LIST.DAT * HMI_MENU.DAT ** TEMPLATES_FIELDS.DAT ** TEMPLATES_DEFS.DAT ** HMI_MENU1.DAT ** HMI_MENU2.DAT ** HMI_MENU3.DAT ** HMI_MENU4.DAT ** HMI_TEXT1.DAT ** HMI_TEXT2.DAT ** HMI_TEXT3.DAT ** HMI_TEXT4.DAT ** WSC_CMD_DEF.DAT ** WSC_CMD_INDEX.DAT ** AFI_TAKEOVER.DAT ** AFI_AJ_TAKEOVER.DAT ** EAM_TO_DEFAULT.DAT ** LF_ACTION_PSO.DAT ** LF_ACTION.DAT ** FILE_ATTRIBUTES.DAT	1,2,3
EPP DATA FILES	FORM_EPP.TXT ERR_EPP.TXT	
OTP/TAMP DATA FILES	TAMP.DAT FORM_OTP.TXT ERR_OTP.TXT	
EPP/MA DATABASE	EPPDB.DAT MADB.DAT	
FDM FORMAT DATABASE	FDM_FMT.DAT	
LF Offloads	OFFLOAD.DAT	

Table 4-26. Files Requiring CMSC (Continued)

Data Set	File Name	Notes
OTP DATABASE FILES	SITE.DAT LRGM.DAT CLIM.DAT CLMNDX.DAT GENERIC.DAT MINSEL.TXT	
CONFIGURATION/TIMER DATA	CONFIG.DAT	

NOTES:

1. The COP Disk Image CMSC is calculated over the COP.SYS file and the COP Database files. The COP Database files are included in the CMSC if the CMSC indicator in FILE_LIST.DAT = 5. The COP.SYS file is the first file processed through the algorithm followed by the COP database files in the order that they appear in FILE_LIST.DAT file. (Refer to Table 4-24)

2. This list reflects the current baseline indicated in FILE_LIST.DAT as described in Note 1.

3. The COP Database file indicated by * is a fixed file; all other COP Database files of the COP Disk Image data set indicated by ** are variable files as defined in Paragraph 6.3.1 of ICD 25 R050.

Source: ICD 25-R060

f. Transmit Tone Present (any line) - This discrete input from the CMPG indicates that tone is present on at least one of the transmitter output lines. If no line has tone present, the discrete is set to 0. Otherwise, it remains a 1.

g. Missile Away - The ten Missile Away discrete input signals are in one of two states: an open line or a grounded line. The open line exists during normal operations; the grounded line exists when the continuity loop at the LF has been broken (i.e., when a missile away indication exists).

h. Select Line n - The ten Select Line discrete outputs to the CMPG are used to select which line is gated to the demodulator. When a Select Line discrete is 1, the corresponding input line is gated into the demodulator. When all Select Line discretes are 0, none of the input lines are gated into the demodulator.

Table 4-27. Printer ASCII Character Set

b_7 / b_6 / b_5				0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
Bits				Column →							
b_4	b_3	b_2	b_1	Row ↓	0	1	2	3	4	5	6	7
0	0	0	0	0	①	①	SP	0	@	P	`	p
0	0	0	1	1	①	①	!	1	A	Q	a	q
0	0	1	0	2	①	①	"	2	B	R	b	r
0	0	1	1	3	①	①	#	3	C	S	c	s
0	1	0	0	4	EOT	①	$	4	D	T	d	t
0	1	0	1	5	ENQ	①	%	5	E	U	e	u
0	1	1	0	6	①	①	&	6	F	V	f	v
0	1	1	1	7	①	①	'	7	G	W	g	w
1	0	0	0	8	①	①	(	8	H	X	h	x
1	0	0	1	9	①	①	)	9	I	Y	i	y
1	0	1	0	10	LF	①	*	:	J	Z	j	z
1	0	1	1	11	①	①	+	;	K	[	k	{
1	1	0	0	12	FF	①	,	<	L	\	l	|
1	1	0	1	13	CR	①	-	=	M	]	m	}
1	1	0	0	14	①	①	.	>	N	^	n	~
1	1	1	1	15	①	①	/	?	O	_	o	■ ②

① Control Code NOT USED

② EOT Symbol

32 Control Codes

64 Character Set

96 Character Set

128 Character Set

4-6b-tbl

Source: ICD 25-R059, Vol. II

i. Computer Clock - The Computer Clock master timing signal is a symmetrical square wave with a nominal frequency of 41.6 KHz (±150 parts per million) and is provided to the CMPG by the WSP. The CMPG uses this signal to derive lower order timing signals.

j. Receive Data clocks - The Cable Receive Data Timing clock signal is a 1.3 KHz signal provided by the CMPG. It is used by the WSP to synchronize the data transferred over the Cable Receive Data channel to the WSP. The Cable Receive Data Transfer Timing signal, derived from the Cable Receive Data Timing signal, is enabled by the WSP for the CMPG to transfer the desired number of data bits to the WSP.

k. The Communication Transmit Clock signal is a 2.6 KHz signal provided by the CMPG. This clock is used to synchronize the data transferred over the Transmit Data Serial channel to the CMPG. The Transmit Data Transfer Timing signal is enabled by the WSP to transfer the desired number of data bits to the CMPG.

4-4.4. Cooperative Launch Switches (CLS).

4-4.4.1. Functions. The COP and WSP interface to three cooperative launch switches to obtain the switch turn indicators necessary for the two-person, four-hand control.

4-4.4.2. Interface Definition. The interface consists of four discretes, three of which indicate whether the corresponding switch has been turned. CLS1, CLS2, and CLS3 are normally 0, becoming 1 for as long as the switch is turned and held. The fourth input, CLS Continuity, is achieved by sending a ground signal from the WSP to CLS1, which sends the return to CLS2, which sends the return to CLS3, which sends the return to the WSP.

4-4.5. Floppy Disk Drive (FDD).

4-4.5.1. Functions. The FDD is used for uploading and downloading files. The files are generally read by COP from the FDD and then written out to the BS/L; or they are read from the BS/L and written to the floppy. The operator selects these transfers by choosing the UPLOAD, DOWNLOAD, or CREW LOG ARCH options from the DATA MANAGEMENT submenus (reference Figure 1-20, Main Menu Hierarchy), and initiates them by pressing the INITIATE key on the OID. The operator can also select the DIAG DATA TO FDD option from the LCC CTRL submenus (reference Figure 1-20, Main Menu Hierarchy), which automatically initiates a transfer of the Diagnostic Data File from the BS/L to the FDD.

4-4.5.2. Electrical Interface. to the FDD is through the synchronous port on the RMB32-A card, using the SDLC protocol. This protocol is built into the firmware of the RMB32 card, and is transparent to COP. It is based on each message and response having the same basic format: Opening Flag, Address Byte, Command Code

Byte, Data Field, Error Check Bytes, Ending Flag. The interface is bidirectional, using pairs of TRANSMITTED DATA lines, RECEIVED DATA lines, TRANSMIT CLOCK lines, and RECEIVE CLOCK lines.

4-4.6. Launch Control Panel (LCP).

4-4.6.1. Functions. The COP and WSP interface to the launch control panel retrieve the Mechanical Code Unit (MCU) codes used by COP for launch message processing.

4-4.6.2. Interface Definition. The interface consists of 51 discrete inputs, with 48 of them carrying the MCU data. The remaining discretes are as follows:

a. COH/CE - This input indicates when either the Launch Switch or the Inhibit Switch is turned past the Code Used position, or when both switches are turned. COH/CE is normally 0, becoming 1 when either switch is turned past the Code Used position. To determine which switch has been turned, look at MCU Bit 56. If MCU Bit 56 is 1, then the Launch Switch has been turned.

b. INJ/CE - This input indicates when the Launch Switch is held at the Launch position, or when the Inhibit Switch is held at the Inhibit position. INJ/CE is normally 0, becoming 1 when either switch is held at the indicated position.

c. LCP Code Dissipated - This input indicates that an MCU code in the LCP has been tampered with. The discrete is normally 0, becoming 1 when any of the MCU codes in the LCP has been dissipated and a switch is turned which relates to the dissipated code.

4-4.7. Launch Enable Panel (LEP).

4-4.7.1. Functions. The COP and WSP interface to the launch enable panel to obtain codes to enable missile launch.

4-4.7.2. Interface Definition. The interface consists of 26 discrete inputs, with 24 of them carrying the MCU data. The remaining discretes are for Code Dissipated and LEP Switch. Code Dissipated is normally 0, becoming 1 when the MCU code has been dissipated and the LEP Switch has been turned. The LEP Switch is normally 0 (closed), becoming 1 (open) when the switch is turned.

4-4.8. Master Alarm Reset (MAR).

4-4.8.1. Functions. There are two Master Alarm Reset buttons (electrically, they are switches), one at each console position. They are used to clear all alarms shown on any VDU screen with a single action. When COP receives a reset from either switch, alarm acknowledgment and reset functions are performed.

4-4.8.2. Interface Definition. The interface consists of two discrete inputs to the WSP, which function as discrete closed or open switch contacts. The switch is normally closed, functions as an inactive input, and is binary 0 equivalent to COP. Depressing either switch results in open switch contacts, which functions as an active input, and is binary 1 equivalent to COP.

4-4.9. Operator Input Device (OID).

4-4.9.1. Functions. The WSP/OID interface is a one-way interface, from the OID to the WSP. Its function is to send characters and signals from the keyboard for display on the VDU screen, or for special action in the case of some function keys; and to send movement and selection data from the trackball for display on the VDU screen, or for special action on the part of COP. Additionally, the OID provides a discrete signal that is processed by COP to indicate that the OID has switched from the WSP to the RMP or back again. Whichever processor the OID is connected to also provides the power for the OID.

4-4.9.2. Protocol. Bytes are transmitted serially from the OID, with the least significant bit transmitted first. Keyboard data, trackball X-Y position data, and trackball switch data are multiplexed by the OID into the single serial line to the WSP. Data sent from the OID to the WSP and COP consist of a single prefix byte, which indicates the type of data, followed by a one or two-byte code with the contents of the data.

a. A8 (hex) indicates ASCII key data from the keyboard. A single byte of ASCII code will follow.

b. A1 (hex) indicates function key data from the keyboard. A single byte code will follow.

c. A4 (hex) indicates one of the trackball buttons was pressed. A single byte code will follow: 40 (hex) for button T1; 41 (hex) for button T2; 42 (hex) for button T3.

d. A2 (hex) indicates trackball X-Y data. Two bytes of data will follow: the first byte represents movement on the X-axis; the second byte represents movement on the Y-axis.

4-4.9.3. OID Connected Indicator. Since the OID can be switched between the WSCE and the HAC/RMPE, a discrete is provided to indicate that the OID is connected to the WSP. This signal is held at logic level 1 by the OID when the OID is connected to the WSCE, and will go to 0 when the OID is no longer connected to the WSCE. Note: If input is received from the OID when this line is at 0, this constitutes an error condition.

4-4.10. Printer (PTR).

4-4.10.1. Functions. The COP and WSP interface with the Printer, using ASCII format (reference Table 4-27), for the hardcopy output of selected data. Data received from RMP or RMPB are automatically queued and output. Print requests from COP originate with the operator, who makes selections from the PRINT submenu of the DATA MANAGEMENT menu (reference Figure 1-20, Main Menu Hierarchy.) The COP controls the printer resource scheduling, giving priority first to RMPB, then to RMP, then to WSP. A block of data (up to 66 lines) is allowed to complete before a higher priority print task takes precedence.

4-4.10.2. Interface Definition. The interface consists of two serial lines, one for output of Printer Control/Data to the printer, one for input of Printer Status from the printer.

4-4.10.3. Control/Data from COP to Printer. Data passed from COP to the printer are in ASCII format (reference Table 4-27), with the following ASCII characters interpreted by the printer as control characters:

a. End of Transmission (EOT) - EOT indicates the end of transmission to the printer. The printer prints the contents of the line buffer, followed by the EOT symbol, and advances the paper 20 lines.

b. Enquiry (ENQ) - ENQ causes the printer to return its status byte to COP.

c. Line Feed (LF) - The printer responds to, but does not print, the LF code. When LF is received, the printer prints the data in the line buffer up to the LF, then advances the active position to the first character position on the next line.

d. Form Feed (FF) - The printer responds to, but does not print, the FF code. When FF is received, the printer prints the data in the line buffer up to the FF, then advances to the top of the next form.

e. Carriage Return (CR) - The printer responds to, but does not print, the CR code. When CR is received, the printer prints the data in the line buffer up to the CR, then advances the active position to the first character position on the next line.

4-4.10.4. Status Byte from the Printer to COP. Upon request (ENQ), or upon change in status, the printer returns a byte of status on the Printer Device Status line to COP. When a status byte is not being transmitted, the line is held in a marking state. The status byte is interpreted as follows:

a. Bit 0 - Not used.

b. Bit 1 - Door open. Paper loading door is open.

c. Bit 2 - Malfunction. Set for any of: paper absent, paper torn, power fault, printhead over-temperature, printhead under-temperature.

d. Bit 3 - Off Line. Set for any of: door open, power off, initial power-up, self-test mode, malfunction is true.

e. Bit 4 - Paper Low. Set for fanfold paper when less than 20 sheets remain, or for roll paper when it is out of paper.

f. Bit 5 - Parity Error. Parity error on data byte received from COP. [The character is printed as a "?"]

g. Bit 6 - Top of Form. Set by FORM FEED from front panel, FF control character, automatic form feed for fan-fold paper.

h. Bit 7 - Not used.

4-4.11. Rapid Message Processor (RMP) (Primary/Backup).

4-4.11.1. Rapid Message Processing Subsystem (RMPS). The rapid message processing subsystem (Figure 4-16) is an integral part of the weapon system control console and consists of the Rapid Message Processor (RMP) and the Rapid Message Processor Backup (RMPB) (Figure 5-1, item 30 and 12). It also includes two workstations on the weapon system control console. Each workstation consists of a Higher Authority (HA) Visual Display Unit (VDU), dedicated to displaying HA communications, and a keyboard and trackball assembly. The keyboard and trackball assembly can be switched to interface with either the rapid message processing subsystem or the weapon system processor. The subsystem enables the missile combat crew to monitor and control the HA communications systems directly from the weapon system control console. The rapid message processing subsystem accomplishes the following:

a. Processes messages received over the Strategic Automatic Command and Control System (SACCS) (Figure 4-38), the Air Force Satellite Communication System (AFSATCOM) (Figure 4-39), the Survivable Low Frequency Communication System (Figure 4-44), the Extremely High Frequency Military Strategic and Tactical Relay (EHF MILSTAR) System (Figure 4-45), and the Intercontinental Ballistic Missile Super High Frequency Satellite Terminal (ISST).

b. Outgoing messages can be composed, stored, and transmitted over SACCS, AFSATCOM, and EHF MILSTAR. Messages transmitted previously can be recalled and transmitted again over another communication system without having to be recomposed.

c. Incoming messages are processed and displayed on the HA VDUs and can be printed on the weapon system printer, if the option is selected.

d. Duplicate messages are automatically suppressed.

e. Communications alarms are displayed on the HA VDU and the resulting Missile Combat Crew Member (MCCM) responses are initiated from the console.

f. When coded messages are received, the messages are decoded by the operators.

g. The Rapid Message Processor Backup (RMPB) provides an independent means for message reception and storage. The incoming messages are converted into a common printer format and are stored in separate buffers. One buffer is provided for each communication channel. When the printer function is enabled, the stored messages are printed, then each new message is printed as it is received. If the RMP fails, the MCCM is alerted by an RMP alarm reported on the weapon system VDU and can enable the printer without losing a message.

h. The RMPB interfaces only with the weapon system printer through the weapon system processor.

4-4.11.2. Rapid Message Processor and Rapid Message Processor Backup. The RMP provides communications interface, message processing, message storage, transmission interface and control of the HA VDU. The RMPB provides communication interface, message storage, and printout for backup if the RMP becomes inoperative. Both the RMP and RMPB contain separate red and black sections (Figure 4-17 and Figure 4-18) to comply with requirements for classified message traffic. To provide its capabilities, the RMP contains a Communication Integrator (CI) function, a Message Processor (MP) function, and a Transmission Integrator (TI) function. It also contains a journal memory loader, and two VDU controllers. The RMPB provides its capability with a CI. The CI in the RMPB is the same as the primary CI in the RMP. However, strapping in the backplane of the RMPB activates instructions in the software to allocate an area of memory for message storage. This allows the same communication processor/SACDIN interface controller (CP/SIC) circuit card (used as the communications processor) to be used in both the primary and backup applications. Paragraphs 4-4.11.3 through 4-4.11.6.2 provide more details of each major function of the RMP and RMPB.

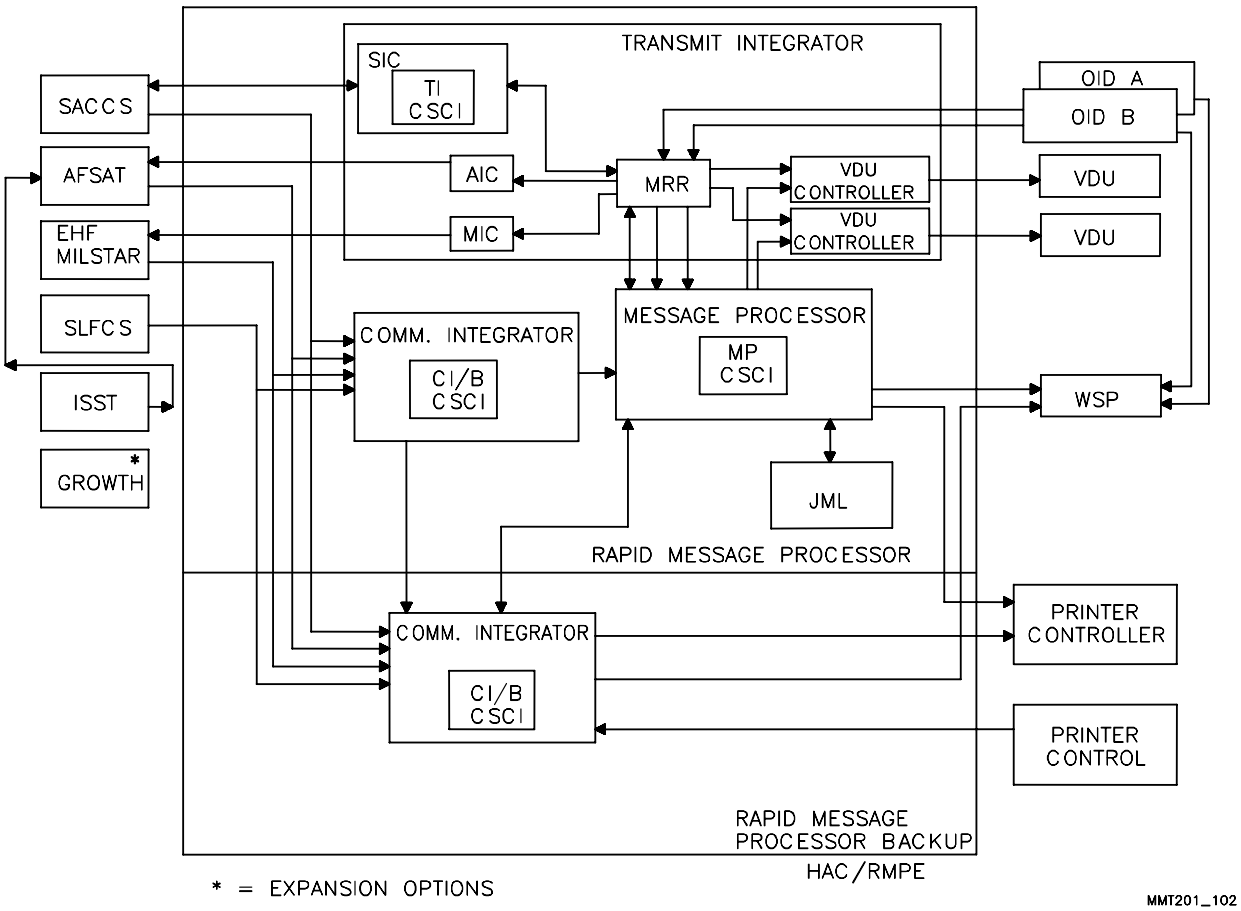


Figure 4-16. HAC/RMPE System

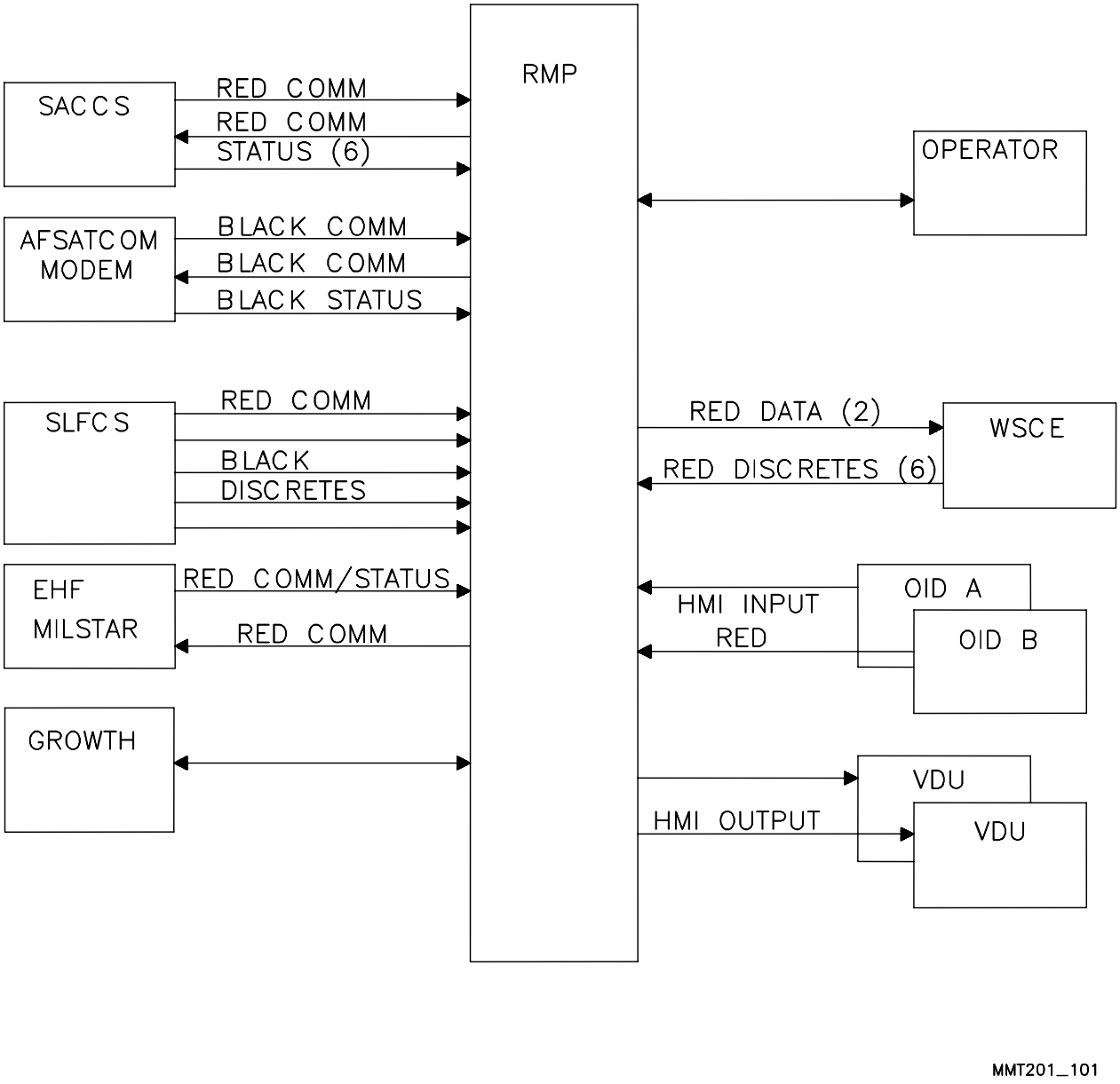


Figure 4-17. RMP Functional Interface Diagram

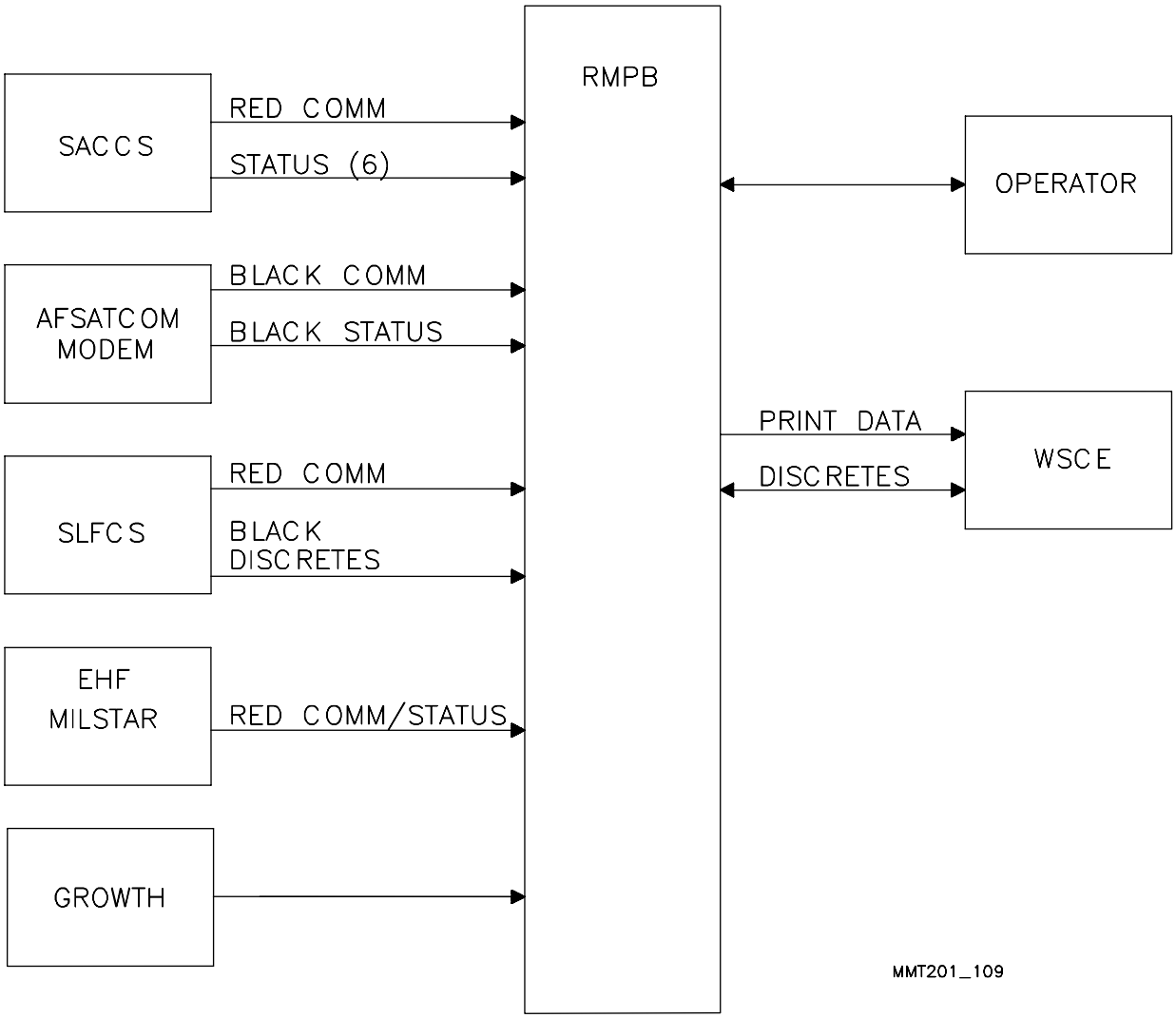


Figure 4-18. RMPB Functional Interface Diagram

4-4.11.3. Communications Integrator (CI). CP/SIC and Level Converter (LVCON) Circuit Care Assemblies (CCA) comprise the CI (see Figure 4-19). The CI interfaces with the HA communications systems for the reception of messages, discrete signals and alarm signals. Red and black level converters are contained on the LVCON CCA and the Communications Processor (CP) is on the CP/SIC CCA. Both the RMP and RMPB include separate CIs. The CP in the RMP is on CP/SIC (A42). The CP in the RMPB is on CP/SIC (A5). The level converter in the RMP is on LVCON (A35). In the RMPB, the level converter is on LVCON (A7). The same computer program is used in both locations. It is the communications integration/backup program. During normal operations, the data stream generated by the CI in the RMP is sent to the message processor in the RMP. When the RMP is inoperable, the data stream from the RMPB is stored in buffers located in the RMPB. One buffer is provided for each communication channel. When the printer function is enabled by the MCCM, the stored messages are sent to the weapon system processor and printed. From then on, each new message is printed until the function is halted by the MCCM. HA communication systems fault data and CI diagnostic data for the CI in the RMPB is sent to the MP for processing.

4-4.11.3.1. RMP Communications Processor. The RMP Communications Processor (CP/SIC A42) is implemented in firmware and executed on an 80C86, 16-bit microprocessor (see Figure 4-20). The microprocessor operates at a 6.4 MHz clock rate. It pre-processes all incoming message traffic and converts it to a serial data stream. The serial data stream is sent to the message processor. The communications integration/backup computer program is stored in the program UVPROM memory. This is an Erasable Programmable Read Only Memory (EPROM). Two Random Access Memories (RAM), message memory and scratch memory are used for message and working data storage. The bus controller receives instructions from the microprocessor and performs read, write and interrupt acknowledge cycles. Many of the CP's functions are implemented in an application specific Integrated Circuit (ASIC). Those functions implemented in the ASIC are identified on Figure 4-20. The CP includes three Universal Asynchronuous Receiver Transmitters (UART) to interface with the MP data port, WS printer and the MP console port. For the RMP CP, only the MP data UART is used. Each UART accommodates simultaneous asynchronous serial reception and transmission. Four interrupt controllers are in the ASIC. The interrupt controllers monitor 28 separate lines for interrupt requests. Three program timers provided in the ASIC are used by the software to generate accurate timing delays. Some CP functions are provided in an Erasable Programmable Logic Device (EPLD). Two are the timebase generator and the watchdog timer used to control wandering software. Two decoders are also implemented in EPLD. One is used to enable memories in the CP and the other is used to enable the three UARTs. There are three ways the hardware can reset the CP; power-up; front panel reset and Nuclear Event Detected (NED) signal from the weapon system. During power-up, power is passed through a RC circuit to a clock generator in the ASIC. The RC circuit assures that the power is stable prior to the end of the reset. The front panel resets the CPU. The NED signal resets the CPU and is used to reset the journal memory loader (JML). All three signals are passed on to other CCAs in the system.

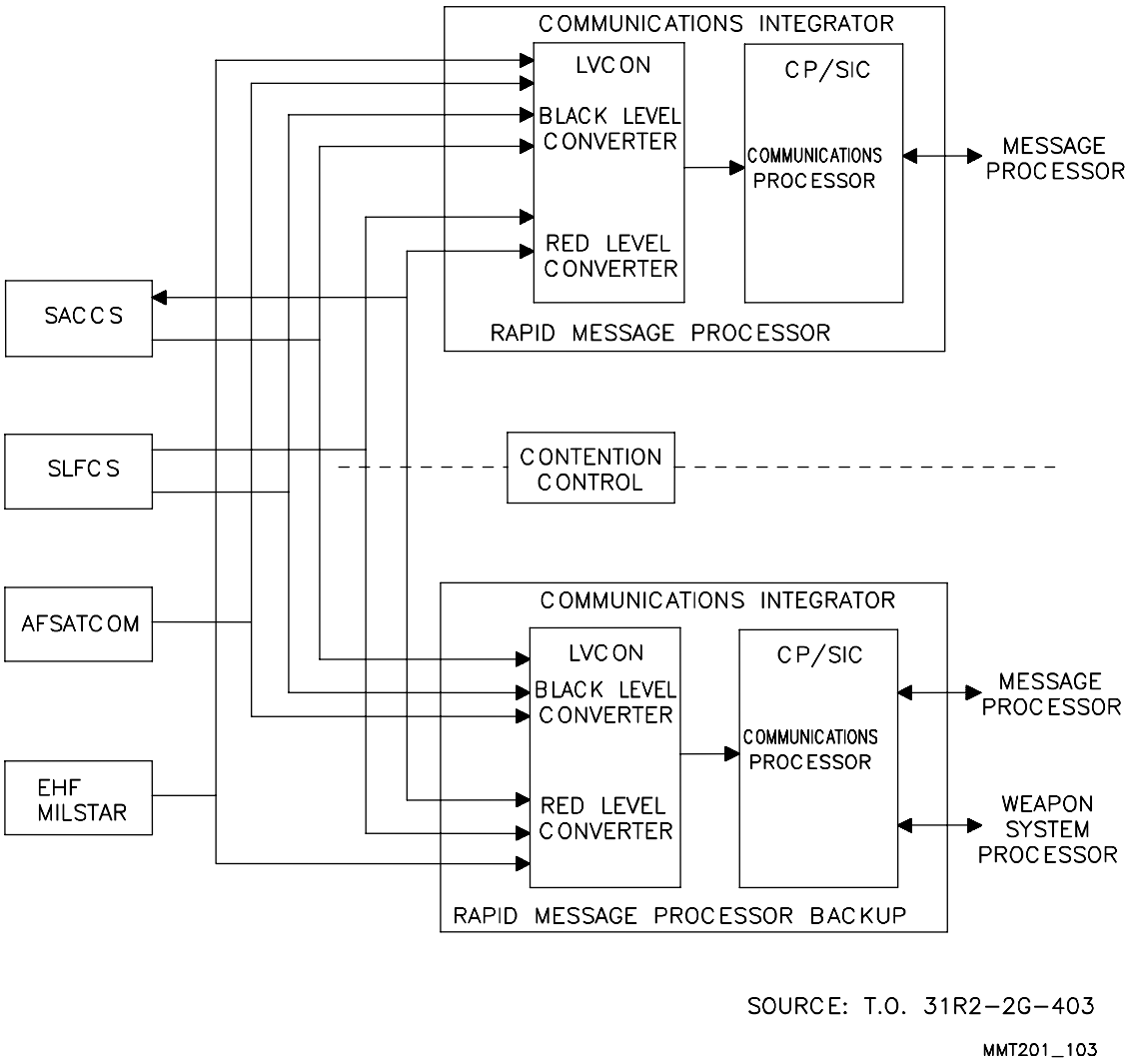
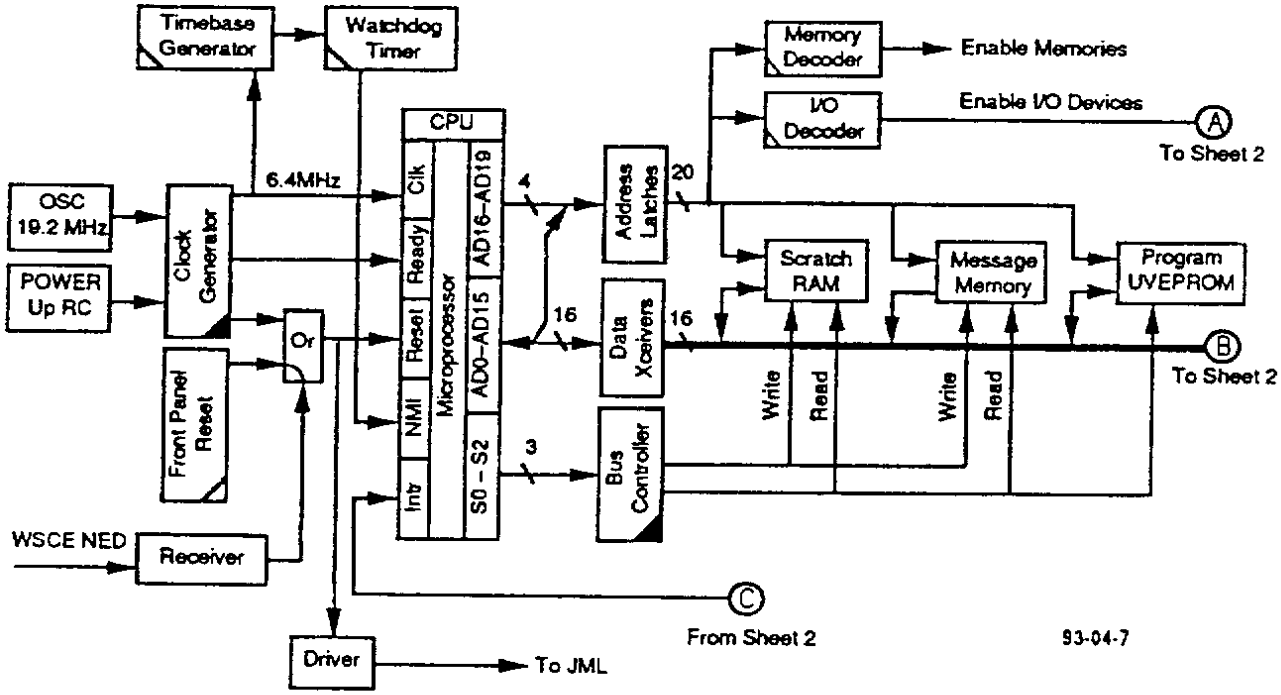


Figure 4-19. Communications Integrator Function Block Diagram

4-4.11.3.2. RMPB Communications Processor. The RMPB CP functions identically to the RMP CP. Both processors use the same computer program. In the RMPB, the serial data stream generated is sent to the console printer rather than the MP. It does interface with the WS printer and can receive data from the MP console port. The RMPB CP uses all three UARTs.

4-4.11.3.3. Level Converter. The level converter function of the CI and CI Backup (CIB) is provided by the LVCON CCA. The LVCON CCA in the RMP has the reference designation A35 and has the reference designation A7 in the RMPB. Figure 4-21 is a block diagram of the LVCON CCA. In both the RMP and RMPB, the LVCON CCA provided red/black isolation and converts the HA communications signal levels and protocols to levels usable by the CP. It contains receivers designed to interface with AFSATCOM, SLFCS, SACCS, and EHF MILSTAR communication systems. The LVCON CCA provides



SOURCE: TO 3142-2G-403

Figure 4-20. Communications Processor Function Block Diagram (Sheet 1 of 2)

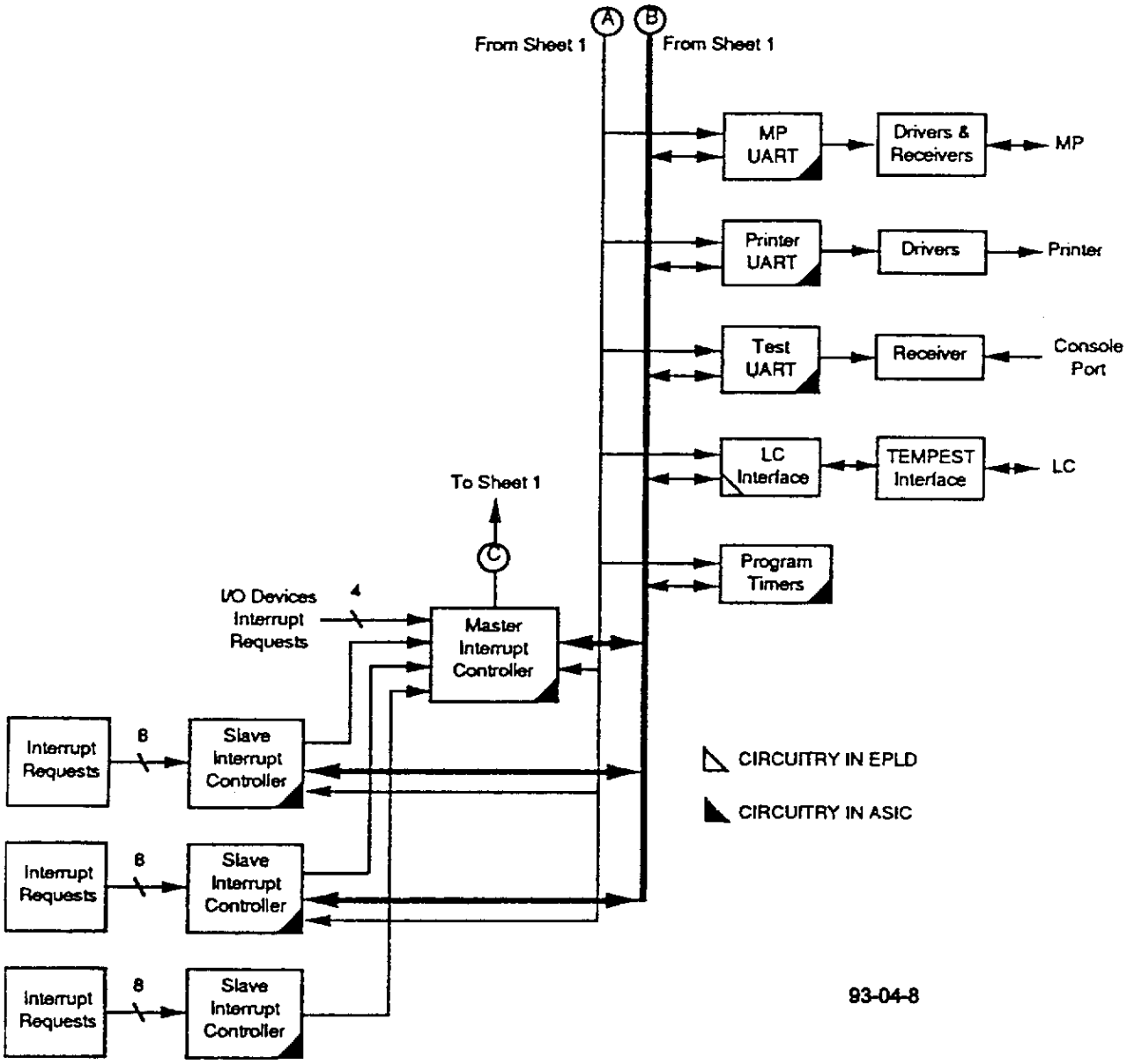


Figure 4-20. Communications Processor Function Block Diagram (Sheet 2 of 2)

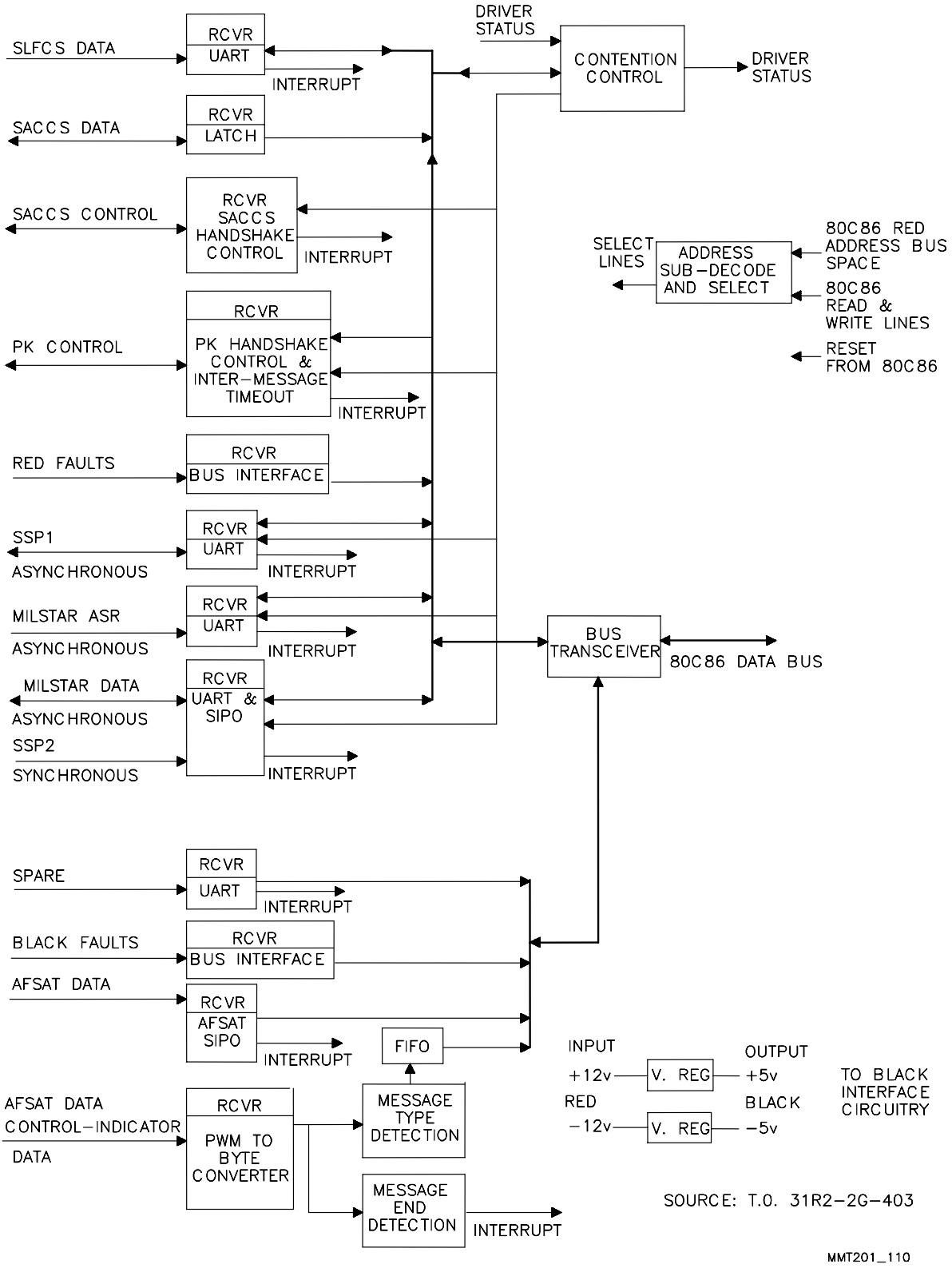


Figure 4-21. LVCON Circuit Card Assembly Function Block Diagram

the handshake signals required by the individual HA communication systems. These handshake signals are controlled by the contention control function provided on the CCA. Both drawers must be able to operate independently or together, but only one can transmit handshake signals while both are receiving message traffic. Contention control allows the CI and CIB to resolve which drawer is enabled. The output signals are controlled by enabling/disabling the output drivers. The red/black interface is on the CCA. Power for the black interface circuits (± 5 vdc) is generated from the red ± 12 vdc on the CCA. Black inputs are double buffered and the red/black interface for these inputs is within the receiver. Four spare signal ports, labeled either SPARE or SSP1 are included on the CCA.

4-4.11.4. Message Processor. The Message Processor (MP) performs the bulk off the primary RMP functions. The MP is ruggedized version of the Digital Equipment Corporation VAX computer housed in the RMP drawer. It is a two board system based on Digital's 32-bit rtVAX300 processor and Digital's VAXELN operating system. It contains 16 megabytes of RAM and input/output capability. The processor performs in excess of 3 Million Instructions Per Second (MIPS) and has 12 asynchronous, one Small Computer Serial Interface (SCSI), and 40 discrete channels. The MP is single module made up of two circuit boards. One is called the VAX board and the second is called the IOC board. An aluminum frame holds the VAX board and IOC board together. The frame makes the assembly rigid and provides mounting flanges to secure the MP into the RMP drawer. The functions that comprise the MP are shown on Figure 4-22.

4-4.11.4.1. Message Processor Functions. The MP hosts the Message Processor Computer Program and performs the bulk of the RMP functions. It controls the transmission of serial data to the weapons system processor and printer controller. MP functions include the following:

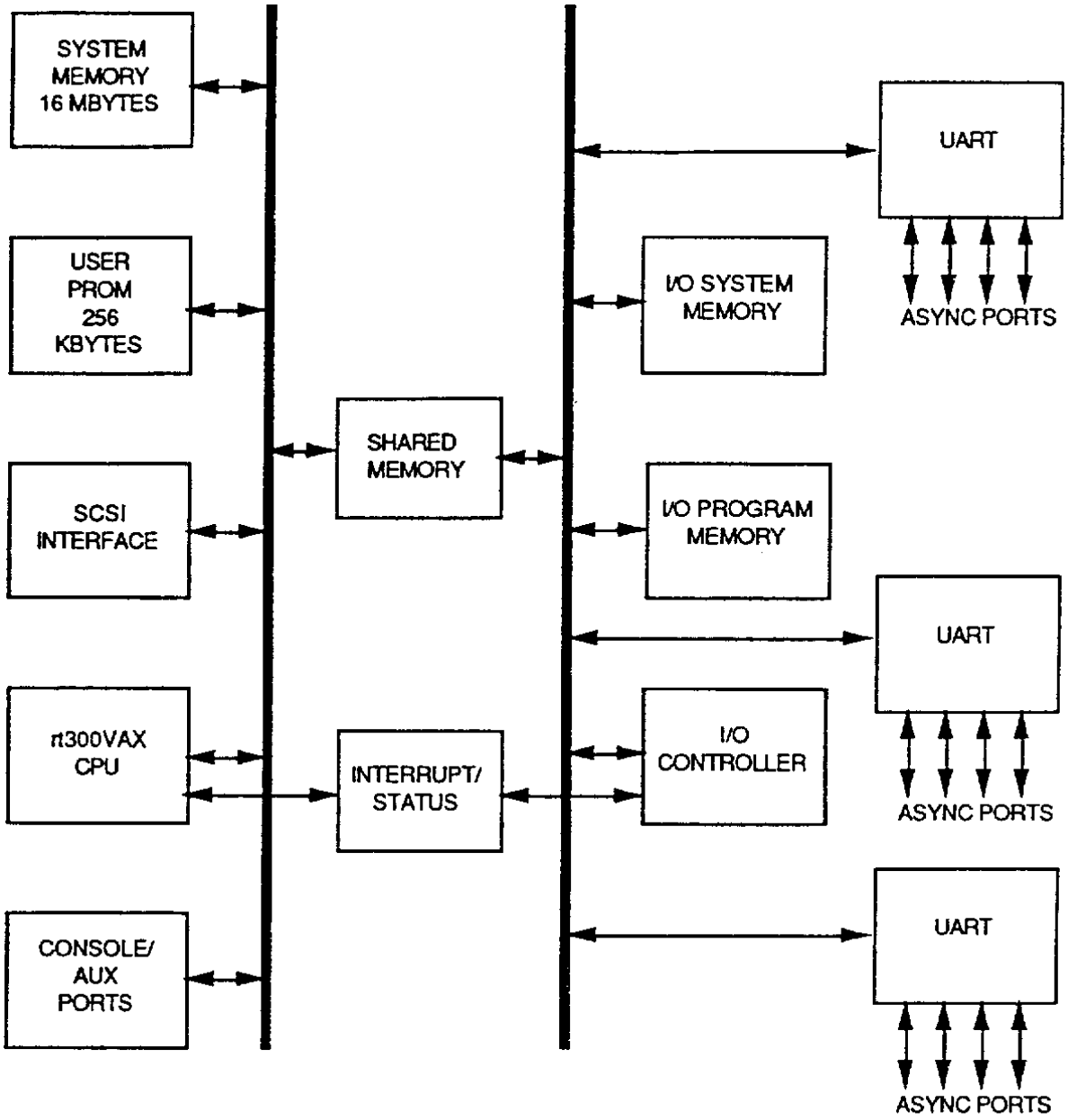
a. Emergency Action Message (EAM), Force Direction Message (FDM), Non Action Message (NAM) and all sortie free launch (AFLS) message processing.

b. Display of message processing results, manual input and editing of messages.

c. Transfer of derived message data and alarm signals to the weapons system console.

d. Centralized monitoring and control of communications terminals (except for control heads).

e. Control of processing, storage, retrieval, and display of messages, status and data, control of alarm setting and resetting message composition, performance and status monitoring, interpretation of MCCM interface device inputs, journaling of system data, and program and data base loading.



SOURCE: T.O. 31R2-2G-403

Figure 4-22. Message Processor

4-4.11.4.2. Message and Alarm Processing. The MP interfaces with the primary and backup CIs for the reception of message traffic and status alarms. Characters are stored according to the channel over which they were received. Message type is determined and the messages are processed according to type and priority rules. The MP determines if the message is an EAM, FDM or NAM. If the message is determined to be an EAM, it is processed and compared with other EAMs previously received over the same communication channel. the comparison is made using the raw message. A perfect match is required to declare it a duplicate. If the EAM is not a duplicate, the message is processed further. It is now compared to the last 100 EAMs received over any of the other communication channels. Again, a perfect match is required. If the EAM is determined to be a duplicate, alarms are suppressed, but EAM reception is logged. If the EAM is determined to be unique, then a visual EAM alarm is generated and a signal is sent to the Weapon System Processor (WSP). This tells the WSP to activate the audible alarm. If the MP determines that the message cannot be automatically corrected, it can be displayed on the HA VDU and the MCCM manually edits and corrects the message. Corrected unique EAMs are manually decoded. Valid, decoded EAMs are entered in to the WSP manually by the MCCM. Unique and uncorrectable EAMs are stored on the JML for potential recovery. The EAM audit table is stored in the MP. If the EAM was received from SACDIN, an acknowledgment is sent to the SACDIN terminal. Validated FDMs are automatically transferred to the WSP. If an FDM fails validation a visual non-EAM alarm is generated and sent to the weapon system processor to activate the audible alarm. The failed FDM is available for display. NAMs can be displayed on the HA VDU and edited by the MCCM. The entire message or a portion of the NAM can be selected and sent to the crew log. A one-way serial path (RS-423) is provided to the WSP to support transfer of FDM data and control messages. Discrete signals from the WSP are used to tell the MP that alarms have been reset by the MCCM. These signals are used by the MP to reset the visual alarms. The MP interfaces with the JML for receipt of program and data base load for the MP, and for inputting data to the JML and for message recovery. Other interfaces are to the VDU controller, WSP, and TI. The MP stores standard and preformatted messages, which can be recalled and tailored for message transmission. The composed message is transferred to the TI for transmission when complete and correct.

4-4.11.4.3. Journal Memory Loader (JML). The JML (Figure 4-23) is a dual disk drive that is used to load the MP computer program and for message storage. It consists of an SCSI interface, a controller, and two disk drives. The two disk drives are controlled by firmware in the JML and code in the MP computer program. A single controller in the JML communicates with the MP over one communication channel. The MP computer program is stored on two diskettes and are loaded by the JML during Initial Program Load (IPL).

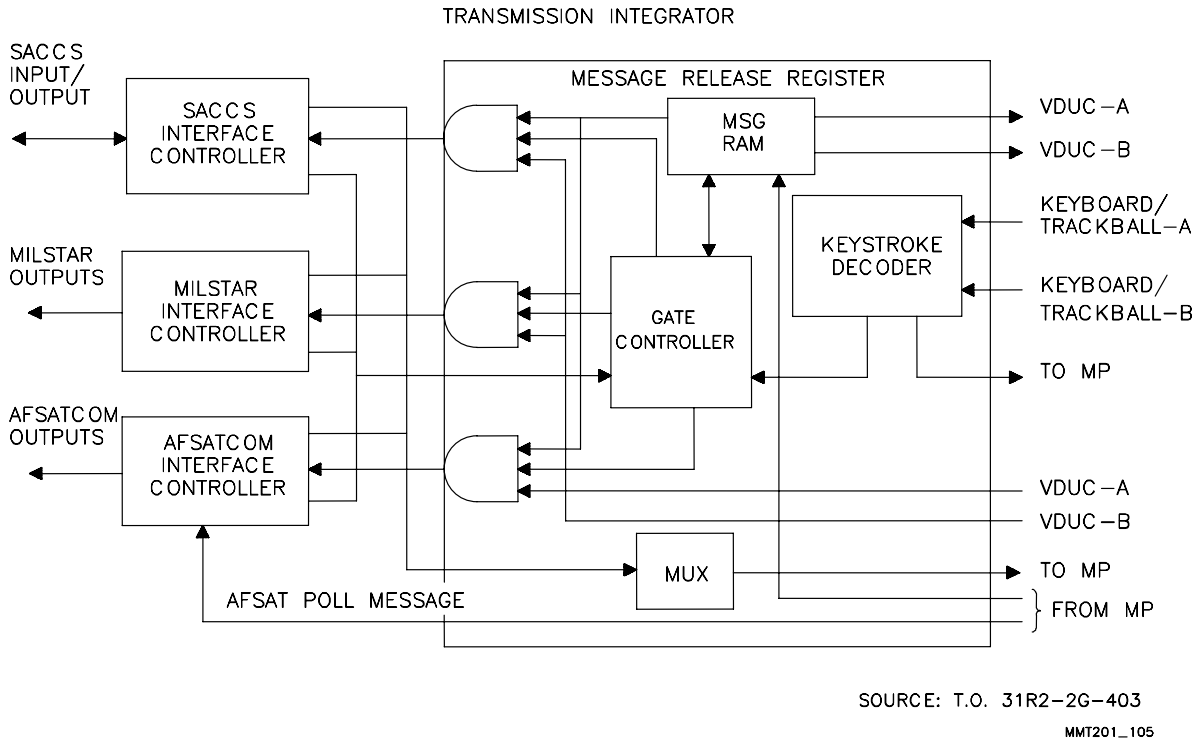
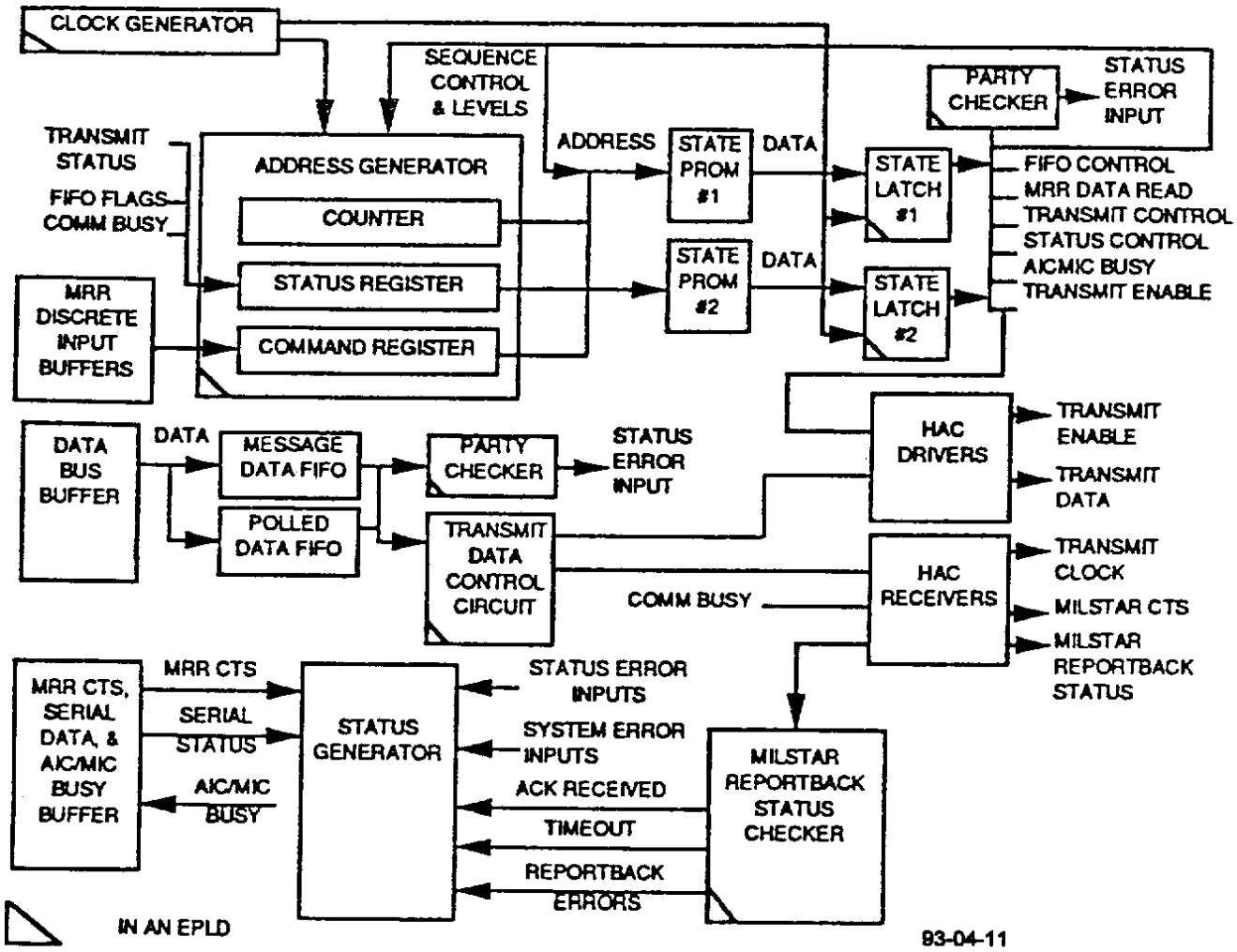


Figure 4-24. Transmission Integrator Functional Block Diagram

composed message for transmission from the MP, but is prevented from transmitting it until it is first displayed on the HA VDU and verified by the MCCM. Upon determining that the message is correct, the crew member will enable the transmission from the keyboard. The detection of this key by the keystroke decoder is a necessary condition for message release. The crew members establish the classification of the message, ensure that it is properly classified and that the message is correct. They also ensure that the selected transmission system and destination are authorized for the message classification level. The interface controllers within the TI make all format and protocol conversions for the selected transmission system.

4-4.11.4.4.2. AFSATCOM Interface Controller/MILSTAR Interface Controller. The AFSATCOM and MILSTAR interface controllers perform the handshaking, buffering, and level conversion necessary for interfacing MRR outputs to the applicable transmission terminal (AFSATCOM or MILSTAR). The AIC/MIC card in location A40 is the AIC (AFSATCOM Interface Controller) and the MIC (MILSTAR Interface Controller) in location A39. All programmable parts (EPLDs and state PROMs) are the same for the AIC and MIC. The clock generator (Figure 4-25) is a 2.4567 MHz oscillator that is divided on the card to provide the various clocks needed to operate the circuits on the CCA.

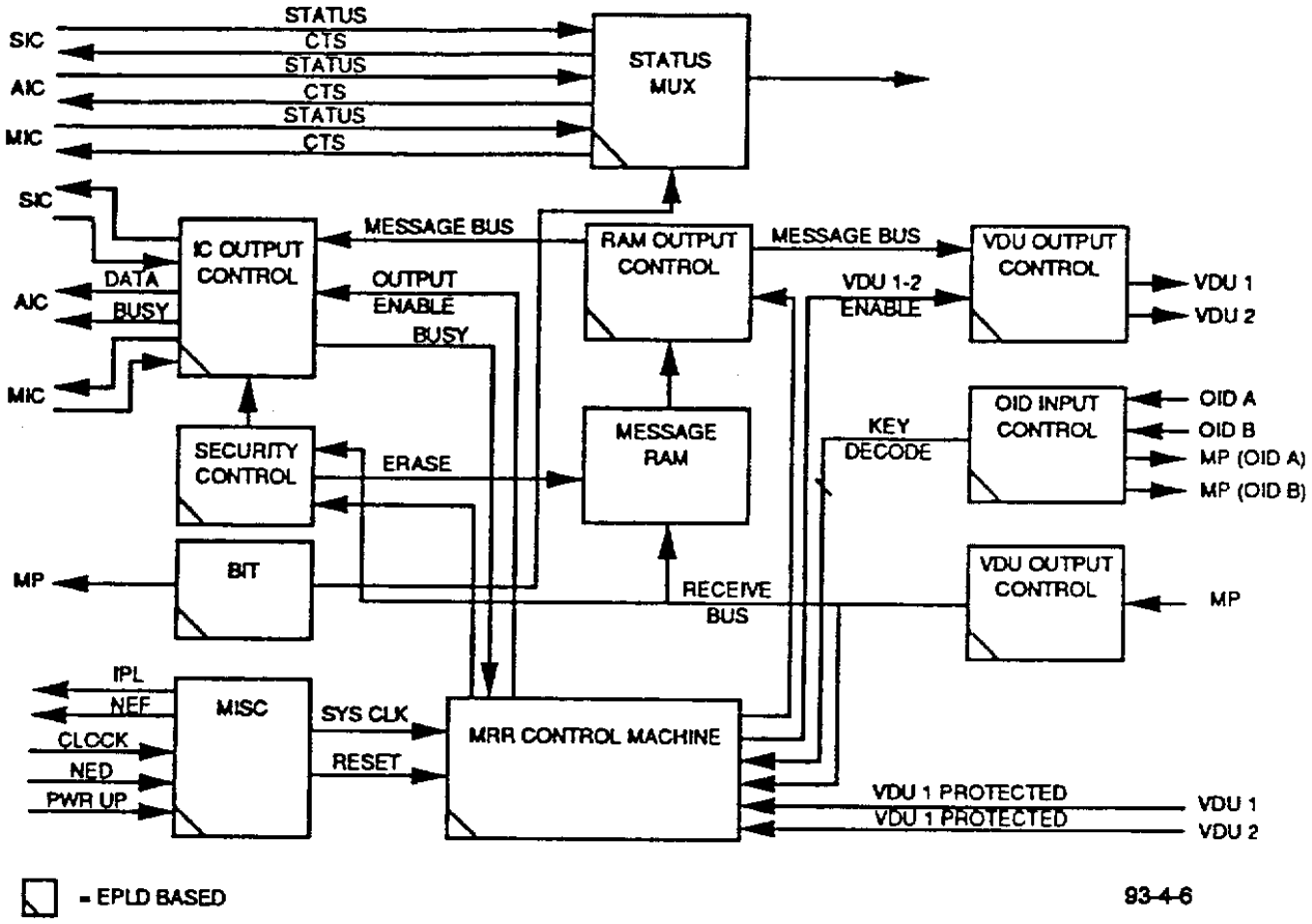


SOURCE: T.O. 31R2-2G-403

Figure 4-25. AIC/MIC Function Block Diagram

AIC/MIC contains a simple state machine that has three basic parts; address generator; two state PROMS; and two state latches. The address generator moves the state machine from state to state by changing the address inputs to the state PROMS. The two state PROMS enable the control lines to be output for each state. The state latch holds the data from the state PROMS for one cycle of the state machine clock. Unused locations in the state PROMS are programmed with illegal parity to cause an error if the state machine enters an illegal state. The AIC/MIC CCA includes buffers to send and receive data between the MRR and the AIC/MIC. Message and polled data FIFO registers are used to temporarily store message and other data from the MRR. The transmit control circuit contains a parallel-to-serial shift register used to format message data. The status generator is used to send status messages to the MP. HAC receivers and drivers are used to input and output signals to the AFSATCOM and MILSTAR communication terminals. The MILSTAR report-back status checker looks for a signal received from MILSTAR every 3 seconds. A timeout occurs if the signal is not received. The MRR CTS buffer assigns a multiplexed time slot for the status report to the MP. See Figure 4-25 for the block diagram.

4-4.11.4.4.3. Message Release Register (MRR). The MRR (A41) is used to enforce access control of the MP to the transmission portions of the subsystem. (See Figure 4-26 for block diagram.) The MRR accepts MCCM inputs from the two MCCM keyboard and trackball input devices. The keyboard outputs are first passed through a keystroke decoder that detects control inputs for the TI. All other entries are forwarded to the MP which interprets the function keys, standard keys, and trackball movements to provide the response. These include the MP input control, RAM control, VDU output control, MCCM input device input control, IC output control, security control, built in test, and status time division multiplexer. The MRR consists of message RAM for storing a message prior to transmission, gate control logic to ensure transmission to the designated HA communication system at the designated classification level, data lines from the MP and to the VDU controller, and control lines from the keystroke decoder and VDU controller. The control line from the VDU controllers signal that a portion of the screen has been protected from writing by the MP, and the MRR may now display its contents for MCCM review prior to transmission. Message release is a necessary condition for message transmission. The gate control logic establishes the connection for transferring a message to an interface controller for transfer to the HA communication system for transmission. The logic requires an input from the keystroke decoder, plus the classification of the message must be acceptable for the communication system. If any input is invalid, the MRR is cleared. Refresh will also cause erasure of the contents of the MRR. The transmission data flow and sequence is as follows: A composed message is sent from the MP to the MRR. The MRR disables the MP input controller after receipt of the message data. It then checks the classification versus the chosen HA terminal. The MRR then notifies the VDU controller that the MRR will control all information in the work area of the HA VDU. The message is transferred to the HA VDU for the MCCM to verify the message integrity. When the input controller is enabled, the keystroke decoder logic scans the



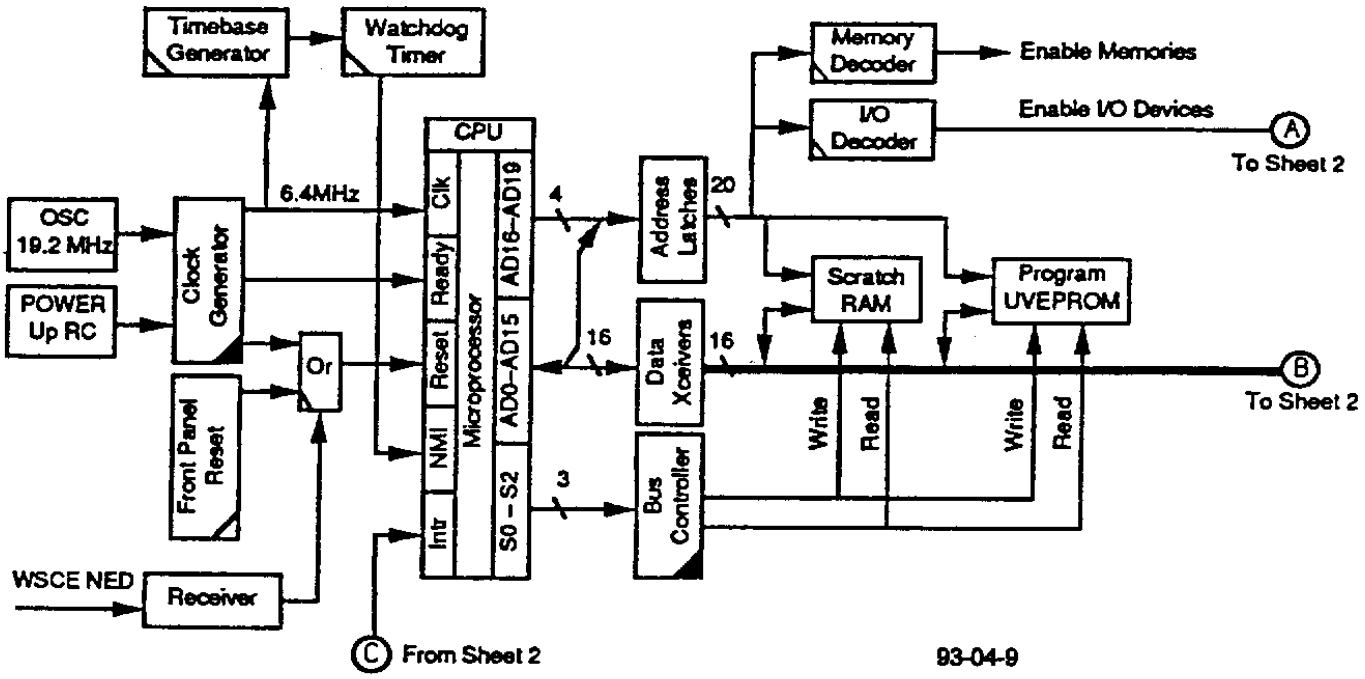
SOURCE: T.O. 31R2-2G- 403

Figure 4-26. MRR Functional Block Diagram

selected MCCM interface device for the function keys. If a transmit key is sensed, the appropriate HA terminal is allowed access to the RAM. Once the input controller has received the last message byte, the output controller is disabled and the security control overwrites the entire RAM. The MRR then sends status to the message processor.

4-4.11.4.4.4. SACDIN Interface Controller. The SACDIN interface controller (CP/SIC A37) is implemented in firmware executed on a 80C86 processor. (Refer to Figure 4-27 for block diagram.) The SACDIN interface controller provides a two-way interface with the control electronics drawer (CED) VDU/keyboard port to accept data and commands meant for the SACDIN VDU, and to provide the SACDIN expected responses and keyboard entries necessary for SACDIN operation. The SIC transfers messages for transmission over SACDIN, commands for SACDIN, and acknowledgments of received EAMs and received status data from SACDIN. Message transfer to SACDIN starts when the SACDIN interface controller receives a properly labeled and addressed message from the MRR. Upon receipt, the current SACDIN session with the SACDIN interface controller is cleared, and a new session established at the security level of the received message. The SACDIN interface controller commands the security level of the SACDIN session and processes the SACDIN response to verify SACDIN compliance. The session remains in effect during the time it takes to transfer the message from the MRR to SACDIN (on the order of milliseconds). The SACDIN interface controller performs any conversions necessary to transform the message from subsystem to SACDIN format. The SACDIN interface controller sends the equivalent of the SACDIN transmit key to initiate SACDIN transmission of the message, and receives the SACDIN response which may indicate successful transmission, or unsuccessful transmission accompanied by an explanation of the error. The SACDIN interface controller clears the session security level after successful message transmission. An error condition results in clearing the SACDIN interface controller of the current message, and transferring the error notification to the MP to alert the MCCM to correct and re-transmit the message. Status and other display data may be sent by SACDIN to the SACDIN interface controller during the interactive message transmission session. If the status if of a higher classification level than the current session, then the status is held by SACDIN until the session is over.

4-4.11.5. Visual Display Unit Controller (VDUC). Two independent VDU controllers (VDUC, A44 and A45) are located in the RMP. One controls the HA VDU in the console left bank and the second controls the HA VDU in the console right bank. The VDUC is contained on a single CCA. It transforms received ASCII display data into video Red-Green-Blue (RGB) bit streams that drive the associated HA VDU (Figure 4-28). The VDUC contains the display memory that refreshes the display. The individual MCCMs operating their keyboard/trackball assemblies may call up separate detailed displays. One may compose a message while the other is reviewing a message for transmission. However, the work area is reserved for the message being reviewed for transmission and is not available to the other MCCM. The transmission process is initiated when the MCCM is satisfied with the message as composed and initiates the transmission function.



SOURCE: T.O. 31R2-2G-403

CIRCUITRY IN EPLD

CIRCUITRY IN ASIC

Figure 4-27. SACDIN Interface Controller Functional Block Diagram (Sheet 1 of 2)

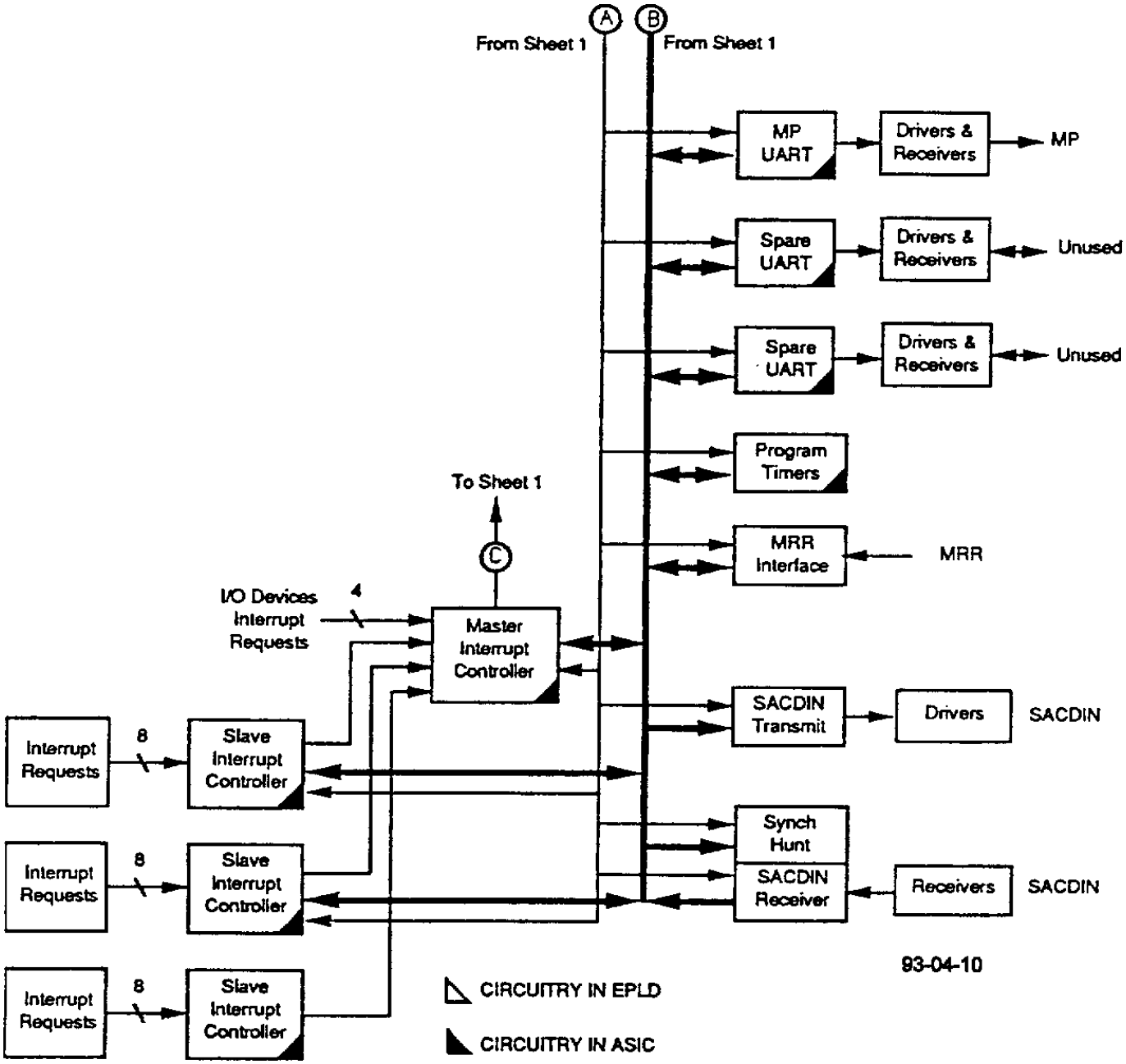


Figure 4-27. SACDIN Interface Controller Functional Block Diagram (Sheet 2 of 2)

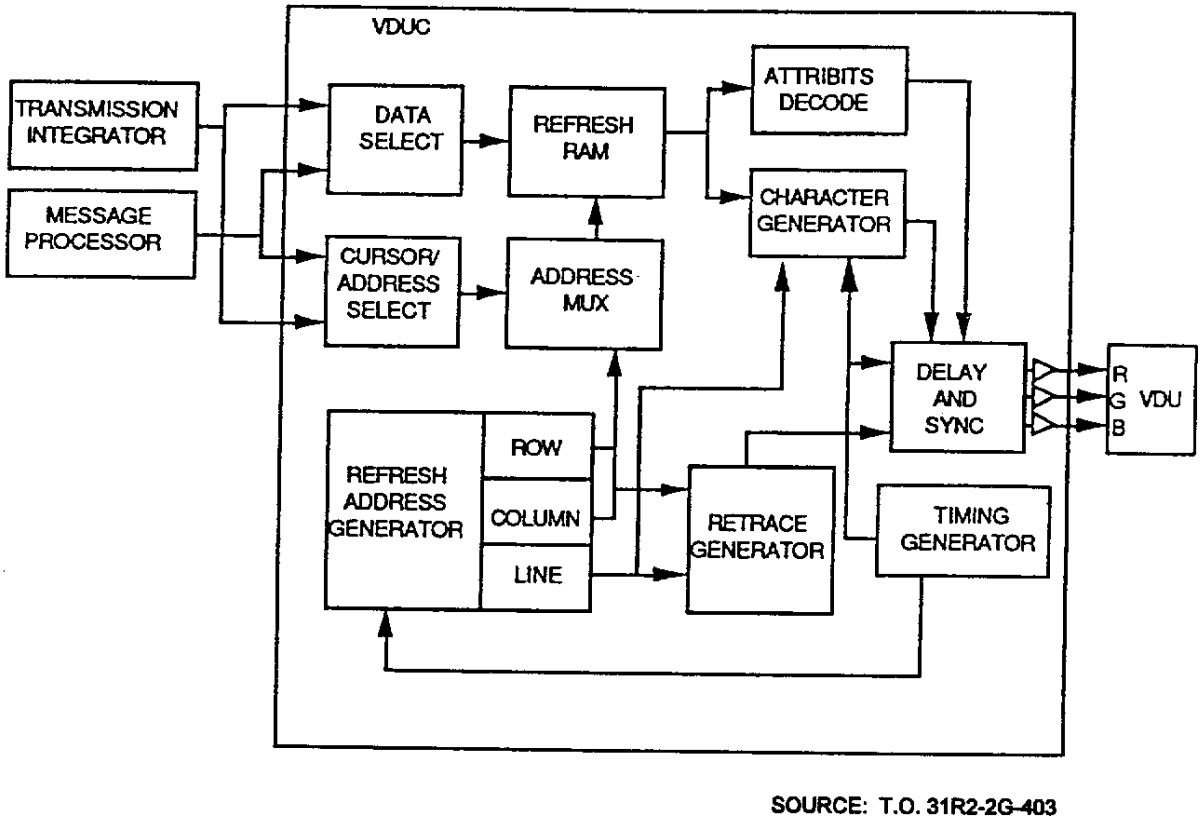


Figure 4-28. Visual Display Unit Controller Functional Block Diagram

Transmission is initiated when the INITIATE function key on the keyboard is pressed and the MRR PAGE function key is then pressed. A portion of the display memory is cleared and dedicated to the message for transmission. The MP is denied access to this portion of memory during message review and transmission. However, the MP may still display information on other areas of the screen. Also, the MP cannot change the contents of the MRR at this time. The TI is notified by a discrete signal from the VDUC that memory is protected and it is ready to receive the message for display. Control lines between VDUC that memory is protected and it is ready to receive the message for display. Control lines between VDUCs lock out the other controller to prevent it from attempting to enter the message release mode. Thus both MCCMs may compose a message simultaneously, but only one may transmit at a time. After the MCCM verifies that the displayed message is correct, the MCCM presses the TRANSMIT function key from the authorized keyboard. In addition to transferring the message to the selected communication system, the TI indicates to the VDUC that it may release the protected memory. The MP is also notified that the memory is released. The other MCCM is now free to transmit a message. A copy of the message text that was transmitted can be saved in the MP for transmission on another communication system without having to be composed again.

4-4.11.6. DC Power Supplies. Both drawers contain power supply modules that provide the dc power required by the electronic circuits within the drawer. Both power supplies are designed as plug in assemblies that mate directly with connectors mounted in the backplane.

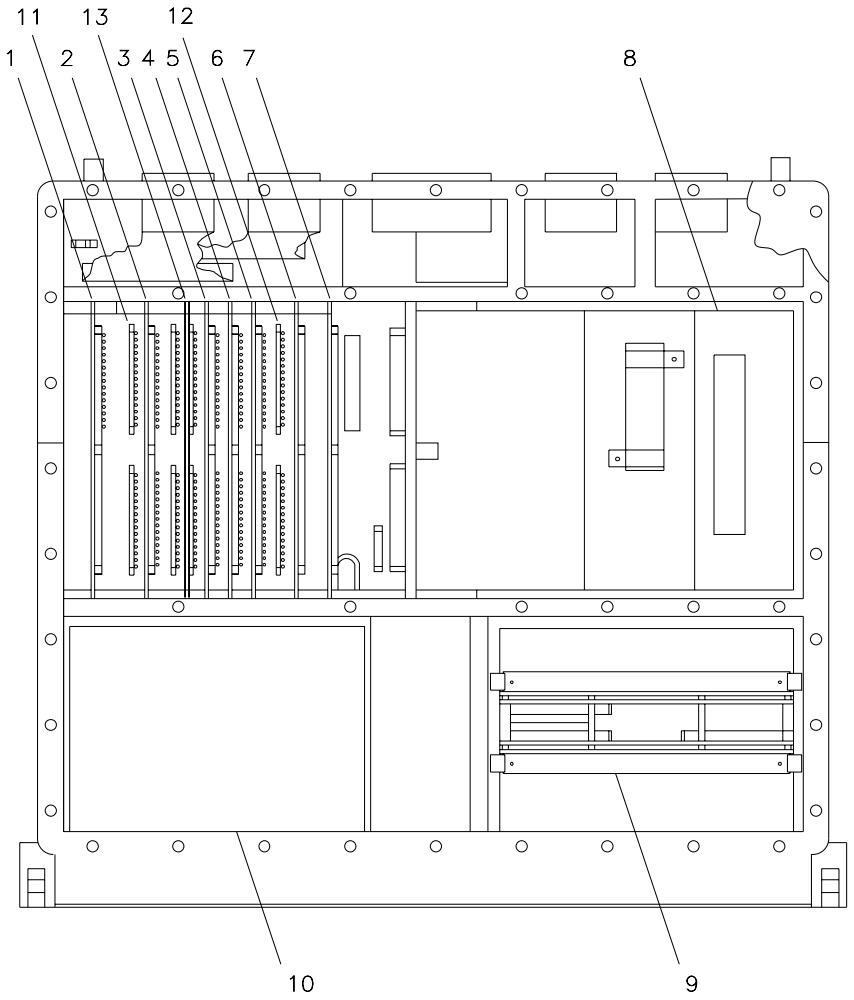
4-4.11.6.1. RMP Drawer DC Power Supply. The dc power supply (PS1) is located in the RMP drawer (See Figure 4-29) and plugs into power supply distribution CCA (A48). It supplies +5 vdc, -5 vdc, -5.2 vdc, +12 vdc and -12 vdc to its loads. The power supply provides dc power to the MP, the RMP nest, the JML, and front panel components. The MP plugs into the MP motherboard (A48). The RMP nest is a wire wrap nest with built in bus bars to distribute the DC power throughout the nest. The MP nest and most of the RMP nest are designated TEMPEST red. One portion of the LVCON (A35) CCA is designated black. All inputs are shielded from the rest of the signals in the nest. The ± 5 vdc required to drive the black circuitry is generated on the CCA from the ± 12 vdc supplied to the CCA from the power supply.

4-4.11.6.2. RMPB/Drawer DC Power Supply Error! Bookmark not defined.**.** The dc power supply (PS2) in the RMPB drawer supplies +5 vdc, -5 vdc, +12 vdc and -12 vdc to loads within the drawer. The power supply provides dc power to the CP/SIC (A5) CCA, the LVCON (A7) CCA and front panel components. The nest is a wire strap nest with built in bus bars to distribute the dc power. As with the RMP drawer, the nest is designated TEMPEST red. One portion of the LVCON (A35) CCA is designated black. All inputs are to this portion of the CCA are shielded from the rest of the signals in the nest. The +5 vdc required to drive the black circuitry is generated on the LVCON CCA from the +12 and -12 vdc supplied to the CCA from the power supply.

4-4.11.7. Interface Definition. See Figure 4-30, RMP and RMPB to WSP Functional Interface Diagram.

4-4.11.8. WSP DATA Transfer Protocol. WSP DATA is used to transfer message and crew log data from RMP on a one-way serial RS-422 type data link operating at 9600 bps as follows:

a. The data is transferred within frames, which contain bytes as shown in Figure 4-31. The data bytes are transmitted Least Significant Bit (LSB) first and Most Significant Bit (MSB) last. Each byte represents a character that consists of one start bit, eight data bits, an even parity bit, and a stop bit.

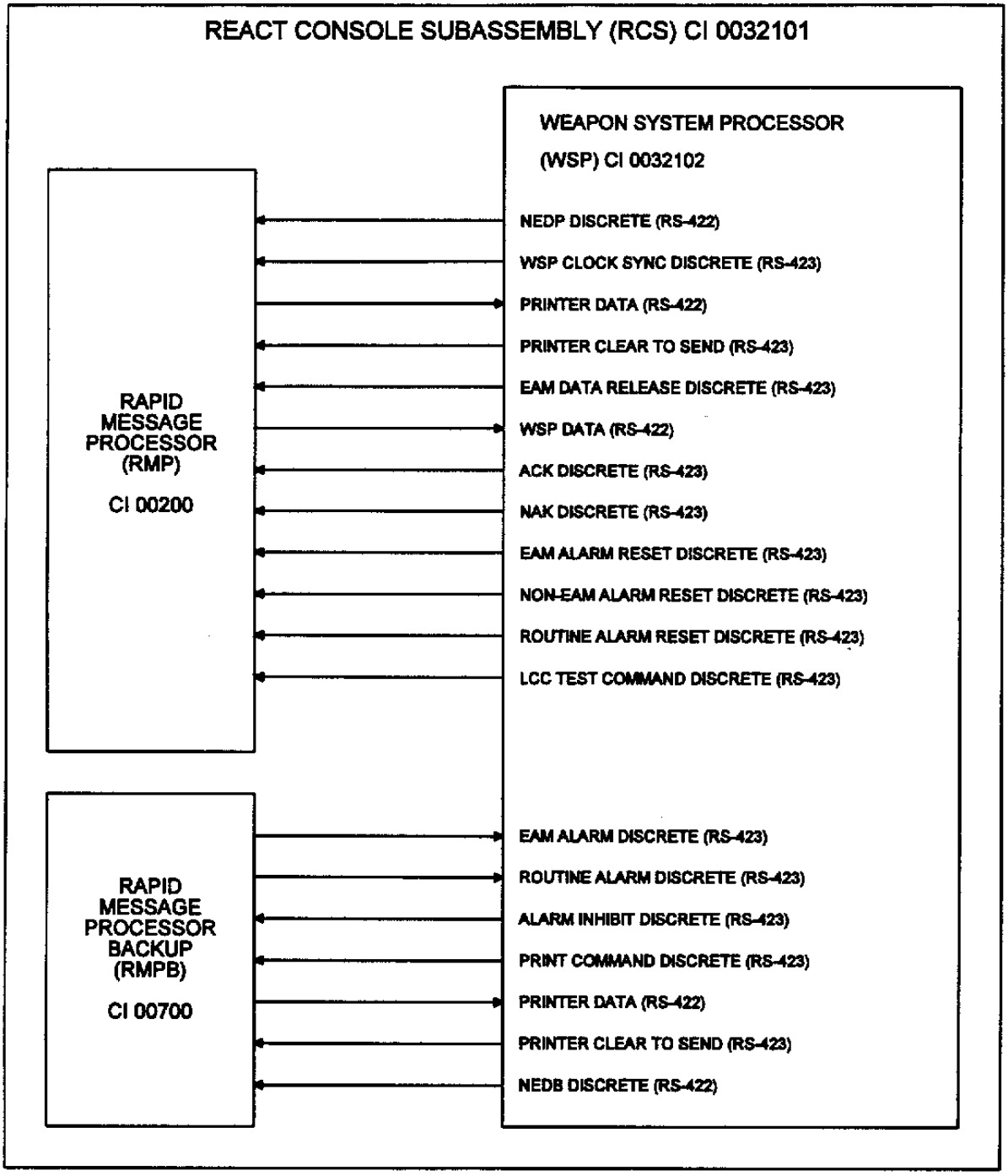


SOURCE: T.O. 31R2-2G-403

MMT201_106

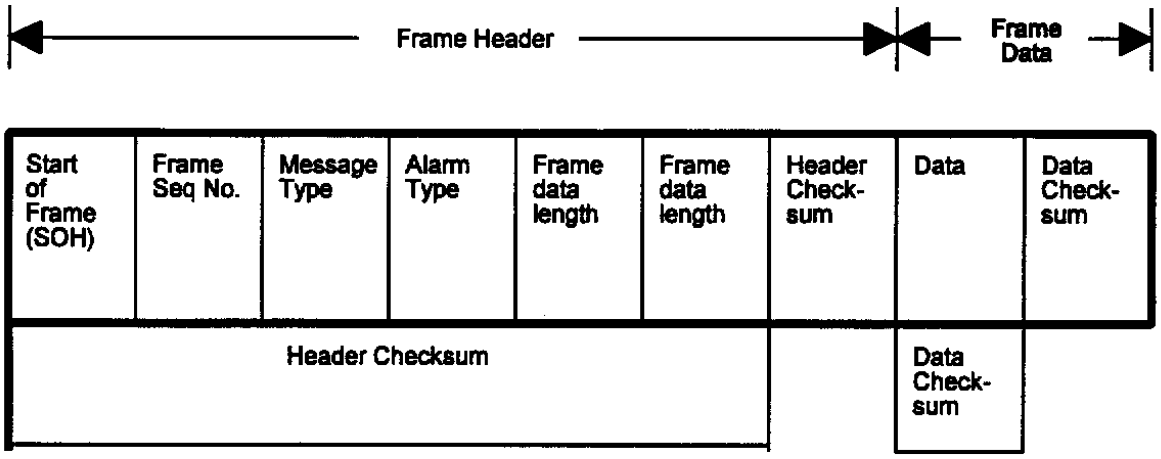
1. LVCON (A35, Level Converter)
2. CP/SIC (A37, SACDIN InterfaceController)
3. AIC/MIC (A40, AFSATCOM Interface Controller)
4. MRR (A41, Memory ReleaseRegister)
5. CP/SIC (A42, Communication Processor)
6. VDCU (A44, Left VDU Controller)
7. VDUC (A45, Right VDU Controller)
8. Power Supply (PS1)
9. Message Processor (A49)
10. Journal Memory Loader (A30)
11. Backplane Support Plate, RMP (A36)
12. Backplane Support Plate, RMP (A43)
13. AIC/MIC (A39, MILSTAR Interface Controller)

Figure 4-29. Rapid Message Processor Drawer - Top View



Source: ICD 25-R030

Figure 4-30. RMP and RMPB to WSP Functional Interface Diagram



Source: ICD 25-R030

Figure 4-31. WSP DATA Transfer Frame Format

b. Error detection is provided by both the parity bit on each character and two checksums on the frame. RMP sums the binary value of each byte mod 256 and sets the checksum byte to the two's complement of this sum. The Header Checksum is over the SOH (byte 1) to frame data length (byte 6) bytes inclusive. The data checksum is over the data bytes that follow the Frame Header. If a parity or any checksum error is detected by the WSP, the NAK discrete from the WSP to the RMP is set to a logic one. If a data error is not detected, the WSP sets the ACK discrete to a logic one.

c. The RMP waits for either an ACK or NAK response from the WSP after the transmission of a frame. If an ACK is received, the next frame (if any) is transmitted. If a NAK is received, or if no response is received within four seconds, RMP will retransmit the entire frame for up to two additional times. After that, RMP sets an error condition and transmits test frames every four seconds until an ACK is received. Following an ACK, RMP sends a reset type frame, then any data frames being held.

d. Data exceeding 480 characters are transferred in multiple frames. The first frame contains a frame sequence number with a value of the number of frames to be transferred. Each succeeding frame has a value one less than the preceding one. The last data frame of a multiple-segment transfer contains the value one.

e. If a multiple-segment message has more than four frames still to be transferred, RMP will terminate the transmission if a higher priority message is ready to be transferred. A Reset frame is transmitted to preempt the transfer. Upon ACK from the WSP, the higher priority data are transferred. Upon successful transfer, the preempted message is restarted at the first frame.

4-4.11.9. WSP DATA Exception Protocol.

a. When the WSP returns to operational status from being down or off line, it sets the NAK discrete to logic one. RMP responds with a test message. If WSP responds with an ACK, RMP resumes transmission. If a multiple-segment message was previously in process, it is retransmitted from the beginning.

b. When no data is transferred within a 4-second period, RMP monitors the status of the interface by transmitting a test frame. The WSP is expected to ACK it. If a NAK or no response is received from the WSP, RMP tries the test message twice more. If still no ACK is received, RMP sets an error condition and continues transmitting test frames. If the WSP fails to receive frames from the RMP within a 10-second period, the WSP sets an error condition.

4-4.11.10. PRINTER DATA Protocol.

a. Printer data may be transferred from RMP or RMPB so long as the PRINTER CLEAR TO SEND discrete is set to TRUE (logic 1) by the WSP. In the case of the RMPB, the PRINT COMMAND DISCRETE must also be FALSE. Printer data is buffered on disk and spooled to the printer as rapidly as system priorities permit. When a buffer is full, the WSP drops the corresponding PRINTER CLEAR TO SEND line until space is available.

b. PRINTER DATA are transferred in the form of a print block containing a maximum of 66 lines of up to 80-characters per line. The block begins with an STX character (see Table 4-27 for the ASCII characters referenced here), followed by ASCII text, and ending with an ETX. The STX and ETX each have their MSB set to 1.

4-4.11.11. Other Discrete Lines.

a. NEDP and NEDB - The WSP provides a signal to each of the RMP and the RMPB indicating the possibility of upset, due to a nuclear environment. The RMP and RMPB set themselves to a known state.

b. WSP CLOCK SYNC - This discrete acts as a "clock set" command from the WSP to the RMP. It is held TRUE for at least 30 milliseconds to transfer the Clock Set command.

c. EAM DATA RELEASE - The RMP will not transfer EAM data unless this discrete (normally held FALSE) is set to TRUE by the WSP for at least 30 milliseconds.

d. Various ALARM RESETs - The WSP will set these discretes to TRUE for at least 30 milliseconds to transfer alarm reset commands.

e. LCC TEST COMMAND - The WSP sets this discrete to TRUE for at least 30 milliseconds to transfer the self-test command to the RMP. The WSP normally holds the discrete TRUE, and interprets all transfers as test results, until the RMP has completed its portion of the LCC Test. However, should the WSP detect an error or an unexpected response, it will drop the line (to FALSE), and recognize future transfers as operational message traffic.

f. EAM ALARM - This discrete is set TRUE by RMPB to indicate the existence of an EAM in the printer data being transferred to the WSP. The discrete cannot be set if the ALARM INHIBIT discrete (set by the WSP) is TRUE.

g. ROUTINE ALARM - This discrete is set TRUE by RMPB to indicate the existence of printer data (other than EAM data) being transferred to the WSP. The discrete cannot be set if the ALARM INHIBIT discrete is set.

h. ALARM INHIBIT - This discrete is set TRUE by the WSP to inhibit the alarm discretes from the RMPB.

4-4.12. Secure Data Unit (SDU).

4-4.12.1. Functions. The SDU, a part of the Coder-Decoder Assembly (CDA) (reference Figure 5-13), is located in the Weapon System Control Console (Reference Figure 5-1, item 35). The SDU provides for encryption and decryption of cable messages. One SDU operates at each LCF and LF. Two modes, Crypto 1 and Crypto 2, provide the message encrypt/decrypt capability. In Crypto 1 a message which has been loaded into the SDU is encrypted for transmission; in Crypto 2 a received encrypted message is decrypted.

4-4.12.2. Interface Definition. The COP and WSP interface to the SDU consists of three discrete outputs, two discrete inputs, one serial input channel, one serial output channel, and one clock control line, as described below and as shown in Figure 4-32:

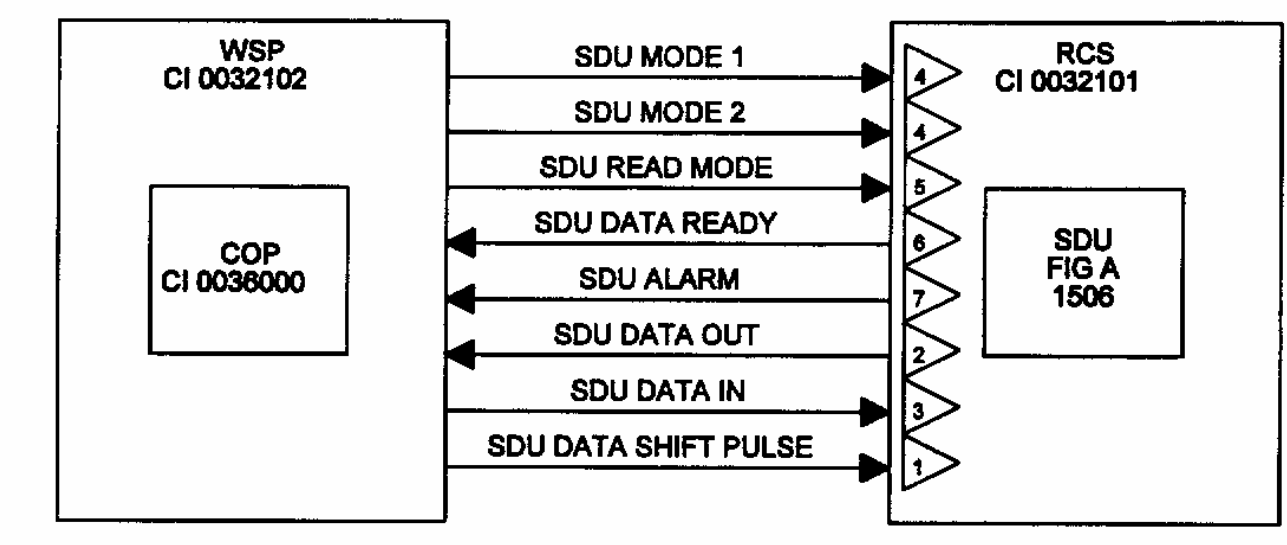
a. SDU Mode 1 is a discrete output to the SDU. In conjunction with the SDU Mode 2 and the SDU Read Mode discrete outputs to the SDU, the SDU Mode 1 discrete output controls the SDU operations. The active value of SDU Mode 1 (high) must be established by the WSP at least 2 microseconds before the pulsing of the SDU Read Mode discrete output to the SDU.

b. SDU Mode 2 is a discrete output to the SDU. In conjunction with the SDU Mode 1 and the SDU Read Mode discrete outputs to the SDU, the SDU Mode 2 discrete output controls the SDU operations. The active value of SDU Mode 2 (high) must be established by the WSP at least 2 microseconds before the pulsing of the SDU Read Mode discrete output to the SDU.

c. The SDU Read Mode discrete output to the SDU is used in conjunction with the SDU Mode 1 and 2 discrete outputs to the SDU, and the SDU Data In signal interface to the SDU. The SDU Read Mode discrete is set by the WSP to 0 (low) for 1.7 - 20 μsec, at least 2 μsec following the setting of the SDU Mode 1 and 2 discrete outputs, and the SDU Data In signal, and then returned to 1 (high). This transition is referred to as pulsing.

d. The SDU Data Ready discrete input from the SDU is 1 (high) to indicate to the WSP that the SDU can accept or transfer data out over the serial data channels.

e. The SDU Alarm discrete input from the SDU is 0 (low) to indicate to the WSP that the SDU has not failed. Under a test mode operation, or as a result of an SDU malfunction, the SDU Alarm discrete will become high and remain high until the SDU performs a crypto operation successfully.



[1> SDU Data Shift Pulses - The 100 kHz clock pulses from the WSP which control the shifting of input or output data to or from the SDU control registers.
[2> SDU Data Out - The serial data line which carries data from the SDU to the WSP.
[3> SDU Data In - The serial data line which carries data from the WSP to the SDU.
[4> SDU Modes 1 and 2 - Tell the SDU the mode of operation to be performed as follows:

MODE 1	2	Operational Mode
L	L	Not Used
L	H	Crypto I Process
H	L	Crypto II Process
H	H	Alarm

[5> SDU Read Mode - Tells the SDU to interpret the Mode 1 and Mode 2 lines.
[6> SDU Data Ready - Indicates to the WSP that the SDU is ready to receive or transmit data.
[7> SDU Alarm - Indicates to the WSP a fault in the SDU operation.

Source: ICD 25-R059, Vol. II

Figure 4-32. COP and WSP to SDU Functional Interface Block Diagram

f. The SDU Data Out signal interface is the serial data output of the SDU that transfers data to the CDA/IPD Interface at a rate of 100 Kilobits per second.

g. The SDU Data In signal interface is the serial data input to the SDU that transfers data from the CDA/IPD Interface at a rate of 100 Kilobits per second. At the completion of SDU data input transfer, the CDA/IPD sets SDU Data In to the interface level directed by the COP for keying variable selection.

h. The SDU Data Shift Pulse clock provides a 100 KHz timing output to the SDU from the WSP. This clock is used to synchronize the shifting of serial data into and out of the SDU. Serial data word length is 48 bits.

4-4.12.3. Operation of SDU Sequences. The SDU has four sequences of operation as described is Figures 4-33 through 4-36. The SDU Data Input Transfer and SDU Data Output Transfer timing to support these sequences is described in Figures 7-10 and 7-11.

a. SDU Crypto 1 Sequence. The Crypto 1 Sequence provides encryption of 48 bits. The Crypto 1 Sequence is accomplished by the serial input transfer of data to the SDU (SDU Data Input), followed by the change mode of SDU Mode 2 to the active state (high) in conjunction with SDU Mode 1 to the inactive state (low). The encrypted bits are extracted from the SDU by the serial output transfer of data from the SDU (SDU Data Output). See Figure 4-33.

b. SDU Crypto 2 Sequence. A Crypto 2 Sequence provides decryption of 48 bits. The Crypto 2 Sequence is accomplished by the serial input transfer of data to the SDU (SDU Data Input), followed by the change mode of SDU Mode 1 to the active state (high) in conjunction with SDU Mode 2 to the inactive state (low). The decrypted bits are extracted from the SDU by the serial output transfer of data from the SDU (SDU Data Output). See Figure 4-33.

c. SDU Half-Add and Encrypt Sequence. The Half-Add and Encrypt Sequence provides for the serial half-adding of 48 bits stored in the SDU to 48 bits provided to the SDU, and the encryption of the resultant 48 bits. The sequence is accomplished by the change mode of SDU Mode 2 to the active state (high) in conjunction with SDU Mode 1 to the inactive state (low), followed by the serial input transfer of data to the SDU (SDU Data Input). The sequence is completed with the serial output transfer of data from the SDU (SDU Data Outputs). See Figure 4-35.

d. SDU Alarm Test Sequence. The SDU Alarm Test sequence tests the SDU circuitry which is not checked by the automatic self test. The SDU Alarm signal will return to the inactive state upon successful completion of the next SDU Crypto 1 or CRYPTO 2 sequence. See Figures 4-36 and 4-34.

e. SDU Failure During Crypto 1 or Crypto 2 Sequence. Should the SDU determine internal failure during Crypto 1 or Crypto 2 sequences, it will provide an active SDU Alarm signal (high) and maintain the SDU Data Out signal in the inactive state (high). See Figure 4-34.

4-4.12.4. Crypto Variable Selection. There are two crypto variables contained in the KI-22. One is used for encryption/decryption of communications, the other for encryption/decryption of CMSC from the BS/L. The state of the Data In line when Read Mode is asserted determines which variable will be used in the subsequent crypto operation. The Data In line set to High selects the HICS Keying variable, and the Data In line set to Low selects the secondary Keying variable.

4-4.13. Site Address Plug (SAP).

4-4.13.1. Functions. The site address plug provides to COP an 8-bit site address that is used during initialization as part of the validation of the COP load process. The site address must match the one stored on the BS/L for the load to continue.

4-4.13.2. Site Address Format. The 8-bit site address is provided as eight discrete inputs to the WSP. They function as discrete open or closed switches, with closed equating to a binary value of 1. Three bits define the binary value for the LCC Number, two bits for the Squadron Identifier, and three bits for the Wing Identifier. When stored as a byte in memory, the order of the identifiers is Wing/Squadron/LCC. Each binary value, when converted to decimal, must be increased by 1 to obtain the standard Wing, Squadron, and LCC numbers.

4-4.14. Time of Day Clock (TODC).

4-4.14.1. Functions. The COP and WSP interface to the time of day clock to provide updates to the time of day display. The initial setting of the clock is commanded by the operator, using the SET CLOCK option of the LCC CTRL menu (reference Figure 1-20, Main Menu Hierarchy), and the CLOCK SYNCH key on the OID (reference Figure 5-3). An initial time is loaded into a WSP buffer, and when the CLOCK SYNCH key is depressed, the WSCE VDU clock is updated, the RMP is notified by a discrete to set its clock to the time in the RMP buffer, and the time in the WSP buffer is sent to the TODC.

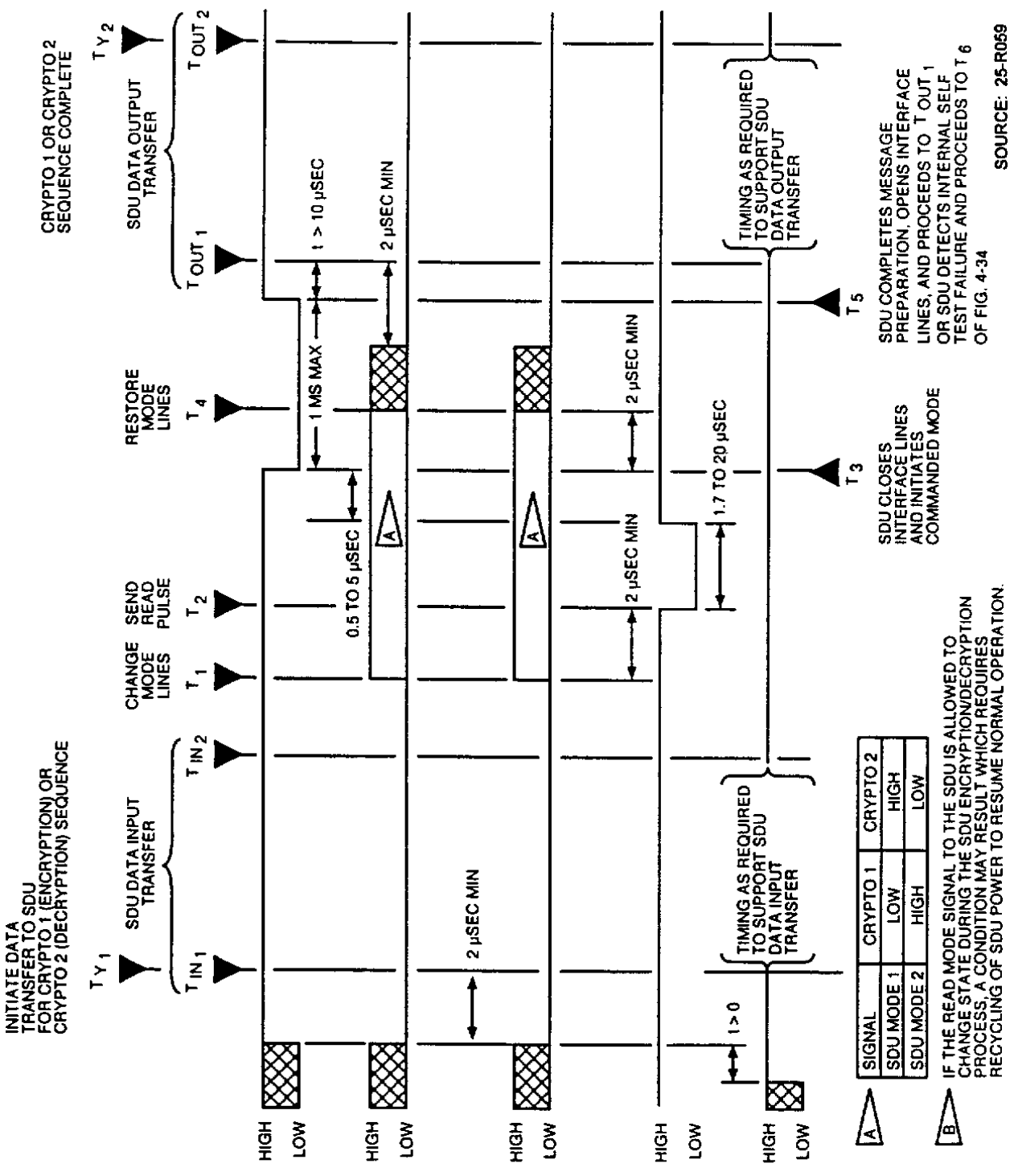


Figure 4-33. Successful SDU Crypto 1 Operation

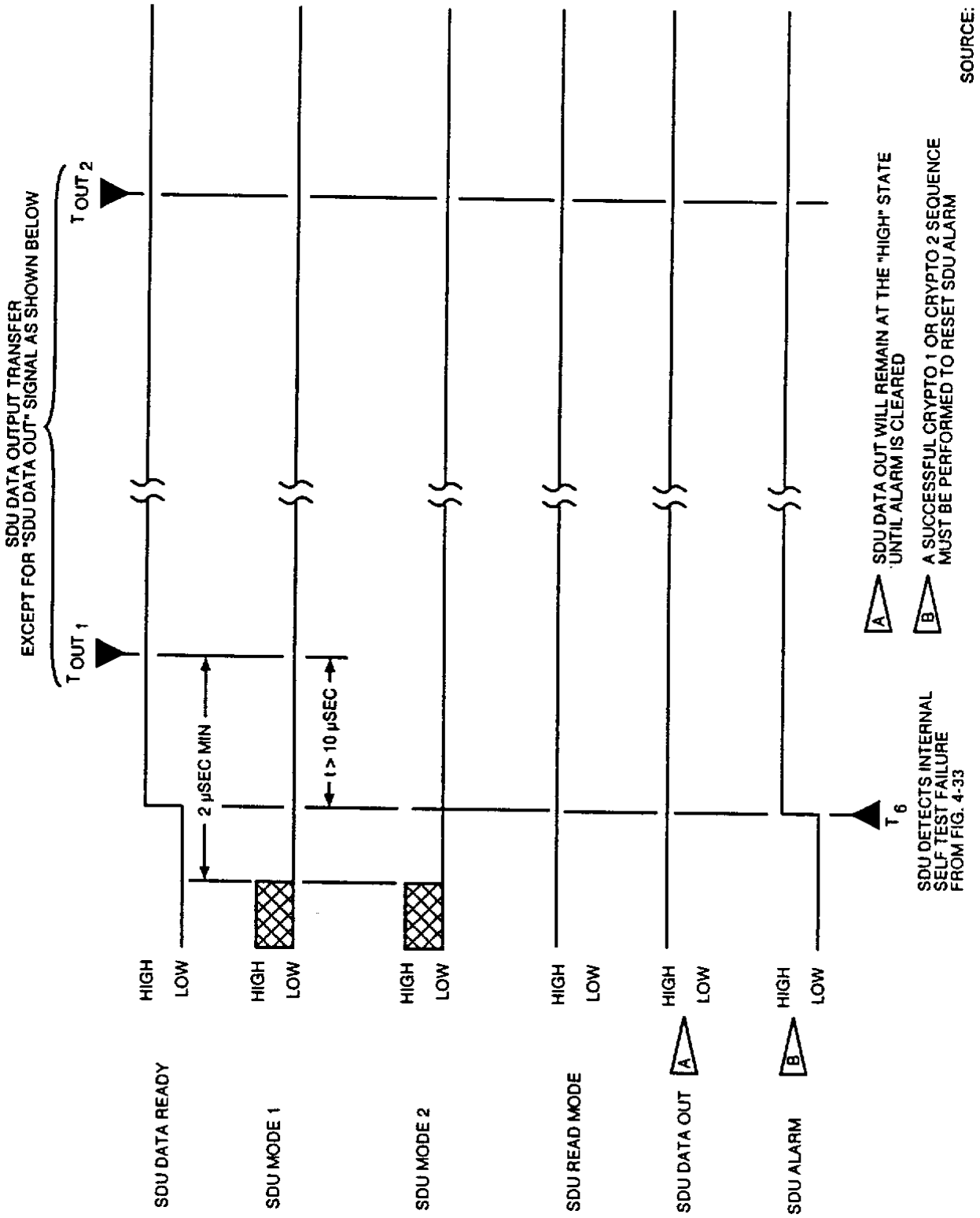


Figure 4-34. Unsuccessful SDU Crypto 1 Operation

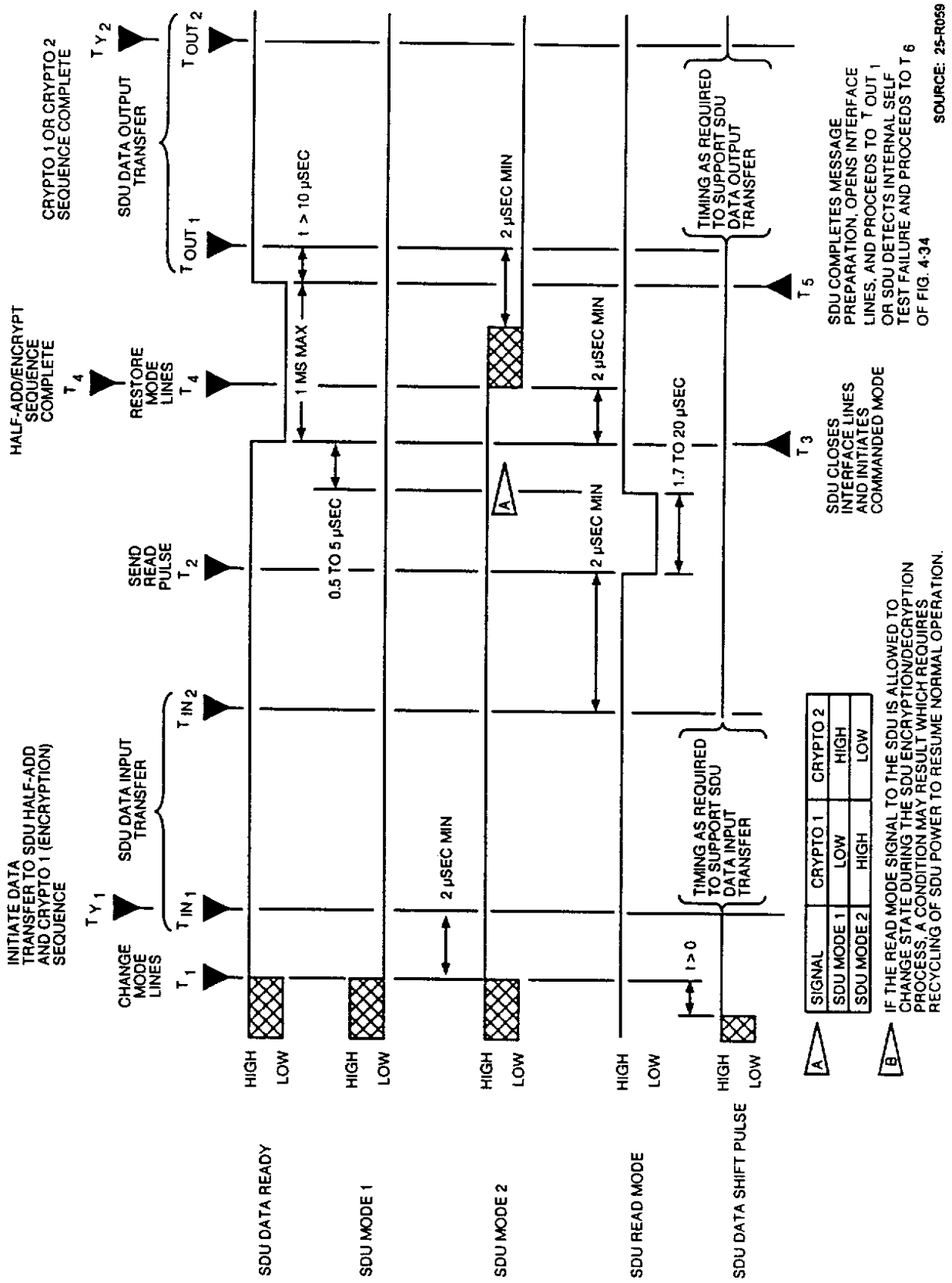


Figure 4-35. Successful SDU Half-Add Sequence

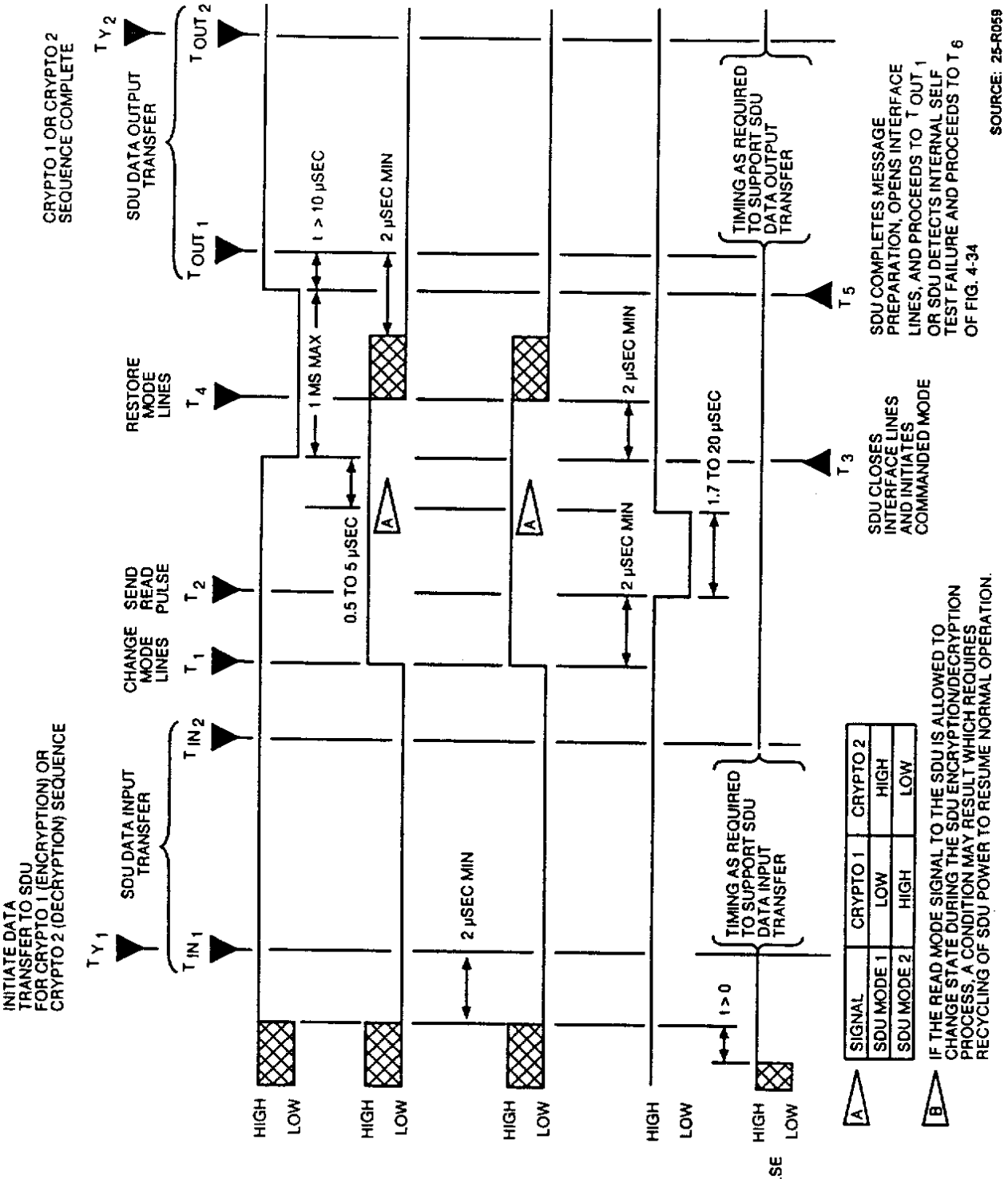


Figure 4-36. Successful SDU Alarm Test Sequence

4-4.14.2. Interface Definition. The COP and WSP interface to the TODC is an asynchronous data channel over which eight bytes of data are sent to the TODC. The first byte is a Start of Text (STX) character, the next two provide the Hours, the next two the Minutes, and the next two the Seconds; the final byte is an End of Text (ETX) character.

4-4.15. Visual Display Unit (VDU).

4-4.15.1. Functions. The COP and WSP interface to the two VDUs to provide identical transmit-only interfaces to the VDUs for displaying data to the Missile Combat Crew Members (MCCMs) at their normal workstations.

4-4.15.2. Interface Definition. The COP and WSP interface to the VDU consists of coaxial Red/Green/Blue composite video signals that conform to EIA RS-343A characteristics. The signals carry line-by-line pixel data for display on the VDUs, including cell pointers, attributes, and standard alphanumeric and punctuation ASCII characters.

4-4.15.3. Control Aspects of Signal Lines. The cell pointers indicate row and column location for each character display position on the 48 row by 102 characters per row display. Each cell consists of 10 horizontal and 16 vertical pixels to compose each character. Attributes include background color, inverse video, flash, and font characteristics. The normal display has black characters on a colored background, but if inverse video is chosen, then the background becomes black, and the characters become what was previously the background color. Fonts are standard, bold, or underline.

4-4.16. Input Power. The WSP receives 500 watts of power from the PCDU of the RCS. The voltage is 120V AC rms (phase to neutral), Phase A, plus or minus 2.4V AC. The frequency is 400 Hz, plus 35 to minus 20 Hz.

4-5. CONSOLE OPERATIONS PROGRAM (COP).

4-5.1. COP Architecture.

4-5.1.1. Hardware Environment. The COP software (also MOTP and EPP) executes on a VAX-based processor using the VAXELN operating system. The processor is the Raytheon Single Module Computer (SMC) Model 810.

4-5.1.2. Operating System. The VAXELN operating system is the operating system used for the WSP. VAXELN is a real-time version of the more versatile VMS operating system. The operating system is a part of the COP CSCI and is identified as the ELN CSC. VAXELN provides the kernel and general purpose I/O capabilities for the COP CSCI, including job scheduling and communications mechanisms between asynchronously running jobs or processes.

4-5.1.3. The VAXELN System. In VAXELN terminology, a system, such as COP, MOTP, and EPP, consists of one or more jobs running under direct control of the VAXELN kernel. Each job is assigned its own priority by the VAXELN kernel. Each job is assigned its own address space and can not directly access data or programs belonging to another job.

4-5.1.4. The VAXELN Job. A job consists of one or more processes, each of which is assigned a priority within the parent job and is independently scheduled by the VAXELN scheduler. Since a process is a subset of a job, the priority of a process is derived from the combination of the priority of its parent, and its own priority within its parent. It is scheduled accordingly by the VAXELN kernel. In the WSP, there are four application jobs: COP [Priority 16], MMIII MOTP [Priority 18], EPP [Priority 18], and Background Memory Test (BMT) [Priority 25]. In addition, the SCSI device driver executes at priority 4 to ensure BS/L access is not blocked by any application program.

4-5.1.5. Processing States. Under VAXELN, processes are in one of the following states: waiting, ready, or running. Processes in the waiting state are held pending completion of the conditions that were defined for the job or process to wait on. Examples are: waiting for a timer interrupt, waiting for an I/O operation to complete, or waiting on an indication from another process or job to continue. Processes in the ready state are available to execute. This state is usually the result of a higher priority activity taking precedence over this activity. There is always exactly one process in the running state. The highest priority activity in the system which is eligible for execution will always be the one in this state. In the event two activities are eligible to be in the running state, and both have the same priority, the scheduler will schedule the same one that last executed.

4-5.1.6. Processing Priorities. VAXELN employs a preemptive priority scheduler which schedules the highest priority job that is in the ready state. The scheduler will allow the selected activity to run either to conclusion of the current activity (until it must wait on some external stimuli) or an interrupt occurs that requires the scheduler to reevaluate the activities in the ready state. At that time, the highest priority task in the ready state will be executed.

a. COP Priority Concept. The priority concept for the COP CSCI (and the WSCE software as a whole) is based on the concept that the processes performing the more time-critical functions receive the higher priorities.

b. Interrupt Service Routines (ISRs). ISRs, used to service interrupts from the hardware, execute at an elevated priority to permit them to receive control quickly so as to prevent hardware register overflow. When an ISR is activated, all interrupts at the level of the executing ISR and below are inhibited. This provides interrupt handling deconfliction and prevents re-entrancy in the ISRs, thereby ensuring the most time-critical ISRs execute first.

c. Job Priorities. Jobs and processes within jobs are prioritized to ensure the time critical functions are operated on first when a choice must be made. The launcher communications interfaces are more time critical than HMI or status processing, so the priorities are set accordingly. The lowest priority in the system is the background checksum test on WSP memory. This test will only execute when no other activity requires processor time. Since this test is a continuously running routine, the processor is never idle, since it is performing the test whenever nothing else is required to be performed.

4-5.1.7. Process Context Maintenance. Every process in the system has a context which contains the processing environment in which it currently exists. The context consists of the registers and other pertinent information on the state of the processing for that process. Each process has within its memory allocation a context save area which is used to maintain the context of a process that is not currently executing. At the time a process in the running state is to be placed in the waiting state, its context (registers, etc.) is preserved in the context save area of the process memory allocation, and the context for the process to go into the running state is restored from its context save area. In this way, the scheduling of any activity can be performed by the scheduler without regard to its previous state since all pertinent information is preserved as a function of the context switch.

4-5.1.8. Compiler. The Ada portions of the COP CSCI are compiled using the DEC VAX Ada Compiler, a fully validated Ada compiler that supports both the VMS and VAXELN operating systems.

4-5.1.9. Use of Re-entrancy. The VAXELN operational environment provides a natural extension to the Ada required capability to generate re-entrant code by building the system so only a single copy of any package (and its associated context, procedures, and functions) exists within the system. If multiple processes within require the same package, then one copy is used, taking advantage of the re-entrancy provided by the compiler, to support all processes using it. This results in a memory savings by avoiding duplication of code where identical capabilities are used, while not significantly increasing the design complexity.

4-5.1.10. Internal Communications Mechanism (ICM). The WSCE software, including the COP CSCI, uses a message-based communications concept known as ICM, with all processes communicating through one of the three standard VAXELN communications mechanisms either with other processes or with the devices:

a. Queues. These provide a simple, low-overhead means to communicate between processes within the same job. Queues are the primary communications mechanism within the COP CSCI. This mechanism is interlocked to prevent concurrent insertions or removals.

b. Circuits. These are primarily used to communicate between jobs and provide a secure first-in, first-out guaranteed delivery communications mechanism that uses remapping of virtual address space to minimize movement of data. Circuits are used to communicate between the COP CSCI and the MOTP and EPP CSCIs, the BMT job and with the SCSI device drivers.

c. Device Drivers. The developed low-level device interfaces are an integral part of ICM. This provides the same flexibility as exists for the queues and circuits.

4-5.1.11. Use of ICM by COP. The COP CSCI provides the Internal Communications Mechanism which is used by all processes within the COP CSCI for all software to software and most software to hardware communications. It employs queues for interprocess communications and allows centralization of all device interfaces except the BS/L. ICM provides a layered communications mechanism that abstracts the method of communication and the physical address of the receiver from the sender of a message. This allows the sender to identify the recipient by name when sending the message, with the ICM determining the routing (which process or job) and which method to use to send the message. The receiver of the message may be in the same process as the sender and can even be the same operation. This allows processing of a lengthy operation to be rescheduled to that other processing in the same process can be executed without excessive delays.

4-5.1.12. Startup Processing. At power-up of the processor, the Boot ROM within the processor is given control. It performs diagnostic checks of the hardware; and if successful, reads the start-up parameters database (table) in the User ROM to determine the start-up processing requirements. Based on the contents of the table, control is transferred to the User ROM, which contains the SUR CSC. The SUR CSC then executes the required tests and loads the software-based portions of the COP CSCI, which includes the VAXELN operating system. Following validations of the program load, control is passed to the starting location in the VAXELN operating system. Following setup of the VAXELN operating environment, VAXELN then initiates execution of the jobs and processes that were identified during the system build process as requiring immediate execution. The only process in the COP CSCI that is in this category is the Master Process (MPR) CSC, which controls the starting of the other processes and programs in an organized manner.

4-5.2. <u>COP Processing Components</u>. The COP CSCI consists of 21 asynchronously running components. There are 20 processes contained within 2 jobs and the ROM-based code. The processes are interrupt-driven, with each process waiting on a given set of inputs, then performing the required operations using the received data. Each process in the COP CSCI has defined a specific set of inputs to which they must respond. These

inputs consist of a mix of internal and external data. At each point in the process that a message is passed from one process to another, a context switch must occur. This, in turn, allows VAXELN to determine the highest priority process available to execute and to place it in the running state. The names, purposes, and priority of each of the processes follow.

4-5.2.1. Background (BKG) Process. [Priority 9]. The BKG process performs all operations involving the floppy disk including Crew Log Archiving, incremental loads (targeting, T.O. Checklist, etc.), disk integrity checks, and TATD generation.

4-5.2.2. Background Memory Test (BMT) Process. [Priority 15]. The BMT process is a separate job under VAXELN, providing a continuously running memory check that executes at the lowest priority in the system.

4-5.2.3. Background Program Load (BPL) Process. [Priority 9]. The BPL process loads and starts the targeting programs (MOTP and EPP) and then waits for them to end, either normally or otherwise.

4-5.2.4. Communications Interface Support (CIS) Process. [Priority 2]. The CIS process maintains the communications interfaces with the rest of the squadron through cable mechanisms. It also provides timing support to all other processes in the CSCI.

4-5.2.5. Checklist (CKL) Process. [Priority 7]. The CKL process manages the T.O. Checklist display capabilities, including display, scrolling, and maintenance of the T.O. Database.

4-5.2.6. Command (CMD) Process. [Priority 7]. The CMD process interprets all command entries, verifies the command content, and sends the command either to the Launcher(s) or to internal processes.

4-5.2.7. Crew Log (CRL) Process. [Priority 7]. The CRL process manages all on-line crew log operations except archiving.

4-5.2.8. Display Generator 1 (DIG1) Process. [Priority 8]. The DIG1 process converts internally formatted data into a format suitable for display. It is one of two such processes provided for this purpose.

4-5.2.9. Display Generator 2 (DIG2) Process. [Priority 8]. The DIG2 process converts internally formatted data into a format suitable for display. It is one of two such processes provided for this purpose.

4-5.2.10. HAC/RMPE Interface Support (HIS) Process. [Priority 3]. The HIS process provides interface control over the HAC/RMPE interface for data messages and controls.

4-5.2.11. IPDM Interface Support (IIS) Process. [Priority 7]. The IIS process buffers and outputs IPD data for the IPD modem.

4-5.2.12. Line Printer (LPR) Process. [Priority 9]. The LPR process collects the HAC/RMPE print data and manages the command interface for print requests.

4-5.2.13. Master Process (MPR) and Actions Pending Queue (APQ) Process. [Priority 0 (MPR), then Priority 6 (APQ)]. This MPR process starts all other processes then becomes the APQ process to manage the APQ display and database, and provides associated task management.

4-5.2.14. Printer Manager (PRM) Process. [Priority 9]. The PRM process manages all spooling aspects of printer functionality. It receives data to be printed in a printer formatted file and outputs it to the printer based on established priorities.

4-5.2.15. Printer Formatter (PRF) Process. [Priority 9]. The PRF process performs formatting of internally generated printer output which is then forwarded to the PRM process.

4-5.2.16. Status (STS) Process. [Priority 7]. The STS process maintains the Launcher and LCC status and provides alarm management.

4-5.2.17. Target Library (TGL) Process. [Priority 7]. The TGL process receives FDMs, EAMs, and operator-entered targeting data; maintains the targeting databases; and interfaces with the MOTP and EPP CPCIs.

4-5.2.18. Time of Day (TOD) Process. [Priority 1]. The TOD process exists to support the transmission of the time to the console clock. This process is required to ensure output to the console clock does not delay any time-critical processing in the CIS process.

4-5.2.19. Workstation Manager 1 (WSM1) Process. [Priority 5]. The WSM1 process provides interface management of the VDU and OID for one operator position. It manages the window allocations, assigning a window area to the requesting process, notifying the affected processes when a window in use is closed or overlaid, and forwarding operator inputs from a specified window to the required process.

4-5.2.20. Workstation Manager 2 (WSM2) Process. [Priority 5]. The WSM2 process provides interface management of the VDU and OID for one operator position. It manages the window allocations, assigning a window area to the requesting process, notifying the affected processes when a window in use is closed or overlaid, and forwarding operator inputs from a specified window to the required process.

4-5.2.21. User ROM (ROM) Process. [Priority not applicable]. The ROM process is the only process that does not function under the VAXELN operating environment. It provides start-up and restart controls, including the loading and verification of the RAM-based software.

4-5.3. COP CSCI Internal Organization. The COP CSCI is structured in Computer Software Components (CSCs), which are the functional allocations of the COP Software Requirements Specification (SRS). Table 4-28 provides a cross reference between the functional tasks of the SRS and the CSCs. The functionality of each CSC is given in the paragraphs below.

4-5.3.1. Command and Status (CAS) CSC. The CAS CSC controls all command execution in the COP CSCI. It identifies the MCCM request and generates the necessary commands to control the operations resulting from the command throughout its lifetime. CAS also maintains the LF and LCC status, determining if operator notifications are required and directing the crew logging of events as appropriate.

4-5.3.2. Crew Log Control (CLC) CSC. The CLC CSC manages the crew log file system, including recording, retrieval, and archiving. It interfaces with several CSCs for the receipt of data for logging, retrieval and archiving commands and the return of responses. CLC interfaces with HMI for the direct transfer of crew log outputs for display. The CLC CSC performs data collection of on-line diagnostic data collection for the HAC/RMPE and communications interfaces.

4-5.3.3. Communications (COMM) CSC. The COMM CSC receives messages from the CAS and TGT CSCs consisting of commands to transmit messages to the specified LF(s), returns transmit status, and provides received and validated LF and LCC messages. The COMM CSC provides basic message protocol, managing communications with the Launchers. The message protocol portions of RDC and similar functions are performed by the COMM CSC, with the higher-level protocol capabilities provided by the appropriate CSC. Any change in status reported by the CMPG card or the interfaces is reported by the CMPG card or the interfaces for operator notification and crew logging.

Table 4-28. SRS Functional Allocations to CSCs

SRS Function	COP CSC	SUR	MPR	IPDM	TMR	CAS	ODI	HMI	TGT	COMM	CRPT	PRN	TST	ELN	UTL	FDT	CLC	TGS	HRC
SRI	Startup, Restart, Initialization	X	X	X															
CCT	Control Clock and Timers				X	X													
ELI	Control LEP, LCP, and CLS					X	X												
HMI	Human Machine Interface					X		X	X										
CSS	Commands, Sequences and Stacks					X		X	X										
MAT	Message Assemble and Transmit									X									
CCL	Crypto Control			X							X								
RLC	Message Reception and Line Checking									X									
MIS	Message Identify/System Status			X		X				X									
WST	WSP Testing	X				X	X	X		X		X	X						
CPI	Console Printer Interface							X				X							
SSR	System Services							X						X	X	X	X		
TMT	Targeting Management and Transmission								X	X	X							X	
PEM	Process EAMs								X	X									X
HRI	HAC/RMPE Interface Control												X						X

4-5.3.4. Encryption/Decryption (CRPT) CSC. The CRPT CSC provides the interface with the cryptographic device, encrypts or decrypts selected data using one of the two variables provided. It encrypts and decrypts the provided data using the requested keying variable, returning the result to the requester. If a change in status of the crypto device is detected, it is reported for crew logging and operator notification.

4-5.3.5. VAXELN Operating System (ELN) CSC. ELN is the real-time operating system for the WSCE and interfaces with all other processes, and jobs within the WSCE. It consists solely of the VAXELN operating system.

4-5.3.6. Floppy Disk Transfer (FDT) CSC. The FDT CSC manages the Floppy Disk Drive and supports all incremental load capabilities. It interfaces with the FDD to output crew log archives, read and write case image transfers, and perform incremental loading, including T.O. checklists. FDT interfaces with HMI and CAS for control over the floppy transfer process.

4-5.3.7. Human Machine Interface (HMI) CSC. This CSC controls all outputs to and inputs from the Missile Combat Crew Members (MCCMs) and forwards the MCCM inputs to the appropriate CSC for further processing after basic input checks are completed. HMI interfaces with both Operator Input Devices and VDUs to provide this capability. HMI receives inputs from associated CSCs for display in one of two forms: simple display requests, which include the data to be displayed, and complex requests, which provide a file identification for the data to be displayed.

4-5.3.8. HAC/RMPE Control (HRC) CSC. HRC provides the interface to the HAC/RMPE processor for receipt of message and status data and the output of commands and responses to the HAC/RMPE processor. It receives and buffers received messages, provides the ACK/NAK as appropriate, then identifies the message and forwards it to the appropriate CSC for further processing.

4-5.3.9. IPD Modem (IPDM) CSC. The IPDM CSC provides the transformation, queuing, and transmission of status data to the IPD Modem external interface. It also reports status changes in the IPD Modem interface for appropriate reporting.

4-5.3.10. Master Process (MPR) CSC. MPR receives control at start-up and whenever a job or process fails. It interfaces with the SUR CSC to receive start-up information and interfaces with all other processes and jobs to control the start-up and shutdown of the system.

4-5.3.11. Operator Discrete Interface (ODI) CSC. The ODI CSC manages the interface with the Discrete inputs from the system which either report status or signal an operator Discrete input. It determines the validity of launch switch action and reports it to CAS, along with the launch codes, if appropriate. ODI also recognizes and reports Inhibited Switch actions and reports them to CAS, along with the associated inhibit code. It also sets an indicator which is read by COMM to verify the launch command prior to transmission. All launch attempts, whether successful or not are reported for crew logging and alarming. It forwards external LCC status changes and reports changes in the Missile Away indications.

4-5.3.12. Print Control (PRN) CSC. PRN provides printer output spooling. It interfaces with the HAC/RMPE Primary and Backup processors as well as COP CSCs to receive print requests and output them to the printer. It also receives printer test requests and, after testing the printer, returns the results to the Command and Status Control CSC.

4-5.3.13. System User ROM (SUR) CSC. SUR executes from the processor's User ROM, receiving control from the Boot ROM on completion of hardware tests, then completes testing of peripherals critical to completing the load of the COP system. It then loads the executable image of the COP system, and performs CMSC testing to ensure a safe load. Prior to releasing control to the COP system image, it passes start-up information to the

MPR CSC. The SUR CSC provides rudimentary communications with the MCCM, allowing status information to be output and inputs to be accepted when required.

4-5.3.14. Targeting Support (TGS) CSC. TGS provides background processing support for targeting-related actions. TGS generates and maintains the Targeting and Timing Document (TATD) for on-line use by the MCCMs. It receives inputs indicating either to generate a whole new document or update a portion based on an Execution Plan Case Input (EPCI) library update.

4-5.3.15. Targeting (TGT) CSC. TGT provides the FDM and weather libraries, and the Target Case and Execution Plan case libraries. The TGT CSC also generates the Execution Option from provided data. In addition, TGT provides the interface to the MOTP and EPP CPCIs. It also maintains the constants libraries and stacks, and controls the Remote Data Change processes.

4-5.3.16. Timer (TMR) CSC. The TMR CSC provides timing support to all CSCs. Tasks requiring timer support make requests to TMR. TMR provides interrupt services for the processes, reporting timer expiration based on the requests. It also provides the ability for a process to remove an item from the timer stack if the need for it has passed due to the occurrence of a related activity.

4-5.3.17. Background Test (TST) CSC. The TST CSC continuously performs the background tests during system operations and if an error is detected, forces a system restart and operator notification by transferring control to the SUR CSC.

4-5.3.18. Utilities (UTL) CSC. This CSC provides the internal communications mechanism and utility routines used by multiple CSCs.

4-6. WSP SELF-TESTS. The WSP employs a variety of self-test mechanisms. The largest number of these are performed at Startup or Restart; others operate in background mode during normal operations; and others may be commanded during operations by the MCCM. In an off-line mode, using commands sent to the SMC810 through the diagnostic port, all of the ROM-based diagnostics provided by Raytheon can be exercised.

4-6.1. Startup Sequences. "Startup" (also called "power-on reset," or "cold start") refers to those times the processor is started from a power-off condition. The startup sequence proceeds from the Boot ROM to the User ROM to the COP code in RAM (EMAD).

4-6.1.1. Boot ROM Startup. The Boot ROM contains diagnostics which 1) perform a self-test; 2) check the on-board registers and most on-board functions; 3) check the 512 kByte RAM; 4) check the MEbus modules and EMAD. The Boot ROM is protected by a 32 bit checksum which is checked during self-test. Detected failures from any diagnostic inhibit further processing. [Failure data can only be gathered when a terminal is connected to the

diagnostic port.] Upon successful completion of diagnostics, control of the processor is passed from the Boot ROM to the User ROM.

4-6.1.2. User ROM Startup. SUR issues a reset to the RMB32 and RSCSI cards, checks the results of the Boot ROM tests for EMAD, RMB32A, RMB32B, and RSCSI cards and outputs a status to the VDU. SUR also provides a Startup indication to the VDU. SUR next obtains the site address from the SAP. [This tests the SMC810-SAP path.] SUR obtains the site address from the BS/L. [This tests the SMC810-BS/L path.] If the two site addresses match, the operator is prompted to initiate the COP load. Upon request, SUR loads COP into memory (EMAD) and overwrites unused memory with halt codes (0's). SUR then authenticates the COP load by computing a CMSC over all addressable, fixed regions of WSP memory (including Boot ROM, User ROM, and RAM), and comparing it to the decrypted version of the encrypted value stored on the BS/L. [This tests the SMC810-SDU path and the operation of the SDU.] Failures during this sequence are reported to the VDU screen and result in an attempt to Restart. After COP load validation, SUR relinquishes control to the COP software in RAM.

4-6.1.3. VDU Indications. There are two categories of VDU indications. These VDU indications are displayed during the firmware-processing portion of the Startup/Restart process. During firmware processing, only a limited HMI is available.

One class of messages provides feedback on the status of the startup/restart procedure. The operator prompt message appears in black letters on a white background. The error messages appear in black letters on a yellow background. The VDU indications for this class of messages include:

NOTE: The error codes are for software maintenance use only. They are used to pinpoint where the fault occurred in the software.

a. Power-on Restart In Progress

b. NED Detected Circumvention Restart In Progress

c. Watchdog Timeout Restart In Progress

d. Hardware Initiated Restart In Progress

e. Software Initiated Restart In Progress

f. Background Test Failure Restart In Progress

g. Operator Initiated WSP (RAM) Overwrite In Progress

h. Operator Initiated BSL Overwrite In Progress

i. Operator Initiated Emergency Overwrite In Progress

j. Commanded Restart in Progress

k. Restart In Progress - Unknown Cause

l. Error retrieving character from the OID

m. Error Transmitting Data. Error Code: xxxxxxxx

n. RMB32x reset failed

o. RMB32x Port y Initialization Failed

p. SMC810 overwrite error

q. EMAD overwrite error

r. SCSI Driver Initialization Failed

s. SCSI Self test failure. See SCSI Status

t. WSP Initialization Successful

u. WSP Initialization failed, Error Code: xxxxxxxx

v. Site Address Validation Failed, Error Code: xxxxxxxx

w. Error retrieving Site Address from the plug

x. Invalid Character Received

y. Invalid Site Address

z. Valid Site Address

aa. Press SHIFT + LOAD/RESTART keys to begin COP Software Load

ab. COP Load In Process

ac. COP Load Successful

ad. COP Load Failed. Error Code: xxxxxxxx

ae. Invalid Response

af. BS/L (Read) Transfer Error. See SCSI Status

ag. BS/L (Write) Transfer Error. See SCSI Status

ah. BS/L File Open Error, Error Code: xxxxxxxx

ai. BS/L File Read Error, Error Code: xxxxxxxx

aj. BS/L Interface Failed to Initialize

ak. Error writing block: xxxxxxxx

al. Failed 2 Successive Overwrites

am. RAM error. Address: xxxxxxxx

an. ROM error. Address: xxxxxxxx

ao. COP Authentication In Process

ap. COP Authentication Successful

aq. COP Authentication Failed. Error Code: xxxxxxxx

ar. SDU Alarm test failed

as. Error performing operator initiated overwrite of BS/L

at. Error Performing Encrypt. Error Code: xxxxxxxx

au. Error Performing Decrypt. Error Code: xxxxxxxx

av. Encrypt CDA Loopback test failed

aw. Decrypt CDA Loopback test failed

ax. Encrypt/Decrypt test failed

ay. Error Performing BI DMA Transfer During a CDA/IPD Read

az. Error Performing BI DMA Transfer During a CDA/IPD Write

ba. Error initializing the CDA/IPD card

bb. Error Clearing The Interrupts On The CDA/IPD Card

The other category of VDU indications is the Device/Register Summary (Figure 4-37), which displays status and register information for various devices (i.e., SMC810, RMB32A, RMB32B, SCSI, CDA/IPD, and EMAD) involved in startup/restart processing (see Table 4-29). All VDU indications are a direct result of MCCM or system initiation of startup or restart procedures. Prior to startup, the screen is black and VDU indications appear upon initiation of the startup command. In the case of restart, the screen blanks to black (status is saved) and then the messages are displayed on the VDU. If the user ROM enters the idle mode, an indication of IDLE appears in the center of the interwindow dividing the screen. This indication consists of bold black text on a yellow background.

After COP software has been successfully loaded and authenticated, COP software performs the remainder of the startup process.

4-6.1.4. Remaining COP Startup. COP logs the startup event and enables interrupts. From this point on, the exact sequence of events is interrupt-driven through receipt of data over the enabled interfaces. Errors are reported to the VDU in the format specified in Table 6-6.

a. COP sets the interface parameters on the RMB32A and B cards, and enables the interfaces.

b. COP requests BDI card status, which enables that interface. COP executes the BDI board test: (1) COP commands the BDI card lines to be set low (called Diagnostic 0) and reads them; (2) COP commands the BDI card lines to be set high (called Diagnostic 1) and reads them.

DEVICE/REGISTER SUMMARY

Device	Status	Register A	Register B	Register C	Register D	Register E
SMC81Ø	Pass	ØØ1Ø3Ø91	ØØ1Ø3Ø93	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
RMB32 A	Pass	Ø2Ø18Ø15	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
RMB32 B	Pass	Ø2Ø18Ø17	ØØØØØØØØ	FFFFFFFF	FFFFFFFF	FFFFFFFF
SCSI	Fail	ØØØØØØØØ	FFFFFFFF	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
CDA/IPD	Pass	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
EMAD	Pass	FFFFFFFF	ØØØØØØØØ	FFFFFFFF	FFFFFFFF	FFFFFFFF

POWER-ON RESTART

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Figure 4-37. Device/Register Summary

c. COP executes CMPG module diagnostics and enables the interface. The diagnostics consist of: (1) serial I/O loopback of a 54-bit test message, which moves data through the portion of the module that interfaces with the RMB32B card; (2) Diagnostic 1 (sets lines high); (3) Diagnostic 0 (sets lines low); (3) CMPG loopback of a 54-bit test message, which moves data through the portion of the module that interfaces with the CMPG. The returned message contains the preamble, unique sync bits, and is diphase encoded.

d. COP tests the IPD portion of the CDA/IPD card and enables the interface (the CDA portion has been checked implicitly during the load and validation of COP by SUR). The IPD test is a loopback test of 54 bits of alternating 1s and 0s.

e. COP loads the EPP and MOTP programs from the BS/L into RAM, and validates the load via a CMSC computation and comparison.

4-6.2. Restart Sequences. "Restart" refers to those times the WSP is started up without experiencing a power-off. Restart types are: hardware-initiated, software-initiated, circumvention, and watchdog timer. All types result in the same restart sequence.

4-6.2.1. Boot ROM Restart. The Boot ROM contains diagnostics which 1) perform a self-test; 2) check the on-board registers and most on-board functions; 3) check the 512 kByte RAM resident on the SMC810 board. The Boot ROM is protected by a 32 bit checksum which is checked during self-test. Detected failures from any diagnostic inhibit further processing. [Failure data can only be gathered when a terminal is connected to the diagnostic port.] Upon successful completion of diagnostics, control of the processor is passed from the Boot ROM to the User ROM.

4-6.2.2. User ROM Restart. SUR issues a reset to the RMB32 and RSCSI cards, and performs a Memory Test and an I/O Test. The Memory Test consists of testing READ capabilities for ROM, and WRITE and READ capabilities for RAM. The I/O Test consists of checking the SMC810 internal bus, and requesting card status from the RMB32-A and B cards, the SCSI card, and the CDA/IPD card. Failures are reported to the VDU, if possible, and result in entering a halt mode (sometimes called "idle mode"). If continuing, SUR displays the type of Restart on the VDU. SUR loads COP into memory (EMAD) and continues with the same processing as for Startup. After COP load validation, SUR relinquishes control to the COP software in RAM.

Table 4-29. Device Status Registers

DEVICE	REGISTER
SMC810	A. BI Control and Status Register B. Bus Error Register C. BCI4 Error Register D. Control and Status Register E. Unused Register
RMB32A	A. VAXBI-M Control and Status (VAXBICSR) Register B. Test Summary (TSMR) Register C. Maintenance (MAINT) Register D. Configuration (CONFIG) Register E. RX FIFO (RBUF) Register
RMB32B	A. VAXBI-M Control and Status (VAXBICSR) Register B. Test Summary (TSMR) Register C. Maintenance (MAINT) Register D. Configuration (CONFIG) Register E. RX FIFO (RBUF) Register
SCSI	A. VAXBI-M Control and Status (VAXBICSR) Register B. Port Status (PS) Register C. Port Error (PE) Register D. Port Data (PD) Register E. Power-up Diagnostic (PUDR) Register
CDA/IPD	A. Unused Register B. Unused Register C. Unused Register D. Unused Register E. Unused Register
EMAD	A. MEbus Control and Status Register B. MEbus Status Register C. Memory Error Register D. MEbus Control and Status Register E. Unused Register

4-6.2.3. Remaining COP Restart. COP logs the Restart event and enables interrupts. From this point on, the exact sequence of events is interrupt-driven through receipt of data over the enabled interfaces. COP sets the interface parameters on the RMB32A and B cards, and enables the interfaces. COP requests BDI card status, which enables that interface. COP resets the CMPG interface to enable CMPG communications. For a circumvention restart, COP also requests a reset of the NED flag indication on the NED/Printer Switch card. COP loads the EPP and MOTP programs from the BS/L into RAM, and validates the load via a CMSC computation and comparison.

4-6.3. Background Tests. The following tests are run in background mode during normal COP operations. Error detection and correction executes on the EMAD each time a READ command is issued. Breakwire tests execute periodically, approximately every 40 seconds. The memory test executes whenever nothing of higher priority is scheduled.

4-6.3.1. EMAD Error Detection and Correction Logic. Single bit error correction and double bit error detection is employed during reads from DRAM. All writes to DRAM must be written as longwords to generate the proper check bit codes. Thus, masked longword transactions are handled as read-modify-writes.

a. If a correctable read error is detected, the logic will correct the read data, set the Correctable Read Error bit in the CSR, latch the Error Syndrome of the bit in error, and generate an ME CRD interrupt (if enabled). The read correction requires an extra 200 nanoseconds to complete.

b. If an uncorrectable read error is detected, the logic will set the Uncorrectable Read Error bit in the CSR, latch the Error Syndrome, and terminate the transaction with an error response on the MEbus.

c. The read portion of a read-modify-write may also generate CRD or URD errors. If a CRD error occurs, the logic will correct the read data, set the Correctable Read Error bit in the CSR, latch the Error Syndrome, and terminate the transaction with an error response on the MEbus without completing the write.

d. If the read portion of a read-modify-write detects an uncorrectable read error, the logic will set the Uncorrectable Read Error bit in the CSR, latch the Error Syndrome, and terminate the transaction with an error response on the MEbus without completing the write.

4-6.3.2. LCP/CLS Breakwire Test. The LCP/CLS Breakwire test first checks that the LCP/CLS lines can be toggled to ones, then that the lines return to zeros automatically. Failures are reported as indicated in Table 6-6.

a. Diagnostic Request portion. COP sends a Diagnostic Request discrete to the LCP interface card, which sets the input lines from the LCP and the CLSs to ones, and returns the data to COP for comparison to expected results.

b. Secure Code Request portion. COP then sends a Secure Code Request discrete to the LCP interface card, which latches the current state of the input lines, and returns the data to COP for comparison to expected results.

c. Check of Discretes. Whenever COP issues a discrete command, COP tests the path of the discrete command (through the CDA card) by verifying the current state of the lines is zero, then commanding the CDA/IPD interface card to enable the LCP card discrete control lines, and then immediately (within 140 μsec) reading the state of the control lines.

d. Read Switches Request portion. COP sends a Read Switches Request discrete to the LCP interface card, which results in two bytes of status data being returned to COP. No data comparison is made, as it is the path that is being checked.

4-6.3.3. LEP Breakwire Test. The LEP Breakwire test functions exactly as the LCP/CLS test does, except that the Diagnostic Request discrete is sent to the LEP interface card (through the CDA card), and the second discrete is called Enable Data Read Request. Failures are reported as indicated in Table 6-6.

4-6.3.4. WSP Memory Check. On a non-interfering basis, a 32-bit linear checksum is calculated over all parts of COP code, EPP code, and MOTP code resident in WSP volatile memory. Each result is compared to the previously calculated result. A discrepancy causes a software-initiated Restart.

4-6.4. MCCM Initiated Tests. The MCCM has the capability to initiate individual hardware component tests or perform a set of these tests as part of the LCC subsystem test. The LCC Subsystem Test is performed in the order shown in the third column of Table 4-30. The individual component tests and those tests included in the LCC subsystem test are listed in Table 4-30, and described in the subparagraphs below.

Table 4-30. MCCM Initiated Tests

NAME	INDIV.	LCC SUBSYSTEM
REACT Alarms Test	X	1
CDA/IPD Test	X	
CMPG Line Seize Test		5
Floppy Disk Drive Test	X	3
Nuclear Event Detector (NED) Test	X	
Operator Input Device (OID) Test	X	
Printer Test	X	2
Video Display Unit (VDU) Test	X	
WSP Bulk Store CMSC	X	8
WSP Bulk Store Test	X	7
RMP Subsystem Test	X	6
SDU Alarm Test		4

4-6.4.1. REACT Alarms Test. The REACT Alarms Test cycles through the five (EAM, Non-EAM, Fire, Critical and Routine) REACT system alarms providing the operator with the visual and audio alarm for each type of alarm. The operator observes the proper/improper operation of the REACT alarms and manually logs and reports any observed failures. Once the operator initiates the Alarms Test a Black Discrete Interface (BDI) board test is performed prior to the actual initiation of the Alarms Test. The BDI Test is the same test performed during startup and is performed to verify proper operation of the BDI board, through which the Alarms Test is executed. Failure of the BDI Test halts the Alarms Test. Indications of improper BDI board operation are presented to the operator as indicated in Table 6-6.

4-6.4.2. CDA/IPD Test. The CDA/IPD Test verifies the capability of CDA/IPD interface card to properly communicate with the SDU. The test should only be initiated after the operator has transferred flight responsibility and released the time slot(s) being used by the LCC.

a. CDA interface loopback portion. This portion tests the ability of the CDA/IPD card to set control lines to the SDU, and to move data through the interface. No SDU operation is performed on the data because the card disables the Read Mode discrete control line to the SDU. (1) COP commands the CDA/IPD card for CDA Self-Test and Encryption of a test word. Upon receiving the command the CDA/IPD card disables the Read Mode discrete control line to the SDU and shifts the 48 bit test word through the SDU

interface. (2) The CDA/IPD card returns a Received SDU Data status message to the COP software indicating the encryption mode and Data Ready Indication, which indicates the loopback test was successful. If the CDA/IPD status is incorrect or no status data is received, that portion of the test fails and the results are presented to the operator as indicated in Table 6-6. (3) If SDU data is received, the 48 bit test word received from the card is compared with the 48 bit test word originally transmitted to the card. If the comparison fails or if no data is received, then that portion of the test fails and the results are presented to the operator as indicated in Table 6-6. (4) COP sends another Transmit SDU Data command to the interface card requesting CDA Self-Test and Decryption of a test word. The same comparisons are made as indicated for the Encryption test. Any failures are provided to the operator as indicated in Table 6-6.

b. SDU Alarm Test portion. COP initiates the SDU Alarm Test, described in paragraph 4-6.4.12.

c. Encryption/Decryption Test portion. COP requests encryption of a 48-bit test pattern using the non-HICS keying variable. Upon receipt of the encrypted pattern, COP requests decryption of the received pattern (using non-HICS keying variable). The result is compared with the orginal test pattern. The same process is then executed for the HICS keying variable. Failure data is provided to the operator as indicated in Table 6-6.

d. IPD Interface Loopback portion. In this test, the outgoing data from COP to the IPD portion of the CDA/IPD card is looped back through the CDA side of the card (since there is no data received from the IPD side of the card). COP requests the loopback, sending a 54-bit message of alternating 1s and 0s. An IPD Transmit Complete indication is expected back, as is the message data. The received message is then compared to the original one. Failure data is provided to the operator as indicated in Table 6-6.

4-6.4.3. CMPG Line Seize Test. The CMPG Line Seize Test is only performed as part of the LCC subsystem test. The CMPG Line Seize Test tests each of the 10 CMPG receive lines until a parity error free message is received during a period of 3.1 ± 0.1 seconds. If a parity error free message is not received prior to the expiration of the allotted time the seized input line will be considered to have failed the test. If a failure occurs during the test the operator is notified as indicated in Table 6-6.

4-6.4.4. Floppy Disk Drive (FDD) Test. The FDD test consists of an FDD ROM/RAM test and an FDD read/write test. Before the operator initiates the test an FDD media must be installed in the FDD. Once the test is initiated, the COP software sends an FDD Control/Data reset command message to the FDD. The command message will reset the

FDD controller, which allows the on-board ROM/RAM test to be performed. An FDD Status/Data message is sent to the COP software containing the results of the ROM/RAM test. If either the ROM/RAM test fails or if no data is received, this portion of the FDD test fails, and the operator is notified of the failure as indicated in Table 6-6. The COP software then initiates a write instruction to the FDD with test pattern data to be written to the FDD media. The test pattern data is retrieved from the FDD media with a read command. If an error is encountered during the read/write operation the operator is notified as indicated in Table 6-6. The retrieved test pattern is compared with the transmitted data and if the comparison fails the operator is notified of the test failure as indicated in Table 6-6.

4-6.4.5. Nuclear Event Detector (NED) Test. The NED Test exercises the self-test circuity of the NED device by initiating a circumvention reset. When the test is initiated by the operator, the COP software transmits a NED Diagnostic Request command message to the NED device. The command messages causes the NED to initiate a circumvention reset. The operator determines the success of the NED Test by observing that the WSP initiates a circumvention restart. If a circumvention restart does not occur, the operator logs and reports the NED test failure.

4-6.4.6. Operator Input Device (OID) Test. The OID Test is initiated from the opposite console position on which the OID test is to be conducted. Upon initiation of the test, the COP software echoes all characters and symbols input from the keyboard/trackball under test on the VDU of the workstation under test for visual verification by the operator. If improper OID operation is observed, the operator logs and reports the indications observed.

4-6.4.7. Printer Test. The Printer Test provides the capability to verify the operation of the WSCE printer. Once the test is initiated by the operator the COP software verifies the status of the printer by issuing a Printer Control/Data command message containing an ENQ control code. The ENQ control code causes the printer to send its current status to the COP software in a Printer Device Status response message. If the printer is unavailable to receive print data or no response is received the operator is notified as indicated in Table 6-6. After verifying that the printer is available the COP software transmits a 16 line 80 character test pattern to the printer. The operator is required to verify that all printable characters are contained in the subsequent hard copy print.

4-6.4.8. Visual Display Unit (VDU) Test. The VDU test provides the operator the capability to visually check the color, linearity and focus of the VDU. Upon operator initiation of the test, the base VDU display is replaced with a full screen test pattern. Any observed errors in the test pattern are manually logged and reported by the operator.

4-6.4.9. WSP Bulk Store CMSC. The WSP Bulk Store CMSC performs a 32-bit CMSC calculation over the individual programs and data bases contained on the BS/L. The CMSC algorithm is specified in ICD 25-R060, paragraph CMSC/Checksum Data Processing. If the CMSC generated during the test does not compare with the stored values, the operator is notified of the authentication failure as indicated in Table 6-6.

4-6.4.10. WSP Bulk Store Test. The WSP Bulk Store Test provides the capability to verify the BS/L read/write operation. The test consists of writing a test pattern to the BS/L and then comparing the retrieved data with the data transmitted. The COP software initiates a BS/L Control/Data message to the BS/L requesting a write operation and transmits the test pattern data. To retrieve the data the COP software initiates a BS/L Control/Data message requesting a read operation and receives the test pattern data in a BS/L Status/Data message. If a BS/L error is reported in the BS/L Status/Data message or if no message is received, the operator is notified as indicated in Table 6-6. Additionally, the operator is notified if the comparison of the transmitted and received data failed.

4-6.4.11. RMP Subsystem Test. The RMP primary processor conducts a test of the RMP system upon request from the COP software. During testing of the primary RMP processor, incoming HA messages are processed by the RMP backup processor. Upon initiation of the test, the COP software sends a Print Command (Enable) to the RMP backup processor. The COP software then sends an LCC Test Command (Enable) to the RMP primary processor to initiate the RMP Subsystem Test. The RMP primary processor begins the RMP primary processor test and controls the backup processor portion of the test. The WSCE/RMP interface portion of the test requires the COP software to respond to various interface messages. At the completion of the RMP Test, the RMP primary processor provides the COP software with the results of the test using a Diagnostic Data message. If data is not received by the COP software during the interface portion of the test or if improper data is received, the COP software terminates the RMP Subsystem Test and notifies the operator of RMP or RMPB errors as indicated in Table 6-6.

4-6.4.12. SDU Alarm Test. The SDU Alarm test verifies the proper operation of the SDU alarm indication. Upon initiation of the test, the COP software initiates a Transmit SDU Data message with the Crypto Data set to zeros and the SDU Control set to Alarm Test. The COP software receives a Receive SDU Data message with the status of the SDU Data Ready Indication and the SDU Alarm Indicator. The COP software compares the data received to determine if the Alarm Test passed or failed. The operator is notified of any error indications as specified in Table 6-6.

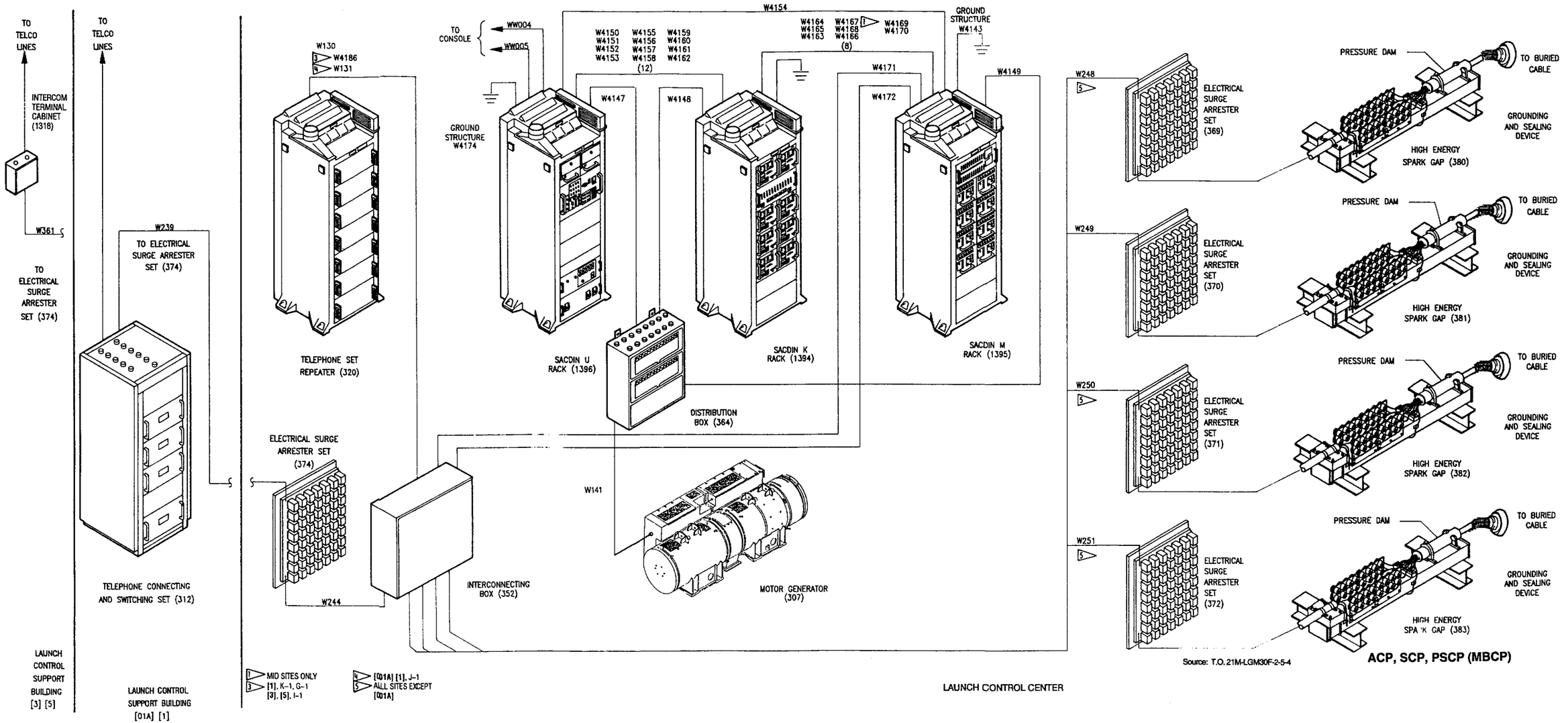


Figure 4-38. SACDIN System (Sheet 1 of 2)

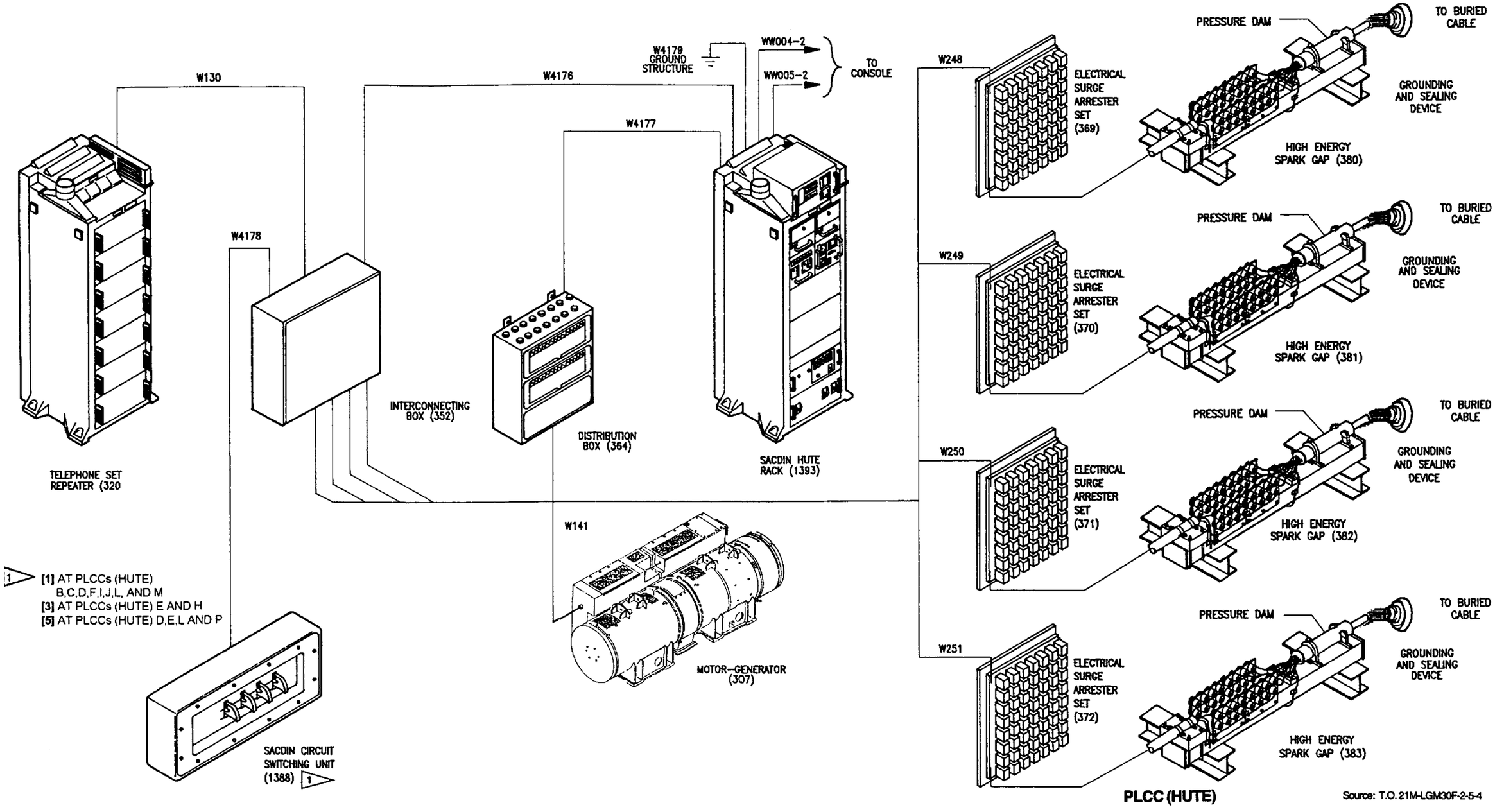
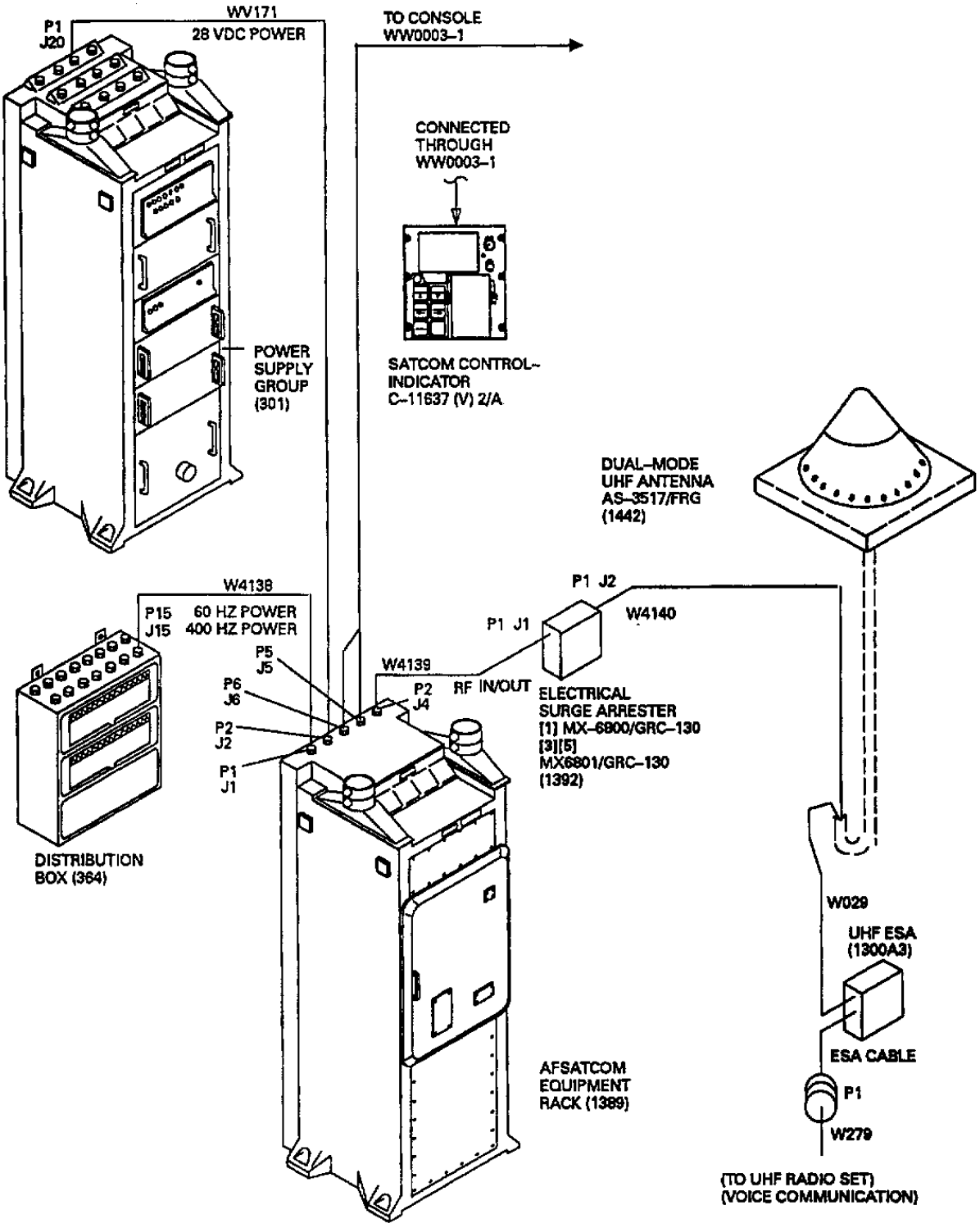
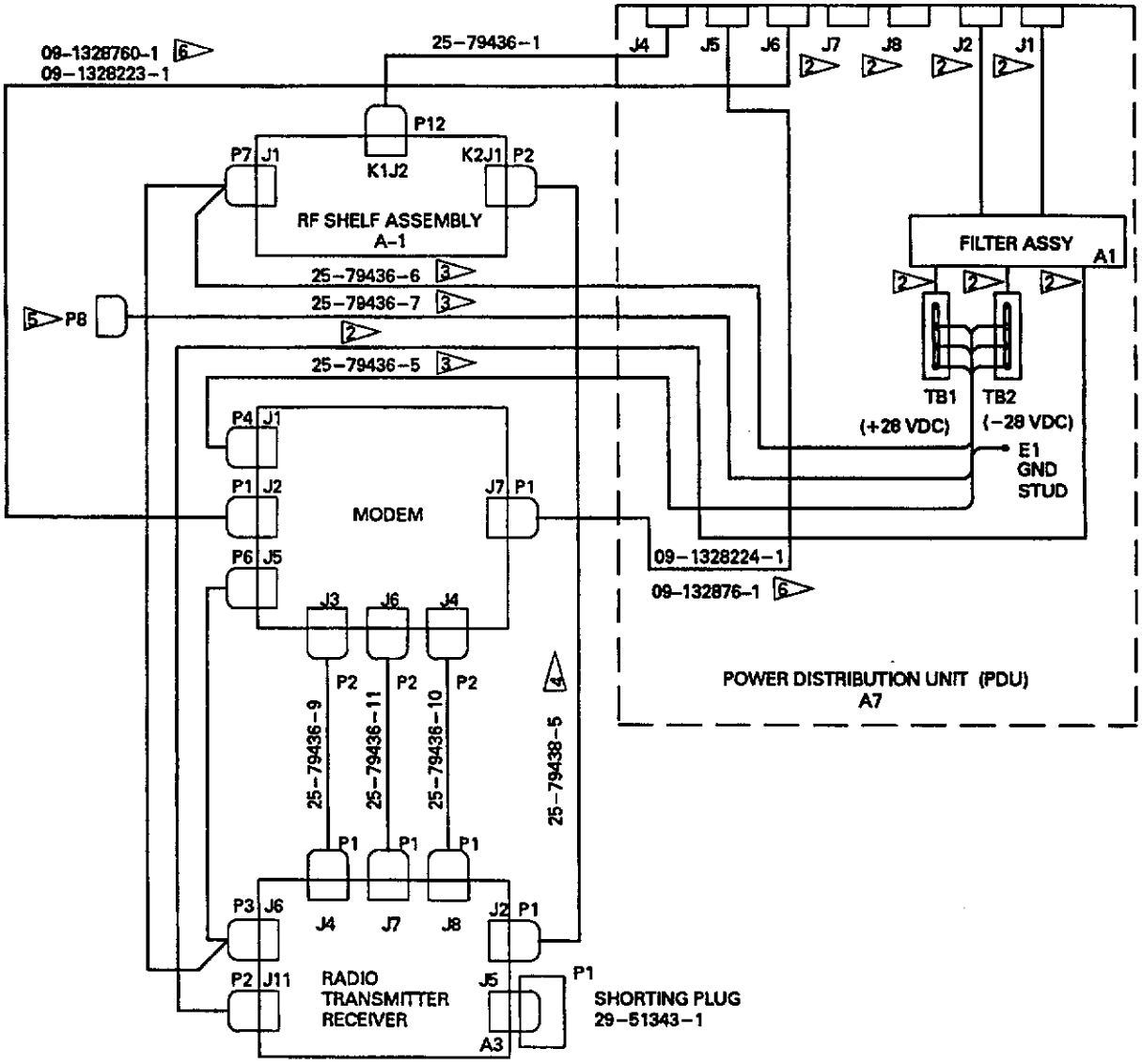


Figure 4-38. SACDIN System (Sheet 2 of 2)



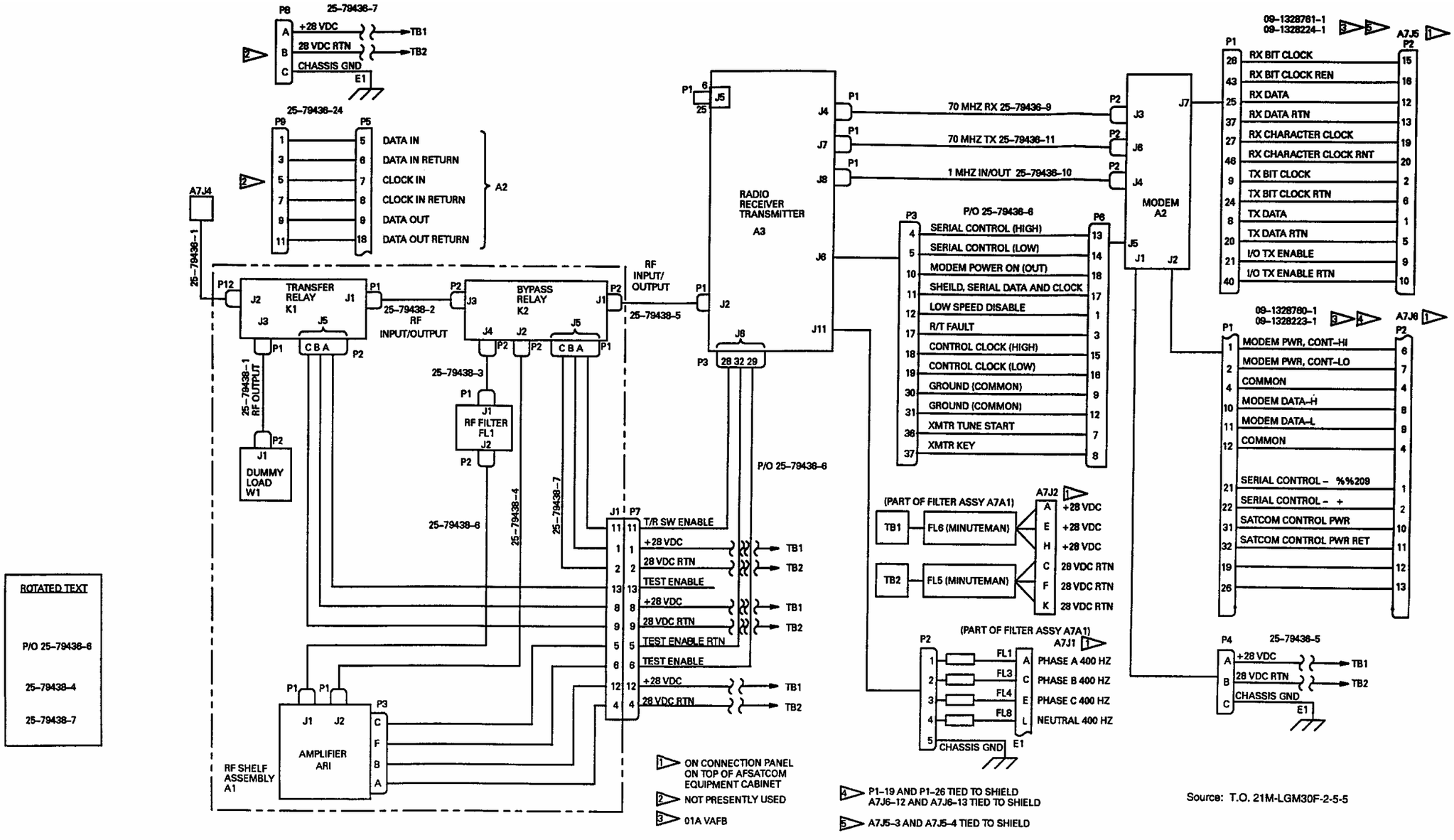
SOURCE: T.O. 21M-LGM30F-2-5-5

Figure 4-39. AFSATCOM System Cabling



SOURCE: T.O. 21M-LGM30F-2-5-5

Figure 4-40. AFSATCOM Equipment Cabinet Cabling



Source: T.O. 21M-LGM30F-2-5-5

Figure 4-41. AFSATCOM Equipment Cabinet Interconnection/Signal Flow Diagram

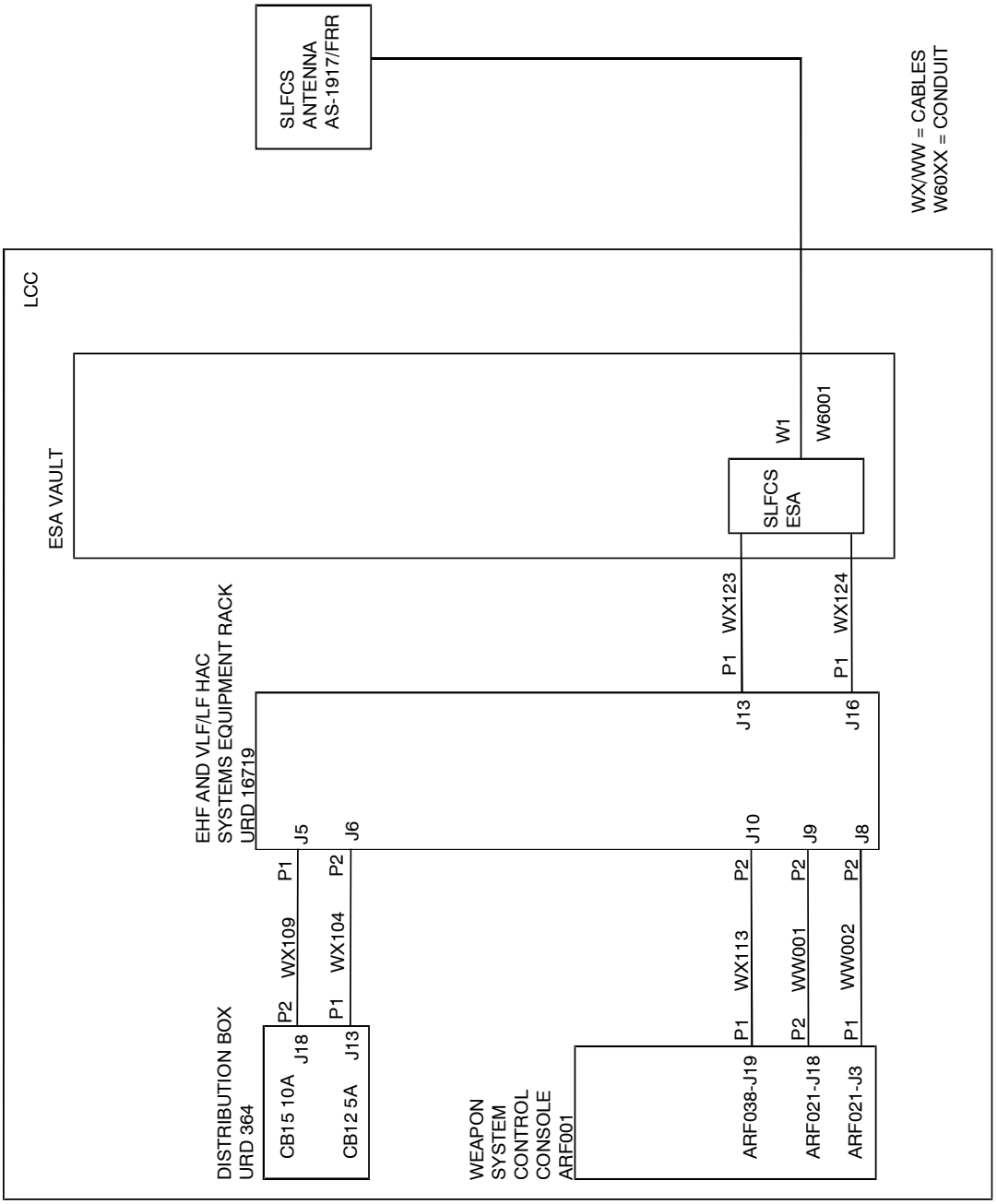


Figure 4-42. SLFCS Cabling

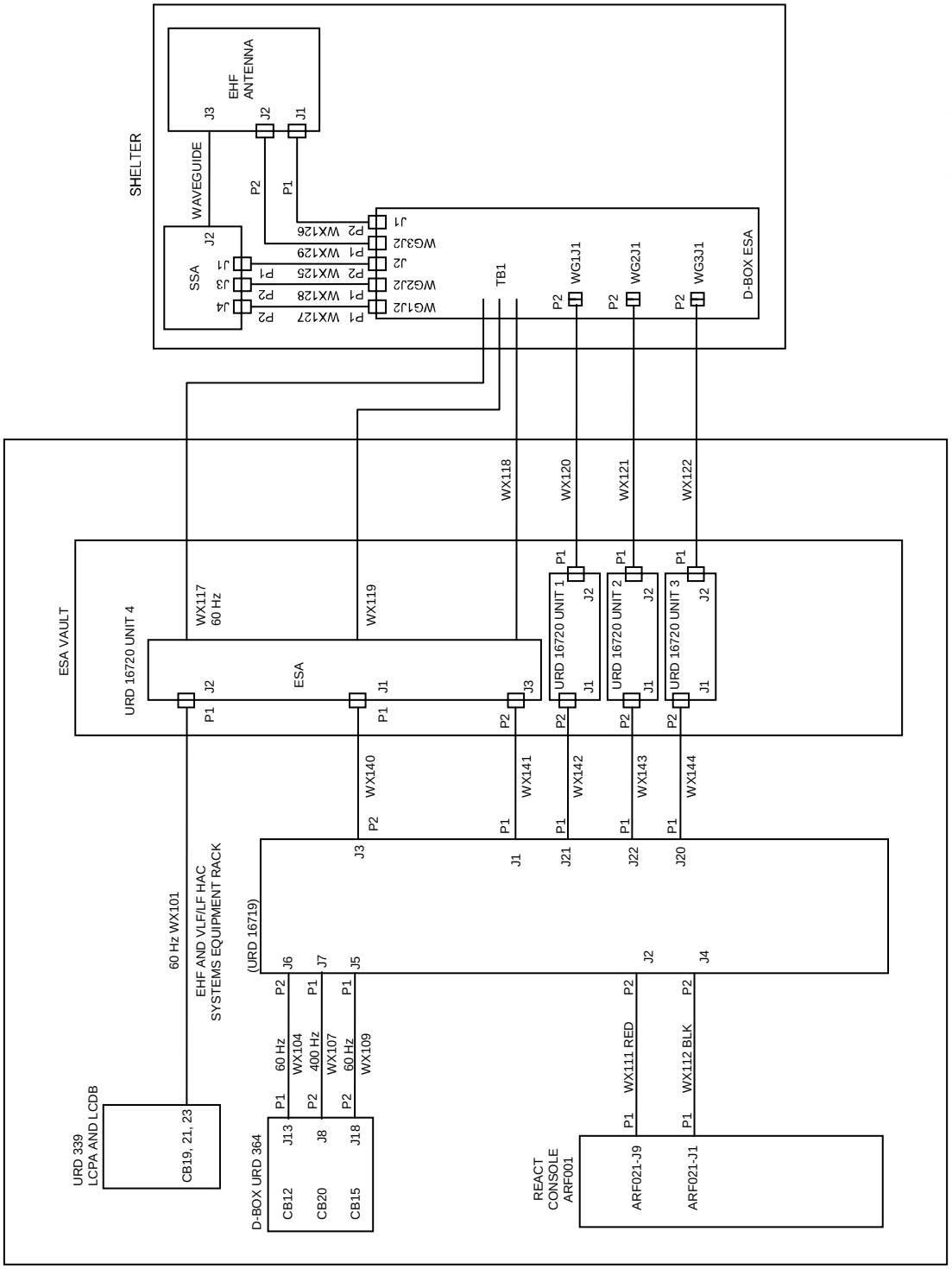
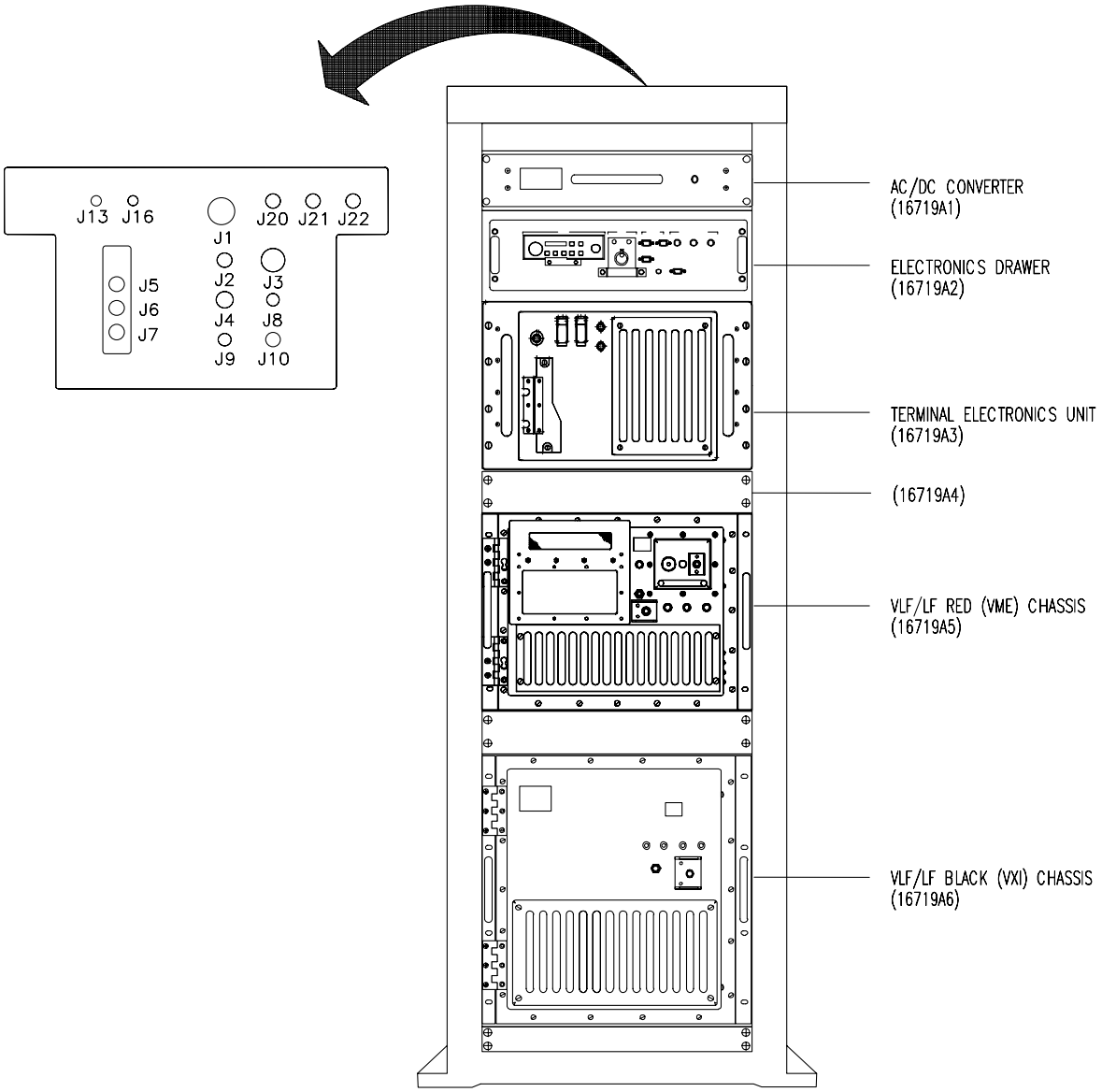
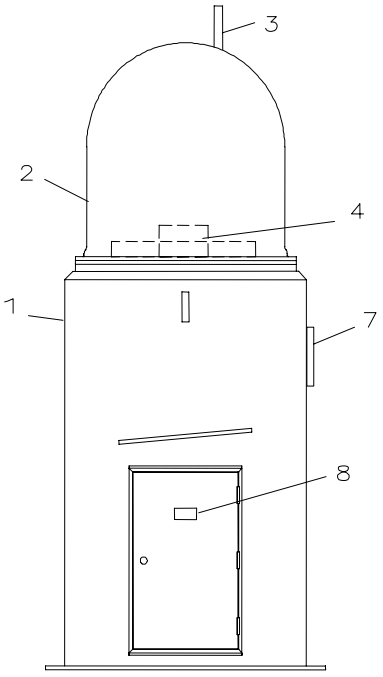


Figure 4-43. EHF MILSTAR System Cabling



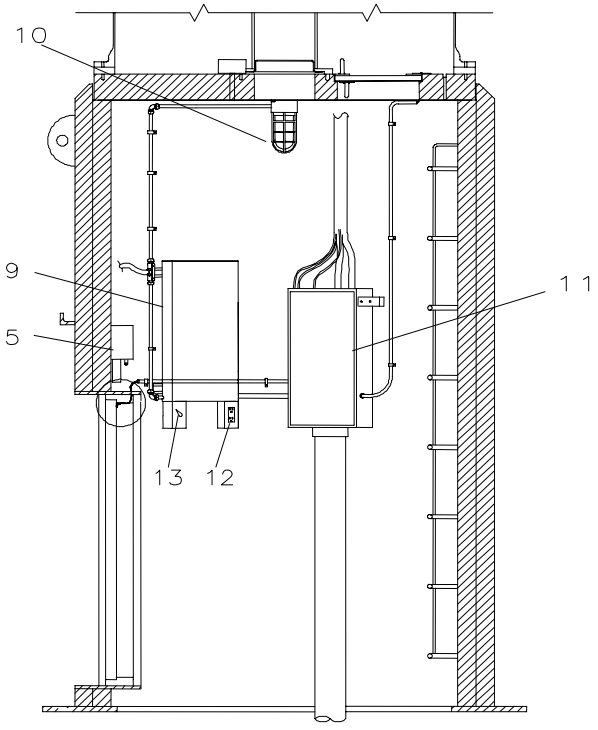
MMMT201_113

Figure 4-43A. EHF and VLF/LF HAC Systems Equipment Rack

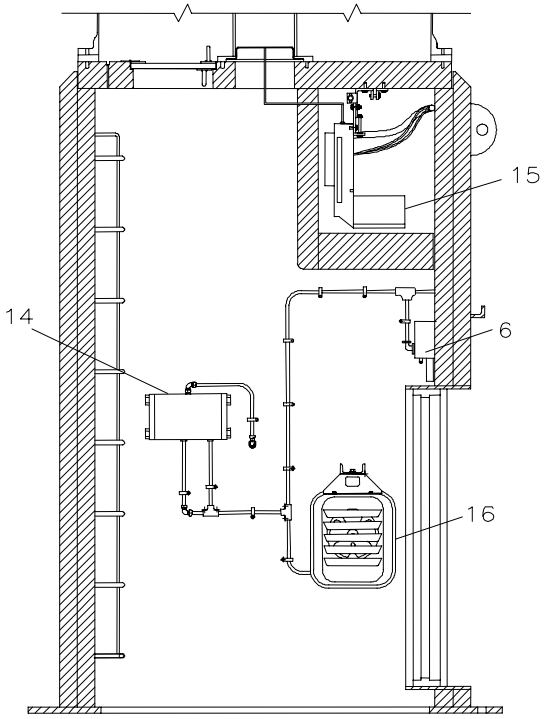


FRONT VIEW

1. SHELTER
2. ANTENNA GROUP (ANTENNA/PEDESTAL ASSEMBLY AND RADOME)
3. LIGHTNING ROD
4. RADOME HEATER
5. RADOME TEMPERATURE SENSOR (INSIDE SHELTER)
6. SHELTER TEMPERATURE SENSOR (INSIDE SHELTER)
7. DEICING MOISTURE/TEMP SENSOR
8. SHELTER DOOR
9. CIRCUIT BREAKER BOX
10. LIGHT FIXTURE
11. DISTRIBUTION BOX
12. ELECTRICAL OUTLET
13. LIGHT SWITCH
14. DEICING CONTROLLER
15. SOLID STATE AMPLIFIER
16. SHELTER HEATER



INSIDE LEFT HAND VIEW



INSIDE RIGHT HAND VIEW

SOURCE T.O. 21M-LGM30F-1-23
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Figure 4-43B. EHF Antenna Shelter

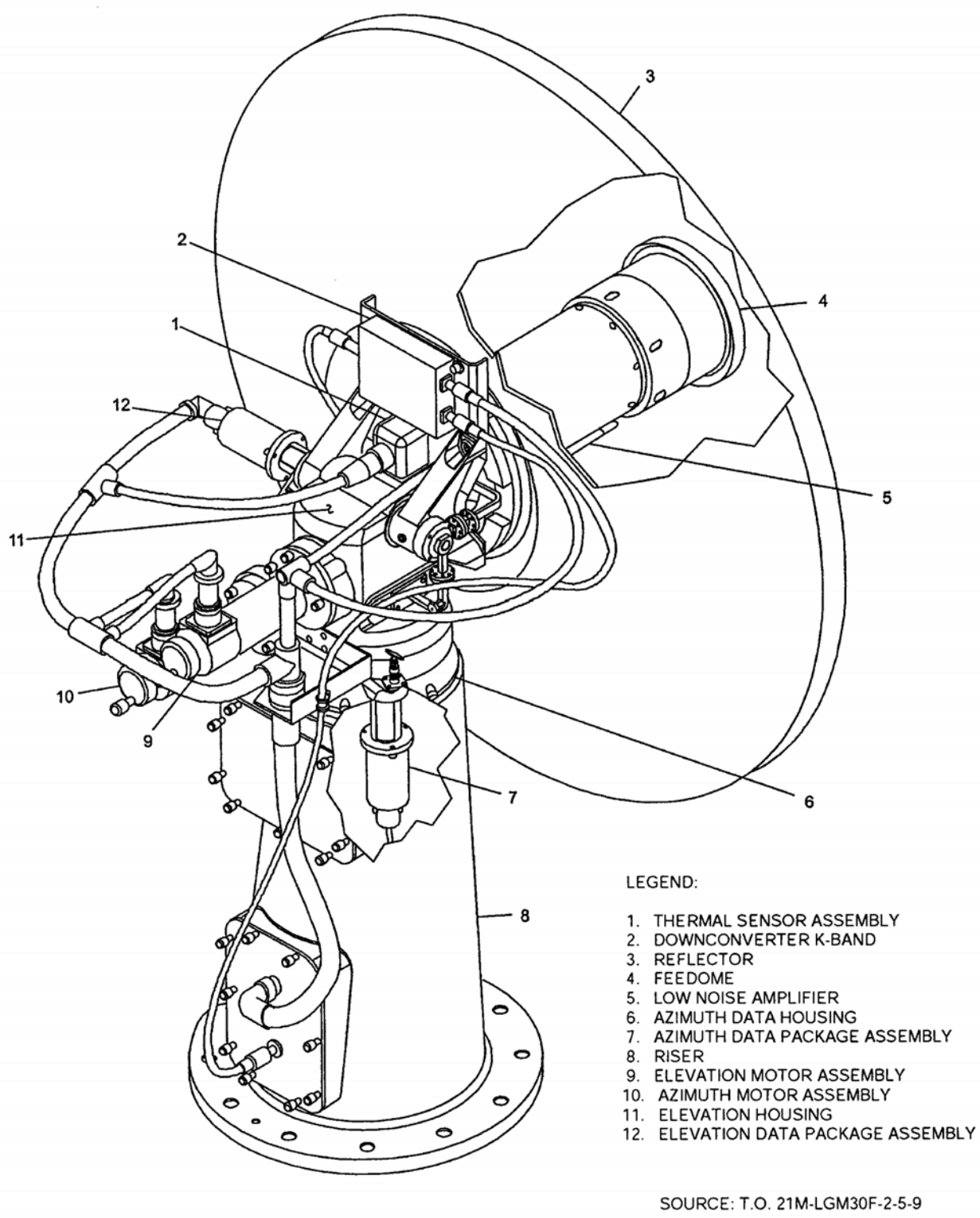
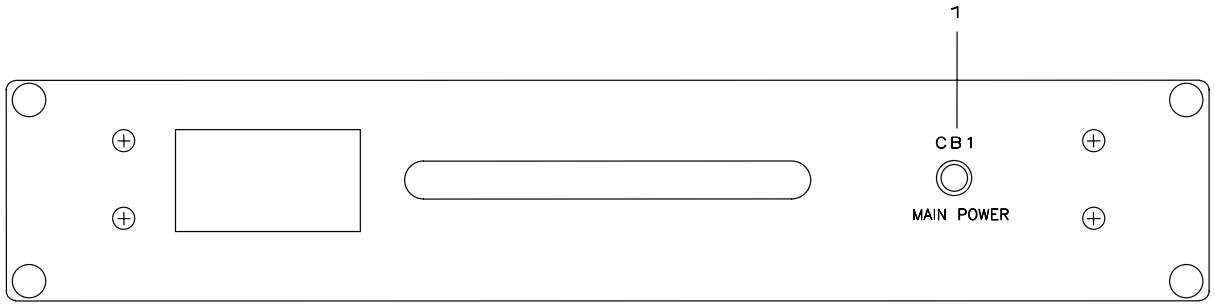


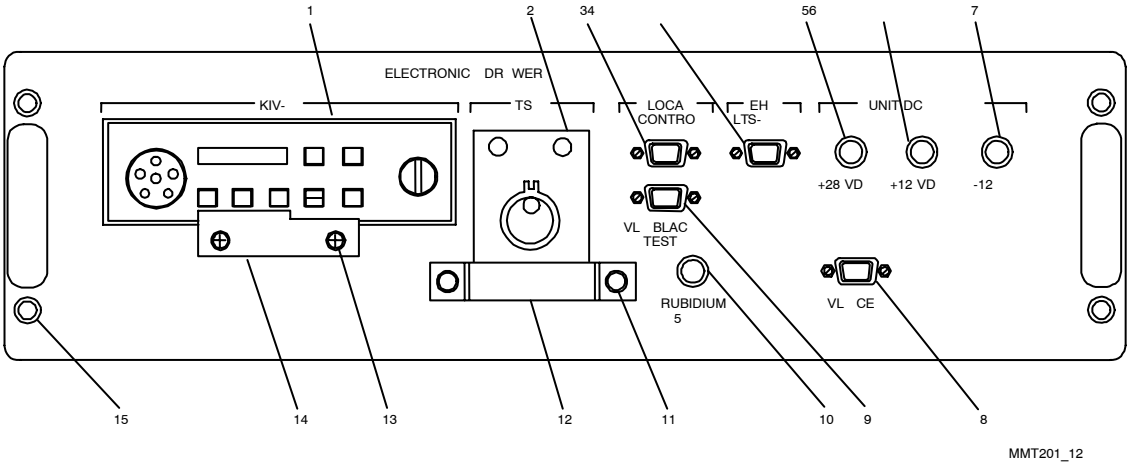
Figure 4-43C. EHF Antenna/Pedestal Assembly



NO.	CONTROL/INDICATOR	FUNCTION
1	MAIN POWER (CB1) circuit breaker	When closed, provides power to unit and 285 Vdc to EHF MILSTAR SSA located in the EHF antenna shelter.

SOURCE T.O. 21M-LGM30F-1-23

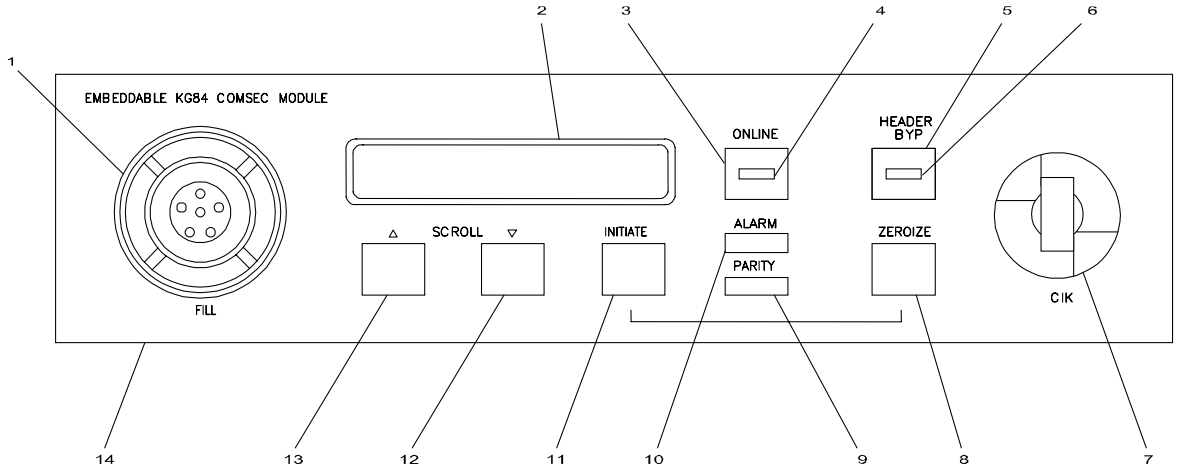
Figure 4-43D. AC/DC Converter



NO.	CONTROL/INDICATOR	FUNCTION
1	KIV-7 cryptographic module (see Figure 4-43F)	Contains keys used for encryption/decryption of EHF MILSTAR messages.
2	TSM port (shown with TSM installed)	Provides interface for Time Standard Module (TSM). TSM is a plug-in device used to set time during VLF/LF startup if EHF MILSTAR is shut down.
3	LOCAL CONTROL port	Provides interface for EHF laptop computer used for maintenance.
4	EHF LTS-PDR port	Provides interface for test equipment used by Contractor Logistics Support (CLS).
5	+28 VDC indicator (green)	Indicates +28 Vdc is present.
6	+12 VDC indicator (green)	Indicates +12 Vdc is present.
7	-12 VDC indicator (green)	Indicates -12 Vdc is present.
8	VLF CEP port	Provides interface for test equipment used by CLS.
9	VLF BLACK port	Provides interface for test equipment used by CLS.
10	RUBIDIUM 5 MHZ port	Provides interface for VLF System Test Set (VSTS) used for maintenance.
11	Thumbscrew	Secures TSM retaining bracket.
12	TSM retaining bracket	Secures TSM when installed in electronics drawer.
13	Screw	Secures KIV-7 retaining bracket.
14	KIV-7 retaining bracket	Secures KIV-7 in electronics drawer.
15	Captive screw	Secures A2 drawer to rack.

SOURCE T.O. 21M-LGM30F-1-23

Figure 4-43E. Electronics Drawer



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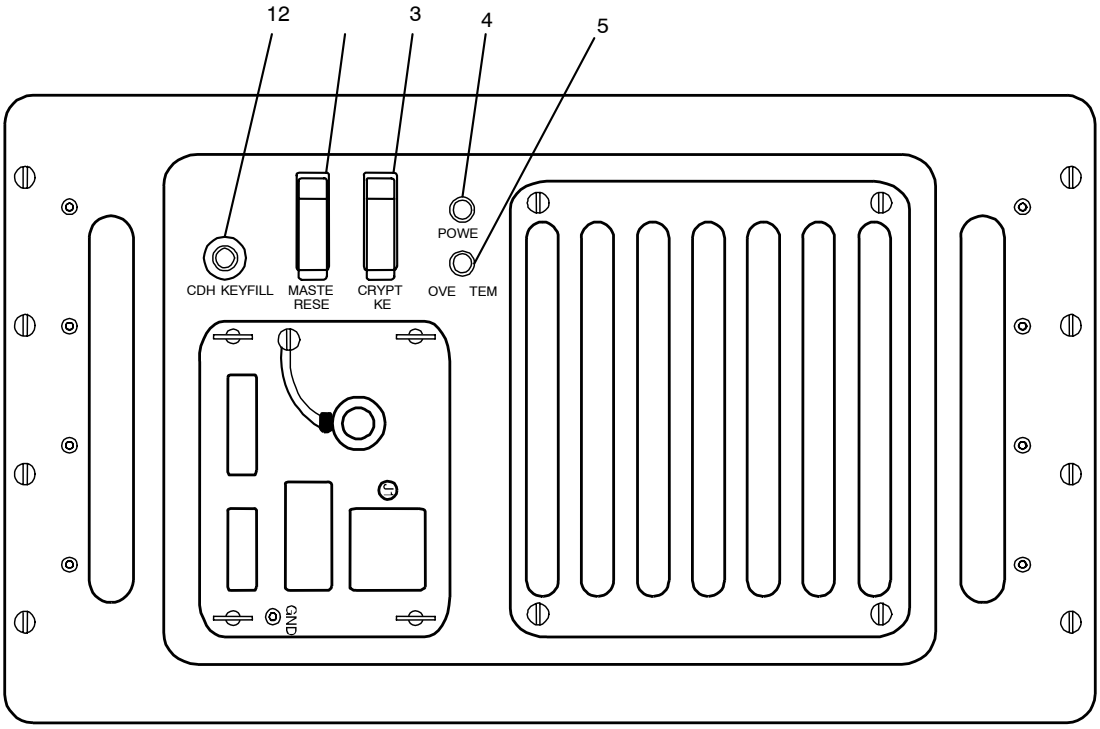
NO.	CONTROL/INDICATOR	FUNCTION
1	FILL connector	Permits connection of the KIV-7 with DS-101 and DS-102 (Common Fill) compatible key fill devices, including the AN/CYZ-10 Data Transfer Device (DTD).
2	Message display	Yellow, eight-character, alphanumeric display which conveys operational prompts, configuration selections, status messages, and error messages. Message viewing and selection is accomplished using the SCROLL ▲, SCROLL ▼, and INITIATE pushbuttons. Display intensity (high, medium, and low) is selectable.
3	ONLINE pushbutton	Toggles the KIV-7 between online secure data communication and offline noncommunicating state. If pressed during header bypass, preempts header bypass and initiates online secure data communication.
4	Online indicator (yellow)	Indicator on – synchronization is complete and the unit is in the secure data communication state. Indicator flashing – synchronization or resynchronization is in progress. At data rates greater than 1,200 bits per second, flashing is not noticeable.
5	HEADER BYPASS pushbutton	Initiates header bypass from the offline state; ignored otherwise. Header bypass terminates when preempted using the ONLINE pushbutton, or automatically when the header bypass limit is reached.
6	Header bypass indicator (red)	Indicator on – header bypass is in progress. Indicator blinking – alarm check is in progress.

Figure 4-43F. KIV–7 (Sheet 1 of 2)

NO.	CONTROL/INDICATOR	FUNCTION
7	CIK receptacle	Accepts a Cryto-Ignition Key (CIK) which is a small key-shaped memory device that is automatically initialized and managed by the KIV-7. Only one CIK may be associated with a given KIV-7; once initialized, the CIK is unique to that KIV-7. The CIK permits the KIV-7 to be treated as an UNCLASSIFIED CCI when the two are NOT collocated. Only authorized users who possess a valid CIK may access the operational features of the KIV-7.
8	ZEROIZE pushbutton	Zeroizes ALL internally stored keys when depressed simultaneously with the INITIATE pushbutton.
9	PARITY indicator (red)	Indicator on – a key parity error is present, or comes on with the ALARM indicator. Indicator blinking – key parity check is successful.
10	ALARM indicator (red)	Indicator on – a cryptographic alarm is present, the CIK is not valid or inserted properly, or all internally stored keys are zeroized. Indicator blinking – alarm check is in progress.
11	INITIATE pushbutton	Used to select entry in message display.
12	SCROLL ▼ pushbutton	Used to scroll down through message display entries.
13	SCROLL ▲ pushbutton	Used to scroll up through message display entries.
14	Speaker (internal)	Provides audible alert. One beep – inserted CIK is valid. Two beeps – synchronization is achieved. Continuous beeps – header bypass is in progress. Chirp – battery voltage is low. Click – front panel pushbutton switch is depressed.

SOURCE T.O. 21M-LGM30F-1-23

Figure 4-43F. KIV–7 (Sheet 2 of 2)



NO.	CONTROL/INDICATOR	FUNCTION
1	CDH KEYFILL port	Used to load cryptographic keys.
2	MASTER RESET switch	Three position switch. Setting switch to RESET (up position) restarts EHF MILSTAR system. During normal operation switch is set to normal (center position). RUN (down position) is not used.
3	CRYPTO KEY switch	Setting switch to SAVE (up position) saves keys already loaded into KGV-11. During normal operation, switch is set to normal (center position). Setting switch to ZEROIZE (down position) erases all keys in KGV-11 and TEU CDH crypto circuit card assemblies.
4	POWER indicator (green)	Comes on when AC power is applied to the TEU.
5	OVER TEMP indicator (red)	Comes on if over temperature condition exists in the TEU (fire isolation procedures are in appropriate weapon system T.O.). Turns off when over temperature condition no longer exists.

SOURCE T.O. 21M-LGM30F-1-23

Figure 4-43G. Terminal Electronics Unit

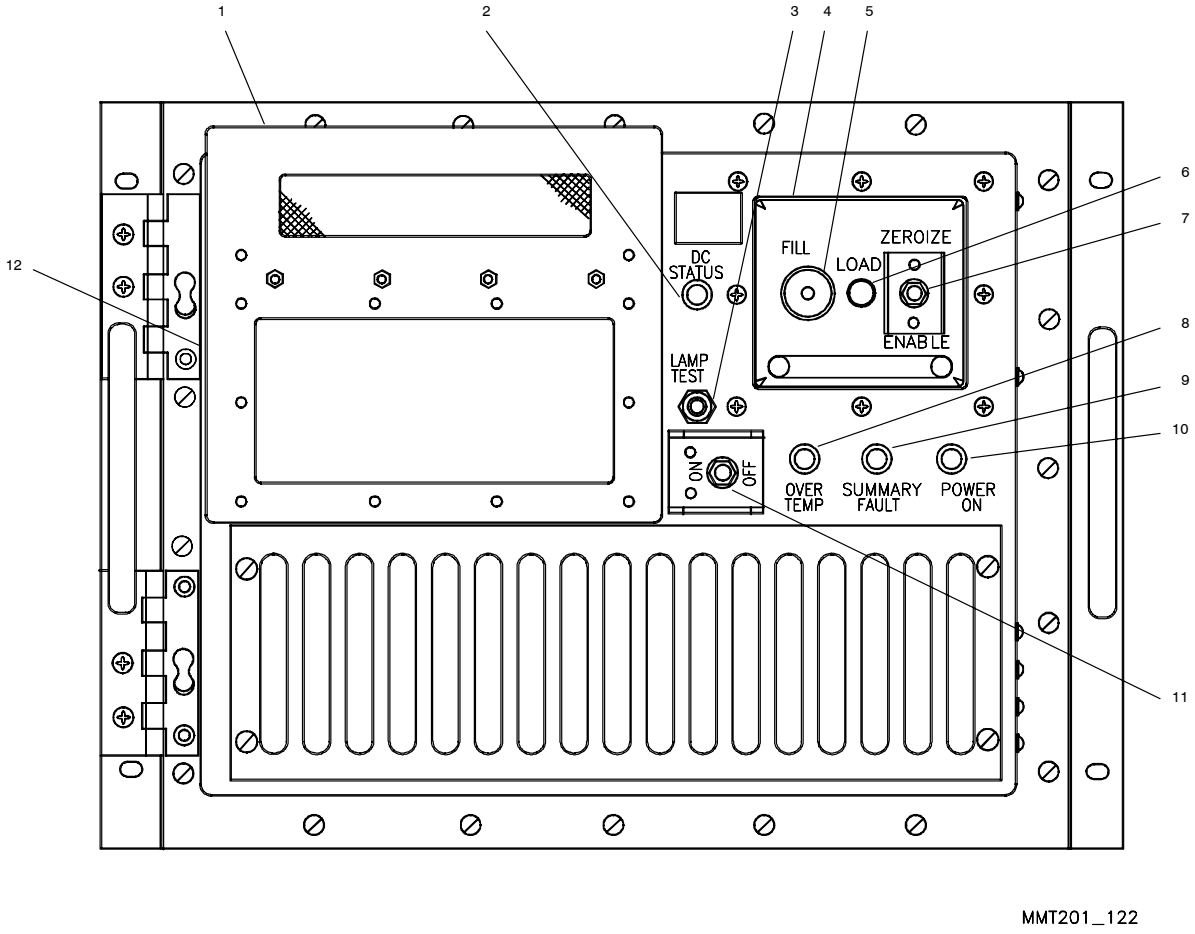
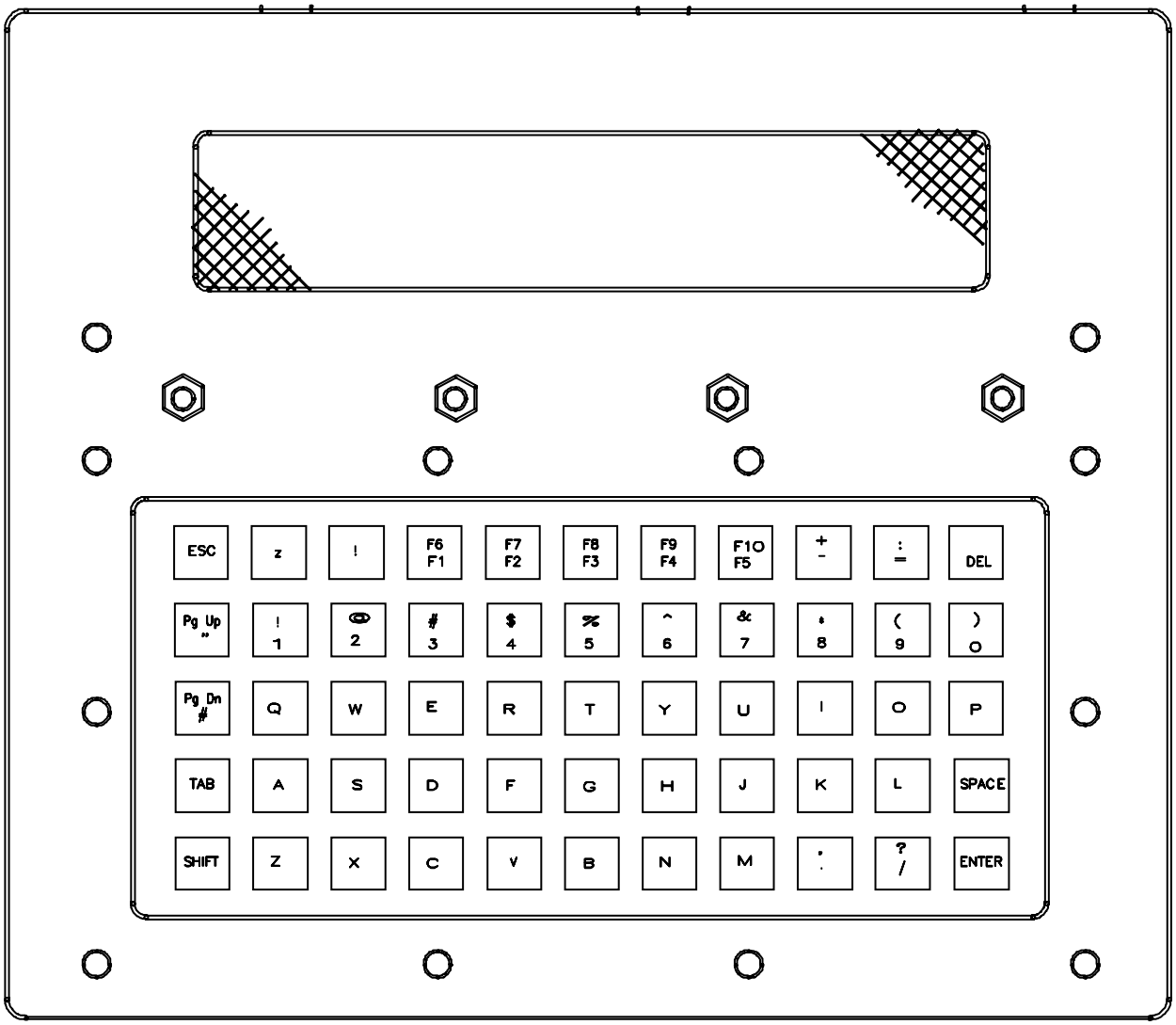


Figure 4-43H. VLF/LF Red (VME) Chassis (Sheet 1 of 2)

NO.	CONTROL/INDICATOR	FUNCTION
1	Local Control Device Module (see figure 4-43I)	Used to perform local control of VME and VXI chassis.
2	DC STATUS indicator (green)	Comes on when dc voltage is present in the VME Chassis.
3	LAMP TEST	When pressed, all chassis indicators come on except for the LOAD indicator and the DC STATUS indicator, which goes off. When released, DC STATUS indicator comes on, POWER ON indicator remains on, and all other indicators go off.
4	KOV-17-1 interface panel	Provide interface to internal KOV-17-1 CCA.
5	FILL connector	Connects to the Data Transfer Device (DTD) to allow loading of keys into the KOV-17-1.
6	LOAD indicator (red)	Momentarily comes on at completion of loading a group of keys from the DTD.
7	ZEROIZE/ENABLE switch	Toggle switch that erases all keys in the KOV-17-1.
8	OVER TEMP indicator (red)	Comes on if overtemperature condition exists in the chassis (fire isolation procedures are in appropriate weapon system T.O.). Cycles during startup.
9	SUMMARY FAULT indicator (red)	Flashes when hardware fault has been detected in chassis. Detailed fault information available at HA VDUs.
10	POWER ON indicator (green)	Comes on when power is applied to chassis.
11	ON/OFF switch	Turns VME chassis on/off.
12	Database memory card cover (tethered)	Covers access hole for database memory card.

SOURCE T.O. 21M-LGM30F-1-23

Figure 4-43H. VLF/LF Red (VME) Chassis (Sheet 2 of 2)



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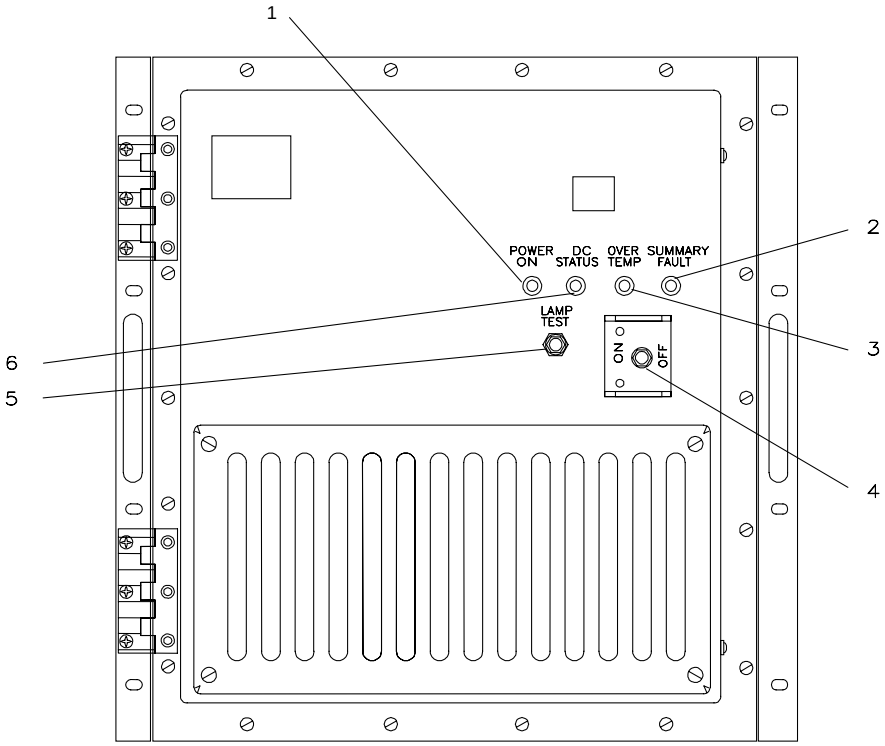
SOURCE T.O. 21M-LGM30F-1-23

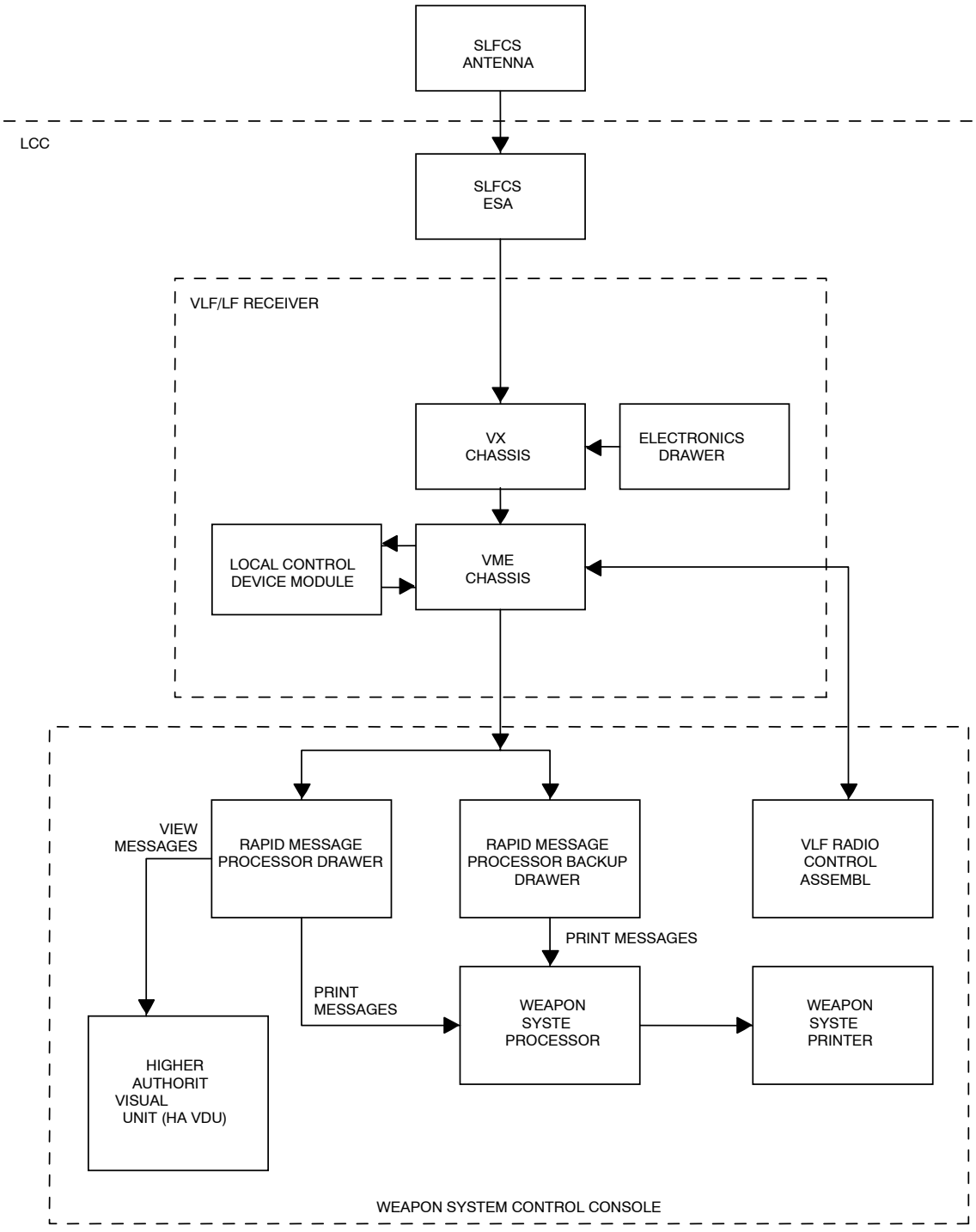
Figure 4-43I. Local Control Device Module



NO.	CONTROL/INDICATOR	FUNCTION
1	POWER ON indicator (green)	Comes on when power is applied to chassis.
2	SUMMARY FAULT indicator (red)	Flashes when hardware fault has been detected in chassis. Detailed fault information available at HA VDUs. Cycles during startup.
3	OVER TEMP indicator (red)	Comes on if overtemperature condition exists in the chassis (fire isolation procedures are in appropriate weapon system T.O.). Cycles during startup.
4	ON/OFF toggle switch	Controls power to chassis.
5	LAMP TEST pushbutton switch	When pressed, all chassis indicators come on except for the LOAD indicator and the DC STATUS indicator, which goes off. When released, DC STATUS indicator comes on, POWER ON indicator remains on, and all other indicators go off.
6	DC STATUS indicator (green)	Comes on when dc voltage is present in chassis.

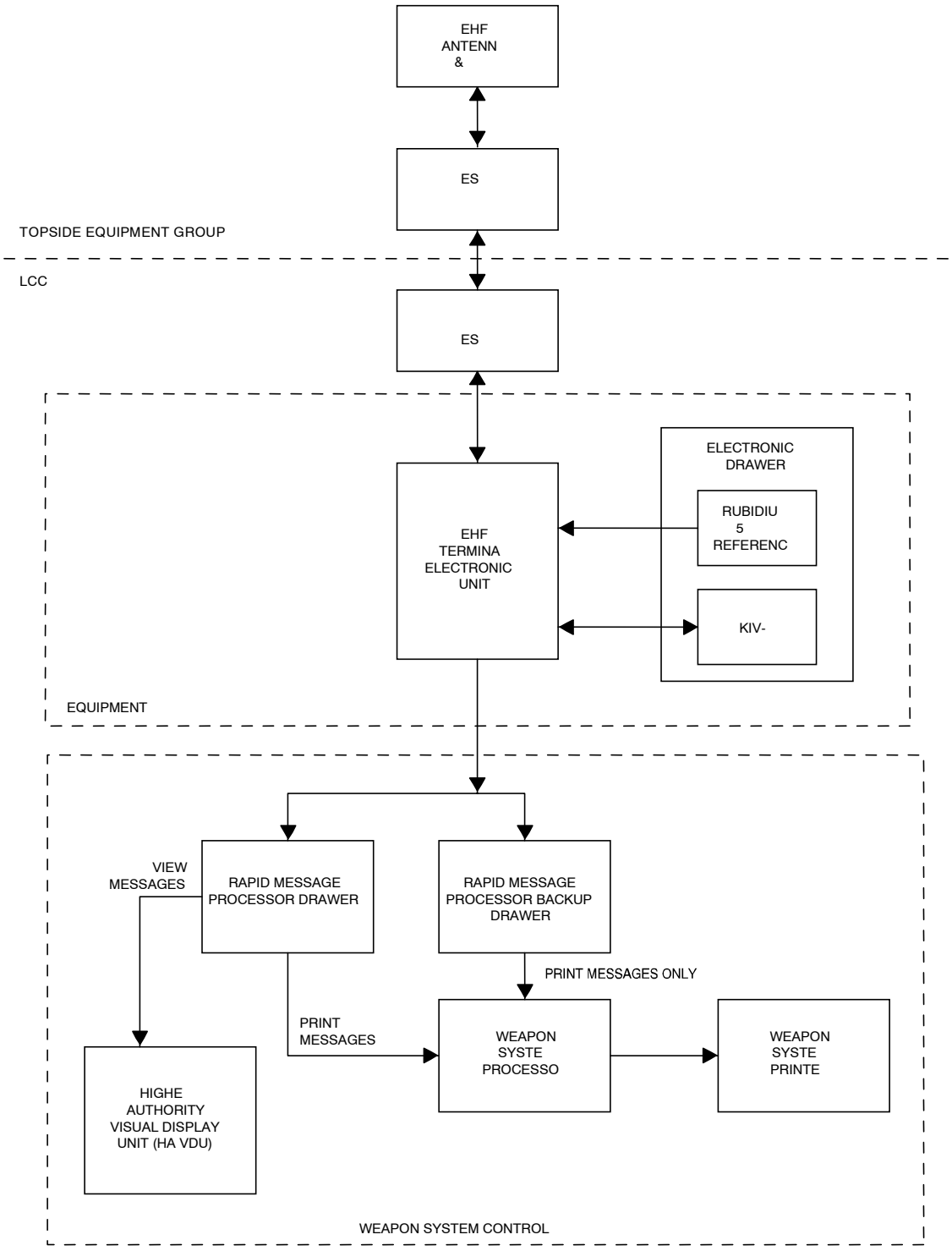
SOURCE T.O. 21M-LGM30F-1-23

Figure 4-43J. VLF/LF Black (VXI) Chassis



Source: T.O. 21M-LGM30F-2-5-5

Figure 4-44. SLFCS Functional Block Diagram



Source: T.O. 21M-LGM30F-2-5-5

Figure 4-45. EHF MILSTAR Functional Block Diagram

SECTION V - ELECTRONIC GROUND SYSTEMS

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SECTION V - ELECTRONIC GROUND SYSTEMS

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LIST OF ILLUSTRATIONS

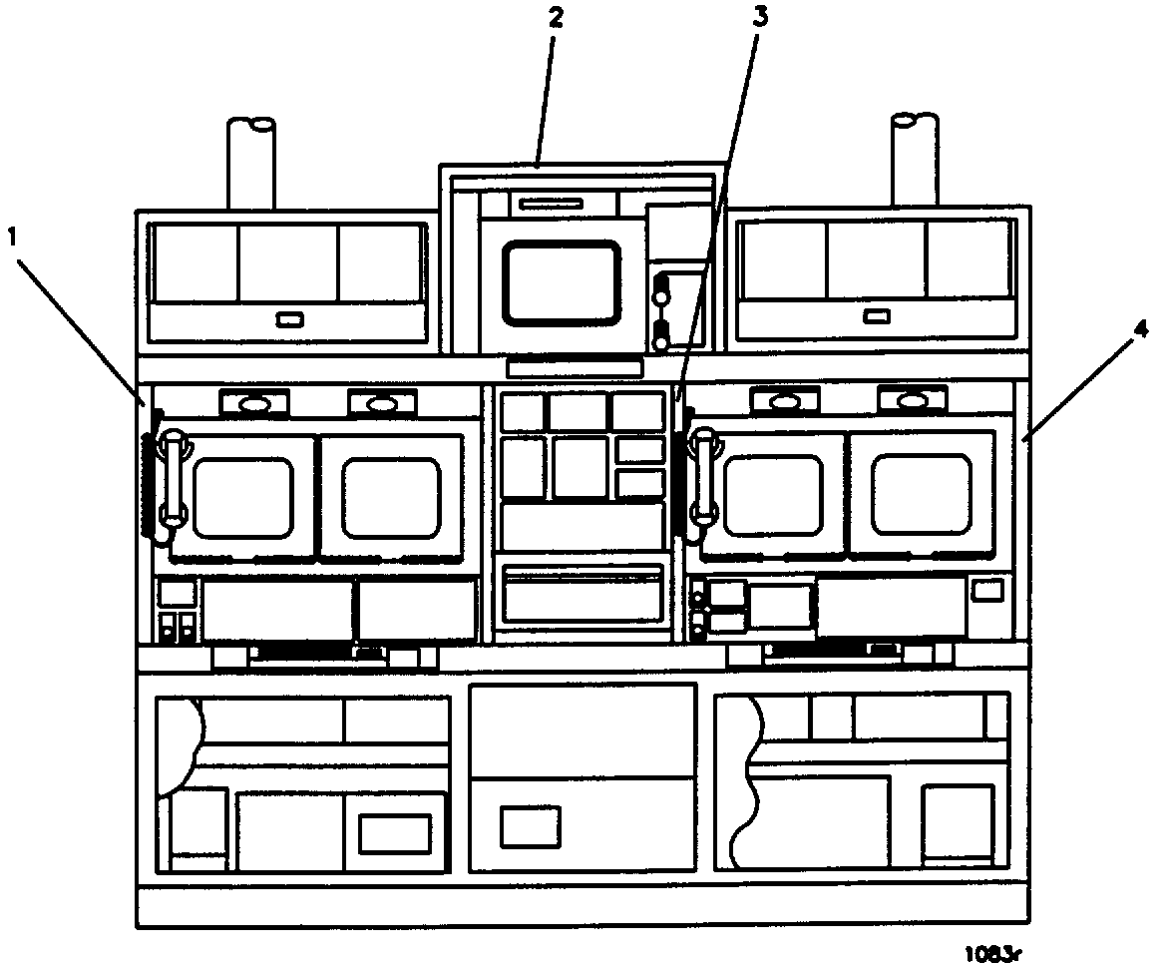
LIST OF ILLUSTRATIONS (Continued)

LIST OF TABLES

5-1. SCOPE. This section consists of a brief description of selected electronic ground system components. Illustrations showing the monitor and control elements including a brief description of their control functions are included.

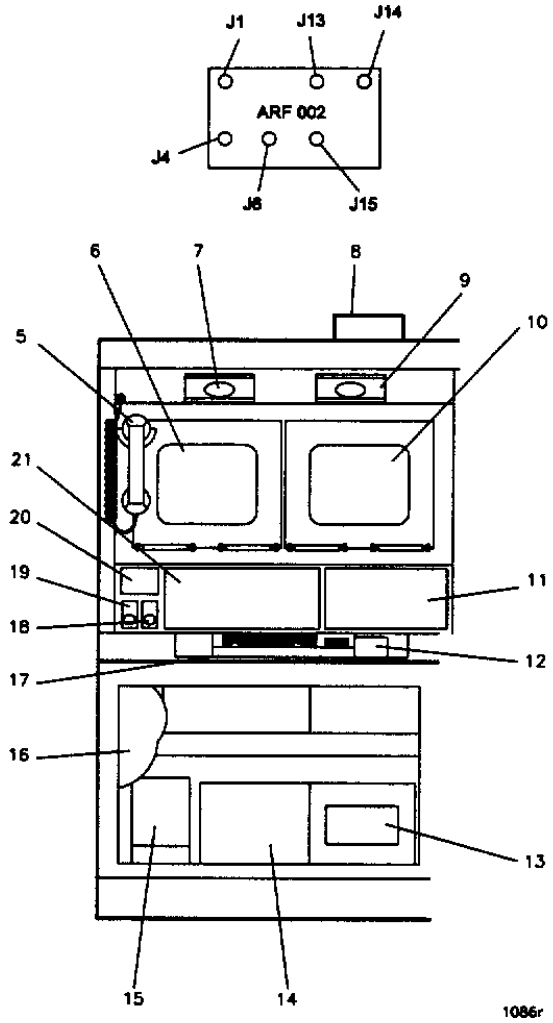
5-2. LCF OPERATIONAL GROUND EQUIPMENT.

5-2.1. Communications Control Console. (Figure 5-1/ARF 001). The REACT console is a dual-position console which serves as the normal duty station for the missile combat crew. The left and right bays of the console form the left (Commander) and right (Deputy) console workstations, with shared equipment in the center bay. Table 5-1 lists all reference designators, identified as ARF XXX, for the REACT console.



1 LEFT BAY, Commander (SEE SHEET 2)
2 CREW SUPPORT EQUIPMENT
3 CENTER BAY (SEE SHEET 3)
4 RIGHT BAY, Deputy (SEE SHEET 4)

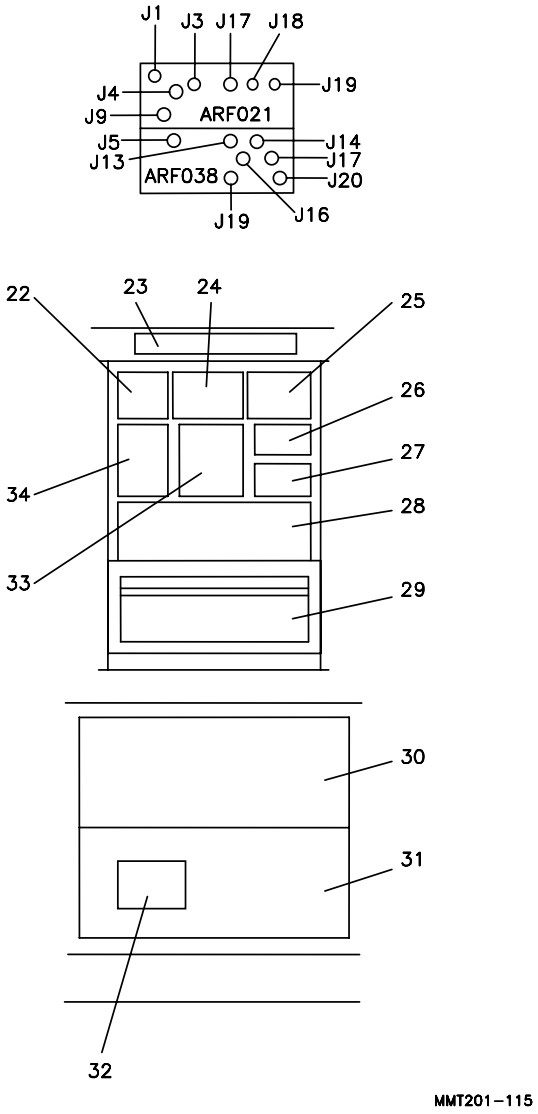
Figure 5-1. REACT Console Subassembly (Sheet 1 of 4)



LEFT BAY

5	TELEPHONE HANDSET
6	HA VISUAL DISPLAY UNIT (SEE FIGURE 5-2)
7	PAS SPEAKER (NOT IN USE)
8	VCP REPEATER
9	VCP SPEAKER
10	WS VISUAL DISPLAY UNIT (SEE FIGURE 5-2)
11	LAUNCH CONTROL PANEL (SEE FIGURE 5-5)
12	TRACKBALL ASSEMBLY (SEE FIGURE 5-3)
13	RMP BACKUP (SEE FIGURE 5-17)
14	BLANK PANEL
15	BULK STORAGE/LOADER (SEE FIGURE 5-8)
16	DOOR
17	KEYBOARD (SEE FIGURE 5-3)
18	MASTER ALARM RESET PUSHBUTTON (SEE FIGURE 5-7)
19	HEADSET JACK
20	COOPERATIVE LAUNCH SWITCH (SEE FIGURE 5-4)
21	VCP (SEE FIGURE 5-14)

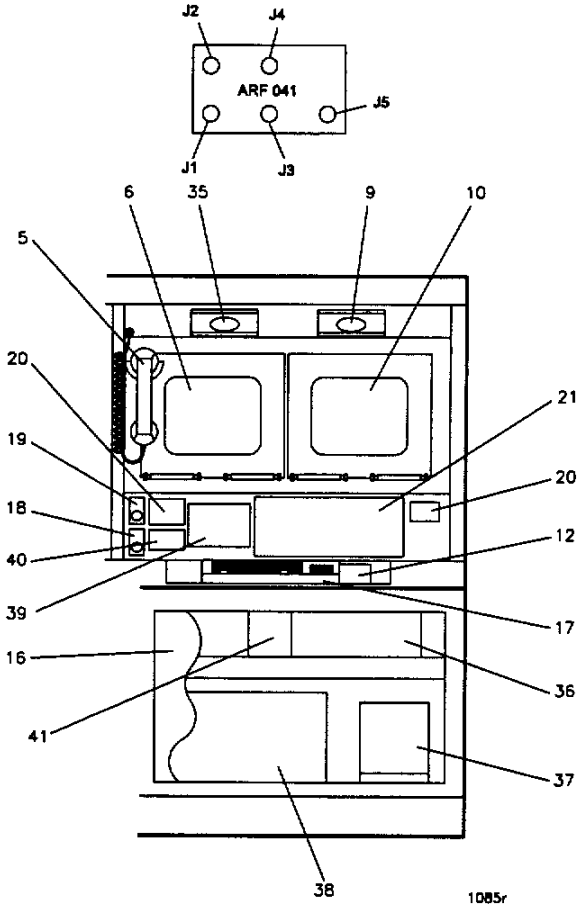
Figure 5-1. REACT Console Subassembly (Sheet 2 of 4)



CENTER BAY

22 BLANK PANEL
23 TIME OF DAY CLOCK (SEE FIGURE 5-10)
24 VLF RADIO CONTROL ASSEMBLY
25 BLANK PANEL
26 BLANK PANEL
27 BLANK PANEL
28 AUXILIARY ALARM PANEL (SEE FIGURE 5-11)
29 PRINTER (SEE FIGURE 5-12)
30 WEAPON SYSTEM PROCESSOR
31 RAPID MESSAGE PROCESSOR (SEE FIGURE 5-16)
32 JOURNAL MEMORY LOADER (SEE FIGURE 5-18)
33 UHF CONTROL PANEL (SEE FIGURE 5-15)
34 SATCOM CONTROL INDICATOR

Figure 5-1. REACT Console Subassembly (Sheet 3 of 4)



SOURCE T.O. 21M-LGM30G-1-22

RIGHT BAY

5	TELEPHONE HANDSET
6	HA VISUAL DISPLAY UNIT (SEE FIGURE 5-2)
9	VCP SPEAKER
10	WS VISUAL DISPLAY UNIT (SEE FIGURE 5-2)
12	TRACKBALL ASSEMBLY (SEE FIGURE 5-3)
16	DOOR
17	KEYBOARD (SEE FIGURE 5-3)
18	MASTER ALARM RESET PUSHBUTTON (SEE FIGURE 5-7)
19	HEADSET JACK
20	COOPERATIVE LAUNCH SWITCH (SEE FIGURE 5-4)
21	VCP (SEE FIGURE 5-14)
35	PAS SPEAKER (NOT IN USE)
36	FLOPPY DISK DRIVE (SEE FIGURE 5-9)
37	CODER-DECODER ASSEMBLY (SEE FIGURE 5-13)
38	CONSOLE POWER CONTROL AND DISTRIBUTION UNIT (SEE FIGURE 5-19)
39	LAUNCH ENABLE PANEL (SEE FIGURE 5-6)
40	SECURE VOICE PANEL
41	DIAGNOSTIC PORT

Figure 5-1. REACT Console Subassembly (Sheet 4 of 4)

Table 5-1. ARF Number to Common Name Cross Reference

ARF #	REFERENCE UNIT (COMMON NAME)	ACRONYM/ABBREVIATION
ARF 001	CONSOLE	
ARF 002	AUXILIARY I/O PANEL LEFT	
ARF 003	PRIMARY ALERT SYSTEM SPEAKER NAFH	PAS SPEAKER NAFH
ARF 004	VOICE CONTROL PANEL SPEAKER LEFT	VCP SPEAKER LEFT
ARF 005	HIGHER AUTHORITY VISUAL DISPLAY UNIT LEFT	HA VDU LEFT
ARF 006	WEAPON SYSTEM VISUAL DISPLAY UNIT LEFT	WS VDU LEFT
ARF 007	COOPERATIVE LAUNCH SWITCH LEFT	CLS LEFT
ARF 008	HEADSET JACK LEFT	
ARF 009	VOICE CONTROL PANEL LEFT	VCP LEFT
ARF 010	LAUNCH CONTROL PANEL	LCP
ARF 011	MASTER ALARM RESET SWITCH LEFT	MAR LEFT
ARF 012	WORKSHELF LEFT	
ARF 013	OPERATOR INPUT DEVICE LEFT A1 – KEYBOARD LEFT A2 – TRACKBALL LEFT	OID LEFT
ARF 014	BULK STORAGE/LOADER	BS/L
ARF 015	GROWTH LEFT	
ARF 016	RAPID MESSAGE PROCESSOR BACKUP	RMPB
ARF 017	RAPID MESSAGE PROCESSOR BACKUP I/O PLATE	RMPB I/O PLATE
ARF 018	AUXILIARY I/O PANEL BOTTOM LEFT	
ARF 019	ADAPTER PANEL (VDU) LEFT	
ARF 020	SPEAKER PANEL LEFT AND HANDSET JACK LEFT	
ARF 021	MAIN I/O PANEL UPPER	
ARF 022	VIDEO GROUP ASSEMBLY	
ARF 023	TIME OF DAY CLOCK	TODC
ARF 024	VCH AUDIO ALARM (GROWTH)	
ARF 025	VLF RADIO CONTROL ASSEMBLY	
ARF 026	AFSATCOM CONTROL HEAD	
ARF 027	DFMR DIGITAL RECEIVER RCU (GROWTH)	
ARF 028	DFMR GWEN RCU (GROWTH)	
ARF 029	SPEAKER AAP	
ARF 030	UHF CONTROL PANEL	UCP

Table 5-1. ARF Number to Common Name Cross Reference (Continued)

ARF #	REFERENCE UNIT (COMMON NAME)	ACRONYM/ABBREVIATION
ARF 031	AUXILIARY ALARM PANEL	AAP
	A1 - FACILITY ALARM CIRCUIT CARD	
	A2 - AUDIO ALARM CIRCUIT CARD	
ARF 032	PRINTER	PTR
ARF 033	WEAPON SYSTEM PROCESSOR	WSP
	A1 - ASYNCHRONOUS/SYNCHRONOUS (RMB32A) CIRCUIT CARD	RMB32A
	A2 - ASYNCHRONOUS/SYNCHRONOUS (RMB32A) CIRCUIT CARD	RMB32B
	A3 - SMALL COMPUTER SYSTEM INTERFACE CIRCUIT CARD	SCSI
	A4 - CDA/IPD INTERFACE CIRCUIT CARD	CDA/IPD INTERFACE
	A5 - SINGLE MODULE COMPUTER (SMC810) CIRCUIT CARD	SMC810
	A6 - EMBEDDED MEMORY ARRAY, DYNAMIC CIRCUIT CARD	EMAD
	A9 - VAX EXPANSION SYSTEM SUPPORT CIRCUIT CARD	VESS
	A10 - VDU CONTROLLER A CIRCUIT CARD	VDU CONTROLLER-A
	A11 - VDU CONTROLLER B CIRCUIT CARD	VDU CONTROLLER-B
	A12 - NED/PRINTER SWITCH CIRCUIT CARD	NED/PRINTER SWITCH
	A14 - BLACK DISCRETE CIRCUIT CARD	BDI
	A16 -CMPG B INTERFACE CIRCUIT CARD	CMPG B INTERFACE
	A17 - CMPG A INTERFACE CARD	CMPG A INTERFACE
	A18 - LCP INTERFACE CIRCUIT CARD	LCP INTERFACE
	A19 - LEP INTERFACE CIRCUIT CARD	LEP INTERFACE
	PSI - POWER SUPPLY	
ARF 034	RAPID MESSAGE PROCESSOR	RMP
ARF 035	SITE ADDRESS PLUG	SAP
ARF 036	WSP I/O PLATE	
ARF 037	RMP I/O PLATE	
ARF 038	MAIN I/O PANEL LOWER	
ARF 039	OID CABLE MOUNTING BRACKET LEFT	
ARF 040	BUS BAR LEFT	
ARF 041	AUXILIARY I/O PANEL RIGHT	
ARF 042	VALENCE	