TECHNICAL REFERENCE HANDBOOK

– SELECT –
SYSTEM ENGINEERING LEVEL EVALUATION CORRECTION TEAM WS133A

F04704-93-C-0020
CDRL C012
F42610-98-C-0001
SDRL A002

Prepared by

Integrated Defense System
3370 Miraloma
P.O. Box 3105
Anaheim, CA 92803-3105

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EQUIPMENT CONFIGURATION STATUS RECORD	
ECPs, TCTOs AND CONTRACTS AFFECTING THIS PUBLICATION ARE LISTED BELOW	
ECP/TCTO/CONTRACT NUMBER	**TITLE**
WS-133 A-M - Boe - 1941 TCTO 21M-LGM30F-1556 (F42600-87-C-2057)	Incorporate LCF Motor-Generator Set Replacement
WS-133 A-M - FEI-0001 TCTO 21M-LGM30-1393 TCTO 21M-LGM30F-1557 TCTO 21M-LGM30G-833 TCTO 31X4-1-660 (F42600-88-C-1344)	Incorporate Lithium Batteries in Wing V Launch Facilities
WS-133 A-M - FEI-0001 TCTO 21M-LGM30-1393C TCTO 21M-LGM30-1446 (F42600-88-C-1344)	Modification of Distribution Box, P/Ns 25-23468-237, -262, to Incorporate MESP Program Improvements
TCTO 21M-LGM30-1428 (F42600-90-C-1522)	Modification of 36 Amp Power Supply to Prevent Electrical Overstress in the LGM30/LG118A Missile Systems
TCTO 21M-LGM30-1449 (F42600-91-C-0010) EPR MM-92B-OE-14059	Launch Facility Conversion of Minuteman II to Minuteman III
RFE 9-7-38905 (F42610-91-C-0144)	Incorporate Replacement Control Monitor
21M-LGM30-1457 (F04704-91-C-0037)	System Level Modification of AM Launch Control Center
21M-LGM30-1468 (F04704-91-C-0037)	Modification of AM Connector Adapter Set, P/N 25-27488
21M-LGM30-1467 (F04704-91-C-0037)	Modification of AM Electrical Equipment Hoisting Unit, HLU-84/A, P/N 25-23490
21M-LGM30-1451 (F04704-91-C-0037)	Modification of AM Launch Control Center Operator Seat, P/N 25-79445
21M-LGM30-1456 (F04704-91-C-0037)	Modification of AM Command Message Processing Group, P/N 25-66170-57
21M-LGM-30-1452 (F04704-91-C-0037)	Modification of AM Power Distribution System, Distribution Box, P/N 25-27307
21M-LGM30-1453 (F04704-91-C-0037)	Modification of AM Power Supply Group, P/N 25-24197
21M-LGM30-1455 (F04704-91-C-0037)	Modification of AM Launch Control Facility Environmental Control Systems
21M-LGM30-1466 (F04704-91-C-0037)	Modification of AM Interconnecting Box (I-box), P/N 25-29556

EQUIPMENT CONFIGURATION STATUS RECORD	
ECPs, TCTOs AND CONTRACTS AFFECTING THIS PUBLICATION ARE LISTED BELOW	
ECP/TCTO/CONTRACT NUMBER	**TITLE**
21M-LGM30-1457 (F42610-92-D-0058)	System Level Modification of AM Launch Control Center (REACT)
21M-LGM30-1526 (F42610-93-C-0048)	Modification of LF Cable Set (fig A 1248) and Installation of Switch Box for Wings I, III, V and VAFB (CI 05202AA)
F04704-93-C-0020	Guidance Replacement Program which updates missile guidance set to NS50A configuration
TCTO 21M-LGM30-1561 (F42610-98-C-0001)	Replacement of the Expanded Missile Data Analysis System (EMDAS) Inertial Measurement Unit Performance Data (IPD) Drawer (CI0017791)
TCTO 21M-LGM30-1565 (F42610-98-C-0001)	Modification to Missile Alert Facilities (MAFs) to Incorporate the Minuteman MEECN Program (MMP) – Wing I AM System and VAFB site 01A
TCTO 21M-LGM30-1566 (F46210-98-C-0001)	Modification to Missile Alert Facilities (MAFs) to Incorporate the Minuteman MEECN Program (MMP) – Wing III and V and Hill AFB AM System SMIC
TCTO 21M-LGM30-1569 (F46210-98-C-0001)	Modification to Missile Alert Facilities (MAFs) to Incorporate the Minuteman MEECN Program (MMP) – HAC/RMPE

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INTRODUCTION

This manual provides pertinent Minuteman (WS133A) technical data in a convenient form for use by the Systems Engineering Level Evaluation Correction Team (SELECT). The data is presented in a form that assumes the user possesses an extensive knowledge of overall weapon system operation. A minimum explanation of material is included. The data has been compiled to provide a technical reference for in depth investigation of technical problems which are beyond the capabilities provided with the operational weapon system.

This manual is printed and distributed in accordance with OOALC Regulation 66-19 on a restricted basis. SELECT members and a limited number of support personnel are issued copies. Revisions will be forwarded according to the most recent mailing data supplied by manual holders. Change of address, requests to include specific data in the manual, and information concerning corrections should be coordinated with OOALC/SELECT.

MINUTEMAN OPERATIONAL WING CODING. Code symbols are used in this manual to show which information is applicable to a particular wing or group of wings. When code symbols appear in paragraph titles, illustration titles, illustrations or procedural steps, the information applies only to the wing represented by the code symbol. Where no coding appears, the information is applicable to all wings and squadrons covered in this manual. The following coding symbols are used:

[1]	Wing I (Squadrons 1, 2 and 3), Malmstrom Air Force Base
[3]	Wing III, Minot Air Force Base
[5]	Wing V (Squadrons 1, 2 and 3), F. E. Warren Air Force Base
[ACP]	Wing Alternate Command Post **[3]** LCC I, **[5]** LCC T, **[1]** LCC T
[SCP]	Squadron Command Post **[3]** LCCs C, M, **[5]** LCCs A, I, O, **[1]** LCCs A, G, K
>	"THRU" or "AND ON"
<	End of coded information (when required)

In addition to the above, certain data in this manual is applicable to Wings I, III and V configured sites at Vandenberg AFB (VAFB). The following coding is used to indicate VAFB effectivity:

[0]	Vandenberg AFB
[04]	Launch Facility 04
[09]	Launch Facility 09
[10]	Launch Facility 10
[01A]	Launch Control Facility 01A

FLAGNOTES. The symbol __ or **[>** is used in figures to list clarification data.

RELEVANT DOCUMENTATION. A listing of data related to Wings I, III and V equipment and/or operation is provided in Table 1. This data should be used, in addition to this manual, to provide a more complete or more detailed description of an operation or piece of equipment. The listing is limited to those documents most likely to be needed and is not intended to be a complete listing of all available documentation.

SOURCE DATA/REFERENCES. A listing of data used to compile this manual is provided in Table 2. Throughout the manual, illustrations used directly from another source without modification of its technical content are listed as "SOURCE" data in the appropriate illustrations. When an illustration was prepared especially for this manual or an illustration from another source was modified for use in this manual, its source is identified on the appropriate illustration as a "REFERENCE." Table 2 lists both source and reference data, including the revision number/letter of the data used. All data referenced in Table 2 is also included in Table 1.

ABBREVIATIONS AND ACRONYMS. A listing of abbreviations and acronyms used in this manual is provided in Table 3.

DOCUMENT ORGANIZATION. In most cases, figures and tables in this document are located within the text. Each figure number and table number is prefaced by the section number in which it is located (Figure 3-4 is the fourth figure in Section III). To assist in printing and assembling this manual, figures longer than 17 inches have been grouped at the back of each section. An "FO" designator preceding the figure number in the text indicates that the particular figure is a foldout and will be found at the back of that section.

Table 1. Relevant Data

AIR FORCE TECHNICAL ORDERS GENERAL		WING EFFECTIVITY
00-25-107	Technical Manual Maintenance Assistance	[0] [1] [3] [5]
21M-LGM30F-01	List of Applicable Publications	[0] [1] [3] [5]
21M-LGM30F-06-1	Airborne Missile Equipment - LGM30	[0] [1] [3] [5]
21M-LGM30F-12	Safety and EMI Provisions	[0] [1] [3] [5]
WEAPON SYSTEM OPERATION INSTRUCTIONS		
21M-LGM30F-1-15	Operational Training Launch	[0]
21M-LGM30F-1-23	Communications & Ancillary Equipment	[0] [1] [3] [5]
21M-LGM30G-1-1	Minuteman Weapon System Description	[3] [5]
21M-LGM30G-1-17	Improved Simulated Electrical Launch, MM	[0] [1] [3] [5]
21M-LGM30G-1-22	Weapon System Operating Instructions	[3] [5]
21M-LGM30G-1-24	Weapon System Operating Instructions	[0] [1]
ORGANIZATIONAL MAINTENANCE INSTRUCTIONS		
21M-LGM30F-2-2-1	Missile Handling and Transportation	[0] [1] [3] [5]
21M-LGM30F-2-4-3	LF Security System	[3] [5]
21M-LGM30F-2-4-4	LF Security System	[1]
21M-LGM30F-2-4-4-1	LF Security System (Secret Supplement)	[1]
21M-LGM30F-2-5-4	Communications Systems	[0] [1] [3] [5]
21M-LGM30F-2-5-5	Communications Systems (Radio)	[0] [1] [3] [5]
21M-LGM30F-2-5-6	Communications Systems (Missile Control)	[0] [1] [3] [5]
21M-LGM30F-2-5-7	Communications Systems (HICS Pressure Monitor System)	[1] [3] [5]
21M-LGM30F-2-5-9	Antenna/Pedestal Assembly	[0] [1] [3] [5]
21M-LGM30F-2-5-10	Terminal Electronics Unit	[0] [1] [3] [5]
21M-LGM30F-2-5-11	Very Low Frequency/Low Frequency Receiver	[0] [1] [3] [5]
21M-LGM30F-2-5-13	Local Control Device	[0] [1] [3] [5]
21M-LGM30F-2-7-4	LF and MAF Environmental Control System	[0]
21M-LGM30F-2-7-10	LF Environmental Control System	[1]
21M-LGM30F-2-7-12	LCF Environmental Control System	[1]
21M-LGM30F-2-12-3	Computer Program Loading and Command & Status System Maintenance	[1]
21M-LGM30F-2-17-1	OTL Missile Roll Transfer	[0]
21M-LGM30F-2-17-2	OTL Integration and Checkout of G&C Section and Instrumentation Section	[0]
21M-LGM30F-2-17-3	Operational Test Launch Systems Preparation	[0]
21M-LGM30F-2-17-4	Operational Training Launch Systems	[0]
21M-LGM30F-2-17-5	Missile and PSRE Modification	[0]
21M-LGM30F-2-17-9	OTL Electro-Mechanical Systems Procedures	[0]
21M-LGM30F-2-19	LF Personnel Access Systems	[0] [1] [3] [5]
21M-LGM30F-2-20-1	Hardened Intersite Cable System	[0] [1] [3] [5]
21M-LGM20F-2-21-8	LF & MAF Intrasite Cabling	[1]
21M-LGM30F-2-23	Hard LF Antenna System	[0] [1] [3] [5]
21M-LGM30F-101	LGM30 Weapon System Corrosion Control and Treatment	[0] [1] [3] [5]
21M-LGM30F-102	Minuteman Operational Capability and Characteristics (Secret Supplement)	[0] [1] [3] [5]
21M-LGM30F-112	General Inspection & Repair Procedures	[1] [3] [5]
21M-LGM30F-6	Scheduled Inspection and Maintenance Requirements	[0] [1] [3] [5]
21M-LGM30G-2-1-7	Organizational Maintenance Control	[0] [3] [5]
21M-LGM30G-2-1-8	Organizational Maintenance Control	[0] [1]
21M-LGM30G-2-4	LF Security System	[1] [3] [5]
21M-LGM30G-2-6	Ground Guidance and Control Liquid Cooling System	[0] [1] [3] [5]
21M-LGM30G-2-7-4	LF Environmental Control System	[3] [5]
21M-LGM30G-2-7-5	MAF Environmental Control System	[3] [5]

Table 1. Relevant Data (Continued)

ORGANIZATIONAL MAINTENANCE INSTRUCTIONS (Continued)		WING EFFECTIVITY
21M-LGM30G-2-8	Payload Transporter Operations for AVE	[0] [1] [3] [5]
21M-LGM30G-2-10	LF and Support Building Procedures	[0] [1] [3] [5]
21M-LGM30G-2-11	Power Subsystems	[0] [1] [3] [5]
21M-LGM30G-2-12-2	Computer Program Loading and Command Status System Maintenance	[0] [1] [3] [5]
21M-LGM30G-2-12-4	Launch Control Facility Command and Control Equipment	[0] [1] [3] [5]
21M-LGM30G-2-18	Refurbishment Procedures - CTL	[0]
21M-LGM30G-2-21-3	LF and MAF Intrasite Cabling	[3] [5]
21M-LGM30G-2-21-5	LF and MAF Intrasite Cabling	[0]
21M-LGM30G-2-22	Umbilicals and Missile Suspension	[0] [1] [3] [5]
21M-LGM30G-2-28	Ancillary Mechanical Systems	[1] [3] [5]
21M-LGM30G-2-29	UHF Command Radio and EMP Hardened Antenna Systems, Depot Mobile Team Maintenance	[0] [1] [3] [5]
21M-LGM30G-2-30	LER Shock Isolation System, Launcher Closure Actuating and Locking Mechanism, Missile Support Suspension and Alignment System	[1] [3] [5]
21M-LGM30G-2-31	Weapon System Hardness Preservation and Installation Hardware	[1] [3] [5]

GROUND ELECTRICAL AND ELECTRONIC EQUIPMENT		WING EFFECTIVITY
31R3-4-24-2	Guidance and Control Coupler (C604)	[0] [1] [3] [5]
31X2-24-31-2	Code Change-Verifier/Verifier Simulator	[0] [1] [3] [5]
31X2-32-3-2	Data Analysis Central (AN/GYK-1)	[0] [1] [3] [5]
31X2-56-8-1	Connector Adapter Set	[0] [1] [3] [5]
31X3-12-13-2	Programmer Group	[1] [3]
31X3-27-6-3	Command Signals Decoder (KY-412/GYK-2)	[0] [1] [3] [5]
31X3-31-9-2	Receiver-Transmitter Alarm Set	[1] [3] [5]
31X4-1-142	Wire Assemblies & Electrical Surge Arrestors	[0] [1] [3] [5]
31X8-2-2-1	Wing Code Processing System	[0] [1] [3] [5]
31X8-2-2-2	Wing Code Processing System	[0] [1] [3] [5]
33D9-29-14-1	Fault Locating Indicator	[0] [1] [3] [5]
33D9-38-15-21	Explosive Set Circuitry Test Set	[0] [1] [3] [5]
33D9-54-100-1	Nuclear Certification Test Station	[1] [3] [5]
33D9-61-51-1	Inertial Performance Data Collection System Terminal Processor Group	[0] [1] [3] [5]
33D9-61-57-21-1	Operating Instructions for HP-ATS-E35	[0] [1] [3] [5]
33D9-61-58-2	Repair of OGE and Programmer Group Test Set	[0] [1] [3] [5]
33D9-61-96-2	Radio Frequency Test Set Launch Support System (LSS)	[0] [1] [3] [5]
33D9-74-42-2	Portable IPD MODEM	[0] [1] [3] [5]
33D9-111-35-2	Controller-Monitor	[0] [1] [3] [5]
33M1-1-101	Miscellaneous Systems	[0] [1] [3] [5]

Table 1. Relevant Data (Continued)

ILLUSTRATED PARTS BREAKDOWN (IPB)		WING EFFECTIVITY
21M-LGM30F-4-1	Introduction and Pictorial, Numerical and Reference Designation Indices for 21M-LGM30F- 4 Series IPBs	[0] [1] [3] [5]
21M-LGM30F-4-1-1	LGM30 Weapon System - OTL	[0]
21M-LGM30F-4-1-2	AGE, VAFB and All Wings (SECRET)	[0] [1] [3] [5]
21M-LGM30F-4-2	Operational Ground Equipment (Unique)	[0] [1] [3] [5]
21M-LGM30F-4-2-1	Guidance Control System (IPB)	[0] [1] [3] [5]
21M-LGM30F-4-4	Maintenance Ground Equipment (Common)	[0] [1] [3] [5]
21M-LGM30F-4-5	Maintenance Ground Equipment (Unique)	[0] [1] [3] [5]
21M-LGM30F-4-7	OGE (Common) and Missile Parts Limited to LF Maintenance	[0] [1] [3] [5]
21M-LGM30F-4-8	LGM30G and LG118A Hardened Intersite Cable System Components	[0] [1] [3] [5]

Table 1. Relevant Data (Continued)

AIR FORCE SYSTEM MANUALS

CEM 21-SM80A-2-21-1	Power Generation and Distribution	**[01A] [04]**
CEM 21-SM80A-2-21-1-1	Power Generation and Distribution	**[04]**
CEM 21-SM80A-2-21-2	Power Generation and Distribution	**[1]**
CEM 21-SM80A-2-26-1	Miscellaneous Systems	**[01A]**
CEM 21-SM80A-2-26-2	Miscellaneous Systems	**[1]**
CEM 21-SM80B-2-21-2	Power Generation and Distribution	**[3]**
CEM 21-SM80B-2-21-4	Power Generation and Distribution	**[5]**
CEM 21-SM80B-2-21-5	Power Generation and Distribution	**[09]**
CEM 21-SM80B-2-21-5-2	Power Generation and Distribution	**[10]**
CEM 21-SM80B-2-26-2	Miscellaneous Systems	**[3]**
CEM 21-SM80B-2-26-4	Miscellaneous Systems	**[5]**
CEM 21-SM80B-2-26-5	Miscellaneous Systems	**[09] [10]**
CEM 35R-1-451-1	Power Generation and Distribution	**[01A] [04]**
CEM 35R-1-451-2	Power Generation and Distribution	**[1]**
CEM 35R-1-481-1	Miscellaneous Systems	**[01A] [04]**
CEM 35R-1-551-2	Power Generation and Distribution	**[3]**
CEM 35R-1-551-4	Power Generation and Distribution	**[5]**
CEM 35R-1-551-5	Power Generation and Distribution	**[09]**
CEM 35R-1-551-5-2	Power Generation and Distribution	**[10]**
CEM 35R-1-581-2	Miscellaneous Systems	**[3]**
CEM 35R-1-581-4	Miscellaneous Systems	**[5]**
CEM 35R-1-581-5	Miscellaneous Systems	**[09] [10]**

INTERFACE CONTROL DRAWINGS

OO-ALC Report 62-46-1	Minuteman Interface Control Drawings
D25-65000, Vol. IX	LF Operations - Programming and Timing - D37 (B0/AN), APPENDIX I, GRP
D25-65002, Vol. V	LCF Operations/LF Intertie - Programming and Timing (BO/TRW-S)
D25-65043	Secure Data Unit/Universal Interfaces - Mechanical, Electrical and Signal Timing (BO/SYL/TRW-S/UN)
D25-92851	EHF and VLF/LF HAC Systems Equipment Rack to EHF ESA Units Electrical – Raytheon/Boeing
D25-92852	EHF and VLF/LF HAC Systems Equipment Rack to the LCC – Mechanical, Electrical, Cooling – Raytheon/Boeing/General Dynamics
D25-92853	Higher Authority Communications Integration and Control and Rapid Message Processing Element (HAC/RMPE) to the EHF Terminal Programming and Timing/Electrical – Raytheon/General Dynamics/Boeing/Lockheed Martin
D25-92854	Higher Authority Communications Integration and Control and Rapid Message Processing Element (HAC/RMPE) to the VLF/LF Terminal Programming and Timing/Electrical – Raytheon/General Dynamics/Boeing/Lockheed Martin
D25-92855	EHF Antenna Radome Heater ESA to LCC Power Electrical – GD-CS/Boeing
D25-92856	EHF and VLF/LF HAC Systems Equipment Rack to the VLF/LF ESA-HAC Electrical – Raytheon/Boeing/Westinghouse
C-2250	ALCC Operation to WS-133A-M/B, Launch Facility Intertie - Program and Timing (BO/SYL/AN/OOALC)
25-R001	Rack, Electrical Equipment, MT-6900(V)1/G, Computer, Digital, CP-2076(V)1/GSW, and Console Operations Program to Command Message Processing Group and Digital Data Group - Electrical, Programming and Timing - Loral/OO-ALC
25-R017	Rack, Electrical Equipment, Mt-6900(V)/G, Computer, Digital, CP-2076(V)/GSW and Console Operations Program to Inertial Measurement Unit Performance Data Processor Unit - Electrical, Programming and Timing - Loral/OO-ALC

Table 1. Relevant Data (Continued)

INTERFACE CONTROL DRAWINGS (Continued)

25-R030	Higher Authority Communications Integration and Control and Rapid Message Processing Element (HAC/RMPE) of the Rapid Execution and Combat Targeting (REACT) Program to Console, Weapon System Control, OJ-673(V)/GSW, Digital Interfaces - Programming and Timing, Electrical - GTE/Loral
25-R036	Missile Combat Crew Member to REACT Segment - Human Machine Interface - Loral/GTE/ESC/AFSPACECOM
25-R048	Transfer Unit, Programmable Cartridge, MU-1042/GSW to Wing Code Processing System - Mechanical, Electrical, Programming and Timing, Environmental - Loral/AUC
25-R050	Rapid Execution and Combat Targeting Console, Weapon System Control, OJ-673(V)/GSW Programs and Databases to Wing Code Processing System - Programming, Sizing and Data Format - Loral/AUC/AFSPACECOM
25-R055	Higher Authority Communications Integration and Control and Rapid Message Processing Element (HAC/RMPE) of the Rapid Execution and Combat Targeting (REACT) Program to Console, Weapon System Control, OJ-673(V)/GSW - Electrical Power, Mechanical, Envelope, Environmental - Loral/GTE
25-R059, Vol. I & II	Console, Weapon System Control, OJ-673(V)/GSW Components - Mechanical, Envelope, Electrical, Environmental, Programming and Timing - Loral/Logicon
25-R060	Console Operations Program, Transfer Unit, Programmable Cartridge, MU-1042/GSW and Disk Drive Unit, MU-1043/GSW to Wing Code Processing System - Programming - Loral/AUC

SYSTEM DIAGRAMS

21-52700	Master Index - Functional Signal Flow Diagrams
21-52707 SH 1	Communications System Block Diagrams
21-52707 SH 2	Communications System Functionals
21-52709 SH 2	Autonetics AGE
21-52711	Operational Wing I Support Systems
21-52717 SH 2	Programmer Group Detail Circuit Schematics
21-52743	Operational Support Systems Wing III
21-52747	System Diagrams - AVE (LGM-30G)
21-52751	Command and Status LCF OGE
21-52752	Command and Status LF OGE
21-52755	Operational Support Systems Wing V
21-52772	Major Signal Flow Diagrams, Security Systems

SYSTEM SPECIFICATIONS

S-133-128B	Minuteman III, Wings I, III and V Weapon System Specification (SECRET)
S-133-05204	Prime Item Development Specification for MAF Topside Equipment Group (CI 005204)
S-133-05206	Prime Item Development Specification for LCC Electrical Surge Arrestor (ESA) Assembly Set, CI 05206
S-133-05207	Prime Item Development Specification for EHF and VLF/LF HAC Systems (CI 005207)
S-133-09259	System Segment Specification for EHF and VLF/LF Higher Authority Communications Systems
S-133-19251	Software Requirement Specification for the Operational Ground Program of the Minuteman III Guidance Replacement Program
S-133-30001A	Prime Item Development Specification for Weapon System Control Element (WSCE) of Rapid Execution and Combat Targeting (REACT) Segment
S-133-36000B	Software Requirements Specification for the Console Operations Program (COP)

Table 2. Bibliography

AIR FORCE TECHNICAL ORDERS

21M-LGM30F-1-18	Change 20 dated 15 July 1992
21M-LGM30F-1-22	Change 15 dated 11 January 1993 **[1>**
21M-LGM30F-2-5-7	Change 11 dated 23 November 1992 **[1>**
21M-LGM30F-2-12-3	Change 8 dated 16 October 1992
21M-LGM30F-2-17-3	Change 28 dated 09 November 1992
21M-LGM30F-2-20-1	Change 20 dated 15 November 1992
21M-LGM30F-2-21-8	Change 43 dated 29 January 1993
21M-LGM30G-1-14	Change 22 dated 30 November 1992
21M-LGM30G-1-15	Change 22 dated 06 November 1992 **[1>**
21M-LGM30G-1-17	Change 12 dated 24 February 1993 **[1>**
21M-LGM30G-1-22	Change 0 dated 17 June 1994
21M-LGM30G-2-1-5	Change 35 dated 24 February 1993 **[1>**
21M-LGM30G-2-6	Change 78 dated 12 February 1993
21M-LGM30G-2-11	Change 104 dated 25 November 1992 **[1>**
21M-LGM30G-2-12-2	Change 9 dated 28 December 1992 **[1>**
21M-LGM30G-2-12-4	Change 0 dated 1 July 1992
21M-LGM30G-2-21-4	Change 62 dated 15 January 1993 **[1>**

AIR FORCE SYSTEM MANUALS

CEM 21-SM80B-2-21-2	Change 12 Dated 1 December 1987
CEM 21-SM80B-2-21-4	Change 8 dated 21 September 1987

INTERFACE CONTROL DRAWINGS

C-2250	Revision B dated 15 December 1986
D25-65000, Vol. IX	Original dated 20 October 1986, plus Appendix I dated 22 December 1995
D25-65002, Vol. V	Revision D dated 21 March 1988
D25-65043	Revision D dated 15 October 1984
D25-92851	Revision A dated 9 March 2004
D25-92852	Revision A dated 9 March 2004
D25-92853	Revision B dated 29 March 2004
D25-92854	Revision B dated 29 March 2004
D25-92855	Revision A dated 16 March 2004
D25-92856	Revision A dated 16 March 2004
25-R001	Revision A dated 07 April 1992
25-R030	Revision B dated 23 December 1992
25-R036	Revision B dated 05 February 1993
25-R050	Revision C dated 11 February 1994
25-R059, Vol. I	Revision A dated 10 September 1993
25-R059, Vol. II	Revision A dated 18 November 1991

SYSTEM DIAGRAMS

21-52747	Revision M dated 7 February 1977, will be updated as part of GRP
21-52752	Revision U dated 15 May 1984, will be updated as part of GRP

SYSTEM SPECIFICATIONS

S-133-05204	1 May 2003
S-133-05206	29 May 2003
S-133-05207	1 May 2003
S-133-09259	2 Mar 2000
S-133-19251	22 February 1999
S-133-30001A	19 December 1990
S-133-36000B	Revision B dated 20 December 1993

[1> Including REACT Supplement

Table 3. Abbreviations and Acronyms

A/B	Airborne
A/D	Arm/Disarm
AAP	Auxiliary Alarm Panel
AAU	Angular Accelerometer Unit
ACI	Attitude Control Injection
ACK	Acknowledge
ACP	Alternate Command Post
AE	Auxiliary Equipment
AFB	Air Force Base
AFRB	Air Force Report Back
AFI	Automatic Flight Interrogation
AFS	Arming and Fuzing Safety
AFSAT	Air Force Satellite
AFSATCOM	Air Force Satellite Communications System
AFSPACECOM	Air Force Space Command
AGE	Aerospace Ground Equipment
AHC	ALCC Holdoff Command
AJ	Anti-Jam
ALCC	Airborne Launch Control Center
ALRM	Alarm
AM	Alarm Monitor; Amplitude Modulation
AN	Autonetics
AOTT	All Ordnance Thrust Termination
A/PA	Antenna/Pedestal Assembly
APQ	Action Pending Queue
ASE	Auxiliary Status Enable
ASR	Auxiliary Status Reply
ASU	Auxiliary Switching Unit
ATM	ALCC Test Message
AUC	Autonetics Code Processing
AVE	Aerospace Vehicle Equipment
BCD	Binary Coded Decimal
BCP	Base Communications Processor
BDI	Black Discrete Interface
BITE	Built-In Test Equipment
BKG	Background (Process)
BMT	Background Memory Test (Process)
BO	The Boeing Company
BOA	Breakout Adapter
BOB	Breakout Box
BPL	Background Program Load (Process)
BPS	Bits per Second
BSL; BS/L	Bulk Storage/Loader
BSY	Busy
C/R	Circumvention Reset
C/RGT	Cable/Radio Gated Timing
CAL	Calibrate
CAS	Command and Status (CSC)
CB	Circuit Breaker
CCL	Crypto Control (Function)
CCS	Common Command Set
CCT	Control Clock and Timers (Function)
CCW	Counterclockwise
CDA	Coder-Decoder Assembly
CDI	Coder-Decoder Indicator
CEIU	Communications Equipment Interface Unit
CEP	Circular Error Probable
CFPA	CMOS Floating Point Accelerator
CI	Configuration Item
CIS	Communications Interface Support (Process)
CIV	Code Insertion Verifier
CKL	Checklist (Process)
CLC	Crew Log Control (CSC)
CLD	Critical Leads Disconnect
CLK	Clock
CLS	Cooperative Launch Switch
CMCC	Computer Memory Confidence Check
CMD	Command (Process)
CMD	Commanded
CMD	Cable Message Enable
CML	Commercial
CMOS	Complimentary Metal Oxide Semiconductor
C-MON	Controller-Monitor
CMPG	Command Message Processing Group
CMSC	Computer Memory Security Check
CMVC	Computer Memory Verification Check
CO; C.O.	Character Output
COMM	Communications (CSC)
COP	Console Operations Program
CP	Command Post; Central Processor
CPC	Computer Program Component
CPI	Console Printer Interface (Function)
CPU	Central Processing Unit
CR	Circumvention Reset
CRD	Confidential Restricted Data
CRL	Crew Log (Process)
CRPT	Cryptographic (CSC)

Table 3. Abbreviations and Acronyms (Continued)

CSC	Computer Software Component
CSCI	Computer Software Configuration Item
CSD(G)	Command Signals Decoder (Ground)
CSD(M)	Command Signals Decoder (Missile)
CSO	Critical Status Override
CSR	Command Status Register; Command Summary Report; Cable Status Ready
CSS	Commands, Sequences, and Stacks (Function)
CT	Clear Text
CTA	Clear Text Allowed
CTE	Cable Termination Equipment
CTS	Clear to Send
CTU	Cartridge Tape Unit
CW	Clockwise
D	Decoder
D-Box	Distribution Box
D/L	Down Link
DAC	Digital to Analog Converter
DB	Distribution Box
DCU	Digital Computer Unit
DD	Disable Discretes
DEU	Diesel Engine Unit
DI	Discrete Input
DISEN	Disenabled
DMA	Direct Memory Access
DO	Discrete Output
DPE	Data Processing Equipment
DRAM	Dynamic Random Access Memory
DTG	Date/Time Group
EAM	Emergency Action Message
EC; ECS	Environmental Control System
EDAC	Error Detection and Correction
EEP	Expanded Execution Plan
EEPROM	Electronic Erasable PROM
EGS	Electronic Ground System
EHF	Extremely High Frequency
ELC	Execute Launch Command
ELI	Control LEP, LCP, and CLS (Function)
ELN	VAXELN Operating System (CSC)
ELPD	Engineering Laboratory Production Drawing
EMAD	Embedded Memory Array Dynamic
EMDAS	Expanded Missile Data Analysis System
EMP	Electromagnetic Pulse
ENBL	Enable
ENC	Enable Command
ENTC	Enable Test Command
EOF	End of File
EOT	End of Text, End of Test
EPG	Execution Plan Generation
EPP	Execution Plan Program
EPROM	Erasable PROM
ESA	Electrical Surge Arrestor
ESMC	Embedded Single Module Computer
ETX	End of Text
EW	Enable Write
EWO	Emergency War Order
F/C	Flight Control
FCID	Flight Constants Identification
FDD	Floppy Disk Drive
FDM	Force Direction Message
FDT	Floppy Disk Transfer (CSC)
FDW	Fault Data Word
FIFO	First In First Out
FLT	Flight
FOIO	Flight Control and Ordnance Input/Output
G&C	Guidance and Control
GCA	Gyrocompass Assembly
GCC	G&C Cooler
GES	Ground Electronic System
GMI	Ground Maintenance Interrogation
GMR	Ground Maintenance Response
GMT	Greenwich Mean Time
GND	Ground
GODT	Ground Ordnance Discretes Test
GRD	Ground
GRND	Ground
GRP	Guidance Replacement Program
GSP	Gyro Stabilized Platform
HA	Higher Authority
HAC	Higher Authority Communications
HAF	High Altitude Fuzing
HDA	Head Drive Assembly
HDLC	High Level Data Link Control
HF	High Frequency

Table 3. Abbreviations and Acronyms (Continued)

HICS	Hardened Intersite Cable System
HIDAR	High Data Rate
HIS	HAC/RMPE Interface Support (Process)
HMI	Human Machine Interface (also CSC) (also Function)
HRC	HAC/RMPE Control (CSC)
HRI	HAC/RMPE Interface Control (Function)
HUTE	Hard User Terminal Element
HVC	Hardened Voice Communications; Hardened Voice Channel
I/O	Input/Output
IB	Interconnecting Box
ICD	Interface Control Drawing
ICM	Internal Communications Mechanism
IIS	IPDM Interface Support (Process)
ILC	Inhibit Launch Command
ILCS	Improved Launch Control System
IMPSS	Improved Minuteman Physical Security System
IMU	Inertial Measurement Unit
IMUCC	Inertial Measurement Unit Calibrate Command
INC	Inhibit Command
INHBT	Inhibit
IPB	Illustrated Parts Breakdown
IPD	IMU Performance Data
IPDC	IPD Command
IPDH	IPD Halt
IPDM	IPD Modem
IPDR	IPD Reply
IRTI	IMU Real Time Interrupt
IRM	Insulation Resistance Monitor
ISR	Interrupt Service Routine
ISST	ICBM SHF Satellite Terminal
ITSC	Instruction Transfer Security Check
IZ	Inner Zone
J-Box	Junction Box
LAI	Large Angle Indicator
LCC	Launch Control Center
LCCS	Loral Command & Control Systems
LCEB	Launch Control Equipment Building
LCF	Launch Control Facility
LCFT	Launch Control Facility Test
LCM	Launch commanded Mode
LCMVV	LCM Validation Variable
LCP	Launch Control Panel
LCS	Launch Control Switch
LCSB	Launch Control Support Building
LCT	Launch Commanded Timer
LD	Level Detector
LDR	Low Data Rate
LDT	Launch Delay Time
LED	Light Emitting Diode
LEP	Launch Enable Panel
LER	Launcher Equipment Room
LES	Launch Enable Switch
LF	Launch Facility; Low Frequency
LFAD	LF Activity Data
LFDN	LF Down
LFLC	LF Load Cartridge
LFNA	LF Not Authenticated
LFNG	LF No-Go
LFNI	LF Not Interrogated
LFOS	LF Out-of-Sync
LFSB	LF Support Building
LIP	Launch In Progress
LIT	Launch Inhibit Time
LITVC	Liquid Injection Thrust Vector Control
LLS	Low Level Seismic
LNA	Low Noise Amplifier
LS	Line Seize
LSB	Least Significant Bit; Launcher Support Building; Lower Side Band
M/G; M-G	Motor-Generator
M.T.	Missile Test
MAF	Missile Alert Facility
MAP	Maintenance Assist Panel
MAR	Master Alarm Reset
MAT	Message Assemble and Transmit (Function)
MBCP	Missile Base Communications Processor
MCC	Missile Calibration Command; Missile Combat Crew
MCCM	Missile Combat Crew Member
MCU	Mechanical Code Unit
MEBus	Memory Bus
MESP	Minuteman Extended Survival Power
MGC	Missile Guidance Computer

Table 3. Abbreviations and Acronyms (Continued)

MGS	Missile Guidance Set
MGSC	Missile Guidance Set Control
MIPS	Million Instructions per Second
MIS	Message Identify/System Status (Function)
MM	Minuteman
MMD	Missing MOSR Data
MMOC	Missile Maintenance Operations Center
MNU	Menu (Process)
MOSI	Missile Operational Status Interrogation
MOSR	Missile Operational Status Response
MOTP	Minuteman Operational Targeting Program
MPP	Minuteman Power Processor
MPR	Master Process (CSC)
MPX	Multiplexer
MR	Master Reset
MRT	Minimum Reaction Time
MSB	Most Significant Bit
MSG	Message
MSL	Missile
MSS	Missile Suspension System
MTC	Missile Test Command
MTU	Magnetic Tape Unit
MUX	Multiplexer
N/C	No Connection
NAFH	Numbered Air Force Headquarters
NAK	Negative Acknowledge
NCU	Nozzle Control Unit
NED	Nuclear Event Detector
NEP	Nuclear Event Protection
NGM	No-Go Monitor
NOM	Nominal
NRZ	Non Return to Zero
OSI-AJ	OSI, Anti-Jam
ODI	Operator Discrete Interface (CSC)
OER	Optical Electrical Resolver
OES	Operator Entered Status
OFP	Operational Flight Program
OGDEN ALC	Ogden Air Logistics Command
OGE	Operational Ground Equipment
OGP	Operational Ground Program
OID	Operator Input Device
OMGE	Organizational Maintenance Ground Equipment
OOALC	Ogden Air Logistic Center
ORD	Ordnance
OS	Ordnance Switch
OSI	Operational Status Interrogation
OSR	Operational Status Response
OTAR	Over the Air Rekeying
OTL	Operational Test Launch; Output Timing Level
OWC	Overwrite Command
OWIP	Overwrite In Process
OWT	Overwrite Terminate
OZ	Outer Zone
P/A	Pen Aid
P/G	Programmer Group
PI/O	Parallel Input/Output, Programmed Input/Output
PAN	Panel
PAS	Performance Assessment Software
PCP	Primary Commands Post
PBPS	Post Boost Propulsion System
PCDU	Power Control and Distribution Unit
PCMR	Probability of Correct Message Receipt
PDB	Program Data Buffer
PEM	Process EAMs (Function)
PGLC	PIGA Leveling Command
PGLVL	PIGA Leveling
PIGA	Pendulous Integrating Gyroscopic Accelerometer
PLC	Preparatory Launch Command
PLCA; PLC-A	Preparatory Launch Command - A
PLCB; PLC-B	Preparatory Launch Command - B
PLCC; PLC-C	Primary Launch Control Center, Preparatory Launch Command-C
PLCO	Phonetic Letter Spelled Out
PLS	Pre-Launch Sequence
PMRT	Pressure Monitoring Receiver - Transmitter
PPM	Parts per Million
PRF	Printer Formatter (Process)
PRM	Printer Manager (Process)
PRN	Print Control (CSC)
PS	Power Supply
PSAT	Perturbation Self alignment Technique
PSDU	Power Signal Distribution Unit
PSO	Primary, Secondary, Other
PSRE	Propulsion System, Rocket Engine

Table 3. Abbreviations and Acronyms (Continued)

PTR	Printer
PWM	Pulse Width Modulator
PWR	Power
R/S; RS	Reentry System
R/T	Receiver-Transmitter
R/V	Reentry Vehicle
R.O.	Readout
RAM	Random Access Memory
RB	Report Back
RBD	ROM Based Diagnostics
RCV	Receive
RCVR	Receiver
RD	Radiation Detector
RDA	Remote Data Authorization
RDC	Remote Data Change
RDCP	Remote Data Change - Program Data
RDCT	Remote Data Change - Targeting
RDH	Remote Data Halt
RDI	Remote Data Interrogation
RDR	Remote Data Reply
RDT	Remote Data Terminate
RDV	Remote Data Verify
RDW	Remote Data Word
REACT	Rapid Execution and Combat Targeting
REG	Regulated
REQ	Request
RESP	Responsibility
RET	Return
RF	Radio Frequency
RGB	Red, Green, Blue
RLC	Message Reception and Line Checking (CSC)
RMP	Rapid Message Processor
RMPB	RMP Backup
RMPE	RMP Equipment
RMR	Remote Missile Restart
ROM	Read Only Memory; User ROM
RPIE	Real Property Installed Equipment
RSA	Restart Alignment
RSCSI	Raytheon Small Computer System Interface
RSET	Reset
RSI	Resync Inquiry
RSR	Remote Synchronization Reply
RTC	Real Time Clock
RTN	Return
RVR	Remote Verification Reply
RXD	Receive Data
RZ	Return to Zero
S&A; A/A	Safe and Arm
SA; S/A	Strategic Alert
S/N	Signal to Noise Ratio
SACCS	Strategic Automatic Command and Control System
SACDIN	Strategic Air Command Digital Network
SAHC	Short ALCC Holdoff Command
SAT	Self Alignment Technique
SATCAL	SAT Calibration
SATCC	SAT Calibrate Command
SBNG	Standby No-Go
SCC	Security Control Center
SCN	Sensitive Command Network; Specification Change Notice
SCNT	Sensitive Command Network Test
SCP	Squadron Command Post
SCS	Safety Control Switch
SCSI	Small Computer System Interface
SCST	Safety Control Switch Test
SDC	Safety Device Control
SDU	Secure Data Unit
SEL	Select
SELECT	System Engineering Level Evaluation Correction Team
SELM	Simulated Electronic Launch Minuteman
SI	Serial Input
SIN	Support Information Network
SLFCS	Survivable Low Frequency Communications System (VLF/LF)
SMC	Single Module Computer
SMSB	Strategic Missile Support Base
SO	Serial Output
SOH	Start of Header
SPAT	Survival Power Allowed Timer
SRAM	Static Random-Access Memory
SRI	Startup, Restart, Initialization (CSC)
SRS	Software Requirements Specification
SSA	Solid State Amplifier
SSMU	Solid State Memory Unit
SSR	System Services (Function)
STBNG	Standby No-Go
STBY	Standby
STS	Status (Process)
STX	Start of Text
SUR	System User ROM (CSC)

Table 3. Abbreviations and Acronyms (Continued)

SYL	Sylvania
SYNC	Synchronize
T.O.	Technical Order
TATD	Targeting and Timing Document
TCD	Terminal Countdown
TCG	Target Constants Generation
TDC	Target Data Change
TDR	Target Data Reply
TEU	Terminal Electronics Unit
TGL	Target Library (Process)
TGS	Targeting Support (CSC)
TGT	Target
TGT	Targeting (CSC)
TMR	Timer (CSC)
TMT	Targeting Management and Transmission (CSC)
TOD	Time of Day
TODC	Time of Day Clock
TRW	Thompson Ramo Woolridge
TSM	Time Standard Module
TVC	Thrust Vector Control
TVI	Target Verification Interrogation
TVR	Target Verification Response
TXD	Transmit Data
U/L	Up Link
UHF	Ultra High Frequency
UIO	Umbilical Input/Output
UMB	Umbilical
UN	Univac
URD	Unit Reference Designator
USB	Upper Side Band
UTC	Coordinated Universal Time
UTL	Utilities (CSC)
UVEPROM	Ultra Violet Erasable PROM
VLF/LF	Very Low Frequency/Low Frequency
VAFB	Vandenberg Air Force Base
VAX	Virtual Address Extension
VAXBI-M	Modified VAX Bus Interface
VDU	Video Display Unit
VDUC	VDU Controller
VESS	VAX Extended Support System
VHF	Very High Frequency
VLF	Very Low Frequency
VME	Versa Module Eurocard
VMS	Virtual Memory System
VXI	VMEbus Extension for Instrumentation
WCP	Wing Command Post
WCPS	Wing Code Processing System
WS	Weapon System
WSC	Wing Security Control
WSCC	Weapon System Control Console
WSCE	Weapon System Control Element
WSM	Workstation Manager (Process)
WSP	Weapon System Processor
WST	WSP Testing (CSC)
XFER	Transfer
XMIT	Transmit

SECTION I - GENERAL INFORMATION

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LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF TABLES

1-1. SCOPE. This section contains information of a general nature that could be useful to SELECT but does not readily fit into the remaining sections of this manual, such as the Julian Calendar on Figure 1-1. This figure also includes a matrix for conversion of the Universal Time Code (UTC or GMT) to local time. Also included are overview descriptions of the communications systems, the flight takeover rules, and the operator interface to the Weapon System Control Console (WSCC).

1-2. LGM-30G MISSILE. The LGM-30G missile is used at Wing I, Wing III and Wing V. The missile is shown in Figure 1-2. Access locations for arm/disarm device and safing pin removal or installation are also shown.

1-3. ROUTE MAPS. Figures 1-3 and 1-4 show a general layout and route maps of Malmstrom AFB (Wing I). Figures 1-5 and 1-6 show a general layout and route maps of Minot AFB (Wing III) and Figures 1-7 and 1-8 portray F. E. Warren AFB (Wing V). Detailed route maps and local road reports are available from AFSPC.

1-4. COMMUNICATIONS AND CONTROL SYSTEMS.

1-4.1. Command and Control System. The command and control system is a squadron-wide, hardened, command-control and status monitoring system. The system permits any LCC in the squadron to generate and transmit commands to all LFs in the squadron. The system also allows each LCC to monitor the operational status of each missile and LF. Each launch facility has from two to five electrically connected LFs as well as its parent launch control facility. Tables 1-1, 1-2 and 1-3 provide a listing of the electrically adjacent launch facilities.

1-4.2. Hardened Voice Channel. The Hardened Voice Channel (HVC) is a telephone circuit between LCCs used for the coordination of launch commands and for reporting faults within a squadron. The HVC is a four party line circuit in the control and monitoring system buried cable. See Figures 1-9, 1-10, and 1-11 for HVC interconnectivity.

1-4.3. Emergency War Order Network. Emergency War Order (EWO) Network equipment is located at the wing command post and the squadron command posts. The system consists of primary and secondary EWO circuits. Primary EWO is a party line which interconnects the four locations using soft commercial telephone facilities. Primary EWO may use separate telephone lines or existing LCC dialing facilities on a preemptive basis. Secondary EWO is a separate party line interconnecting the three SCPs of a wing by means of the hardened cable network with relays through other LCCs and LFs as necessary. See Figures 1-12, 1-13 and 1-14 for intersite EWO circuits.

1-4.4. Primary Alert System. The Primary Alert System is inoperative. Its equipment has been abandoned in place. It no longer serves a functional purpose.

TIME CONVERSATION TABLE

UTC (ZULU TIME)	WING I MOUNTAIN TIME			
	STD		DST	
	12 HR	24 HR	12 HR	24 HR
0100	6 PM	1800	7 PM	1900
0200	7	1900	8	2000
0300	8	2000	9	2100
0400	9	2100	10	2200
0500	10	2200	11 PM	2300
0600	11 PM	2300	12 AM	2400
0700	12 AM	2400	1	0100
0800	1	0100	2	0200
0900	2	0200	3	0300
1000	3	0300	4	0400
1100	4	0400	5	0500
1200	5	0500	6	0600
1300	6	0600	7	0700
1400	7	0700	8	0800
1500	8	0800	9	0900
1600	9	0900	10	1000
1700	10	1000	11 AM	1100
1800	11 AM	1100	12 PM	1200
1900	12 PM	1200	1	1300
2000	1	1300	2	1400
2100	2	1400	3	1500
2200	3	1500	4	1600
2300	4	1600	5	1700
2400	5	1700	6 PM	1800

PRIOR DAY CURRENT DAY

JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC	
1 / 1 2 / 2	32 / 32 33 / 33	60 / 61 / 61 62 / 62	91 / 92 / 92 93 / 93	121 / 122 / 122 123 / 123	152 / 153 / 153 154 / 154	182 / 183 / 183 184 / 184	213 / 214 / 214 215 / 215	244 / 245 / 245 246 / 246	274 / 275 / 275 276 / 276	305 / 306 / 306 307 / 307	335 / 336 / 336 337 / 337	2
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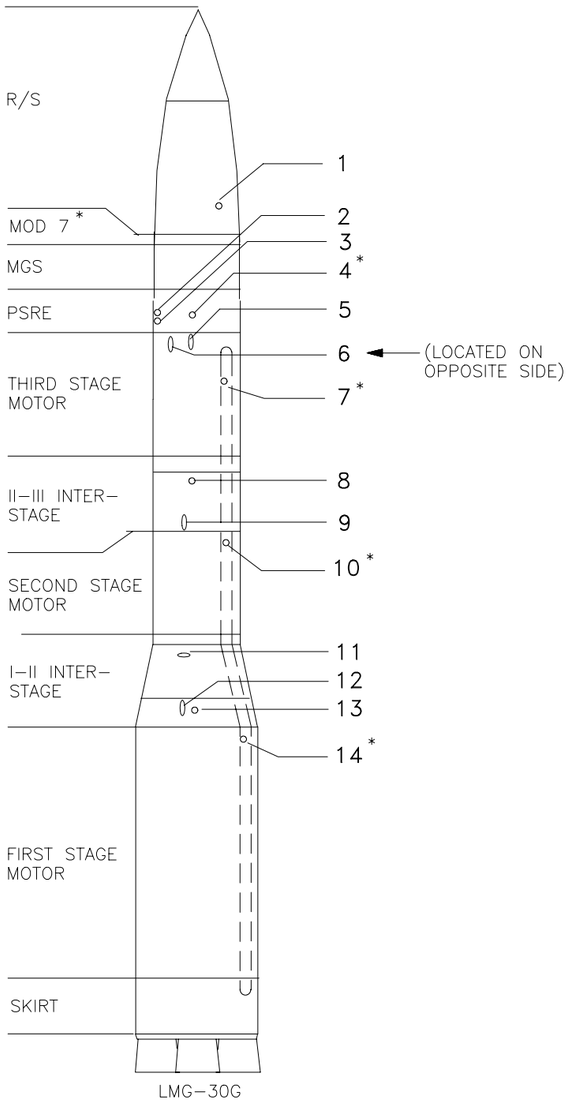
19 / 19 20 / 20	50 / 50 51 / 51	78 / 79 / 79 80 / 80	109 / 110 / 110 111 / 111	139 / 140 / 140 141 / 141	170 / 171 / 171 172 / 172	200 / 201 / 201 202 / 202	231 / 232 / 232 233 / 233	262 / 263 / 263 264 / 264	292 / 293 / 293 294 / 294	323 / 324 / 324 325 / 325	353 / 354 / 354 355 / 355	20
21 / 21 22 / 22	52 / 52 53 / 53	80 / 81 / 81 82 / 82	111 / 112 / 112 113 / 113	141 / 142 / 142 143 / 143	172 / 173 / 173 174 / 174	202 / 203 / 203 204 / 204	233 / 234 / 234 235 / 235	264 / 265 / 265 266 / 266	294 / 295 / 295 296 / 296	325 / 326 / 326 327 / 327	355 / 356 / 356 357 / 357	22
23 / 23 24 / 24	54 / 54 55 / 55	82 / 83 / 83 84 / 84	113 / 114 / 114 115 / 115	143 / 144 / 144 145 / 145	174 / 175 / 175 176 / 176	204 / 205 / 205 206 / 206	235 / 236 / 236 237 / 237	266 / 267 / 267 268 / 268	296 / 297 / 297 298 / 298	327 / 328 / 328 329 / 329	357 / 358 / 358 359 / 359	24
25 / 25 26 / 26	56 / 56 57 / 57	84 / 85 / 85 86 / 86	115 / 116 / 116 117 / 117	145 / 146 / 146 147 / 147	176 / 177 / 177 178 / 178	206 / 207 / 207 208 / 208	237 / 238 / 238 239 / 239	268 / 269 / 269 270 / 270	298 / 299 / 299 300 / 300	329 / 330 / 330 331 / 331	359 / 360 / 360 361 / 361	26
27 / 27 28 / 28	58 / 58 59 / 59	86 / 87 / 87 88 / 88	117 / 118 / 118 119 / 119	147 / 148 / 148 149 / 149	178 / 179 / 179 180 / 180	208 / 209 / 209 210 / 210	239 / 240 / 240 241 / 241	270 / 271 / 271 272 / 272	300 / 301 / 301 302 / 302	331 / 332 / 332 333 / 333	361 / 362 / 362 363 / 363	28
29 / 29 30 / 30	60	88 / 89 / 89 90 / 90	119 / 120 / 120 121 / 121	149 / 150 / 150 151 / 151	180 / 181 / 181 182 / 182	210 / 211 / 211 212 / 212	241 / 242 / 242 243 / 243	272 / 273 / 273 274 / 274	302 / 303 / 303 304 / 304	333 / 334 / 334 335 / 335	363 / 364 / 364 365 / 365	30
31 / 31		90 / 91	151 / 152			212 / 213	243 / 244		304 / 305		365 / 366	31

REGULAR 365 DAY YEAR / LEAP YEAR 366 DAY YEAR

MMT201_070K

Figure 1-1. Julian Calendar



NO.	MISSILE MARKINGS	DESCRIPTION
1	REENTRY SYSTEM SAFING AND INDICATOR ACCESS	ACCESS TO R/S SAFE–ARM DEVICE SAFING PIN
2	ACCESS–POST BOOST SEPARATION SAFING PIN NO. 2	ACCESS TO PSRE ARM–DISARM DEVICE SAFING PIN
3	ACCESS–POST BOOST SEPARATION SAFING PIN NO. 1	ACCESS TO PSRE ARM–DISARM DEVICE SAFING PIN
4	ACCESS–COMMAND DESTRUCT SAFE AND ARM *	ACCESS TO COMMAND DESTRUCT SAFE–ARM DEVICE SAFING PIN
5	THIRD STAGE IGNITION SAFING AND INDICATOR ACCESS	ACCESS TO THIRD STAGE IGNITION SAFE–ARM DEVICE SAFING PIN AND S/A INDICATOR
6	ACCESS–ALL ORDNANCE THRUST TERMINATION (AOTT) SAFING PIN	ACCESS TO ALL ORDNANCE THRUST TERMINATION ARM–DISARM SAFE–ARM SWITCH SAFING AND S/A INDICATOR
7	PREMATURE SEPARATION DESTRUCT SAFING AND INDICATOR ACCESS STAGE III *	ACCESS TO PREMATURE STAGE SEPARATION ARM–DISARM MECHANISM SAFING PIN AND S/A INDICATOR
8	STAGE SEPARATION SAFING AND INDICATOR ACCESS	ACCESS TO STAGE SEPARATION ARM–DISARM MECHANISM SAFING PIN AND S/A INDICATOR
9	SECOND STAGE IGNITION SAFING AND INDICATOR ACCESS	ACCESS TO SECOND STAGE IGNITION SAF–ARM DEVICE SAFING PIN AND S/A INDICATOR
10	PREMATURE SEPARATION DESTRUCT SAFING AND INDICATOR ACCESS STAGE II *	ACCESS TO PREMATURE STAGE SEPARATION ARM–DISARM MECHANISM SAFING PIN AND S/A INDICATOR
11	SECOND STAGE ACI SAFING AND INDICATOR ACCESS	ACCESS TO SECOND STAGE ATTITUDE CONTROL INJECTION UNIT ARM–DISARM MECHANISM SAFING PIN AND S/A INDICATOR
12	FIRST STAGE IGNITION SAFING AND INDICATOR ACCESS	ACCESS TO FIRST STAGE IGNITION SAFE–ARM DEVICE SAFING PIN AND S/A INDICATOR
13	STAGE SEPARATION SAFING AND INDICATOR ACCESS	ACCESS TO STAGE SEPARATION ARM–DISARM MECHANISM SAFING PIN AND S/A INDICATOR
14	PREMATURE SEPARATION DESTRUCT SAFING AND INDICATOR ACCESS STAGE 1 *	ACCESS TO PREMATURE STAGE SEPARATION ARM–DISARM MECHANISM SAFING PIN AND S/A INDICATOR

* VAFB OTL MISSILE ONLY

SOURCE: T.O. 21M–LGM30F–2–17–3

MMT201_041K

Figure 1-2. Location of Missile Safing Pins

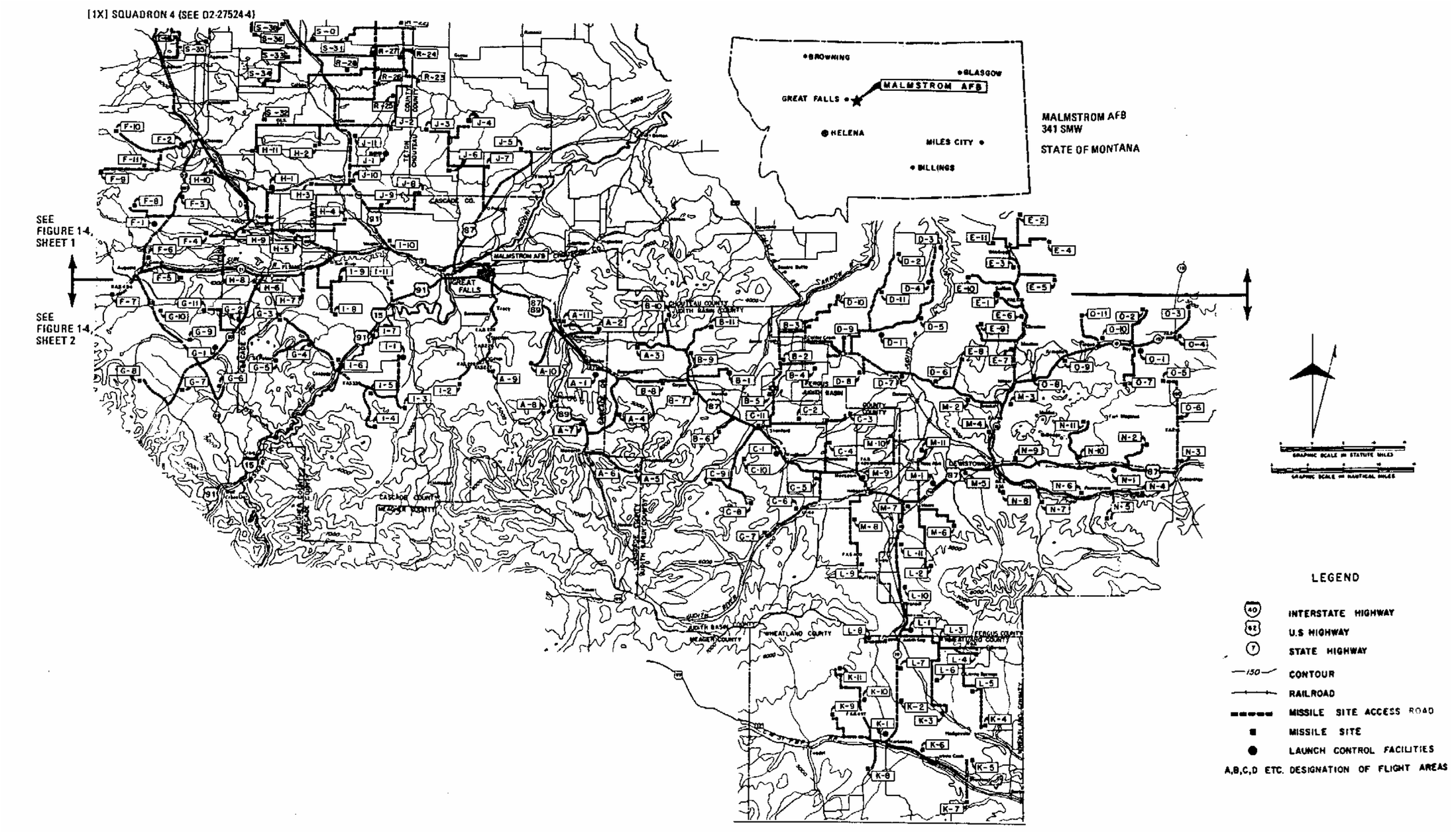


Figure 1-3. [1] Site Configuration

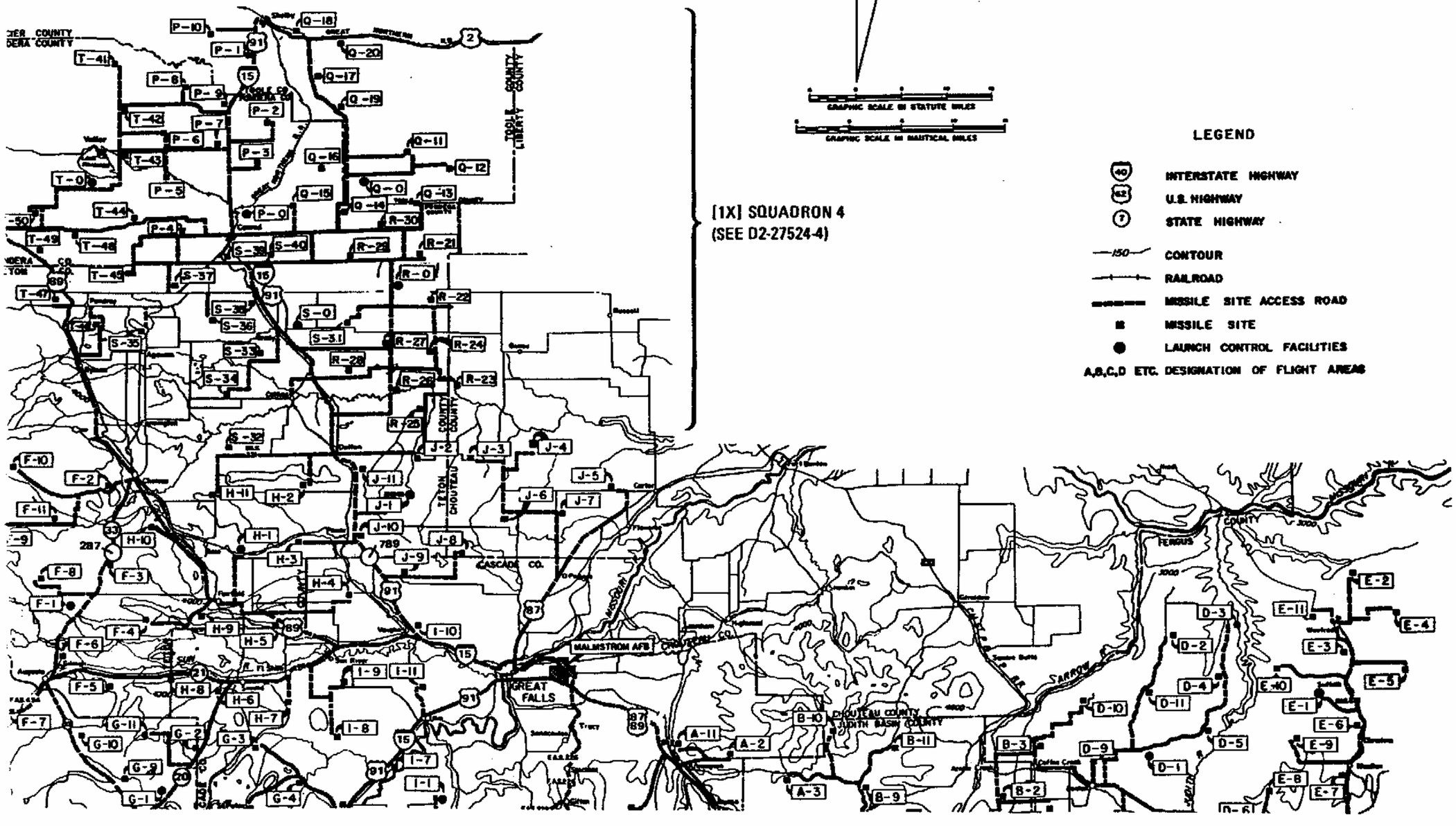


Figure 1-4. [1] Route Maps (Sheet 1 of 2)

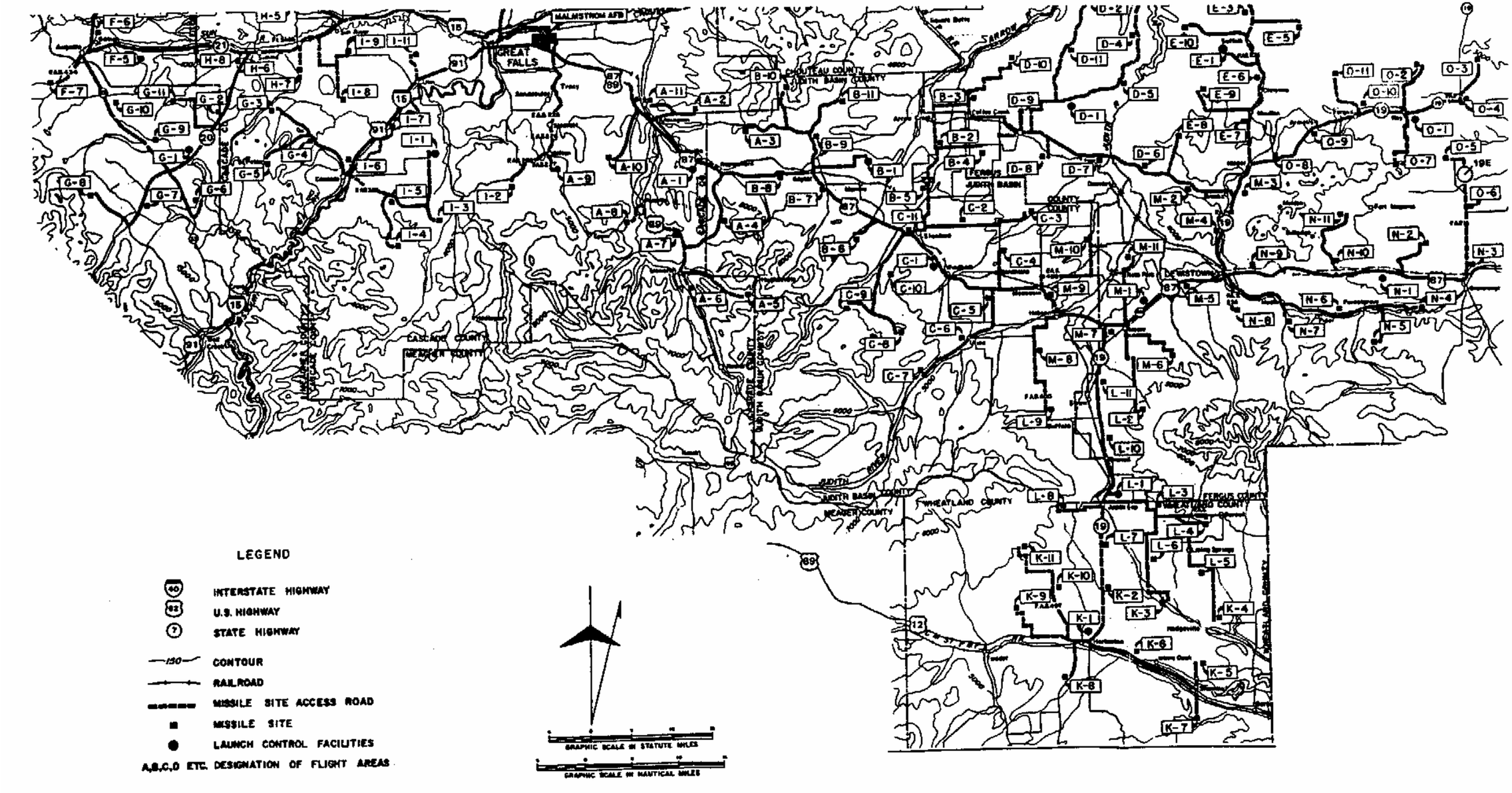


Figure 1-4. [1] Route Maps (Sheet 2 of 2)

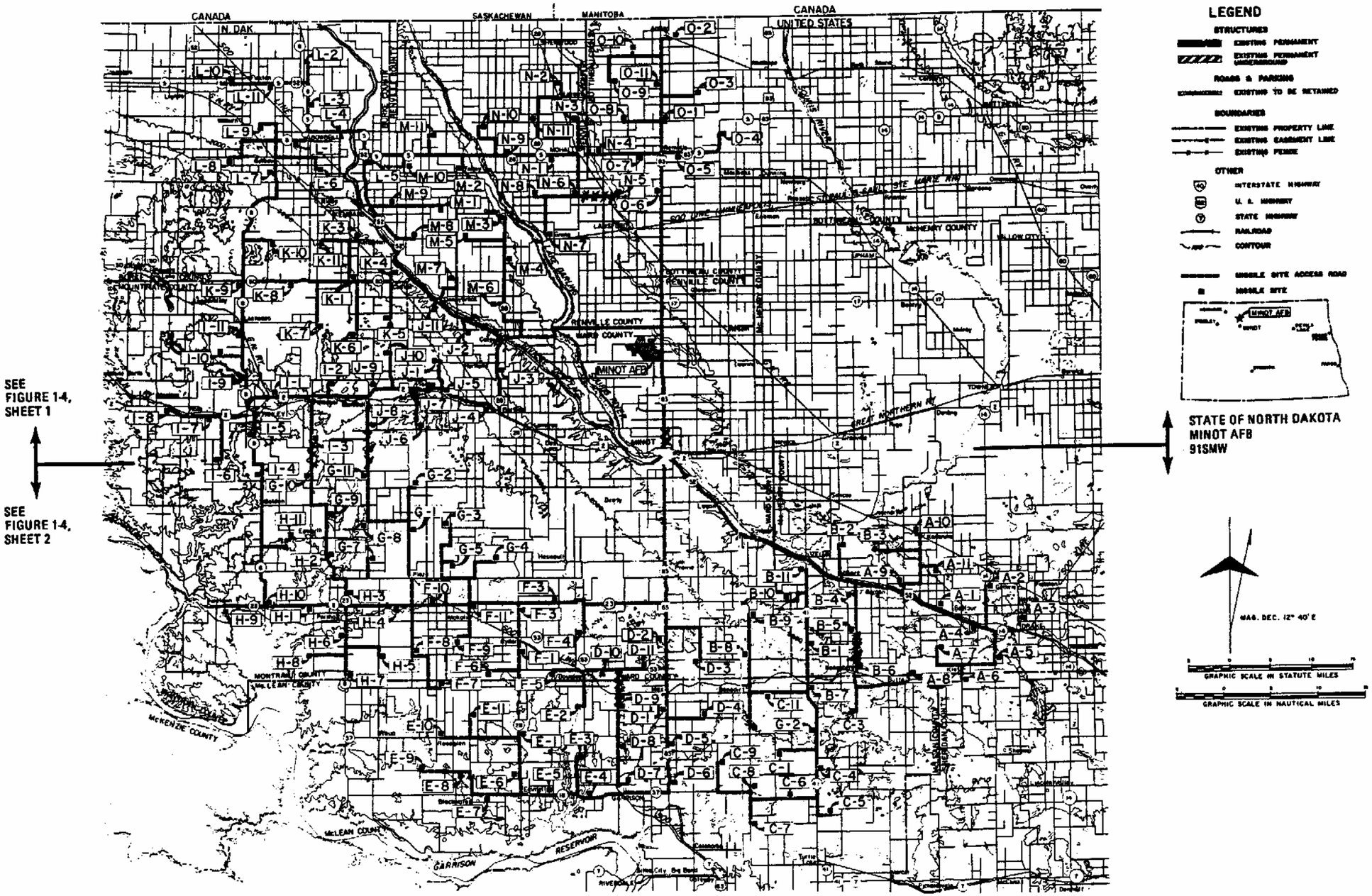


Figure 1-5. [3] Site Configuration

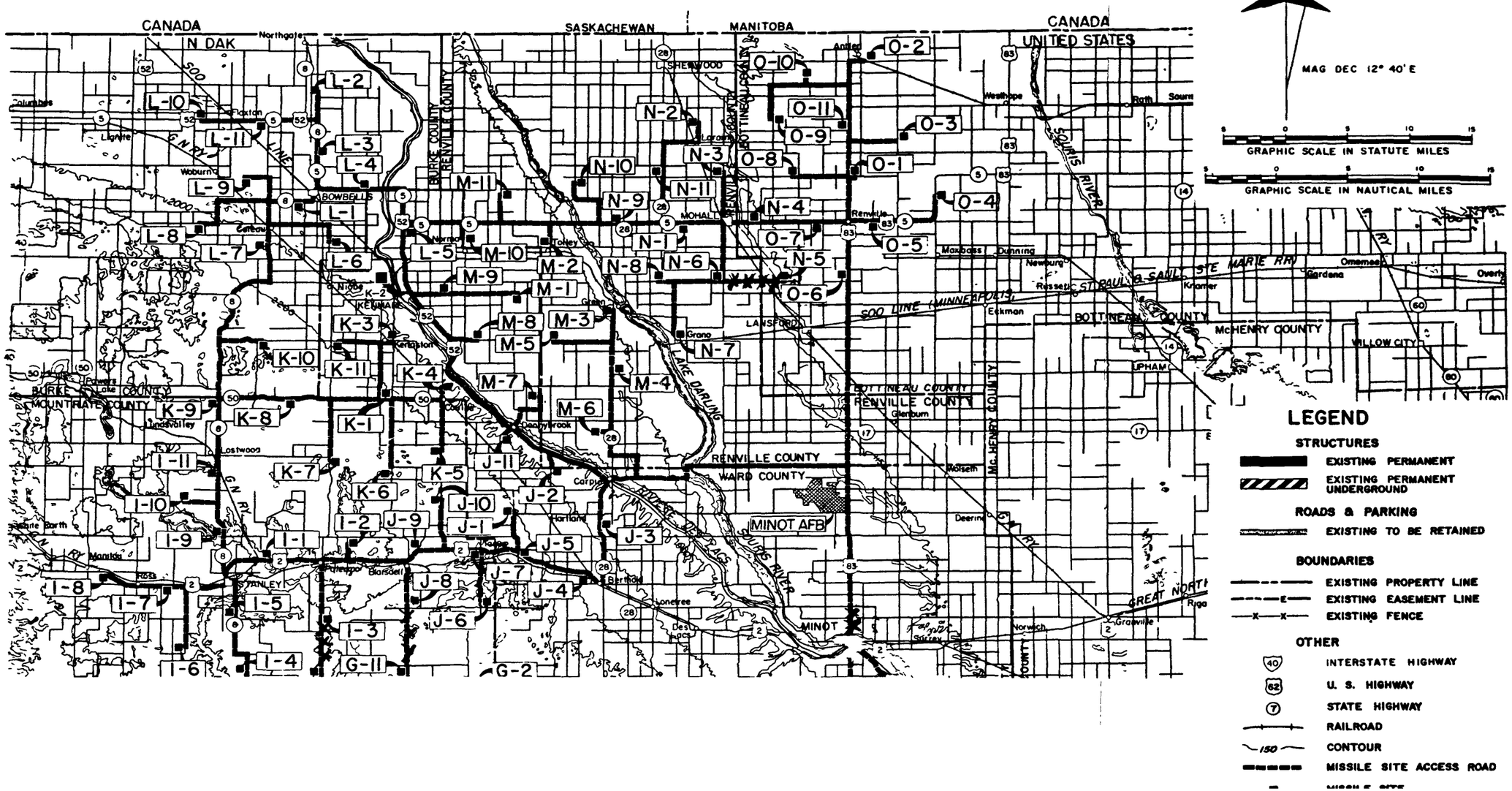


Figure 1-6. [3] Route Maps (Sheet 1 of 2)

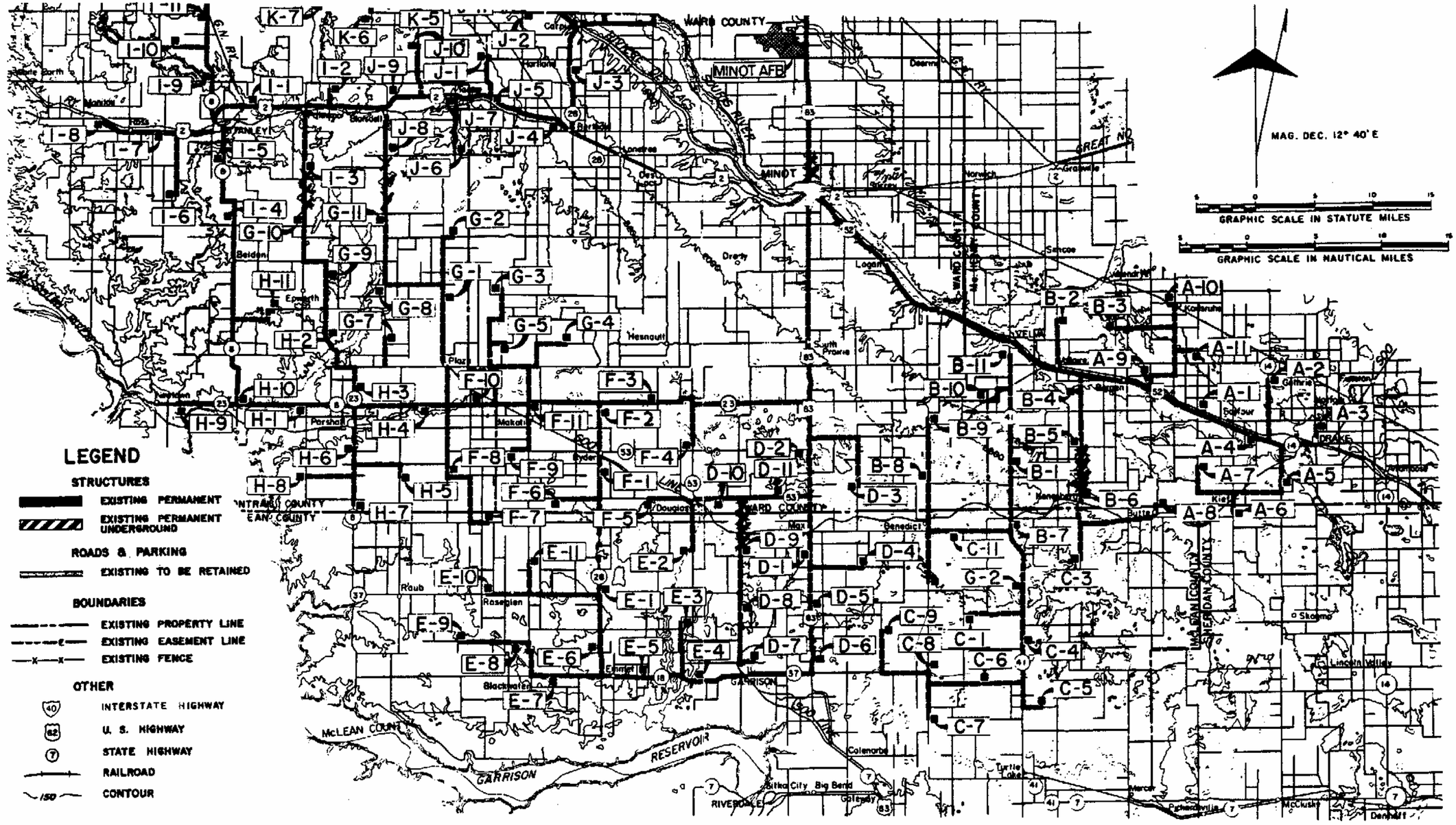


Figure 1-6. [3] Route Maps (Sheet 2 of 2)

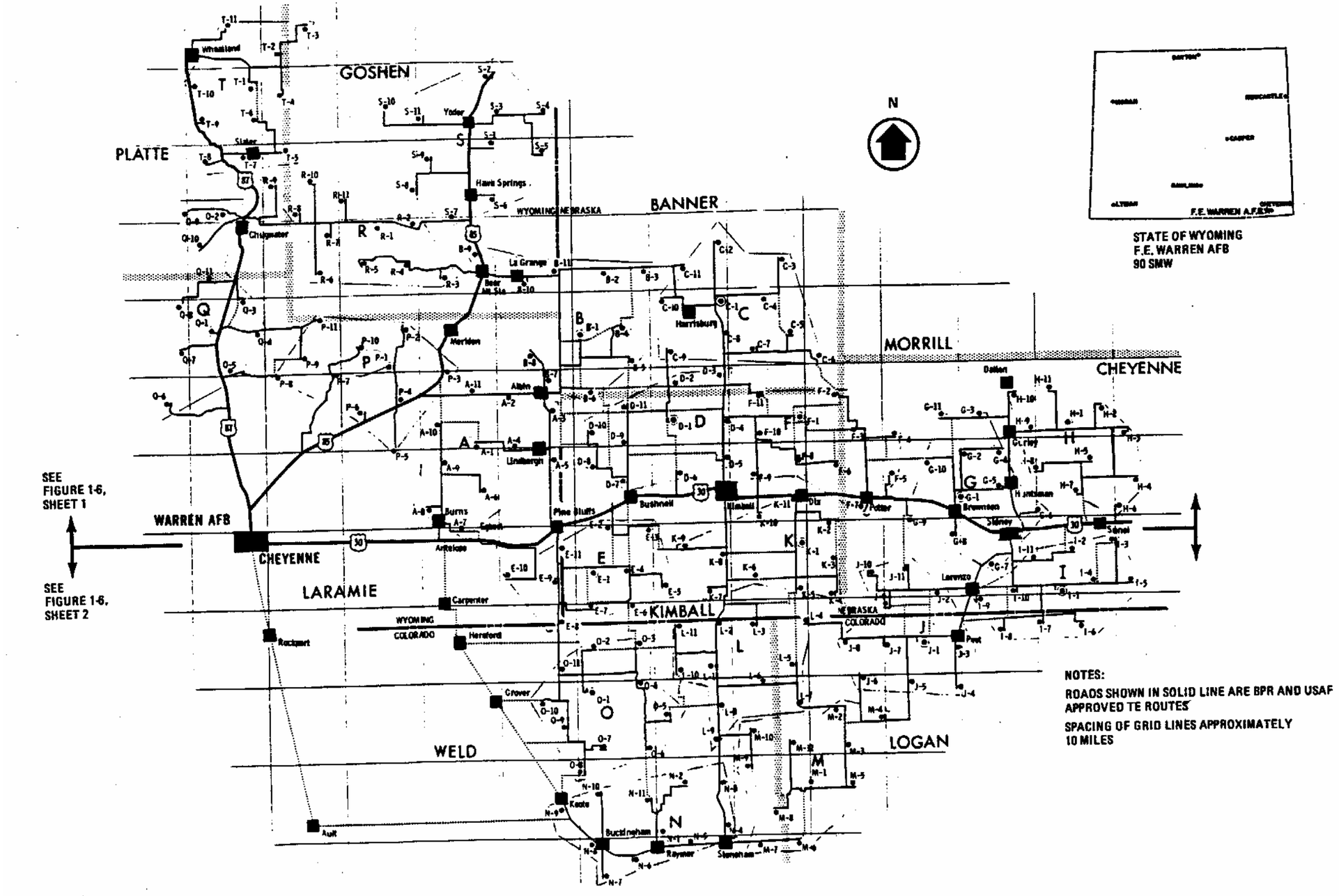


Figure 1-7. [5] Site Configuration

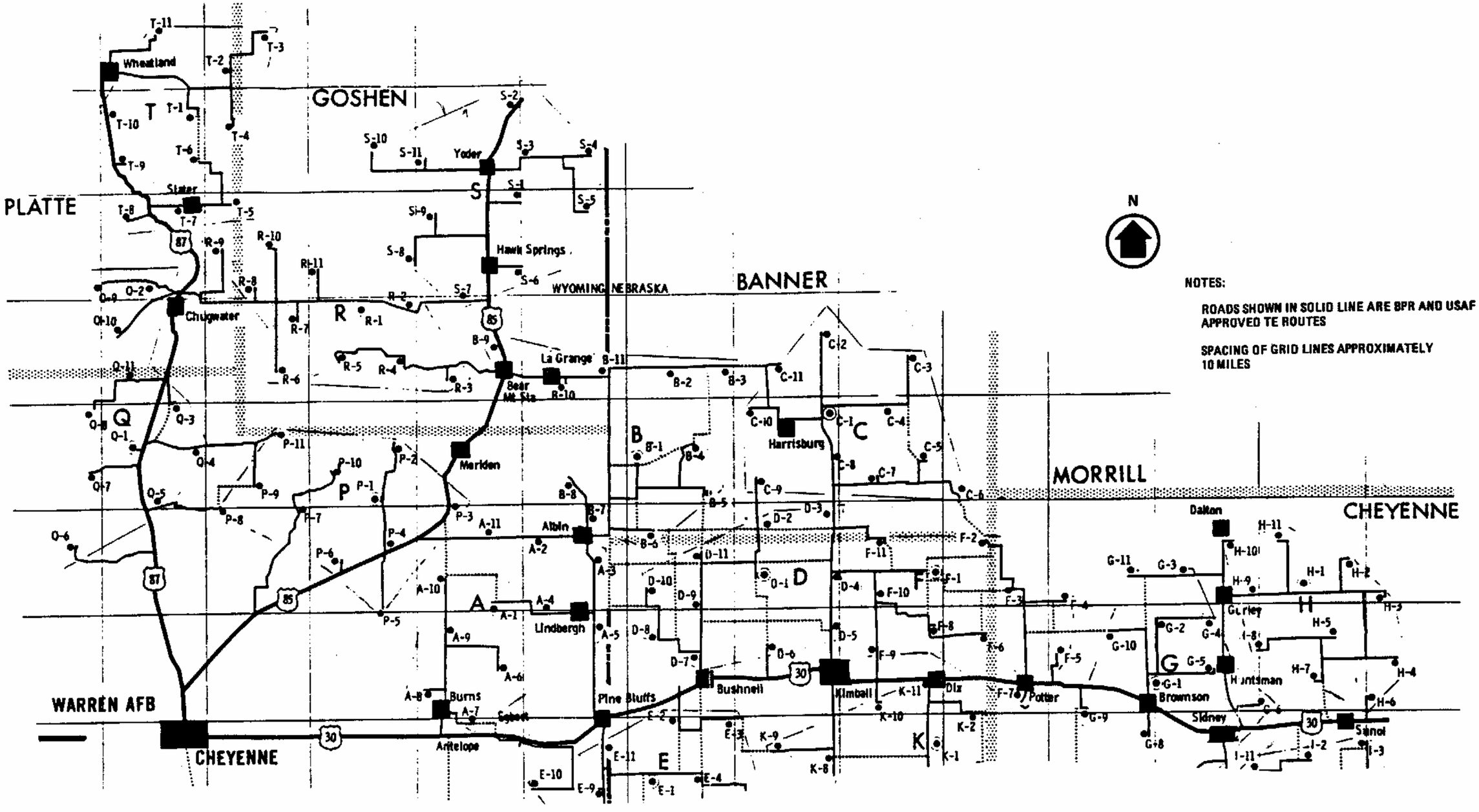
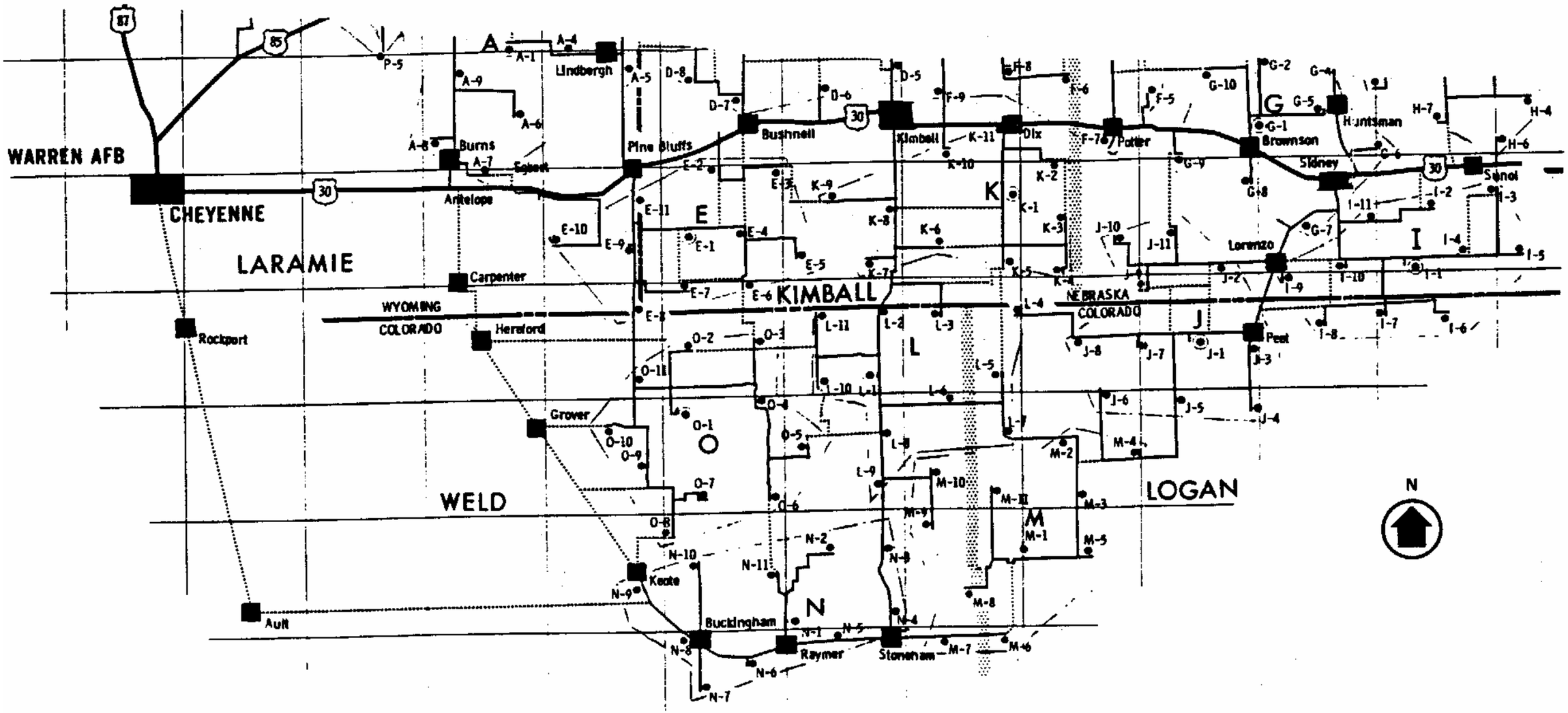


Figure 1-8. [5] Route Maps (Sheet 1 of 2)



NOTES:

ROADS SHOWN IN SOLID LINE ARE BPR AND USAF APPROVED TE ROUTES

SPACING OF GRID LINES APPROXIMATELY 10 MILES

Figure 1-8. [5] Route Maps (Sheet 2 of 2)

Table 1-1. [1] LF Interconnectivity

SQUADRON I		SQUADRON II		SQUADRON III	
LF NO.	ELECTRICALLY ADJACENT LF'S	LF NO.	ELECTRICALLY ADJACENT LF'S	LF NO.	ELECTRICALLY ADJACENT LF'S
A-2	A-3 A-11 B-7 B-8	F-2	F-3 F-11 H-10	K-2	K-3 K-10 L-4 L-6
A-3	A-2 A-4 B-9 B-10 B-11	F-3	F-2 F-4 G-10 G-11 H-11	K-3	K-2 K-4 L-4 L-7
A-4	A-3 A-5 B-8 B-9 B-11	F-4	F-3 F-5 G-10 H-9 H-11	K-4	K-3 K-6 L-6 L-7
A-5	A-4 A-6	F-5	F-4 F-7 G-7 G-9	K-5	K-6 K-7
A-6	A-5 A-7	F-6	F-7 F-8 G-2 G-9 G-11	K-6	K-4 K-5 L-4 L-6
A-7	A-6 A-8 B-8 B-10	F-7	F-6 F-5 G-2 G-7 G-9	K-7	K-5 K-8
A-8	A-7 A-9	F-8	F-6 F-9 G-10 G-11 H-10	K-8	K-7 K-9 L-5 L-8
A-9	A-8 A-10	F-9	F-8 F-10	K-9	K-8 K-11 L-3 L-5
A-10	A-9 A-11	F-10	F-9 F-11	K-10	K-2 K-11 L-5 L-10
A-11	A-10 A-2 B-9 B-10	F-11	F-10 F-2 H-10	K-11	K-9 K-10 L-7 L-8
B-2	B-3 B-11 C-11 D-10 D-11	G-2	G-3 G-11 I-8 F-6 F-7	L-2	L-3 L-10 M-8 M-9 M-10
B-3	B-2 B-4 D-2 D-5 D-7	G-3	G-2 G-4 I-4 I-5 I-7	L-3	L-2 L-4 M-6 M-7 K-9
B-4	B-3 B-5 C-10 D-8 D-9	G-4	G-3 G-5 I-4 I-5 I-6	L-4	L-3 L-5 K-2 K-3 K-6
B-5	B-4 B-6 C-11 D-9 D-10	G-5	G-4 G-6 I-6 I-7 I-8	L-5	L-4 L-6 K-9 K-8 K-10
B-6	B-5 B-7 C-6 C-7 C-8	G-6	G-5 G-7 I-6 I-7 I-8	L-6	L-5 L-7 K-2 K-4 K-6
B-7	B-6 B-8 C-2 C-10 A-2	G-7	G-6 G-8 F-5 F-7	L-7	L-6 L-8 K-3 K-4 K-11
B-8	B-7 B-9 A-2 A-4 A-7	G-8	G-7 G-9	L-8	L-7 L-9 M-8 K-8 K-11
B-9	B-8 B-10 A-3 A-4 A-11	G-9	G-8 G-10 F-5 F-6 F-7	L-9	L-8 L-11 M-7 M-9 M-11
B-10	B-9 B-11 A-3 A-7 A-11	G-10	G-9 G-11 F-3 F-4 F-8	L-10	L-2 L-11 M-5 M-11 K-10
B-11	B-2 B-10 C-10 A-3 A-4	G-11	G-10 G-2 F-3 F-6 F-8	L-11	L-9 L-10 M-5 M-6 M-10
C-2	C-3 C-11 D-9 B-7	H-2	H-3 H-11 J-4 J-6 J-9	M-2	M-3 M-11 N-8 O-8 O-9
C-3	C-2 C-4 D-5 D-6 D-10	H-3	H-2 H-4 J-3 J-6 J-8	M-3	M-2 M-4 O-8 O-9 O-10
C-4	C-3 C-5 D-7 D-11	H-4	H-3 H-6 J-11	M-4	M-3 M-5 N-8 O-8 0-9
C-5	C-4 C-6 D-8	H-5	H-6 H-7 J-11	M-5	M-4 M-6 N-7 L-10 L-11
C-6	C-5 C-7 B-6	H-6	H-4 H-5	M-6	M-5 M-7 N-7 L-11 L-3
C-7	C-6 C-8 B-6	H-7	H-5 H-9	M-7	M-6 M-8 N-9 L-3 L-9
C-8	C-7 C-9 B-6	H-8	H-9 H-10	M-8	M-7 M-9 N-8 L-8 L-2
C-9	C-8 C-10	H-9	H-7 H-8 F-4	M-9	M-8 M-10 N-9 L-2 L-9
C-10	C-9 C-11 B-4 B-7 B-11	H-10	H-8 H-11 F-2 F-8 F-11	M-10	M-9 M-11 N-9 L-2 L-11
C-11	C-10 C-2 D-8 B-5 B-2	H-11	H-2 H-10 J-10 F-3 F-4	M-11	M-2 M-10 N-7 L-9 L-10
D-2	D-3 D-11 E-3 E-10 B-3	I-2	I-3 I-4	N-2	N-3 N-11 O-5 O-6 O-7
D-3	D-2 D-4 E-4 E-6 E-9	I-3	I-2 I-9	N-3	N-2 N-4 O-2 O-4 O-10
D-4	D-3 D-5 E-2 E-5 E-10	I-4	I-2 I-5 G-3 G-4	N-4	N-3 N-5 O-5
D-5	D-4 D-6 E-11 C-3 B-3	I-5	I-4 I-6 G-3 G-4	N-5	N-4 N-6 O-7
D-6	D-5 D-7 E-7 E-8 C-3	I-6	I-5 I-8 G-4 G-5 G-6	N-6	N-5 N-7 O-5 O-7
D-7	D-6 D-8 E-8 C-4 B-3	I-7	I-8 I-11 G-3 G-5 G-6	N-7	N-6 N-8 M-5 M-6 M-11
D-8	D-7 D-9 C-5 C-11 B-4	I-8	I-6 I-7 G-2 G-5 G-6	N-8	N-7 N-9 M-2 M-4 M-8
D-9	D-8 D-10 C-2 B-4 B-5	I-9	I-3 I-10	N-9	N-8 N-10 M-7 M-9 M-10
D-10	D-9 D-11 C-3 B-2 B-5	I-10	I-9 I-11 J-3 J-4 J-10	N-10	N-9 N-11 O-6
D-11	D-2 D-10 E-11 C-4 B-2	I-11	I-7 I-10 J-2 J-8 J-9	N-11	N-2 N-10 O-6
E-2	E-4 E-11 D-4	J-2	J-3 J-11 I-11	O-2	O-3 O-11 N-3
E-3	E-4 E-5 D-2	J-3	J-2 J-4 H-3 I-10	O-3	O-2 O-4
E-4	E-2 E-3 D-3	J-4	J-3 J-6 H-2 I-10	O-4	O-3 O-5 N-3
E-5	E-E E-6 D-4	J-5	J-7 J-8	O-5	O-4 O-6 N-4 N-6 N-2
E-6	E-5 E-7 D-3	J-6	J-4 J-7 H-2 H-3	O-6	O-5 O-7 N-2 N-10 N-11
E-7	E-6 E-8 D-6	J-7	J-5 J-6	O-7	O-6 O-8 N-2 N-5 N-6
E-8	E-7 E-9 D-6 D-7	J-8	J-5 J-9 H-3 I-11	O-8	O-7 O-9 M-2 M-3 M-4
E-9	E-8 E-10 D-3	J-9	J-8 J-10 H-2 I-11	O-9	O-8 O-10 M-2 M-3 M-4
E-10	E-9 E-11 D-2 D-4	J-10	J-9 J-11 H-11 I-10	O-10	O-9 O-11 M-3 N-3
E-11	E-2 E-10 D-5 D-11	J-11	J-2 J-10 H-4 H-5	O-11	O-2 O-10

Source: T.O. 21M-LGM30G-1-24

Table 1-2. [3] LF Interconnectivity

SQUADRON I		SQUADRON II		SQUADRON III	
LF NO.	ELECTRICALLY ADJACENT LF'S	LF NO.	ELECTRICALLY ADJACENT LF'S	LF NO.	ELECTRICALLY ADJACENT LF'S
A-2	A-4 A-11 B-3 B-5 B-11	F-2	F-3 F-11 G-4 H-3 J-6	K-2	K-3 K-11 L-2 L-9 L-10
A-3	A-4 A-5 B-3 B-5 B-7	F-3	F-2 F-4 G-5 H-3 H-5	K-3	K-2 K-4 L-2 L-9 M-5
A-4	A-2 A-3 B-2 B-4 B-6	F-4	F-3 F-5 G-4 H-3 H-4	K-4	K-3 K-5 L-4 N-7 N-9
A-5	A-3 A-6 B-4 C-2 C-3	F-5	F-4 F-6 G-3 H-4 H-7	K-5	K-4 K-6 L-7 M-6 N-8
A-6	A-5 A-7 B-6 C-3 C-11	F-6	F-5 F-7 G-6 H-7 H-8	K-6	K-5 K-7 L-6 M-4 M-5
A-7	A-6 A-8 B-2 B-7 C-4	F-7	F-6 F-9 G-7 H-4 H-8	K-7	K-6 K-9 L-6 M-6 M-7
A-8	A-7 A-9 B-6 B-8 C-4	F-8	F-9 F-10 G-7 H-6 H-9	K-8	K-10 K-11 L-4 L-8 M-7
A-9	A-8 A-10 B-10 B-11 C-4	F-9	F-7 F-8 G-6 H-5 H-6	K-9	K-7 K-10 L-7 M-5 M-8
A-10	A-9 A-11 B-5 B-10 C-11	F-10	F-8 F-11 G-9 H-8 H-10	K-10	K-8 K-9 L-7 L-8 M-9
A-11	A-2 A-10 B-4 B-11 C-3	F-11	F-2 F-10 H-11 J-5 J-7	K-11	K-2 K-8 L-9 L-10 L-11
B-2	B-3 B-11 A-4 A-7 D-3	G-2	G-3 G-11 I-7 J-2 J-11	L-2	L-3 L-11 K-2 K-3 M-9
B-3	B-2 B-4 A-2 A-3 D-3	G-3	G-2 G-4 F-5 J-3 J-10	L-3	L-2 L-4 M-8 M-10 M-11
B-4	B-3 B-5 A-4 A-5 A-11	G-4	G-3 G-5 F-2 F-4 J-9	L-4	L-3 L-5 K-4 K-8 N-8
B-5	B-4 B-6 A-2 A-3 A-10	G-5	G-4 G-6 F-3 H-7 J-4	L-5	L-4 L-6 M-4 M-7 N-11
B-6	B-5 B-7 A-4 A-6 A-8	G-6	G-5 G-7 F-6 F-9 H-6	L-6	L-5 L-7 K-6 K-7 N-9
B-7	B-6 B-8 A-3 A-7 C-5	G-7	G-6 G-8 F-7 F-8 H-9	L-7	L-6 L-8 K-5 K-9 K-10
B-8	B-7 B-9 A-8 D-5 D-6	G-8	G-7 G-9 I-8 I-9 J-3	L-8	L-7 L-10 K-8 K-10 M-9
B-9	B-8 B-10 D-4 D-5 D-6	G-9	G-8 G-10 F-10 I-8 I-10	L-9	L-10 L-11 K-2 K-3 K-11
B-10	B-9 B-11 A-9 A-10 D-4	G-10	G-9 G-11 H-9 I-10 I-11	L-10	L-8 L-9 K-2 K-11 M-11
B-11	B-2 B-10 A-2 A-9 A-11	G-11	G-2 G-10 H-5 J-2 J-10	L-11	L-2 L-9 K-11 M-10 M-11
C-2	C-3 C-11 A-5 D-2 D-3	H-2	H-3 H-11 I-6 I-7 J-8	M-2	M-3 M-11 O-7 O-8 O-9
C-3	C-2 C-4 A-5 A-6 A-11	H-3	H-2 H-4 F-2 F-3 F-4	M-3	M-2 M-4 O-7 O-8 O-9
C-4	C-3 C-5 A-7 A-8 A-9	H-4	H-3 H-5 F-4 F-5 F-7	M-4	M-3 M-6 K-6 L-5 N-6
C-5	C-4 C-6 B-7 D-7 E-4	H-5	H-4 H-7 F-3 F-9 G-11	M-5	M-6 M-7 K-3 K-6 K-9
C-6	C-5 C-7 D-8 E-3 E-4	H-6	H-7 H-8 F-8 F-9 G-6	M-6	M-4 M-5 K-5 K-7 N-7
C-7	C-6 C-8 E-2 E-5 E-6	H-7	H-5 H-6 F-5 F-6 G-5	M-7	M-5 M-8 K-7 K-8 L-5
C-8	C-7 C-9 E-5 E-7 D-8	H-8	H-6 H-9 F-6 F-7 F-10	M-8	M-7 M-9 K-9 L-3 N-10
C-9	C-8 C-10 E-2 E-7 E-8	H-9	H-8 H-10 F-8 G-7 G-10	M-9	M-8 M-10 K-10 L-2 L-8
C-10	C-9 C-11 E-2 E-5 E-6	H-10	H-9 H-11 F-10 I-3 I-4	M-10	M-9 M-11 L-3 L-11 N-11
C-11	C-2 C-10 A-6 A-10 D-2	H-11	H-2 H-10 F-11 I-5 I-6	M-11	M-2 M-10 L-3 L-10 L-11
D-2	D-3 D-11 C-2 C-11 E-3	I-2	I-3 I-9 J-2 J-4 J-6	N-2	N-3 N-11 O-3 O-6 O-10
D-3	D-2 D-4 B-2 B-3 C-2	I-3	I-2 I-4 H-10 J-3 J-5	N-3	N-2 N-4 O-4 O-6 O-11
D-4	D-3 D-5 B-9 B-10 E-3	I-4	I-3 I-5 H-10 J-5 J-11	N-4	N-3 N-5 O-2 O-5 O-11
D-5	D-4 D-6 B-8 B-9 E-8	I-5	I-4 I-6 H-11 J-10 J-11	N-5	N-4 N-6 O-3 O-5 O-10
D-6	D-5 D-7 B-8 B-9 E-6	I-6	I-5 I-7 H-2 H-11 J-6	N-6	N-5 N-7 M-4 O-4 O-11
D-7	D-6 D-8 C-5 E-8 E-11	I-7	I-6 I-8 G-2 H-2 J-7	N-7	N-6 N-8 K-4 M-6 O-7
D-8	D-7 D-9 C-6 C-8 E-9	I-8	I-7 I-10 G-8 G-9 J-8	N-8	N-7 N-9 K-5 L-4 O-8
D-9	D-8 D-10 E-9 E-10 E-11	I-9	I-2 I-11 G-8 J-4 J-9	N-9	N-8 N-10 K-4 L-6 O-10
D-10	D-9 D-11 E-9 E-10 E-11	I-10	I-8 I-11 G-9 G-10 J-8	N-10	N-9 N-11 M-8 O-6 O-9
D-11	D-2 D-10 E-4 E-7 E-10	I-11	I-9 I-10 G-10 J-7 J-9	N-11	N-2 N-10 L-5 M-10 O-2
E-2	E-4 E-11 C-7 C-9 C-10	J-2	J-3 J-11 G-2 G-11 I-2	O-2	O-3 O-11 N-4 N-11
E-3	E-4 E-5 C-6 D-2 D-4	J-3	J-2 J-5 G-3 G-8 I-3	O-3	O-2 O-4 N-2 N-5
E-4	E-2 E-3 C-5 C-6 D-11	J-4	J-5 J-6 G-5 I-2 I-9	O-4	O-3 O-5 N-3 N-6
E-5	E-3 E-6 C-7 C-8 C-10	J-5	J-3 J-4 F-11 I-3 I-4	O-5	O-4 O-6 N-4 N-5
E-6	E-5 E-7 C-7 C-10 D-6	J-6	J-4 J-7 F-2 I-2 I-6	O-6	O-5 O-7 N-2 N-3 N-10
E-7	E-6 E-8 C-8 C-9 D-11	J-7	J-6 J-8 F-11 I-7 I-11	O-7	O-6 O-8 M-2 M-3 N-7
E-8	E-7 E-9 C-9 D-5 D-7	J-8	J-7 J-9 H-2 I-8 I-10	O-8	O-7 O-9 M-2 M-3 N-8
E-9	E-8 E-10 D-8 D-9 D-10	J-9	J-8 J-10 G-4 I-9 I-11	O-9	O-8 O-10 M-2 M-3 N-10
E-10	E-9 E-11 D-9 D-10 D-11	J-10	J-9 J-11 G-3 G-11 I-5	O-10	O-9 O-11 N-2 N-5 N-9
E-11	E-2 E-10 D-7 D-9 D-10	J-11	J-2 J-10 G-2 I-4 I-5	O-11	O-2 O-10 N-3 N-4 N-6

Source: T.O. 21M-LGM30G-1-21

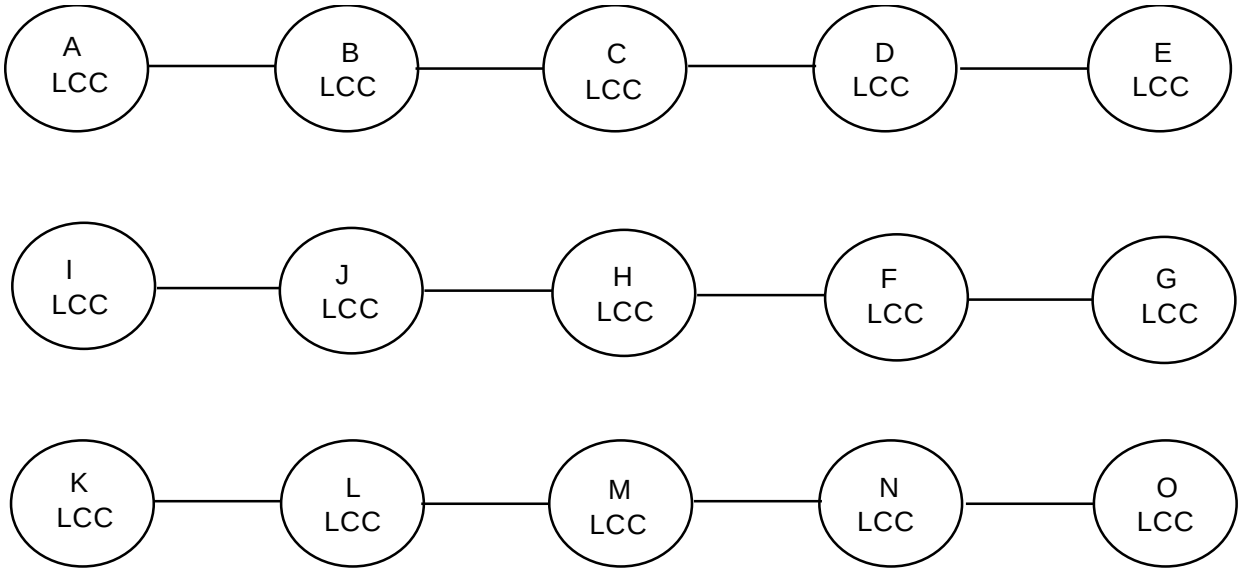
Table 1-3. [5] LF Interconnectivity

SQUADRON I		SQUADRON II	
LF NO.	ELECTRICALLY ADJACENT LF'S	LF NO.	ELECTRICALLY ADJACENT LF'S
A-2	A-4 A-11 B-4 E-2 E-11	F-2	F-4 F-11 G-2 G-3 H-9
A-3	A-4 A-5 C-9 C-10 E-5	F-3	F-4 F-6 G-4 H-9 H-10
A-4	A-2 A-3 B-3 B-7 E-3	F-4	F-2 F-3 H-10 H-11 J-10
A-5	A-3 A-6 B-8 E-3 E-9	F-5	F-6 F-7 I-8 J-4 J-9
A-6	A-5 A-7 B-7 E-6 E-7	F-6	F-3 F-5 G-7 J-2 J-11
A-7	A-6 A-8 B-6 E-6 E-7	F-7	F-5 F-8 H-8 J-3 J-10
A-8	A-7 A-9 E-8 E-9 E-11	F-8	F-7 F-9 G-3 G-8 J-2
A-9	A-8 A-10 D-10 E-8 E-10	F-9	F-8 F-10 G-9 G-10 J-11
A-10	A-9 A-11 D-10 E-10 E-11	F-10	F-9 F-11 G-9 G-10 G-11
A-11	A-2 A-10 B-5 B-6 D-11	F-11	F-2 F-10 G-2 G-10 G-11
B-2	B-3 B-11 C-4 C-11 D-4	G-2	G-3 G-11 F-2 F-11 H-6
B-3	B-2 B-4 A-4 C-3 C-5	G-3	G-2 G-4 F-2 F-8 H-2
B-4	B-3 B-5 A-2 C-2 C-6	G-4	G-3 G-5 F-3 H-3 I-4
B-5	B-4 B-6 A-11 C-3 E-4	G-5	G-4 G-6 H-5 H-11 J-9
B-6	B-5 B-7 A-7 A-11 C-2	G-6	G-5 G-7 H-4 I-3 J-8
B-7	B-6 B-8 A-4 A-6 E-3	G-7	G-6 G-8 F-6 H-5 J-7
B-8	B-7 B-9 A-5 C-10 E-2	G-8	G-7 G-9 F-8 H-7 J-6
B-9	B-8 B-10 C-10 D-10 D-11	G-9	G-8 G-10 F-9 F-10 J-5
B-10	B-9 B-11 C-8 C-9 D-11	G-10	G-9 G-11 F-9 F-10 F-11
B-11	B-2 B-10 C-7 C-11 D-3	G-11	G-2 G-10 F-10 F-11 H-11
C-2	C-3 C-11 B-4 B-6 D-2	H-2	H-3 H-11 G-3 I-3 I-11
C-3	C-2 C-4 B-3 B-5 D-3	H-3	H-2 H-5 G-4 I-2 I-4
C-4	C-3 C-5 B-2 D-2 D-4	H-4	H-5 H-6 G-6 I-6 I-11
C-5	C-4 C-6 B-3 D-4 D-5	H-5	H-3 H-4 G-5 G-7 I-5
C-6	C-5 C-7 B-4 D-3 D-6	H-6	H-4 H-7 G-2 I-7 I-10
C-7	C-6 C-8 B-11 D-7 D-9	H-7	H-6 H-8 G-8 I-7 J-11
C-8	C-7 C-9 B-10 D-8 E-2	H-8	H-7 H-9 F-7 I-9 J-9
C-9	C-8 C-10 A-3 B-10 D-6	H-9	H-8 H-10 F-2 F-3 I-2
C-10	C-9 C-11 A-3 B-8 B-9	H-10	H-9 H-11 F-3 F-4 I-3
C-11	C-2 C-10 B-2 B-11 D-5	H-11	H-2 H-10 F-4 G-5 G-11
D-2	D-3 D-4 C-2 C-4 E-4	I-2	I-3 I-11 H-3 H-9 J-3
D-3	D-2 D-11 B-11 C-3 C-6	I-3	I-2 I-4 G-6 H-2 H-10
D-4	D-2 D-5 B-2 C-4 C-5	I-4	I-3 I-5 G-4 H-3 J-4
D-5	D-4 D-6 C-5 C-11 E-5	I-5	I-4 I-6 H-5 J-4 J-5
D-6	D-5 D-9 C-6 C-9 E-5	I-6	I-5 I-7 H-4 J-6 J-7
D-7	D-8 D-9 C-7 E-6 E-7	I-7	I-6 I-8 H-6 H-7 J-8
D-8	D-7 D-10 C-8 E-4 E-8	I-8	I-7 I-10 F-5 J-8 J-10
D-9	D-6 D-7 C-7 E-9 E-10	I-9	I-10 I-11 H-8 J-5 J-7
D-10	D-8 D-11 A-9 A-10 B-9	I-10	I-8 I-9 H-6 J-2 J-6
D-11	D-3 D-10 A-11 B-9 B-10	I-11	I-2 I-9 H-2 H-4 J-3
E-2	E-3 E-10 A-2 B-8 C-8	J-2	J-3 J-11 F-6 F-8 I-10
E-3	E-2 E-4 A-4 A-5 B-7	J-3	J-2 J-4 F-7 I-2 I-11
E-4	E-3 E-5 B-5 D-2 D-8	J-4	J-3 J-5 F-5 I-4 I-5
E-5	E-4 E-6 A-3 D-5 D-6	J-5	J-4 J-7 G-9 I-5 I-9
E-6	E-5 E-7 A-6 A-7 D-7	J-6	J-7 J-8 G-8 I-6 I-10
E-7	E-6 E-8 A-6 A-7 D-7	J-7	J-5 J-6 G-7 I-6 I-9
E-8	E-7 E-9 A-8 A-9 D-8	J-8	J-6 J-9 G-6 I-7 I-8
E-9	E-8 E-11 A-5 A-8 D-9	J-9	J-8 J-10 F-5 G-5 H-8
E-10	E-2 E-11 A-9 A-10 D-9	J-10	J-9 J-11 F-4 F-7 I-8
E-11	E-9 E-10 A-2 A-8 A-10	J-11	J-2 J-10 F-6 F-9 H-7

Table 1-3. [5] LF Interconnectivity (Continued)

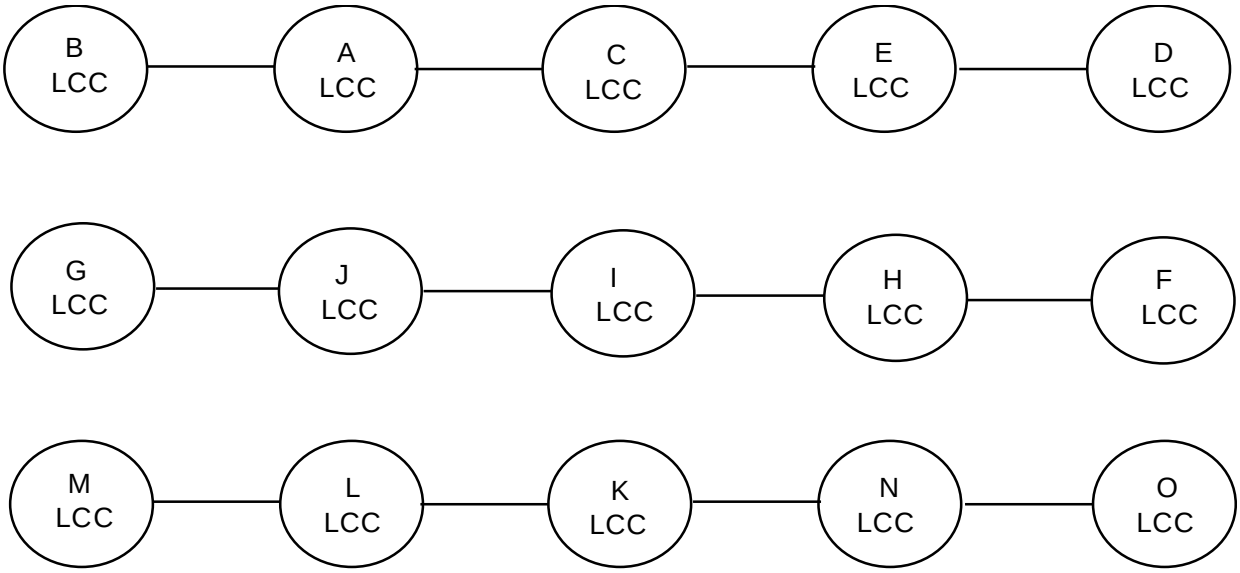
SQUADRON III		SQUADRON IV	
LF NO.	**ELECTRICALLY ADJECENT LF'S**	**LF NO.**	**ELECTRICALLY ADJACENT LF'S**
K-2	K-3 K-11 L-3 L-5 M-10	P-2	P-3 P-10 S-9 S-10 S-11
K-3	K-2 K-4 L-6 L-8 M-11	P-3	P-2 P-4 S-6 S-7 S-9
K-4	K-3 K-5 L-7 M-2 M-3	P-4	P-3 P-5 R-3 R-7 S-7
K-5	K-4 K-6 L-5 M-3 M-11	P-5	P-4 P-6 R-5 R-6 S-8
K-6	K-5 K-7 L-9 M-9 O-4	P-6	P-5 P-7 Q-4 Q-5 R-3
K-7	K-6 K-9 M-10 O-5 O-11	P-7	P-6 P-8 Q-5 Q-6 Q-7
K-8	K-9 K-10 L-10 O-2 O-4	P-8	P-7 P-9 Q-4 Q-8 Q-11
K-9	K-7 K-8 L-4 L-9 O-7	P-9	P-8 P-11 Q-3 Q-6 S-8
K-10	K-8 K-11 L-2 L-11 O-3	P-10	P-2 P-11 Q-6 S-6 S-9
K-11	K-2 K-10 L-2 L-4 O-3	P-11	P-9 P-10 Q-5 Q-7 S-7
L-2	L-4 L-11 K-10 K-11 O-8	Q-2	Q-9 Q-10 T-4 T-10 T-11
L-3	L-4 L-5 K-2 M-5 O-3	Q-3	Q-4 Q-10 P-9 T-7 T-9
L-4	L-2 L-3 K-9 K-11 M-3	Q-4	Q-3 Q-5 P-6 P-8 T-8
L-5	L-3 L-7 K-2 K-5 M-4	Q-5	Q-4 Q-6 P-6 P-7 P-11
L-6	L-7 L-8 K-3 M-2 N-2	Q-6	Q-5 Q-7 P-7 P-9 P-10
L-7	L-5 L-6 K-4 M-6 N-5	Q-7	Q-6 Q-8 P-7 P-11 T-8
L-8	L-6 L-9 K-3 M-5 O-2	Q-8	Q-7 Q-11 P-8 T-7 T-8
L-9	L-8 L-10 K-6 K-9 M-4	Q-9	Q-2 Q-11 T-2 T-3 T-11
L-10	L-9 L-11 K-8 O-9 O-11	Q-10	Q-2 Q-3 T-4 T-5 T-10
L-11	L-2 L-10 K-10 N-10 O-10	Q-11	Q-8 Q-9 P-8 T-7 T-9
M-2	M-3 M-11 K-4 L-6 N-4	R-2	R-4 R-11 S-3 S-4 S-5
M-3	M-2 M-4 K-4 K-5 L-4	R-3	R-4 R-5 P-4 P-6 S-4
M-4	M-3 M-5 L-5 L-9 N-3	R-4	R-2 R-3 S-2 S-4 S-5
M-5	M-4 M-6 L-3 L-8 N-3	R-5	R-3 R-6 P-5 S-5 S-6
M-6	M-5 M-7 L-7 N-5 N-11	R-6	R-5 R-7 P-5 T-4 T-6
M-7	M-6 M-8 N-8 N-9 O-6	R-7	R-6 R-8 P-4 S-11 T-6
M-8	M-7 M-9 N-8 N-9 O-5	R-8	R-7 R-9 S-2 T-2 T-9
M-9	M-8 M-10 K-6 N-4 N-6	R-9	R-8 R-10 T-3 T-10 T-11
M-10	M-9 M-11 K-2 K-7 N-2	R-10	R-9 R-11 S-3 S-10 T-3
M-11	M-2 M-10 K-3 K-5 N-5	R-11	R-2 R-10 S-2 S-3 T-2
N-2	N-3 N-11 L-6 M-10 O-7	S-2	S-3 S-11 R-4 R-8 R-11
N-3	N-2 N-4 M-4 M-5 O-6	S-3	S-2 S-4 R-2- R-10 R-11
N-4	N-3 N-5 M-2 M-9 O-8	S-4	S-3 S-5 R-2 R-3 R-4
N-5	N-4 N-6 L-7 M-6 M-11	S-5	S-4 S-6 R-2 R-4 R-5
N-6	N-5 N-7 M-7 M-9 O-6	S-6	S-5 S-7 P-3 P-10 R-5
N-7	N-6 N-8 M-7 O-5 O-7	S-7	S-6 S-8 P-3 P-4 P-11
N-8	N-7 N-9 M-8 O-2 O-9	S-8	S-7 S-9 P-5 P-9 T-5
N-9	N-8 N-10 M-8 O-4 O-8	S-9	S-8 S-10 P-2 P-3 P-10
N-10	N-9 N-11 L-11 O-10 O-11	S-10	S-9 S-11 P-2 R-10 T-6
N-11	N-2 N-10 M-6 O-9 O-10	S-11	S-2 S-10 P-2 R-7 T-5
O-2	O-3 O-11 K-8 L-8 N-8	T-2	T-3 T-4 Q-9 R-8 R-11
O-3	O-2 O-4 K-10 K-11 L-3	T-3	T-2 T-11 Q-9 R-9 R-10
O-4	O-3 O-5 K-6 K-8 N-9	T-4	T-2 T-5 Q-2 Q-10 R-6
O-5	O-4 O-6 K-7 M-8 N-7	T-5	T-4 T-6 Q-10 S-8 S-11
O-6	O-5 O-7 M-7 N-3 N-6	T-6	T-5 T-7 R-6 R-7 S-10
O-7	O-6 O-8 K-9 N-2 N-7	T-7	T-6 T-8 Q-3 Q-8 Q-11
O-8	O-7 O-9 L-2 N-4 N-9	T-8	T-7 T-9 Q-4 Q-7 Q-8
O-9	O-8 O-10 L-10 N-8 N-11	T-9	T-8 T-10 Q-3 Q-11 R-8
O-10	O-9 O-11 L-11 N-10 N-11	T-10	T-9 T-11 Q-2 Q-10 R-9
O-11	O-2 O-10 K-7 L-10 N-10	T-11	T-3 T-10 Q-2 Q-9 R-9

SOURCE: T.O. 21M-LGM30G-1-22



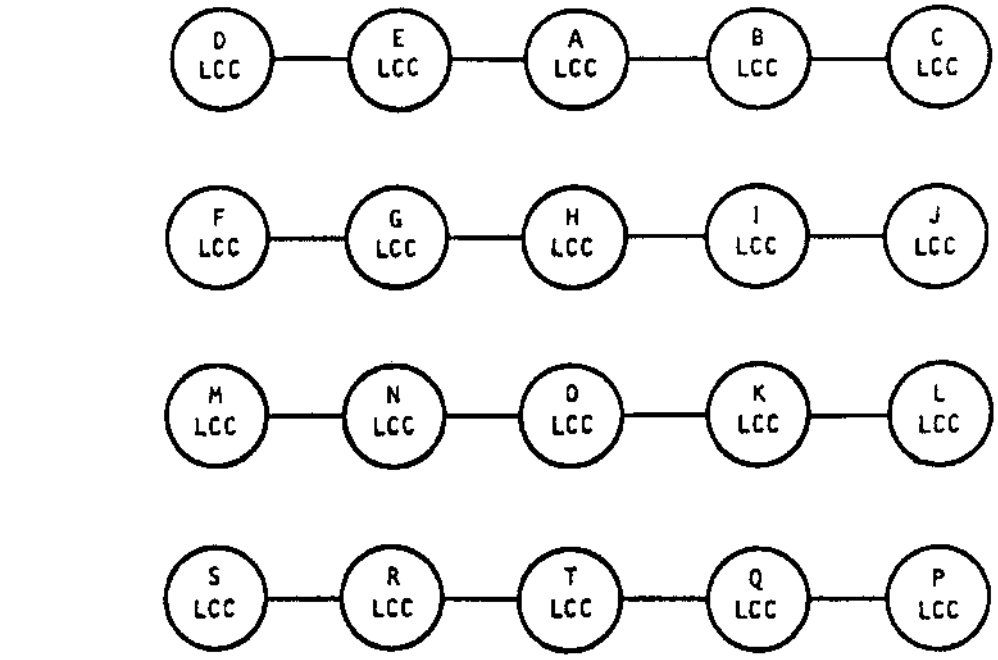
SOURCE: T.O. 21M-LGM30G-1-24

Figure 1-9. [1] Hardened Voice Channel (HVC) Interconnectivity



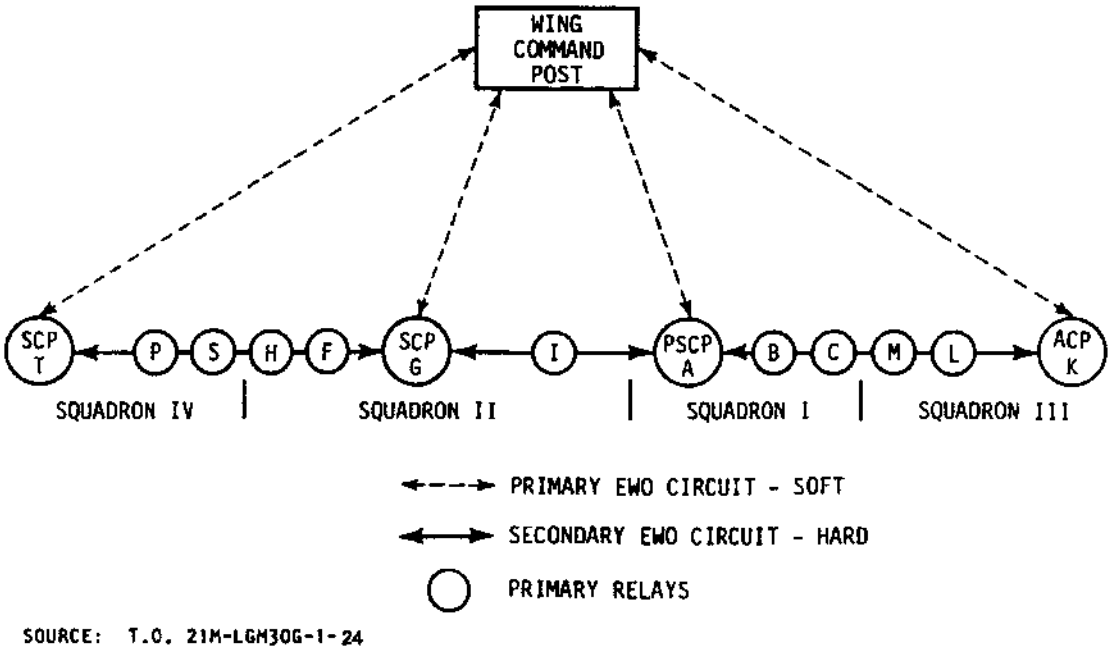
SOURCE: T.O. 21M-LGM30G-1-22

Figure 1-10. [3] Hardened Voice Channel (HVC) Interconnectivity



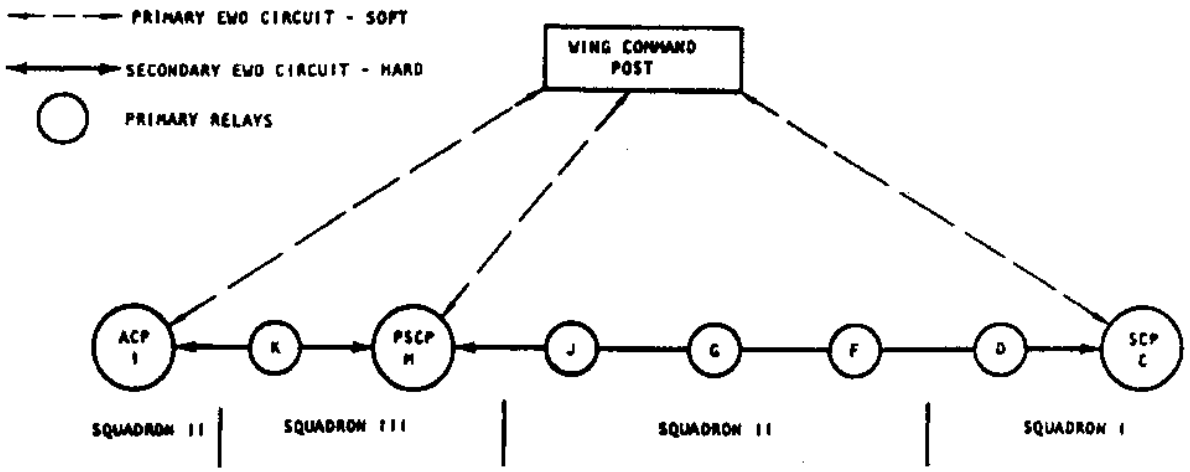
SOURCE: T.O. 21M-LGM30G-1-22

Figure 1-11. [5] Hardened Voice Channel (HVC) Interconnectivety



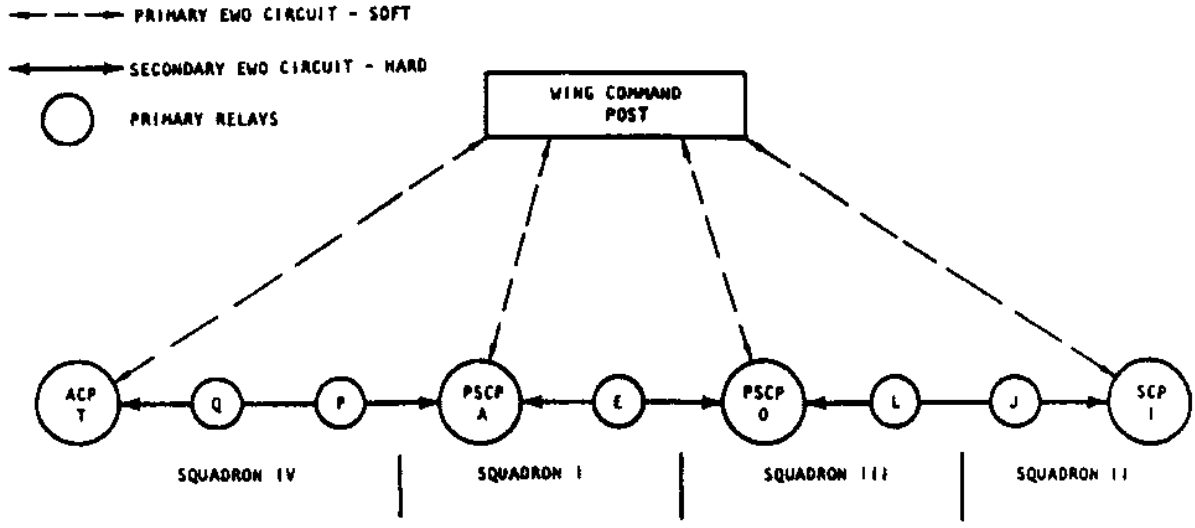
SOURCE: T.O. 21M-LGM30G-1-24

Figure 1-12. [1] Emergency War Order Network



SOURCE: T.O. 21M-LGM30G-1-21

Figure 1-13. [3] Emergency War Order Network



SOURCE: T.O. 21M-LGM30G-1-22

Figure 1-14. [5] Emergency War Order Network

1-4.5. SAC Digital Network (SACDIN). The SAC digital network is a landline digital communications system that supports the command control communications requirements. SACDIN has the capability to deliver Emergency Action Messages (EAMs) in not more than 15 seconds. The SAC digital network system is shown in Figures 1-15, 1-16 and 1-17.

1-4.6. Expanded Missile Data Analysis System (EMDAS). The EMDAS is a network of Hewlett Packard 1000-series computer systems. EMDAS is located at the operational Minuteman wings, at the Vandenberg AFB test launch facility, at the Missile Guidance Set repair depot at Newark AFB, and at the EMDAS computer center at Ogden ALC. The EMDAS employs a collection of computer software that is used to support the maintenance, data analysis and repair of the G&C. The EMDAS software is comprised of three major software components: the Maintenance Management Program (MMP) software, the Performance Assessment Software (PAS), and the Modem Handler software. The Rockwell personnel at the AFSPACECOM (AFSPC) operational Wings, Vandenberg AFB, Newark AFB or within the Guidance Assessment Engineering Unit at Ogden ALC can assist in the execution or interpretation of any of the existing MPP, PAS or Modem Handler software products.

1-4.6.1. MMP System. The MMP system is a software tool that is used by AFSPC maintenance personnel in the field to track all AFSPC maintenance activities. This includes scheduling of work orders, maintenance teams, equipment, security personnel, and vehicles. This system provides the history of all work previously performed and all work identified to be accomplished for each site in the wing.

1-4.6.2. PAS System. The PAS system is a software tool that provides Inertial Performance Data (IPD) and Launch Facility Activity Data (LFAD) that is used to assess the current performance of the Minuteman force. This data is also used to identify trends in the system that are used for future modifications to the G&C and operational software. IPD and LFAD for every G&C that fails in the field are also sent to the repair depot and are used to assist in the identification and repair of the field failure.

1-4.6.3. Modem Handler. The Modem Handler is the software communication system that forms the EMDAS network. This software is the means of communication of data from any EMDAS location to any other EMDAS location. The normal flow of data is from the operational wings or Vandenberg AFB, to Ogden ALC, to Newark AFB.

1-5. LCC STATUS MONITORING RESPONSIBILITIES. Each LCC in the squadron monitors the command/interrogation messages transmitted by other LCCs in the squadron, and the status replies of each LF to those commands or interrogations. Each command received and each change in the operational status reply of an LF is processed and stored in the WSP memory. The stored data is periodically saved on the Bulk Storage/Loader (BS/L) for use on system restart. The monitoring responsibility of the LCC (primary or secondary -- also called "auxiliary") is shown in Table 1-4 and determines the detail of LF

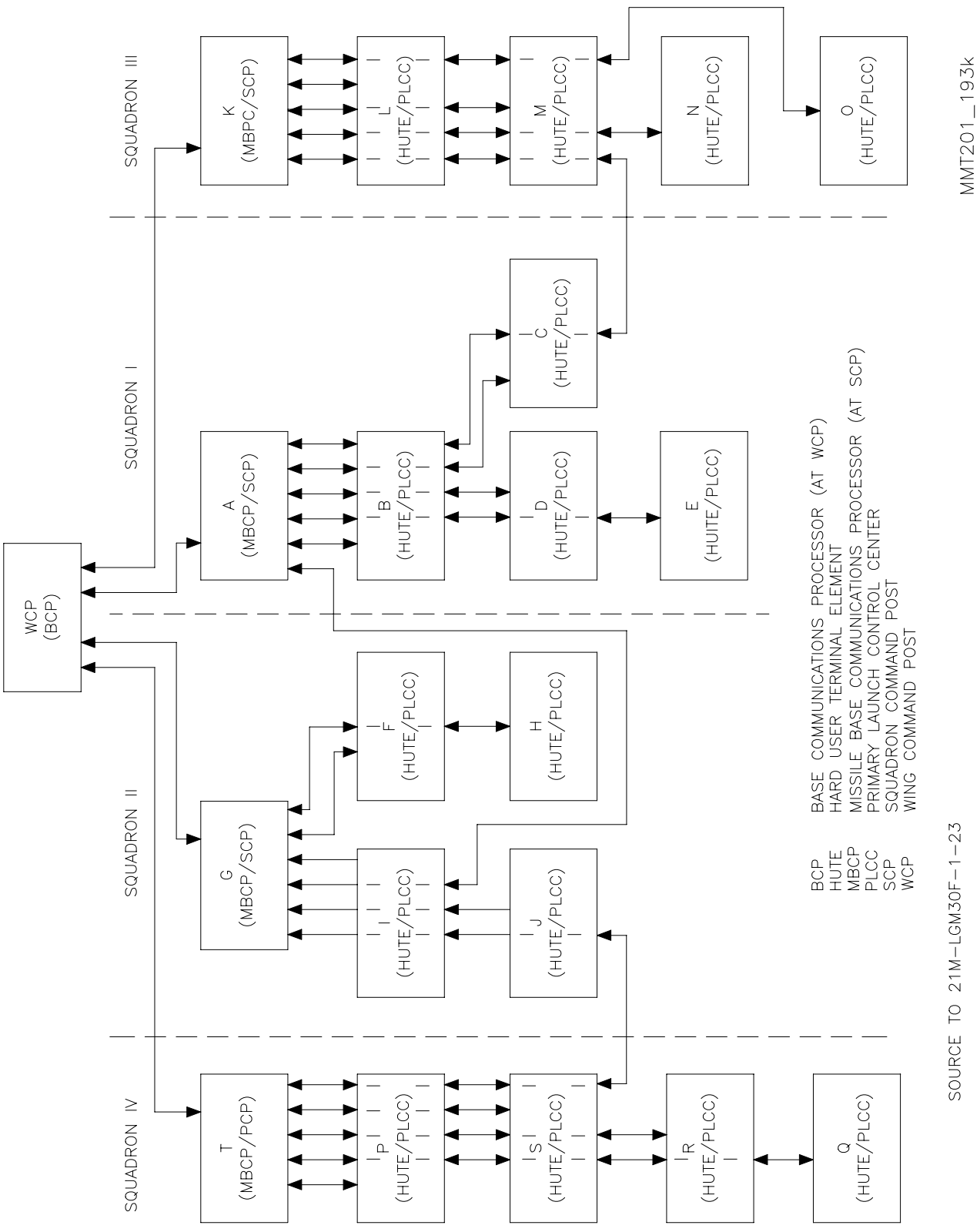


Figure 1-15. [1][1X] SAC Digital Network

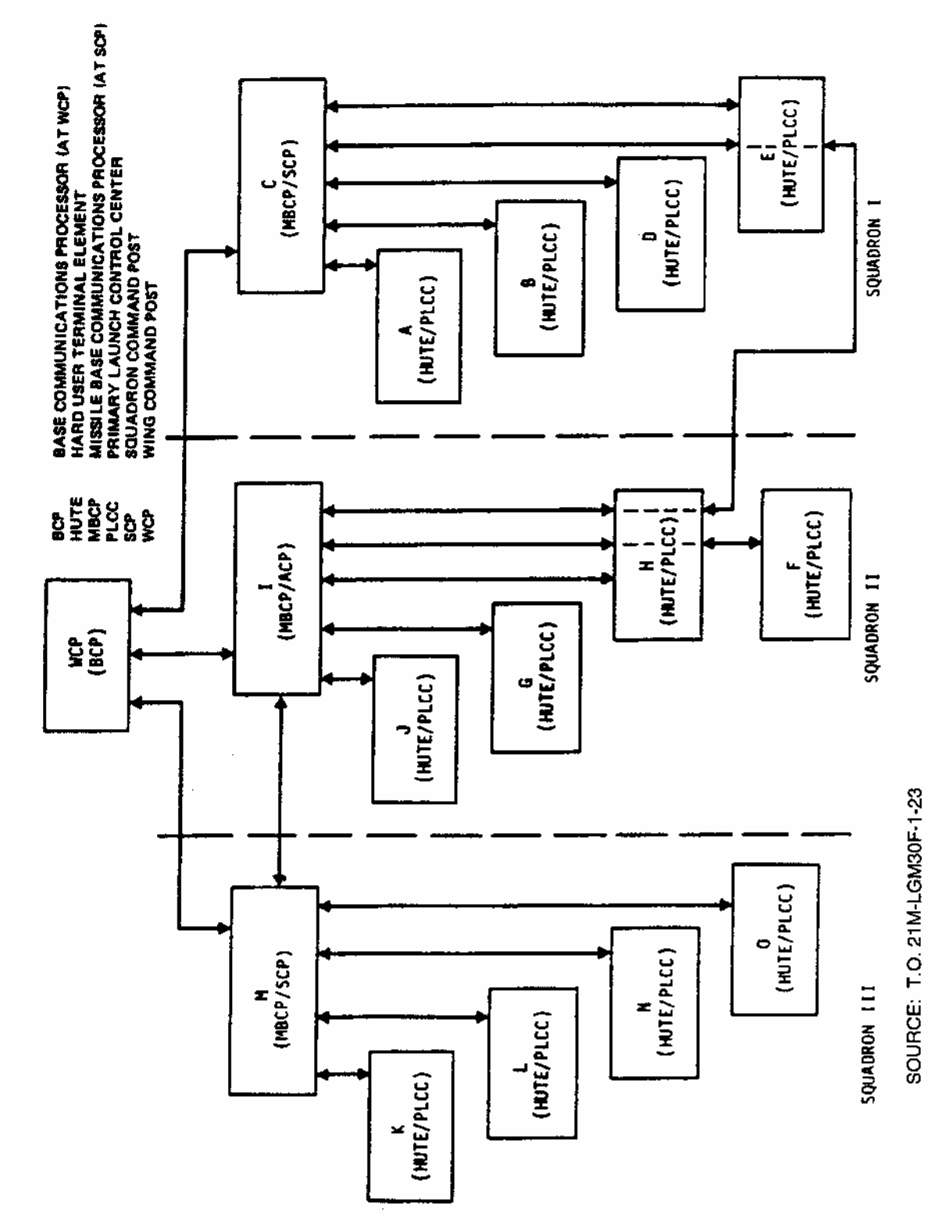
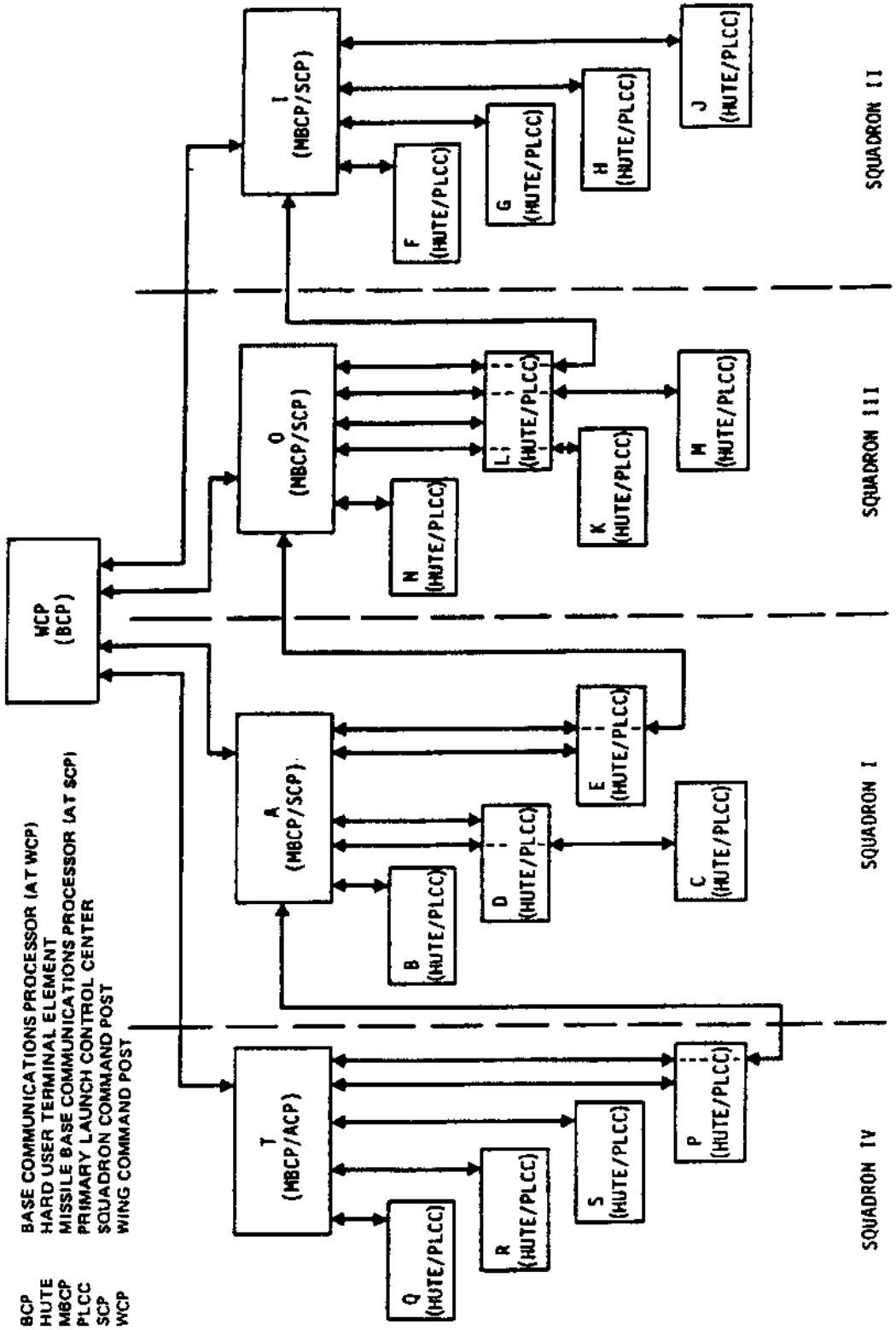


Figure 1-16. [3] SAC Digital Network (SACDIN)



SOURCE: T.O. 21M-LGM30F-1-23

Figure 1-17. [5] SAC Digital Network (SACDIN)

Table 1-4. Primary, Secondary, Automatic and Manual Takeover Flight Responsibility (Normal Mode)

INACTIVE LCF(S)	LCF RESPONSIBILITY									
	LCF 1		LCF 2		LCF 3		LCF 4		LCF 5	
	PRI	SEC	PRI	SEC	PRI	SEC	PRI	SEC	PRI	SEC
None	1	5	2	1	3	2	4	3	5	4
1	-	-	1,2	5	3	1,2	4	3	5	4
2	1	5	-	-	2,3	1	4	2,3	5	4
3	1	5	2	1	-	-	3,4	2	5	3,4
4	1	4,5	2	1	3	2	-	-	4,5	3
5	1,5	4	2	1,5	3	2	4	3	-	-
1,2	-	-	-	-	2,3	1,5	4	2,3	1,5	4
1,3	-	-	1,2	5	-	-	3,4	1,2	5	3,4
1,4	-	-	1,2	4,5	3	1,2	-	-	4,5	3
1,5	-	-	1,2	4,5	3	1,2	4,5	3	-	-
2,3	1,2	5	-	-	-	-	3,4	1,2	5	3,4
2,4	1	4,5	-	-	2,3	1	-	-	4,5	2,3
2,5	1,5	4	-	-	2,3	1,5	4	2,3	-	-
3,4	1	4,5	2,3	1	-	-	-	-	4,5	2,3
3,5	1,5	3,4	2	1,5	-	-	3,4	2	-	-
4,5	1,5	3,4	2	1,5	3,4	2	-	-	-	-
1,2,3	-	-	-	-	-	-	2,3,4	1,5	1,5	2,3,4
1,2,4	-	-	-	-	1,2,3	4,5	-	-	4,5	1,2,3
1,2,5	-	-	-	-	1,2,3	4,5	4,5	1,2,3	-	-
1,3,4	-	-	1,2	3,4,5	-	-	-	-	3,4,5	1,2
1,3,5	-	-	1,2,5	3,4	-	-	3,4	1,2,5	-	-
1,4,5	-	-	1,2,5	3,4	3,4	1,2,5	-	-	-	-
2,3,4	1,2	3,4,5	-	-	-	-	-	-	3,4,5	1,2
2,3,5	1,5	2,3,4	-	-	-	-	2,3,4	1,5	-	-
2,4,5	1,4,5	2,3	-	-	2,3	1,4,5	-	-	-	-
3,4,5	1,4,5	2,3	2,3	1,4,5	-	-	-	-	-	-
1,2,3,4	-	-	-	-	-	-	-	-	1,2,3,4,5	-
1,2,3,5	-	-	-	-	-	-	1,2,3,4,5	-	-	-
1,2,4,5	-	-	-	-	1,2,3,4,5	-	-	-	-	-
1,3,4,5	-	-	1,2,3,4,5	-	-	-	-	-	-	-
2,3,4,5	1,2,3,4,5	-	-	-	-	-	-	-	-	-
1,2,3,4,5	-	-	-	-	-	-	-	-	-	-

Source: T.O. 21M-LGM30G-1-22

status indications presented by the WSP. Major status is displayed in the Flight Status Display area of the Visual Display Unit (VDU) for the flight selected from the pop-up menu associated with the Selected Flight box. For certain changes of status within the squadron, alarms are presented in the Alarms area of the VDU, and Action Pending Queue (APQ) entries are created to allow the Missile Combat Crew Member (MCCM) to obtain further details of the nature of the alarm. The various VDU display areas are described in paragraph 1-6. In addition, the status changes are recorded in the Crew Log. A listing of Alarms, Flight Status Display entries, and Crew Log entries associated with status changes is given in Section VI, Table 6-6. This table should be consulted for specific text associated with the status changes described in the following subparagraphs. The anti-jam mode of operation of Table 1-5 is subject to the constraint that auxiliary responsibility is not dropped until the inactive LCC resumes valid transmissions. This constraint is already built into the portion of the table corresponding to normal transmission mode.

1-5.1. Primary Responsibility. Primary responsibility is defined as automatic status interrogations and complete status monitoring of a flight. Each LCC has primary monitoring responsibility for the flight(s) selected by the MCCM for Automatic Flight Interrogation (AFI), and, if automatic flight takeover is selected, for its own numbered flight and any flights that have been taken over. The LCC sends OSIs in a round-robin fashion to the LFs in the flight(s) for which it has primary responsibility. In order to maintain the status of LFs the LCC has responsibilities for, each LCC will interrupt command queues and RDC operations to send interrogations. Each LCC will use at least one slot out of four time slots for OSI transmittal. The number of OSI slots in each frame of four time slots are shown in Table 1-6. The WSP presents and logs the greatest detail of status indications for these LFs. Refer to Table 6-6 for status indications that occur at the primary monitoring LCC for the LF status changes. Status changes for any flight displayed in the Flight/Squadron Status window will be provided as if that flight were primary. Normally, primary flight(s) should be selected for display. If, however, a non-primary flight is being displayed, alarms and corresponding APQ entries are provided for all alarmable status changes associated with primary flights. A Site Address Plug (SAP) is used to designate the LCC's wing, squadron, and flight addresses.

1-5.2. Secondary Responsibility. Secondary responsibility is defined as automatic monitoring of partial status of a flight. Refer to Table 6-6 for status indication that occur at LCCs with secondary responsibility for the LF status changes. Each LCC has secondary responsibility for each flight that is one number lower than a flight for which the LCC has primary responsibility. This rule is subject to the provisions that within any LCC primary responsibilities take precedence over secondary responsibilities (i.e., primary and secondary responsibilities are mutually exclusive). Also, flight 5 is considered one number lower than flight 1. When automatic flight takeover is active, each LCC has primary and secondary responsibility as defined by Table 1-4, plus any that occur due to manual selection of AFI for a flight, subject to the rules above.

1-5.3. Squadron-Wide Responsibility. Refer to Table 6-6 for status indications that occur at all LCCs for the LF status changes.

Table 1-5. Primary, Secondary, Automatic, and Manual Takeover Flight Responsibility (Anti-Jam Mode)

INACTIVE LCF(S)	DOWN LCC TAKEN OVER BY		
1	1 → 2		
2	2 → 3		
3	3 → 4		
4	4 → 5		
5	5 → 1		
1-2	1 → 5	2 → 3	
1-3	1 → 2	3 → 4	
1-4	1 → 2	4 → 5	
1-5	1 → 2	5 → 4	
2-3	2 → 1	3 → 4	
2-4	2 → 3	4 → 5	
2-5	2 → 3	5 → 1	
3-4	3 → 2	4 → 5	
3-5	3 → 4	5 → 1	
4-5	4 → 3	5 → 1	
1-2-3	1 → 5	3 → 4	
1-2-4		2 → 3	4 → 5
1-2-5		2 → 3	5 → 4
1-3-4	1 → 2		4 → 5
1-3-5	1 → 2	3 → 4	
1-4-5	1 → 2	4 → 3	
2-3-4	2 → 1		4 → 5
2-3-5		3 → 4	5 → 1
2-4-5	2 → 3		5 → 1
3-4-5	3 → 2		5 → 1

→ equals automatic flight takeover.

NOTE: Refer to Normal Mode portion of table for secondary monitoring responsibilities.

Source: T.O. 21M-LGM30G-1-22

Table 1-6. OSI Slot Usage

OSI FRAME			
NUMBER OF SLOTS ASSIGNED	**NUMBER OF FLIGHTS ASSIGNED**	**MINIMUM CONSECUTIVE OSI SLOTS**	**MAXIMUM CONSECUTIVE OSI SLOTS**
1	1 2 3 to 5	1 2 3	2 3 4*
2	1 to 2 3 to 4 5	1 2 3	2 3 4*
3	1 to 2 3 to 5	1 2	2 3
4	1 to 3 4 to 5	1 2	2 3
5	1 to 5	1	2

NOTES:

1. These slot rules are preempted for the clear text PLCA and the first RSI/RSR transmission for a specific out-of-sync condition shall take precedence over OSI slot rules.

2. Upon the (*) conditions above, the fourth OSI slot shall be preempted by any message of priority level 2 or 3 or 4, or by an RDA or RDH when acting as a monitor LCC for RDC.

Source: S-133-36000

1-5.4. Automatic Flight Takeover. Automatic flight takeover is the automatic assumption by an LCC of the primary and secondary responsibilities associated with another LCC that has discontinued its interrogations for any reason. When automatic flight takeover is active, each LCC has assigned automatic flight takeover responsibility for the four other flights as shown in Tables 1-4 and 1-5. An LCC monitors for valid OSIs addressed to each flight for which automatic takeover (sometimes called "auxiliary responsibility") is assigned. Monitored OSIs must be received in the same mode as that in which the LCC is transmitting before being considered as valid. Thus, an auxiliary LCC transmitting in the encrypted mode will not consider clear text OSIs as valid OSIs. An LCC performs automatic takeover when valid OSIs addressed to a flight for which it has assigned auxiliary responsibility are not detected during a 32-second period. In Tables 1-4 and 1-5, this condition is abbreviated as "Inactive LCF".

1-5.5. Assumption of Interrogation Responsibilities. Under normal conditions, each LCC will interrogate two of its local flight of ten LFs with automatic OSIs each time the LCC's assigned time slot comes up. In executing automatic flight takeover, the LCC's transmissions to its own primary flight(s) and its assumed primary flight(s) will occur within its own currently selected time slot(s). Whenever the WSP automatically assumes interrogations for another flight, an alarm, an APQ entry, an update to the LCC Summary Display, and Crew Log entries occur at that LCC: (1) the alarm indicates an LCC status change; (2) the APQ entry for LCC status change is created (if necessary) and alarmed; (3) the "AFI" field in the LCC Summary Display is updated to show the total set of flights being interrogated by the LCC; and (4) a Crew Log entry indicating the assumed responsibility and the totality of flights being interrogated is made, as is an entry to record the vacated slot. Refer to Table 6-6 for text. LCC down indications may follow.

1-5.6. Suspension of Assumed Responsibilities. When the inactive LCC resumes valid transmissions, the auxiliary LCC automatically drops the assumed responsibilities. An alarm, an APQ entry, an update to the LCC Summary Display, and Crew Log entries occur at the auxiliary LCC: (1) the alarm indicates an LCC status change; (2) the APQ entry for LCC status change is created (if necessary) and alarmed; (3) the "AFI" field in the LCC Summary Display is updated to show the total set of flights being interrogated by the LCC; and (4) a Crew Log entry indicating the released responsibility and the totality of flights being interrogated is made, as is an entry to record resetting of the vacated slot. Refer to Table 6-6 for text. If the LCC had previously been indicated as "down", those indications will be reset.

1-6. COMMAND AND CONTROL CAPABILITIES. The WSCC provides two operator work stations which allow each operator the capability to command and monitor status of squadron LFs, LCCs and their own auxiliary equipment. See Figure 1-18 for a console overview. Descriptions of the equipment are given in Section 5. Weapon system command and status monitoring are controlled by the operator through the Operator Input Device (OID) and the Visual Display Unit (VDU) located at each work station. Weapon system auxiliary equipment status monitoring is displayed on the Auxiliary Alarm Panel (AAP).

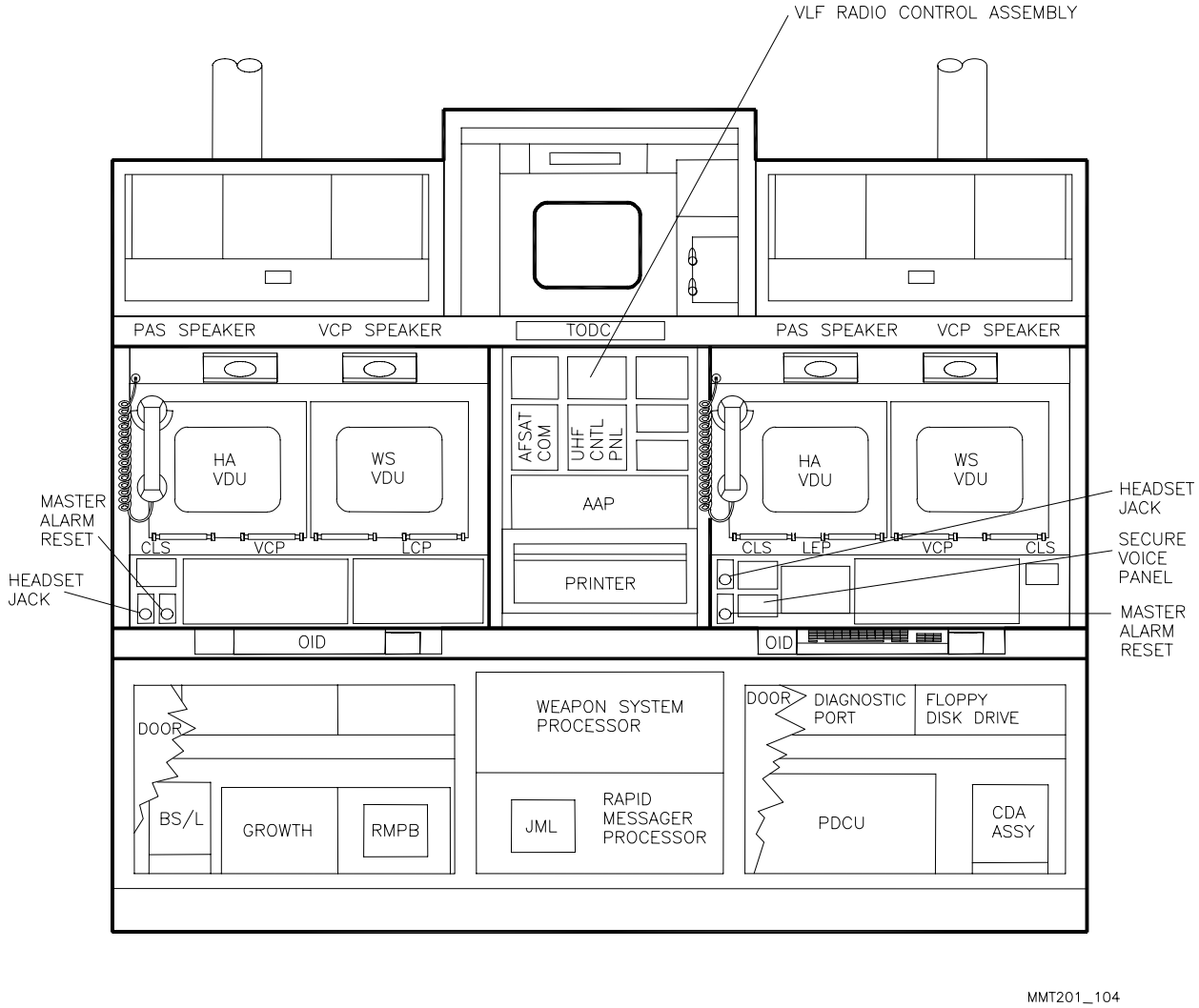


Figure 1-18. WSCC Hardware Configuration

1-6.1. Operator Input Device. The OID consists of a trackball and a keyboard (Figure 5-3). The trackball assembly consists of a trackball with three function keys (buttons). The trackball is used to move the pointer cursor through the various "windows" of the VDU. The trackball function keys allow the operator to select an item highlighted by the pointer cursor. The keyboard portion of the OID is based upon a hardened commercial QWERTY design with function key assignments and arrangement based upon specific functional requirements.

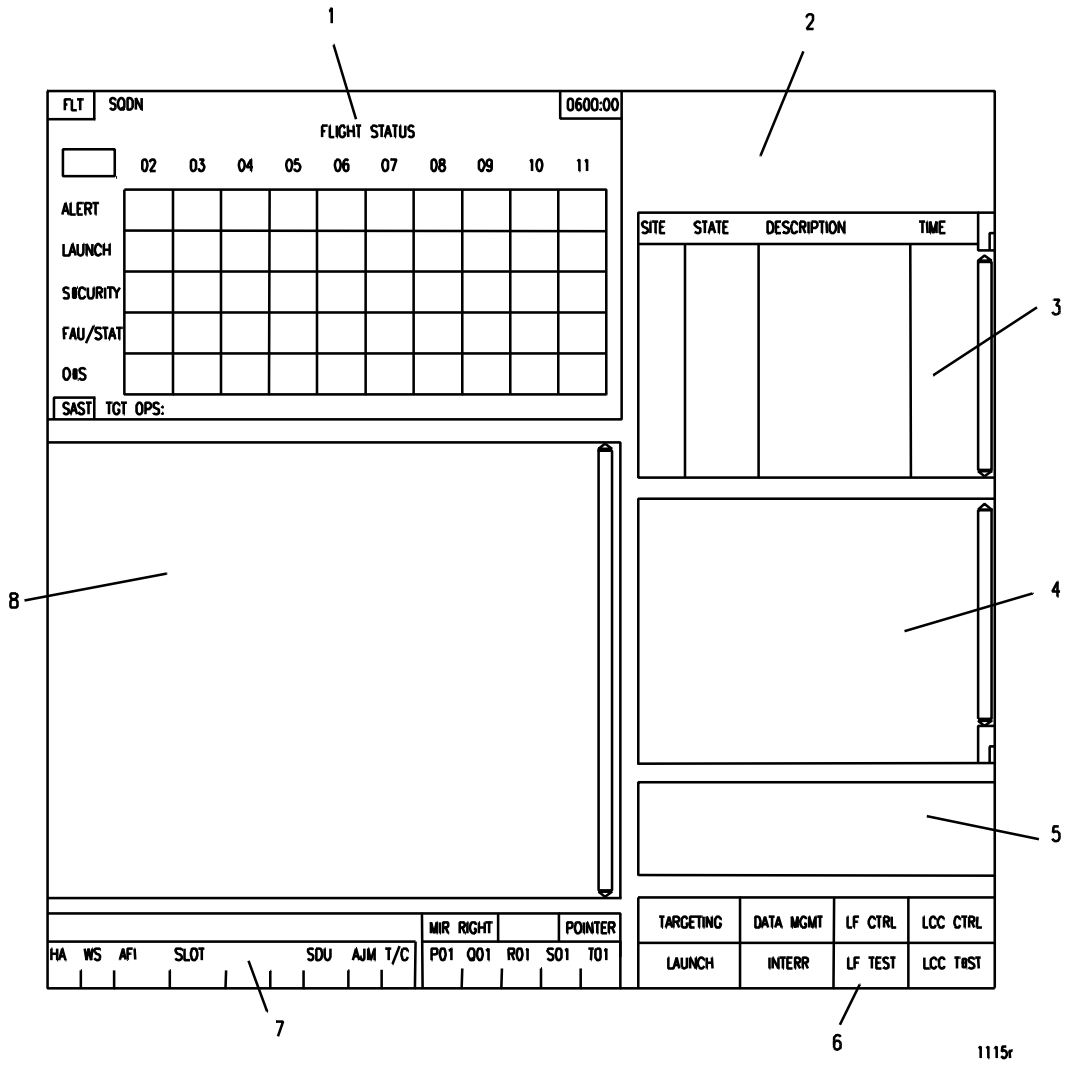
1-6.2. Visual Display Unit. The WS VDU screen (Figure 5-2) displays eight distinct functional areas or "windows". These areas are illustrated in Figure 1-19. The eight areas are: Flight/Squadron Status Area, Alarms Area, Actions Pending Queue Area, T.O Checklist Area, Data Entry Area, Main Menu Area, Work Area, and LCC Summary Status Area. Each of these areas is described in the following sections.

1-6.2.1. Flight/Squadron Status Window. The Flight/Squadron Status window (Figure 1-19, Item 1) contains a grid of ten columns by five rows. The Status window is capable of displaying the status for an individual flight of ten LFs or the entire squadron of 50 LFs. When the Flight/Squadron Status window is displaying an individual flight (any one of the five flights may be displayed), each column contains the status for an LF and the columns are labeled 2 through 11 for each LF in the flight. The status rows are labeled Alert, Launch, Security, FAU/STAT and OES. FAU/STAT indicates that a Fault and/or Status Change has occurred; OES is an Operator Entered Status. Each status row displays the highest priority status reported for that LF within each status category. When an LF is in the normal strategic alert mode, with no additional status items being reported, the display is blank.

The Status window may be switched to display the total squadron status. The display is switched by selecting SQDN in the FLT or SQDN toggle located in the upper left hand portion of the screen. When the Status window is displaying squadron status, each row displays an entire flight. The status displayed for each LF is the highest priority status item reported for an LF.

1-6.2.2. Alarms Window. The Alarms window (Figure 1-19, Item 2) provides the operator with visual alarm elements to accompany audio alarms. The Alarms window consists of five categories of alarms and an alarm banner that provides the operator with a brief summary of the incoming alarm using the name of the corresponding APQ entry, if one exists. The five categories of alarms are: EAM, NON-EAM, CRITICAL, ROUTINE and FIRE.

1-6.2.3. Actions Pending Queue Window. The APQ (Figure 1-19, Item 3) is a displayable, prioritized list of tasks either in work, on hold or awaiting action by the operator. An APQ task is created for changes in LF and LCC status, upon receipt of messages that are of interest to this LCC, through selection of Main Menu items and upon receipt of Higher Authority messages. Operators can use the APQ to manage their various



SOURCE: T.O. 21M-LGM30G-1-22

1. FLIGHT/SQUADRON STATUS WINDOW
2. ALARMS WINDOW
3. APQ WINDOW
4. T.O. CHECKLIST WINDOW
5. DATA ENTRY WINDOW
6. MAIN MENU WINDOW
7. LCC SUMMARY STATUS WINDOW
8. WORK AREA

Figure 1-19. WS VDU Functional Areas

command and control functions. The APQ window consists of four general display elements: the Site column, the State column, the Description column and the Time column. By moving the pointer cursor to a item in the APQ, the operator can select a specific task to work.

1-6.2.4. T.O. Checklist Window. The T.O. checklist window (Figure 1-19, Item 4) is used to display certain portions of the crew operations technical order manual (T.O.). The Checklist window is linked to an APQ task and, when appropriate, to an associated data entry template or Work Area display. When an APQ task is selected by the operator the appropriate portion of the corresponding T.O. checklist is automatically displayed in the Checklist window. A checklist will also appear in the Checklist window when the operator selects a Main Menu task item.

1-6.2.5. Data Entry Window. The Data Entry window (Figure 1-19, Item 5) is used for operator entry of data required to complete commands prior to command initiation. Upon selection of a command from the Main Menu Hierarchy, the associated template appears in the Data Entry window. The operator then enters the required information prior to initiating the command.

1-6.2.6. Main Menu Window. The Main Menu window (Figure 1-19, Item 6) contains eight options from which the operator can select various tasks or functions. The eight top-level menu options are: Targeting, Launch, Data Management, Interrogations, LF Control, LF Test, LCC Control and LCC Test. Each top-level option has sub-options which are displayed once the top-level option is selected. See Figure 1-20 for the various task options contained in the Main Menu Hierarchy.

1-6.2.7. LCC Summary Status Window. The LCC Summary Status window (Figure 1-19, Item 7) displays the operational status of all five LCCs within the squadron and a status summary of specific items within the local LCC.

1-6.2.8. Work Area. The Work Area (Figure 1-19, Item 8) is used to accommodate the various displays and templates initiated within other areas of the VDU display. The Work Area may be split into two areas (a top portion and a bottom portion). If the operator chooses to display an additional flight, the top portion of the Work Area would be used to display the Flight Status grid for that flight. The bottom portion of the display could then be used to display an additional flight or the top portion of any display or template that would normally be displayed in the Work Area.

1-6.3. Operator Initiated LF Tasks. The general processing for operator initiated LF messages begins with an operator selection of a Main Menu (Figure 1-19, Item 6) item. The operator moves the pointer cursor via the trackball to the desired Main Menu item and selects the item by pressing the trackball T1 function key. Once the top-level menu selection is completed, a sub-menu (pop-up menu) appears. The operator would again move the pointer cursor to the desired sub-menu option and select the desired task.

TARGETING	DATA MGMT	LF CTRL	LCC CTRL
PLC-A	ALARM CLOCK	HOLDOFF	SET CLOCK
PLC-B	CREW LOG VIEW	AHC	RESET COMM CNTS
RDH	SPECIFIC DTG	SAHC	MAN COMM MON
ALL CALL	SINCE PREV ARCH	CALIBRATION	SEQUENCE COUNT
SPECIFIC SITE	ENTIRE LOG	IMU CAL 1	VIEW SEQ COUNT
FDMs	CREW LOG ARCH	IMU CAL 2	SET SEQ COUNT
FDM BUFFER	SINCE PREV TO FDD	PHI CAL	LOAD SEQ COUNT
FDM TOTALS	SINCE PREV TO PTR	SAT CAL	CHG SIOP REV ID
LIBRARIES	ENTIRE LOG TO FDD	IMU PERFORMANCE DATA	HA BKUP CONTROL
CASE INPUT LIB	ENTIRE LOG TO PTR	IPDC	PTR SW-NORMAL
ALL CASES	CREW LOG ENTRY	IPDH	PTR SW-BKUP
RANGE OF TGT/EP CASES	CKLIST LIBRARY	OVERWRITE	HA BKUP PTR ON
SITE/SIOP	CYCLING STATUS	LF OW SEQ	HA BKUP PTR OFF
SIOP REV ID/INT CHG #	CYCL STAT RPRT	OWC	HA BKUP ALM ON
CASE LIB CKSUM	CYCL STAT SUP	OWT	HA BKUP ALM OFF
TGT/EP VIEW	CYCL STAT UNSUP	PIGA LEVELING	OVERWRITE
PLC-B LIBRARY	PRINT	PGLC	OW WS BS/L
STACKS	PRINT SQDN STAT	PGLH	OW WSP MEMORY
ACTIVE STACK	PRINT WORK AREA VIEW	CTRL LITHIUM POWER	DIAGNOSTIC DATA
MONITOR STACK	PRINT WORK AREA FILE	CLIPA	HA DIAG DATA
GENERATE STACK	PRINT APQ	CLIPD	I/O
PLC-B STACK	PRINT TGT RPRT	RDCP LIST	I/O & MSG
CONSTS SET STAT	TGT/EP CASE LIB UPDT	RDCP IMU CAL 1	I/O & MSG & FAU ID
TATD	TGT/EP CASE GEN UPDT	RDCP IMU CAL 2	CMPG DIAG DATA
TATD LF VIEW	UPLOAD CASE LIB RPRT	RDCP PHI CAL	I/O
TATD T/P VIEW	DNLOAD CASE LIB RPRT	RDCP SAT CAL	I/O & MSG
TATD A/O VIEW	RDC SUMMARY	RDCP OWC	I/O & MSG & FAU ID
TATD LF PRINT	PLC-A VERIF SMY	RDCP MSL TEST 1	DIAG DATA TO FDD
TATD T/P PRINT	UPLOAD/DNLOAD	RDCP MSL TEST 2	DELETE DIAG DATA
TATD A/O PRINT	UPLOAD T.O. DB	RDCP LOCAL COMM	**LCC TEST**
TATD GENERATE	UPLOAD CASE LIB	RMR	LCC SUBSYS TEST
MANUAL ENTRY	UPLOAD EPP/MA	RSA	HA SUBSYS TEST
CASE ENTRY BFR	UPLOAD FDM FMT	**LF TEST**	BULK STORE TESTS
CASE ENTRY-LIB	UPLOAD CKSUM	SCNT	WS BS/L TEST
LAUNCH	DNLOAD CASE LIB	ENTC	WS BS/L CMSC
PRE LAUNCH SEQ	DNLOAD ALL CASES	MSL TEST 1	ALARMS TEST
SELECTIVE ENBL	DNLOAD HI SIOP CASES	MSL TEST 2	PRINTER TEST
ALL CALL ENABLE	DNLOAD LO SIOP CASES	LF TEST SEQ	FDD TEST
PLC-A	**INTERR**	MSL TEST SEQ	OID TEST
PLC-B	CMVC		VDU TEST
PLC-B STACK	GMI		CDA/IPD TEST
EXEC OPTION GEN	MOSI		NED TEST
PRE LAU SEQ DEF	OSI		
CLR UNLOCK CODE	TVI		
CLR UNLOCK CODE-UNIV			
CLR UNLOCK CODE-SEL			
TRANSLATE CODE			
T/C ACTIVATE			
T/C VERIFY			
T/C DEACTIVATE			

Figure 1-20. Main Menu Hierarchy

(The actions described for the trackball may also be taken on the keyboard. See Figure 5-3, especially the descriptions of the POINTR CURSR and T1, T2, and T3 keys.)

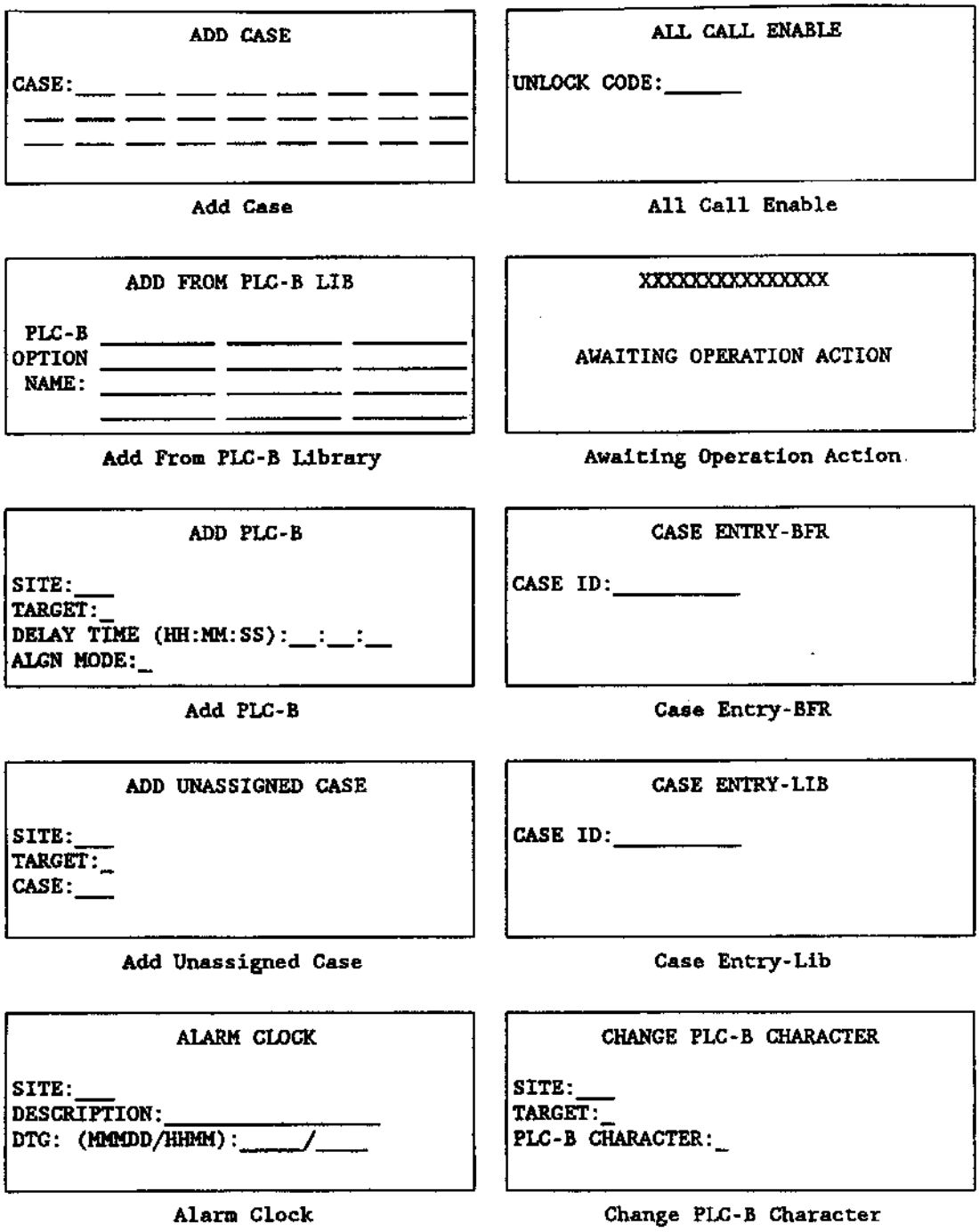
For some LF command and interrogation messages the menu option selection would be completed with the first sub-menu option selection. For certain other command messages additional sub-menu option selections would be required. Once the lowest level of sub-menu selection for the desired command or interrogation has been reached, several additional events occur. An APQ entry is generated and displayed in the APQ window, with the State column showing Selected to identify the task selected by the operator. The T.O. checklist appropriate for the selected task is retrieved and displayed in the Checklist window.

If a data entry template (see Figure 1-21) is required for the selected task, the template is displayed in the Data Entry window. Note that one of these templates says "AWAITING OPERATOR ACTION", which indicates that the operator need only depress the INITIATE key on the OID (see Figure 5-3) to initiate the task. If a data entry template is not required for the selected task, then the address grid (see Figure 1-22) is displayed in Data Entry window for selection of the LF(s) to which the message is to be addressed.

The operator would enter (via the keyboard) any required data for the message in the data entry template. The operator would select (via the trackball) the desired LF(s) address for the message by moving the pointer cursor to the address grid and pressing the trackball T1 function key. A black dot appears in the address grid for the selected LF(s). Command stacking allows a group of LFs (up to ten) to be selected for a particular command. After completing any required data entry and LF(s) address selection, the operator is ready to initiate the message.

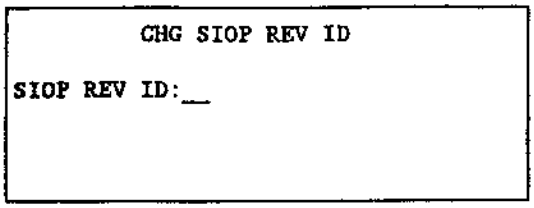
Command and interrogation messages are initiated by the operator by pressing the INITIATE function key located on the OID keyboard. When the message is initiated, several additional events occur. The Work Area and the Data Entry window are cleared. Additionally, the State column in the APQ window for that task is changed to a Commanded State. Once the message is actually transmitted, the State column of the APQ entry is updated to In-Process. The T.O. checklist for the task remains displayed in the T.O. Checklist window to enable the operator to track the progress of the task. Should the operator have additional tasks to perform the T.O. checklist can be removed by operator action.

When the LF responds to the transmitted message with all expected reply messages, the State column of the APQ task entry is updated to an Alarmed state (Green Routine), accompanied by the appropriate visual and audio alarm for the task. When the LF fails to respond with all expected reply messages, the alarm is a Yellow Routine alarm. In either case, when the alarm is acknowledged by the operator, the state of the APQ task entry is updated to Completed. Status changes associated with the reply messages are displayed in the Flight/Squadron Status Area.

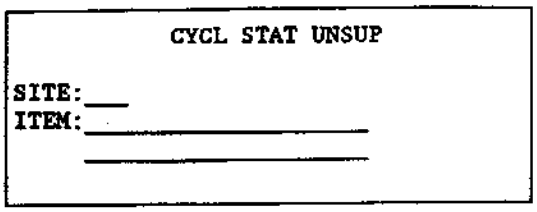


Source 21M-LGM30G-1-22

Figure 1-21. Data Entry Templates (Sheet 1 of 5)



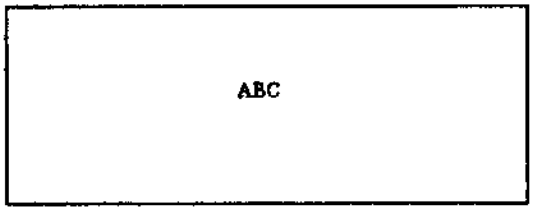
Change SIOP Revision ID



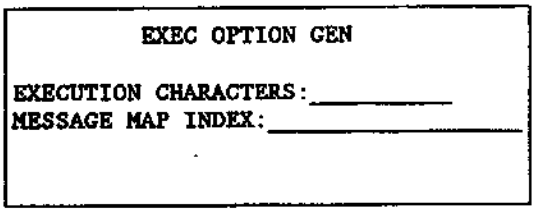
Cycling Status Unsuppression

Cooperative Enable Sequence - Countdown Sequence

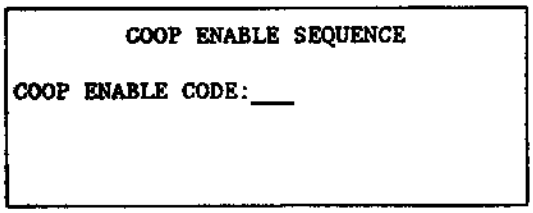
Entire Log



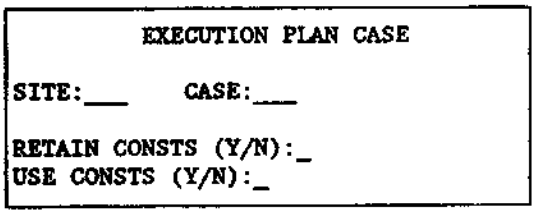
Cooperative Enable Sequence - Enable Code Display



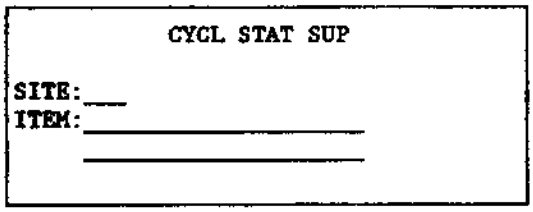
Execution Option Generate



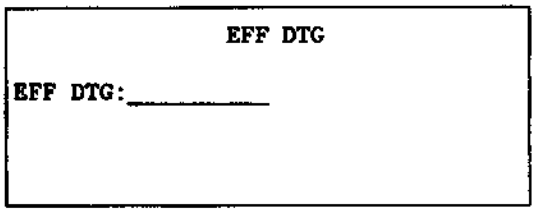
Cooperative Enable Sequence - Input Template



Execution Plan Case



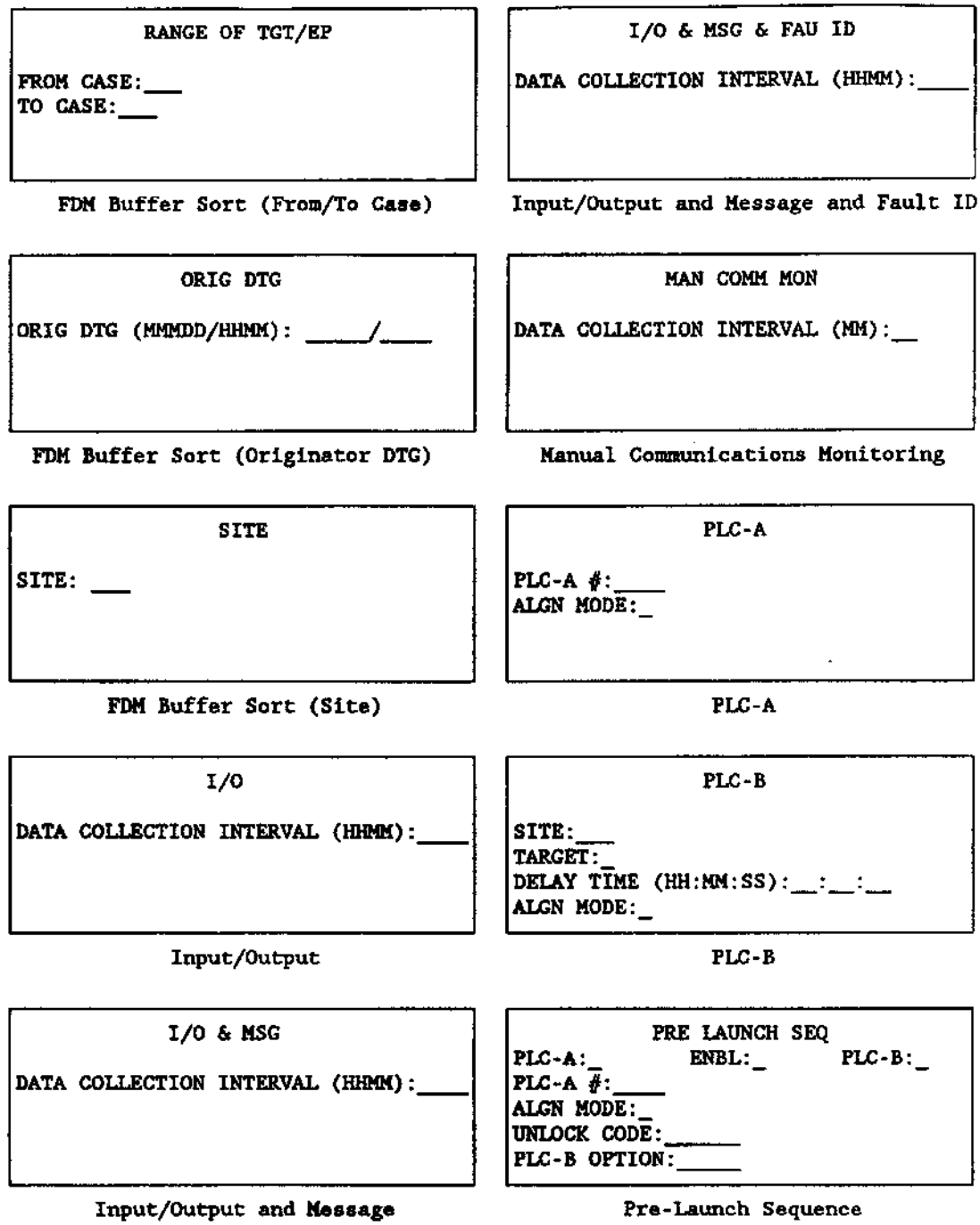
Cycling Status Suppression



FDM Buffer Sort (Effective DTG)

Source: T.O. 21M-LGM30G-1-22

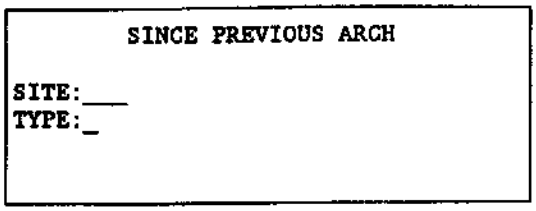
Figure 1-21. Data Entry Templates (Sheet 2 of 5)



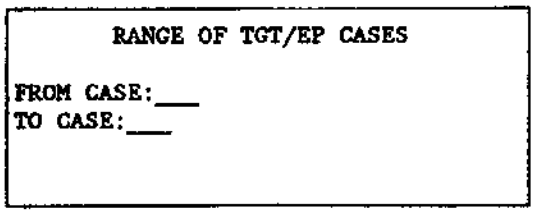
Source: T.O. 21M-LGM30G-1-22

Figure 1-21. Data Entry Templates (Sheet 3 of 5)

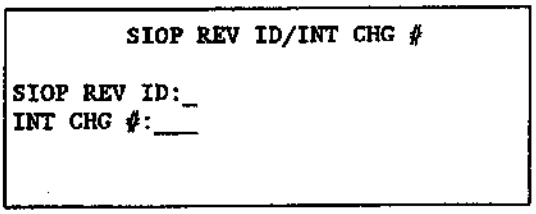
Pre-Launch Sequence Definition



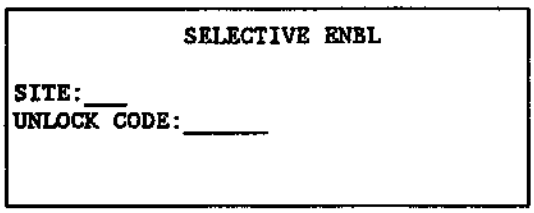
Since Previous Archive



Range of TGT/EP Cases

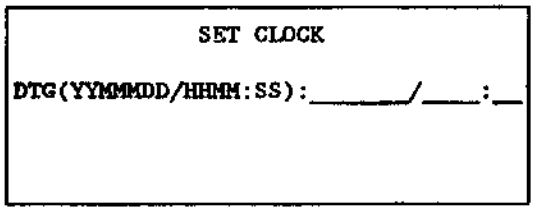


SIOP Revision ID/Interim Change Number

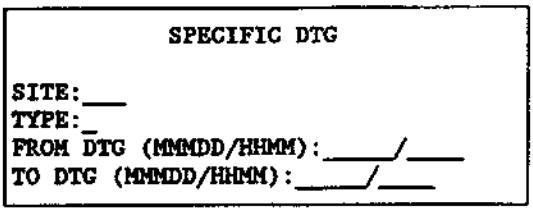


Selective Enable

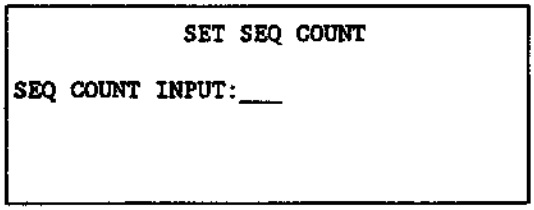
SITE/SIOP



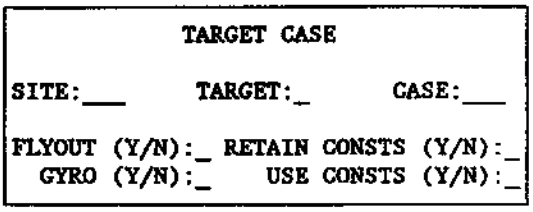
Set Clock



Specific DTG



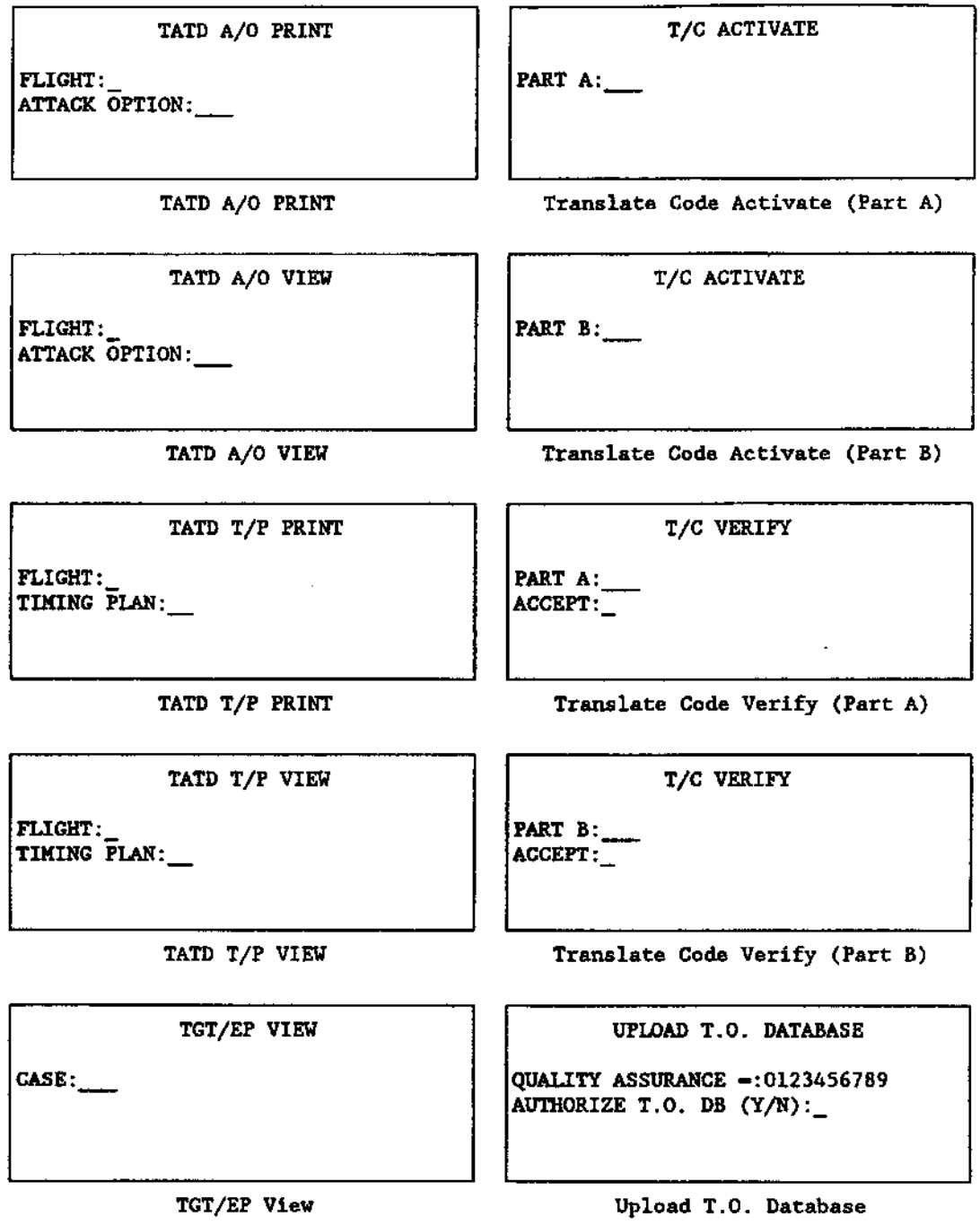
Set Sequence Count



Target Case

Source: T.O. 21M-LGM30G-1-22

Figure 1-21. Data Entry Templates (Sheet 4 of 5)



Source: T.O. 21M-LGM30G-1-22

Figure 1-21. Data Entry Templates (Sheet 5 of 5)

ADDRESS GRID

ALL	02	03	04	05	06	07	08	09	10	11
A										
B										
C										
D										
E										

Source: T.O. 21M-LGM30G-1-22

Figur 1-22. Address Grid

All the responses received from the LF to the transmitted message are collected in a Command Summary Report (CSR). To view the CSR the operator moves the pointer cursor to the APQ task and selects the task entry. The APQ pop-up menu is displayed and the operator chooses the Select option via the pointer cursor. The CSR is then displayed in the Work Area. The CSR contents are determined by message type, by the LF's state at the time of command transmission, and by the LF responses. All CSRs show the command transmission records, the expected non-responses (eg, the LF was LFDN at the time of transmission), and the unexpected non-responses (the LF didn't reply within the timeout period). These latter two are generically called "Exceptions." Some CSRs contain other data that are command-dependent. Details are given in Table 1-7.

1-6.4. Operator Access to Detailed LCC/LF Status. The Flight/Squadron Status window (Figure 1-19, Item 1) and the LCC Summary Status window (Figure 1-19, Item 7) contain summary status information for the LFs and LCCs. Detailed status for any LF is provided in the Detailed LF Status display, while detailed LCC status for any LCC is provided in the Detailed LCC Status display. The Detailed LF Status display is obtained by selecting an LF displayed in the Flight/Squadron Status window or by selecting the status change APQ entry, if available, for that LF from the APQ window. The Detailed LCC Status display is obtained in a similar fashion by selecting the desired LCC from the LCC Summary Status display, or by selecting the status change APQ entry for that LCC, if available. The selections are made by moving the pointer cursor via the trackball to the desired area of the screen and pressing the trackball T1 function key.

1-6.4.1. Detailed LF Status. When the Detailed LF Status display is selected as described in 1-6.4, the display appears in the Work Area window. The Detailed LF Status display (see Figure 1-23) occupies the entire Work Area. The display consists of two parts, a header area which contains five categories of status, and a body which contains Operator Entered Status (OES) entries for that LF, followed by the Crew Log entries for that LF.

The Detailed LF Status display contains all currently reporting status items for the LF. The five categories of status contained in the header area are Miscellaneous (derived) Status (abbreviated MS), Operational Status Response (OSR), Maintenance Operational Status Response (MOSR), Ground Maintenance Response (GMR) and Targeting Status. Each status line contains a Date Time Group (DTG) indicating the time when the latest status message of that type was received.

When a change in status for an LF is detected in an LF response message, the operator is alerted to the change according to the Primary, Secondary, and Other (PSO) rules for that status item. If the LCC has PSO responsibility for the changed status item, then the following events occur. An APQ entry is generated with a State of Alarmed, a Site address of the LF reporting the status change, and a Description of Status Change. A visual alarm is generated with an alarm banner of Status Change, and if the alarm is not acknowledged within 10 seconds, an audio alarm is sounded. If the LF is being displayed in the Flight/Squadron Status window, the highest priority status item is displayed in the appropriate status row. To view the Detailed LF Status display the operator would use one

Table 1-7. Alarm Filtering and Command Summary Reports

[Note 1]

COMMAND/ INTERROGATION (TRANS. IN CSR)	NO RESPONSE EXPECTED [EXPECTED EXCEPTIONS IN CSR]	FILTER CRITERIA [ALARMS THAT WOULD NORMALLY RESULT FROM THESE STATUS CHANGES ARE SUPPRESSED]	COMPLETION CRITERIA FOR TASK/CSR			COMMAND SUMMARY REPORT DATA (MINIMUM REQUIREMENTS)
			SUCCESS (RESPONSES RECEIVED FROM ALL EXPECTED LFs) [GR]	OPPORTUNITY (W/O SUCCESS) [YL]	TIMEOUT (MINS) [YL]	
				[UNEXPECTED EXCEPTIONS IN CSR]		
AHC	LFDN, LFNA, LFOS, LFNG	AHC Accepted	OSR: AHC Accepted	N/A	5	Exceptions.
CLIP	LFDN, LFNA, LFOS, LFNG	MOSR	2 MOSRs	N/A	10	Exceptions. MOSR Data.
CMVC	LFDN, LFNA, LFOS, LFNG	N/A	5 RDRs	N/A	25	Exceptions. RDR Data.
ELC	LFDN, SBNG, LFNG	OSR-Launch Commanded Launch in Process	OSR: Launch Commanded or Launch in Process	N/A	5	Exceptions.
ENC	LFDN, SBNG, LFNG	OSR-Enabled IPD Disabled	OSR: Enabled	N/A	5	Exceptions.
ENTC	LFDN, SBNG, LFNG	OSR-Test Complete NOTE: Filter at Primary & Secondary LCC	OSR: Test Complete	N/A	5	Exceptions. All LF Response Data.
GMI	LFDN	GMR: All	1st GMR	N/A	5	Exceptions. GMR Status Data.
IMUCAL1	LFDN, LFNG	OSR-IMU Calibrate	2nd OSR	N/A	10	Exceptions. OSR Status Data.
IMUCAL2	LFDN, LFNG	OSR-IMU Calibrate	2nd OSR	N/A	10	Exceptions. OSR Status Data.
INC	LFDN, SBNG, LFNG	OSR-Inhibit Test Launch Inhibited Disenable Commanded	OSR: Inhibit Test or Launch Inhibited or Disenable Commanded	N/A	8	Exceptions.
IPDC	LFDN, LFNG	OSR-IPD Disabled (Recovery)	OSR: 1st OSR	N/A	5	Exceptions. OSR Status Data.
IPDH	LFDN, LFNG	OSR-IPD Disabled	OSR: 1st OSR	N/A	5	Exceptions. OSR Status Data.
MOSI	LFDN, LFNG	MOSR-All Missing MOSR Data	2nd MOSR	N/A	10	Exceptions. MOSR Status Data, Missing MOSRData, and/or FDW Status Data.
MTC	LFDN, LFNG	OSR-LF Alarm Fault MOSR-All GMR-All OSR-Test Complete NOTE: Filter at Primary & Secondary LCCs	4th OSR	N/A	10	Exceptions. All LF Response Data.
OSI	LFDN	N/A	End of Half Slot	N/A	N/A	Exceptions. Any Response Data.

Table 1-7. Alarm Filtering and Command Summary Reports (Continued)

[Note 1]

COMMAND/ INTERROGATION (TRANS. IN CSR)	NO RESPONSE EXPECTED [EXPECTED EXCEPTIONS IN CSR]	FILTER CRITERIA [ALARMS THAT WOULD NORMALLY RESULT FROM THESE STATUS CHANGES ARE SUPPRESSED]	COMPLETION CRITERIA FOR TASK/CSR			COMMAND SUMMARY REPORT DATA (MINIMUM REQUIREMENTS)
			SUCCESS (RESPONSES RECEIVED FROM ALL EXPECTED LFs) [GR]	OPPORTUNITY (W/O SUCCESS) [YL] [UNEXPECTED EXCEPTIONS IN CSR]	TIMEOUT (MINS) [YL]	
OWC	LFDN, LFNA, LFOS, LFNG	OSR-SBNG and TDC (which indicates Overwrite-in-Process Status)	RDR	N/A	15	Exceptions. RDR Data.
OWT	LFDN, LFNA, LFOS, LFNG	OSR-LF No-Go GMR-All	2nd OSR	N/A	10	Exceptions. OSR Status Data.
PGLC/V	LFDN, LFNA, LFOS, SBNG, LFNG	OSR-PIGA Leveling Strategic Alert	2nd OSR	N/A	10	Exceptions. OSR Status Data.
PGLH	LFDN, LFNA, LFOS, SBNG, LFNG	OSR-PIGA Leveling (cleared) Strategic Alert	2nd OSR	N/A	10	Exceptions. OSR Status Data (Note 3).
PHICAL	LFDN, LFNG	OSR-IMU Calibrate	2nd OSR	N/A	10	Exceptions. OSR Status Data.
PLC-A	LFDN, SBNG, LFNG	OSR-Target Data Changed Alignment TVR-All	1st TVR and OSR-Target Data Change	N/A	5	Exceptions. TVR Data. Note: When PLC-A is part of Pre-Launch Sequence, there is no PLC-A data report beyond exceptions.
PLC-B	LFDN, SBNG, LFNG	OSR-Target Data Changed Alignment TVR-All	1st TVR and OSR-Target Data Change	N/A	5	Exceptions. TVR Data.
RMR	LFDN, LFNG	OSR-Alignment LF No-Go	2nd OSR	N/A	10	Exceptions. OSR Status Data.
RSA	LFDN, LFNG	OSR-LFNG Alignment	2nd OSR	N/A	10	Exceptions. OSR Status Data (Note 3).
SAHC	LFDN, LFNA, LFOS, LFNG	OSR-Radio Mode	OSR-Radio Mode	N/A	15	Exceptions.
SATCAL	LFDN, SBNG, LFNG	OSR-SAT Calibrate	2nd OSR	N/A	10	Exceptions. OSR Status Data (Note 3).
SCNT	LFDN	OSR: LF Alarm Fault, LIP, OZ, IZ, Primary Power Failure, Radio Mode, Radio Data Present, Warhead Alarm, LF SDU Alarm/Fault, Test Complete, Strategic Alert, No Launch Note: Filter at all LCCs	OSR:Test Complete Transitions to Reset [Note 2]	N/A	10	Exceptions. All LF Response Data.

Table 1-7. Alarm Filtering and Command Summary Reports (Continued)

[Note 1]

COMMAND/ INTERROGATION (TRANS. IN CSR)	NO RESPONSE EXPECTED [EXPECTED EXCEPTIONS IN CSR]	FILTER CRITERIA [ALARMS THAT WOULD NORMALLY RESULT FROM THESE STATUS CHANGES ARE SUPPRESSED]	COMPLETION CRITERIA FOR TASK/CSR			COMMAND SUMMARY REPORT DATA (MINIMUM REQUIREMENTS)
			SUCCESS (RESPONSES RECEIVED FROM ALL EXPECTED LFs) [GR]	OPPORTUNITY (W/O SUCCESS) [YL]	TIMEOUT (MINS) [YL]	
				[UNEXPECTED EXCEPTIONS IN CSR]		
TVI	LFDN, LFNG	N/A	1st TDR	N/A	5	Exceptions. TVR Data. TDR Data.

Note 1 - No Response Expected: LF not expected to respond if in any of the conditions listed. LF deleted at transmission time from list of LFs expected to respond.

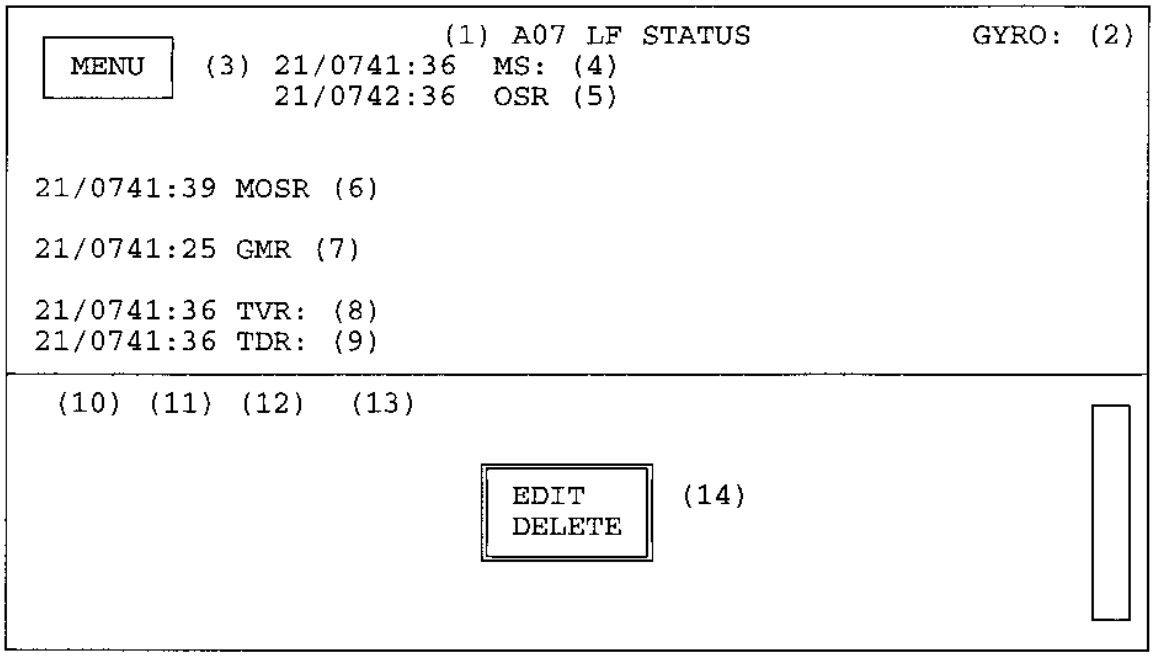
Filter Criteria: Filter on any conditions listed, set or reset, unless noted to the contrary.
Completion Criteria: Applies only to LFs expected to respond. Complete on first completion criterion (success/opportunity/timeout) to occur.
Success: All expected LFs responded in accordance with the success criteria.
Opportunity: If an LF responds, but the response does not meet the success criteria, the CSR shows "INCORRECT RESPONSE" with the time at which the opportunity closed. (Not used in the AM System.)
Timeout: Timeout based on last command xmtd. Value shown is in minutes, +/-10 seconds. When an LF fails to respond, the CSR shows "NOT RESPONDING" with the expiration time.
Command Summary Report Data: Include all items shown, as applicable, in the DATA portion of the CSR.

Note 2 - For IZ/OZ suppress alarms during time it takes to get two OSRs back. After two OSRs have come back from the target LF, do the following:

If IZ was OFF at start: provide YELLOW ROUTINE alarm if there was no IZ change of status shown in the filtered OSRs. Alarm also if the status changed to ON, but did not change to OFF.
If IZ was ON at start: provide YELLOW ROUTINE alarm if there was any IZ change shown in the filtered OSRs.
If OZ was OFF at start: provide YELLOW ROUTINE alarm if there was no change of OZ status shown in the filtered OSRs. Alarm also if the status changed to ON, but did not change back to OFF.
If OZ was ON at Start: provide YELLOW ROUTINE alarm for any OZ change shown in the filtered OSRs.
Note: The alarms are given at the completion of the filtering period, not from the data in each one individually.

Note 3 - Because the RSA Function Code and PGLH Function Code are identical to the SATCAL Function Code, a receiving LCC will process this received message as a SATCAL. Thus when an RSA or PGLH is transmitted, the receiving LCC will have a SATCAL timeout.

Source: S-133-36000



NO.	TITLE	FUNCTION
1	SITE	Displays address of the selected LF.
2	GYRO	Displays the 4-digit decimal serial number associated with the MGS located at the LF.
3	MENU Icon	Selects pop-up menu. The menu options are UPDATE STATUS, CLEAR WORK AREA, OES SHORT FORM, OES LONG FORM, CHECKLIST, START HISTORY RETRIEVAL, STOP HISTORY RETRIEVAL and SHOW SET STATUS ONLY.
4	MS	Displays the Miscellaneous Status (MS) of the specified LF. The status for this category is derived and includes the miscellaneous status of the LF not included in the other status categories. Clearing of items occurs upon receipt of an OSR from the LF after the status condition has cleared. An INV indication for a non-primary LF indicates the message is invalid and the data are not reliable.
5	OSR	Displays the OSRs for the specified LF. The category titles are part of the actual data contained in the message. An INV indication for a non-primary LF indicates the message is invalid and the data are not reliable.
6	MOSR	Displays the MOSR for the specified LF. The category title is part of the actual data contained in the message. An INV indication for a non-primary LF indicates the message is invalid and the data are not reliable.

Figure 1-23. Detailed LF Status Display (Sheet 1 of 2)

NO.	TITLE	FUNCTION
7	GMR	Displays the GMRs for the specified LF. The category title is part of the actual data contained in the message. An INV indication for a non-primary LF indicates the message is invalid and the data are not reliable.
8	TVR	Displays targeting status for the specified LF, based on the most recent TVR. The status includes whether the alighment mode is the CEP or MRT option; the execution option; the delay time; the target slot number; and whether the targeting was performed by a PLC-A, PLC-B, or if the PLC illegal or the target not authorized.
9	TDR	Displays targeting status for the specified LF, based on the most recent TDR. The status includes target authorization status, the PLC-A capability status, and the program buffer.
10	DTG	The DTG associated with the OES or Crew Log entry.
11	Data Type	Displays whether the OES or Crew Log entry can be archived or stored on the FDD and printer (F) or on the printer only (P).
12	SITE	Displays the specified LF associated with the OES or Crew Log entry.
13	DESCRIPTION	Displays a textual description associated with the OES or Crew Log entry. This field includes the identifiers MS, OES, OSR, MOSR, GMR, TVR, and TDR. For OES entries, this also consists of the DESCRIPTION field of the OES. For Crew Log entries, this also consists of the alphanumeric codes associated with the status category, in the same format as for the Detailed LF STATUS header.
14	Item Pop-up Menu	Allows the MCCM to edit and delete OES entries associated with the specified LCC. The menu options are EDIT and DELETE.

SOURCE: T.O. 21M-LGM30G-1-22

Figure 1-23. Detailed LF Status Display (Sheet 2 of 2)

of the selection methods identified in paragraph 1-6.4. When the display appeared in the Work Area window, all currently reporting status items would be displayed in the header area. To identify newly set status items from previously reporting status items, each new status item will be preceded by the letter "n". For example, a newly set inner zone security violation would be displayed on the OSR line as "nIZ". All reset status items are grouped at the end of the response message status line and are preceded by the letter "r" to identify newly reset status items from the currently reporting status items. For example, a newly reset outer and inner zone security violation would appear as "r:OZ IZ. A typical display for an LF in Strategic Alert mode with a newly reporting alarm fault and outer zone security violation would appear as:

21/0702:40 OSR SALRT nFAU nOZ

When these status items reset, the display would appear as:

21/0712:40 OSR SALRT r:FAU OZ

The Detailed LF Status display is a static display. Once the display appears in the Work Area window, subsequent status changes are not updated within the display. The operator may update the display by choosing the Menu icon located in the upper left hand corner of the Work Area display. Upon selecting the Menu icon via the trackball pointer cursor, a pop-up menu appears. By selecting the UPDATE STATUS option, the operator can refresh the display to include all currently reporting status. When the operator has completed reviewing and reporting pertinent status changes to the appropriate agencies, the Detailed LF Status display can be reset to show only current set status items. To reset the display, the operator selects the Menu icon to obtain the Detailed LF Status pop-up menu. The operator would then select the SHOW SET STATUS ONLY option. Upon selecting the option all reset status items in the header area of the display are removed leaving only the set status items.

The body area of the display is a scrollable area. Contained in this area are the OES entries for the selected LF displayed at the top, followed by the Crew Log entries for the selected LF. The OES entries are listed in priority order. The OES priority is assigned by the operator upon creation of the OES entry. The Crew Log entries are displayed in reverse chronological order. The operator does not interact with the body area of the display except to scroll through the displayed Crew Log data and create, edit or delete OES entries. OES entries are created by selecting the Menu icon to obtain the Detailed LF Status display pop-up menu. The operator then selects the OES entry form and fills in the desired information. An OES item specific pop-up menu is available which enables the operator to edit or delete OES entries.

1-6.4.2. Detailed LCC Status. The purpose of the Detailed LCC Status display is to provide the operator with more detailed status of a specific LCC, than is available in the LCC Summary Status window. The Detailed LCC Status display is displayed in the Work Area window and occupies the entire Work Area (see Figure 1-24). The Detailed LCC Status display is selected by the operator as outlined in paragraph 1-6.4. The display consists of two parts, a header area which contains selected status items and a body area

which contains a State column, a Description column and a Time column for displaying OES entries and status entries. For non-parent Detailed LCC Status displays, status within the header area which can be derived by the system is automatically updated. Status which cannot be derived by the system is labeled "N/A".

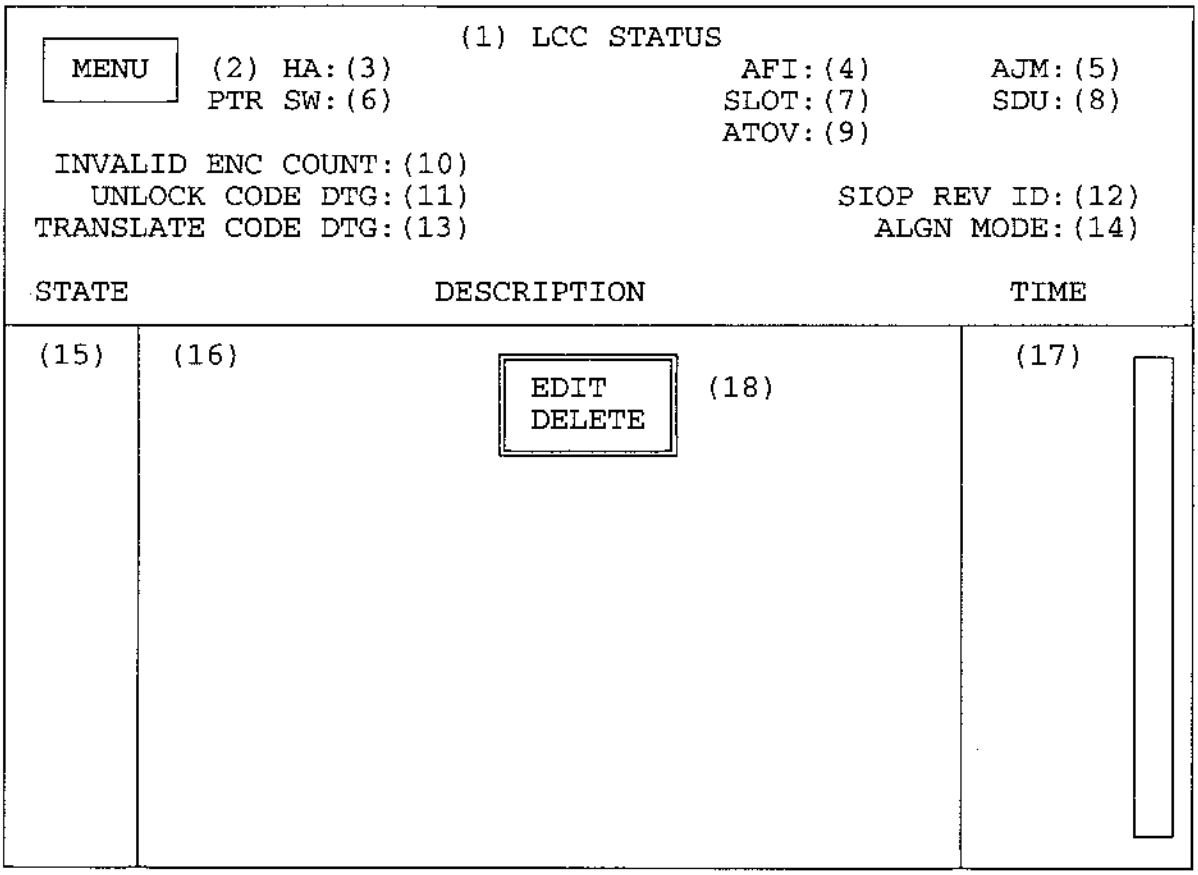
The body of the Detailed LCC Status display is a scrollable area. Reporting status items are displayed at the top of the body area followed by OES entries. Following the OES entries are any reset status items. Once a status item has reset (marked with CLR in the State column) the operator may clear the reset items by accessing the Detailed LCC Status pop-up menu. The pop-up menu is obtained by selecting the Menu icon (via the trackball pointer cursor). When the pop-up menu appears, the operator selects the SHOW SET STATUS option. Upon selecting the SHOW SET STATUS option all reset status indications are deleted.

The Detailed LCC Status display is a static display. Once the display appears in the Work Area window, subsequent status changes are not updated within the display. The operator may update the display by choosing the Menu icon (via the trackball pointer cursor) and then selecting the UPDATE STATUS option on the Detailed LCC Status pop-up menu.

1-6.5. Other Operator Initiated Tasks. The operator performs a variety of other LCC tasks through selections made at the Main Menu. As with operator initiated LF tasks, the specific tasks to be performed are contained in sub-menus, which appear after the selection of the Main Menu option. Once the sub-menu option is selected, an APQ task entry is generated in the APQ window, the appropriate T.O. checklist appears in the Checklist Window, and any required Data Entry templates appear in the Data Entry window.

A complete list of Main Menu sub-options is contained in Figure 1-20. All of these tasks are performed in a similar fashion. The following two examples of performing a Crew Log View task and building an RDC stack will illustrate the typical sequence of events associated with any of these tasks.

1-6.5.1. Crew Log View. The Crew Log View display is selected by the operator via the Main Menu. To select the Crew Log function the operator moves the pointer cursor to the DATA MGMT option and presses the trackball T1 function key. A sub-menu appears, and the operator highlights the Crew Log View function with the pointer cursor and presses the trackball T1 function key. The Crew Log View sub-menu appears. From the Crew Log View sub-menu the operator selects one of three options which allows the operator to specify how much of the Crew Log to display. The Specific DTG option allows the operator to specify the range of time of Crew Log entries to view. The Since Previous Archive option displays the Crew Log entries which have been made since the last Crew Log Archive. The Entire Log option displays the entire contents of the Crew Log. After selection of one of these options, an APQ entry is generated in the APQ window, the Crew Log View template appears in the Data Entry window, and the associated checklist appears in the Checklist window.



NO.	TITLE	FUNCTION
1	SITE	Shows the LCC selected.
2	MENU Icon	Selects pop-up menu. The menu options are UPDATE STATUS, CLEAR WORK AREA, OES SHORT FORM, OES LONG FORM, CHECKLIST, COMMUNICATIONS GRID, and SHOW SET STATUS.
3	HA	Displays the up/down condition of the RMP processor. The two levels of status for the processor are blank (operational) and DOWN.
4	AFI	Automatic Flight Interrogation - displays all flights currently being automatically interrogated. Display elements are any combination of applicable flights. Flights may have been selected by the MCCM or the WSP according to rules for automatic takeover of flight interrogation responsibilities. Selection is made from the COMMUNICATIONS GRID.
5	AJM	Displays whether the LCC is in the anti-jam mode or not. The data elements for this field are AJ (anti-jam) and blank (not in anti-jam). Selection is made from the COMMUNICATIONS GRID.

Figure 1-24. Detailed LCC Status Display (Sheet 1 of 2)

NO.	TITLE	FUNCTION
6	PTR SW	Displays the state of the Nuclear Event Detection NED printer switch. Data elements for this field are NORM or BKUP (backup).
7	SLOT	Displays which slots the LCC is currently using. Display elements for this category are 1, 2, 3, 4, 5, or any combination of 1 through 5. Selection is made from the COMMUNICATIONS GRID.
8	SDU	Displays SDU mode. The possible states for the SDU are ENCR (encrypted), CLR (clear), or CODE (code change). Selection is made from the COMMUNICATIONS GRID.
9	ATOV	Automatic Takeover - displays whether the automatic takeover of flight interrogations is ON or OFF. Selection is made from the COMMUNICATIONS GRID.
10	INVALID ENC COUNT	Displays the number of invalid Enable Commands ENCs attempted without success. The data elements for this field are 00 through 16, generated by the system.
11	UNLOCK CODE DTG	Displays the presence of a universal or selective unlock code. The possible data elements are blank (inactive unlock code) and DTG (DD/HHMM:SS activated unlock code). SEL, UNIV or BOTH following the DTG entry designate selective unlock code, universal unlock code, or both unlock codes, respectively. When an unlock code is received from the RMP, no APQ entry or alarm is generated.
12	SIOP REV ID	Displays the SIOP revision identification code.
13	TRANSLATE CODE DTG	Displays the presence of a manually-activated translate code. There are two possible data elements associated with this field; blank (no manually-activated translate code exists) and DTG (DD/HHMM:SS). DTG displays the DTG that the existing manually-activated translate code was activated.
14	ALGN MODE	Displays the circular error probable (CEP) or minimum response time (MRT), based on previously commanded PLC-A alignment mode.
15	STATE	Displays the current status of the fault; active (blank), OES (white letters), or clear (CLR, in inverse green letters).
16	DESCRIPTION	Displays the alphanumeric codes or description associated with the Detailed LCC STATUS entry.
17	TIME	Displays the time the associated item was received or reported.
18	Item Pop-up Menu	Allows the MCCM to edit and delete OES entries associated with the specified LCC. The menu options are EDIT and DELETE.

SOURCE: T.O. 21M-LGM30G-1-22

Figure 1-24. Detailed LCC Status Display (Sheet 2 of 2)

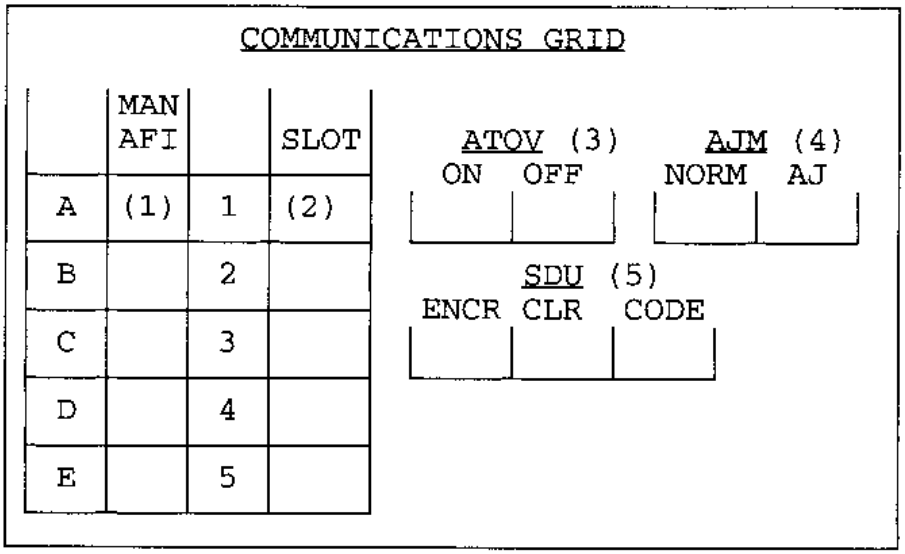
The Crew Log View data entry template for the Since Previous Archive and Entire Log options allows the operator to select a specific site (LF or LCC), an entire Flight or the entire Crew Log. The operator may also specify only type F Crew Log entries, type P Entries or all entries. Note, however, that "F" and "P" are holdovers from a time when certain data (the "P" type) were not to be archived to the floppy disk (F), but only to the printer (P). The requirement to make this distinction was removed, but the "F" and "P" designators remained. These same options are available for the Specific DTG option and in addition the operator must enter a beginning and ending DTG for the display. After entering the required data in the data entry template, the operator presses the initiate function key. Upon initiation the Crew Log View template is cleared from the Data Entry window and the Crew Log data (see Figure 1-26) is displayed in the Work Area.

1-6.5.2. RDC Stack. An RDC active or monitor stack may be created either automatically or manually. Active or monitor stacks are created in a similar fashion and for the purpose of this discussion the term RDC stack applies to both active and monitor stacks. RDC stacks are created automatically when the operator transfers Force Direction Messages (FDMs) from the FDM buffer to their appropriate library files.

To create an RDC stack manually the operator selects the Targeting Main Menu option (via the trackball pointer cursor). A targeting sub-menu would appear and the operator would select the Stacks menu option (via the trackball pointer cursor). The Stacks sub-menu would appear and the operator would select the appropriate option, i.e. Active or Monitor, depending upon the type of stack the operator desired to create. With the selection of Stacks sub-menu option an APQ entry would be created in the APQ window, the appropriate T.O. checklist would be displayed in the Checklist window and the Active Stack Edit display (see Figure 1-27) would be displayed in the Work Area. If no cases had been identified as Active Stack cases the display would be blank except for the display's header information.

To add cases to the stack, the operator would select (via the trackball pointer cursor) the Menu icon located in the upper left hand corner of the Work Area display. The general stack pop-up menu would appear. The operator would select (via the trackball pointer cursor) the ADD CASE option. Upon selection of this option, an ADD CASE template would appear in the Data Entry window. The ADD CASE template allows the operator to type in the case numbers of the cases to be added to the Active Stack. After entering the desired case number(s) the operator presses the initiate function key. The case(s) are displayed in the Active Stack Work Area display and the ADD CASE template is cleared from the Data Entry window. At this point the operator can initiate the RDC stack or review the case(s) prior to initiating the stack.

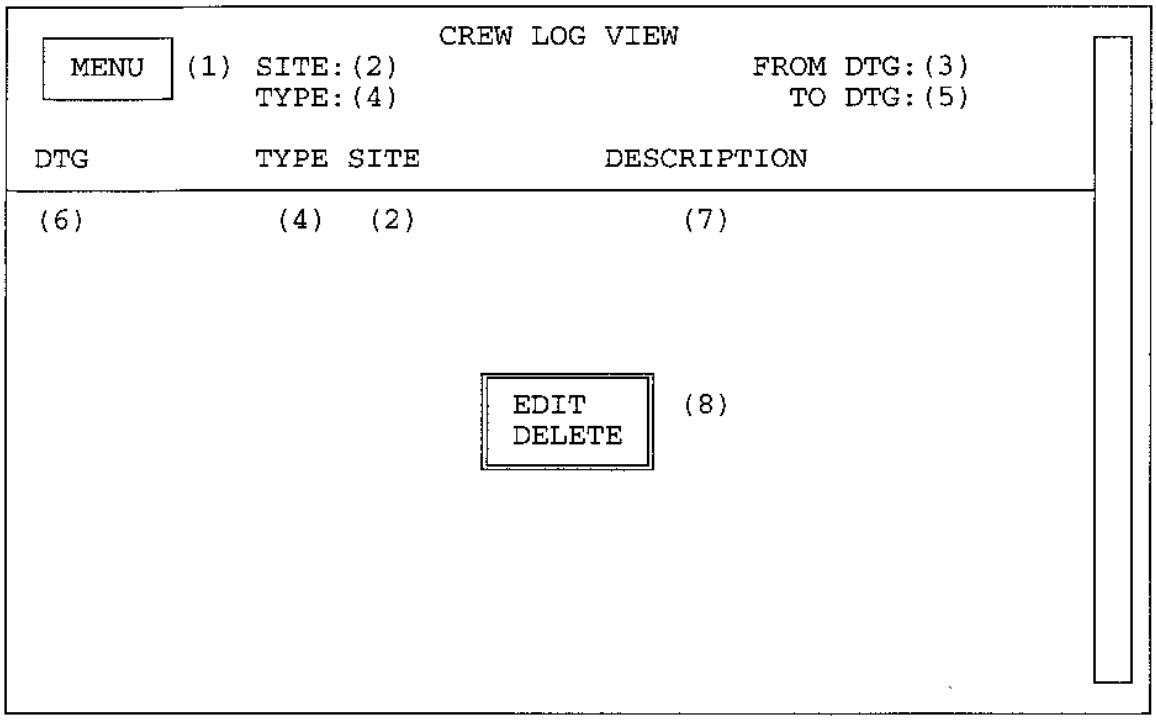
To review a case the operator highlights the case (via the trackball pointer cursor) and presses the trackball T1 function key. A pop-up menu appears which contains three



NO.	TITLE	FUNCTION
1	MAN AFI	Manual Automatic Flight Interrogation - used to manually select flight(s) for automatic interrogation. Manually selected flights are independent of flights selected by COP. Any combination can be selected. Shows current manual selection.
2	SLOT	Used to select which time slot(s) the LCC is currently using. Any combination can be selected. Shows current selection.
3	ATOV	Used to select flight takeover mode. Selections for this field are ON or OFF. Shows current selection.
4	AJM	Used to select either NORM (normal) or AJ (anti-jam mode). Shows current selection.
5	SDU	Used to select encryption mode. Possible selections for this field are ENCR (encrypted), CLR (clear text), or CODE (code change). Shows current selection.

SOURCE: T.O. 21M-LGM30G-1-22

Figure 1-25. Communications Grid Display



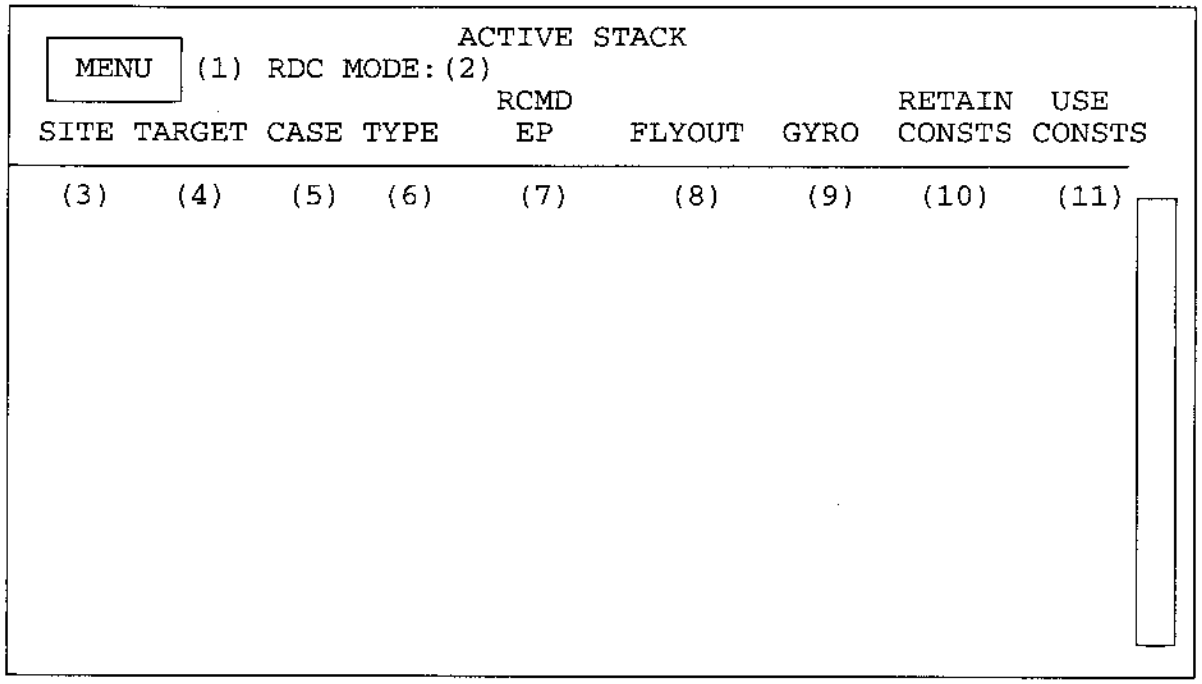
NO.	TITLE	FUNCTION
1	MENU Icon	Selects the pop-up menu. The menu option is CLEAR WORK AREA.
2	SITE	Specifies the LF or LCC location from which the displayed crew log entries originated. Either the entire log, only one site, or flight may be requested through the crew log view template.
3	FROM DTG	Specifies the start time for the date time group (DTG) that the MCCM has directed to be displayed in the work area (format DD/HHMM). The default value for this field is blank. If the field is blank, upon initiation the system automatically inserts the time of the last archive.
4	TYPE	Specifies in the header the types being viewed: F, P, or * (which indicates both F and P, and is the default value for this field). In the body, specifies the type (F or P) of the individual entry. Used originally to distinguish data archived only to the printer (P), or archived both to the printer and the floppy disk (F). The distinction no long exists, and the field has no functional use.

Figure 1-26. Crew Log View Display (Sheet 1 of 2)

NO.	TITLE	FUNCTION
5	TO DTG	Specifies the DTG (format DD/HHMM) end time for the data the MCCM has directed to be displayed in the work area. The default value for the field is blank. If the field is left blank, upon initiation the system inserts the current time.
6	DTG	The date time group, in DD/HHMM:SS format, showing when the crew log entry was made.
7	DESCRIPTION	Includes the type of message and the alphanumeric codes associated with the status category. The alphanumeric codes are identical to those found in the LF STATUS display body.
8	Item Pop-up Menu	Menu appears when an entry is selected. The menu options are ADD/EDIT and DELETE.

SOURCE: T.O. 21M-LGM30G-1-22

Figure 1-26. Crew Log View Display (Sheet 2 of 2)



NO.	TITLE	FUNCTION
1	MENU Icon	Selects pop-up menu. The menu options are UPDATE STATUS, CLEAR WORK AREA, ADD CASE, ADD UNASSIGNED CASE, RDC MODE, BLOCK DELETE, and ABORT.
2	RDC MODE	Displays RDC MODE selected. The data elements for this field are NORM and SOLE.
3	SITE	Displays the sortie address associated with the case. This field is of the format ANN, where the first character is the alphabetic flight designator and the second and third characters are the numeric designators of the LF.
4	TARGET	Displays the target slot number associated with the case (for target cases only).
5	CASE	Displays the case number associated with the entry.
6	TYPE	Displays the type of case (TGT or EP).

Figure 1-27. Active Stack Edit (Sheet 1 of 2)

NO.	TITLE	FUNCTION
7	RCMD EP	Displays the recommended execution plan case associated with the target case. This field is of the format NNN/NNN, where the first NNN is the low SIOP numeric case designator associated with the execution plan, and the second NNN is the high SIOP numeric case designator associated with the execution plan.
8	FLYOUT	Displays whether the target case is to be generated with or without flyout. The possible data elements for this field are YES and NO.
9	GYRO	Displays whether actual or nominal GYRO data are used during constants calculation. The data elements for this field are ACTUAL or NOMINAL.
10	RETAIN CONSTS	Displays the MCCM's desire to store the constants or not. YES indicates that the MCCM wishes to retain the constants after generation. NO generates the constants and discards them.
11	USE CONSTS	Indicates whether or not to use the constants that have already generated. YES indicates that the MCCM wishes to use the constants generated. NO indicates that the MCCM does not wish to use the constants generated.

SOURCE: T.O. 21M-LGM30G-1-22

Figure 1-27. Active Stack Edit (Sheet 2 of 2)

options; Edit, Delete and Move. The Edit option allows the operator to edit the flags for a selected case. Upon selection of this option the associated flag template appears in the Data Entry window. After editing the applicable fields the operator presses the initiate function key, at which time the flag template disappears from the Data Entry window and the Stack display reappears in the Work Area with the revisions reflected in the data. The Delete option allows the operator to remove a highlighted case from the stack. The Move option enables the operator to relocate the highlighted case within the stack. After editing the stack cases, the operator can initiate the stack.

1-6.6. Data Collection for Troubleshooting. The LCC CTRL menu contains a choice entitled "DIAGNOSTIC DATA," with submenus as shown in Figure 1-20. When the operator selects one of the HA or CMPG options for this task, COP collects raw data as received from the interface into an On-line Data Collection (ODC) file on the hard disk. After the operator terminates the task, the file can be transferred, via "DIAG DATA TO FDD," to a floppy disk for off-line analysis, using ODC tools.

1-6.6.1. ODC Data Organization. (Figure 1-28) The ODC diskettes are organized into blocks of 512 bytes. The first block of the first ODC diskette is the CONTROL BLOCK. The remaining blocks are data blocks and, combined, can span more than a single diskette. The maximum size of the ODC data is four megabytes; this maximum size can be accommodated by three high density diskettes.

1-6.6.2. ODC Control Block. (Figure 1-29) The Control Block contains information regarding the organization of the data on the diskettes. The Control Block consists of five fields: Basing Mode (AM,B), Start block, Start byte, End Block, and End Byte. The remaining bytes in the Control Block are not used. Several of the fields are relics from previous versions of COP and are no longer used by the ODC Reduction software. Currently, the fields used are Start Block, Start Byte, and Data Length. Start Block and Start Byte together specify where the ODC data begins. Data Length specifies the size of the file in bytes and, by inference, where the last byte of data is located.

1-6.6.3. ODC Record Format. (Figure 1-30) The ODC Data is organized into variable length records. Each record contains a header portion that consists of: the total length of the record, the associated time stamp, the port-ID, and the status. The remaining bytes in the record are the actual data bytes recorded by COP. The value of the length field is the length of the record, in bytes, excluding the four bytes occupied by the length field itself. The time stamp field denotes the time the record was recorded. The format of the time stamp is in what COP refers to as "epic time". It is the count of elapsed seconds and microseconds from epic time which is 00:00:00.00 January 1st, 1989. The first four bytes are elapsed seconds, the next four bytes are elapsed microseconds. The Port_ID field denotes the COP defined logical port number for the collected data. The Status field is next and its value can be good or bad. A "bad" value means that COP determined that the message was invalid for some reason. The remaining bytes in the record are the actual recorded data.

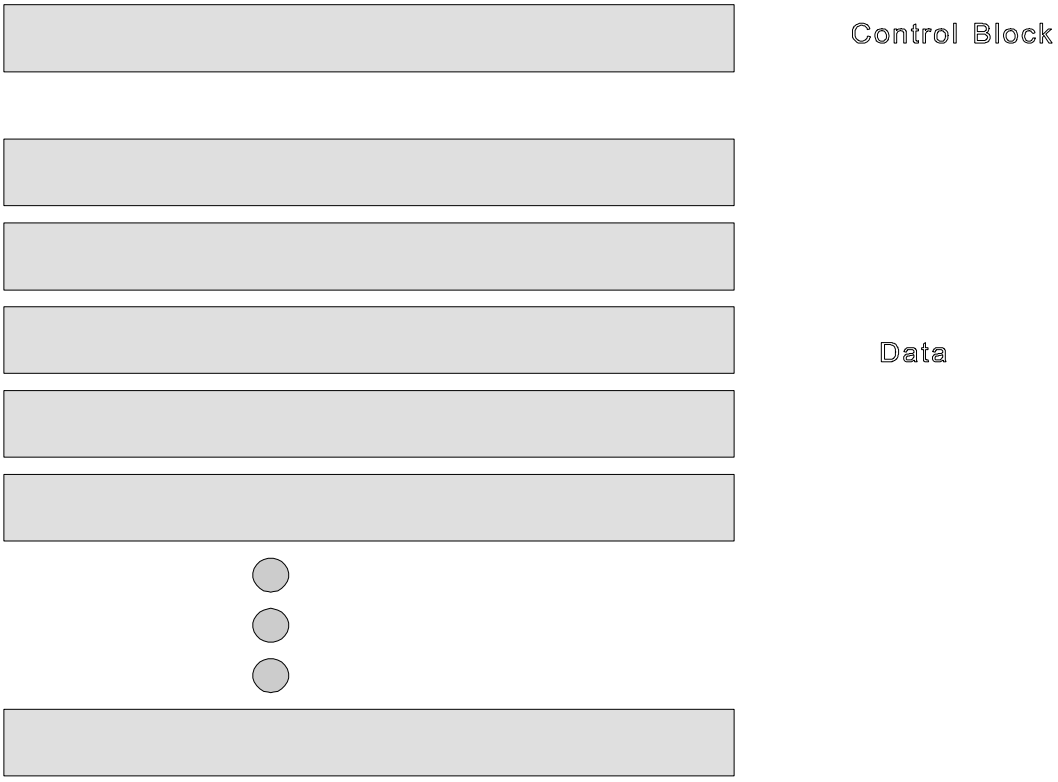


Figure 1-28. ODC Data Organization

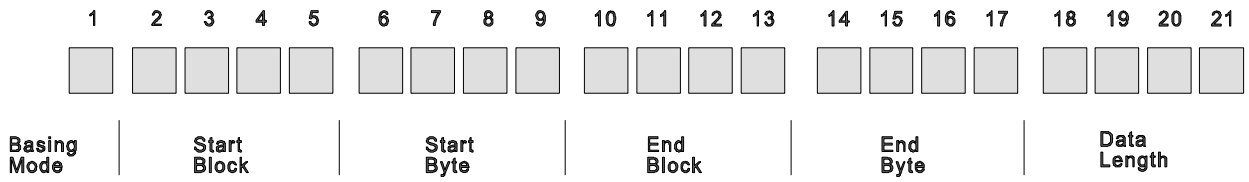


Figure 1-29. ODC Control Block Format

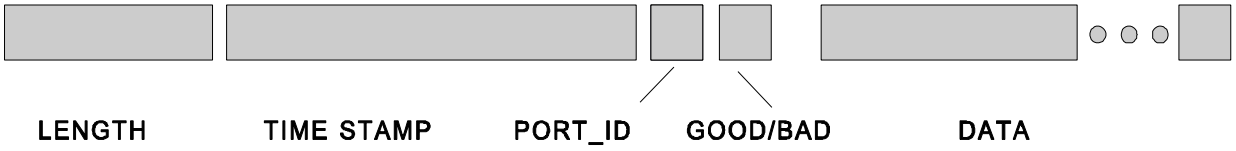


Figure 1-30. ODC Record Format

Figure 1-31. OSI Message Format

1-6.6.3.1. OSI Message Format. (Figure 1-31) The format of the data portion of each record is specific to the type of data recorded. At the highest level, the Port_ID field in the Record Header identifies the type of data recorded. For example, for a given record the Port_ID may be CMPG_In. This identifies to the software that the recorded data is one of the possible message types. Given this information, the software can examine the data and completely parse the message. The software ICD's should be referenced for more details regarding recorded data formats. However, there are a couple of formatting peculiarities that need mentioning here. In messages COP stores the information in a bit-reversed manner. The byte ordering is correct but the bits in each byte are the mirror image of what they should be. This is important when decoding specific fields within a message or when displaying the data in a Hexadecimal or Octal format. As an example, an OSI message is identified by function code "36" hex or "00110110" decimal. However, a raw OSI message as stored on diskette by COP will have a function code value of "6C" hex or "01101100" decimal. This is a mirror image of the correct function code value. A recorded message starts with the second bit of the "Unique Sync" field; the first bit is not recorded by COP.

1-6.6.4. ODC File Structure. The ODC file consists of:

Disk Header Information

Serial # of the Floppy Disk (n of 4)

File Control Block

Basing Mode

Start Block

Start Byte

End Block

End Byte

Data Length

Message Information

ODC Header

Length

Time Stamp

Port ID

Message Status

Message Text (format varies by port id, basing mode)

Note: ICDs 25-R001, 25-R007, and 25-R030 provide descriptions of the message text fields. The Message Text portion of each ODC record is in reverse bit format from the message text described in the ICDs.

1-6.6.5. ODC Formats. The individual types of formats are listed below and defined in the following paragraphs.

a. Input HICS Message.

b. Output HICS Message.

c. Output CMPG Card Control Message.

d. Output CMPG Card Time Data Message.

e. Tone Present Status Message.

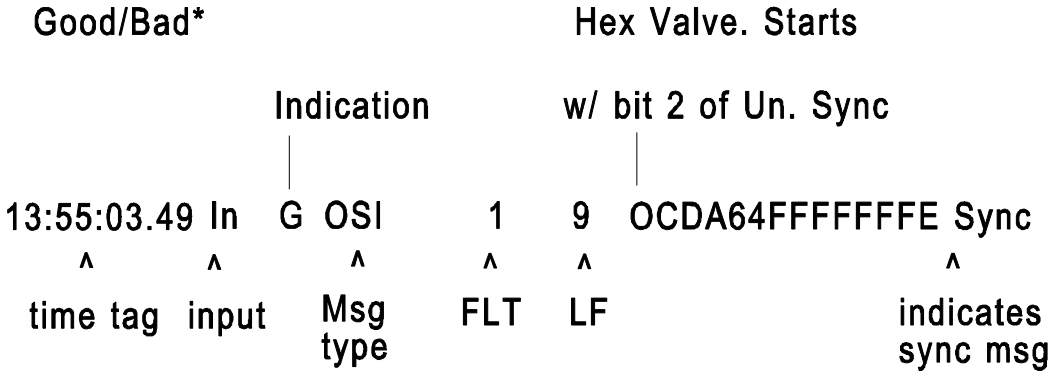
f. Tone Present Plus 1 Status Message.

g. Time Data Data Present Time Status Message.

h. No Data/Data Fault Indicator Status Message.

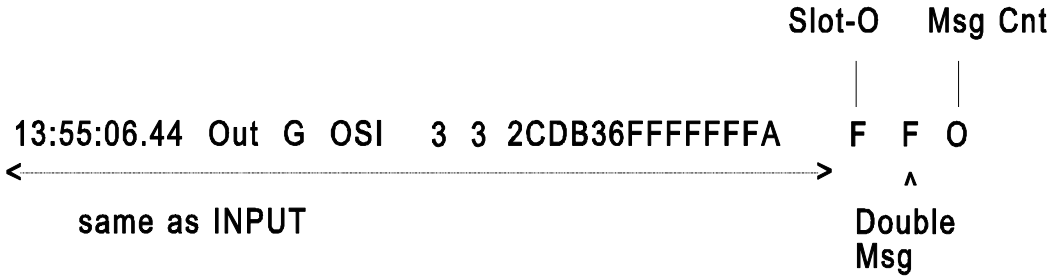
i. HAC/RMPE Message.

1-6.6.5.1. Input HICS Message. This format is valid for all input HICS Messages.

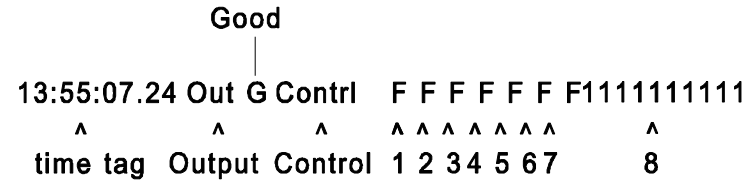


* If the value of the Good/Bad field is "Bad" then all fields to the right of this field are suspect and may, in fact, be garbage.

1-6.6.5.2. Output HICS Message. This format is valid for all output HICS Messages. The format as shown below is the same as for the input messages with the exception of the last 3 bits as indicated.

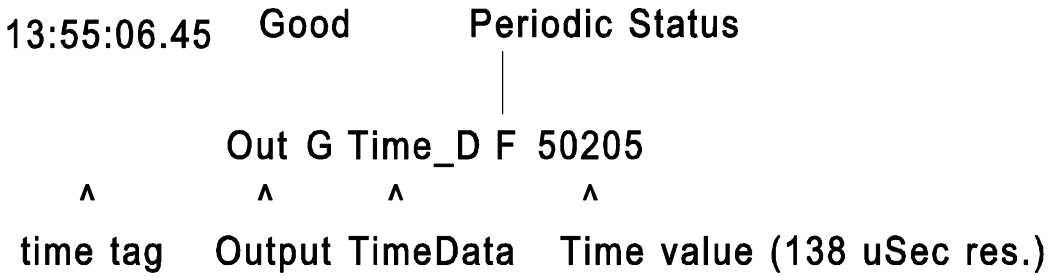


1-6.6.5.3. Output CMPG Card Control Message. The purpose for this control message is to configure the CMPG Car.



1. Periodic Status
2. Seize_Line
3. Req_TimeStamp
4. Loop CMPG
5. Loop RMB32
6. Diag High
7. Diag Low
8. Line Enable Flags

1-6.6.5.4. Output CMPG Card Time Data Message. The time value in this message is used to control when the start of slot occurs.



1-6.6.5.5. Tone Present Status Message. This status message is how the CMPG Card notifies COP that tone on line has been detected.

Time Tag	Status	Good	Tone Present Msg	Select Lines	
13:55:00.19	STS	G	Tone_P	0000000001	
				L1	L10

1-6.6.5.6. Tone Present Plus One Status Message. This status message is how the CMPG Card notifies COP that tone present plus one has occured.

Time Tag	Status	Good	Status Msg								L1		L10		
13:55:00.21	STS	G	Status	TP_P_1	T	F	T	F	1	1	1	1	1	F	F	F
				1		2	3	4	5		6		7	8	9	

1. Tone Present Plus One
2. Receive Data
3. XMT Tone lost
4. XMT Tone present
5. Frame Error
6. Tone on line
7. No Data
8. Data Timing
9. Transmit Clock

1-6.6.5.7. Time Data/Data Present Time Status Message. This status message is the time data that indicates when data present was detected.

Time Tag	Status	Good	Time Data Msg	Time (128 uSec Res.) Value
13:55:00.24	STS	G	Time_D_D_P_TIME	62483

1-6.6.5.8. No Data/Data Fault Indicator Status Message. This message indicates either no data was detected or a data fault was detected.

```
Time Tag
                Status  Good   Time Data ND_ind - No data indicator
                               Msg       DF_ind - Data Fault indic

     |           |      |        |           |

13:55:00.24   STS    G   ND_IDF    ND_Ind
```

1-6.6.5.9. HAC/RMPE Message Formats. This format is used for HAC/RMPE Data.

```
Time Tag       PortID  Good/Bad    Msg Type         Frame      Data
                                                    Data       Chksum
                                                    Length

     |            |      |            |               |           |

             HR_DATA  G   1    1         NO_ALARM  480   23   240

  16:51:12.00              |    |    TEST     |              |

                     Start      Frame      Alarm        Hdr
                     of Frame   Seq Num    type         Chksum
```

```
<------------------------------------------- Data -------------------------------------------->
*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U
*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U
*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U
*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U
*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U
*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U
*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U
*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U*U
```

SECTION II - LF SEQUENCES

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2-1. SCOPE. This section contains information concerning launch facility operating sequences. Charts and diagrams are included where there is unique application. For general application, diagrams references will be made to pertinent flow charts in section VIII and timing diagrams in section VII.

2-2. STARTUP. Startup from an unpowered condition consists of sequentially applying OGE and AVE power and performing the necessary operations which will result in the missile attaining strategic alert. (See Figure 2-1, Sheet 1 of 2)

2-2.1 OGE Power Startup. AC power (400 Hz, 120 VAC) is applied to the power supply group, programmer group, and G&C cooler. The 28 VDC power is then applied to the DC portion of the programmer group.

2-2.2 AVE Power Startup. The DC power to the missile is enabled by closing the G&C power circuit breaker which applies power up to the distribution box relays. Upon receipt of a G&C power on command gyro start power (40 VDC) is applied for about 6 seconds to start the IMU gyros, and 28 VDC is supplied to provide ground and flight control electronics power to the missile. (See Figure 2-1, Sheet 2)

The required power is now present to begin initialization and alignment when commanded. Upon successful completion of the alignment sequence the DCU will enter strategic alert and be in a launch readiness mode.

2-3. G&C PROGRAM ROUTINES. The Missile Guidance Set sequences through the various operating states and modes shown on Figure 2-33 as the result of the automatic sequencing, message response, faults detected etc. Those modes entered are the result of responding to command messages described in section VI. The auto sequencing functions not in direct response to command messages are described in the following paragraphs. See Figure 2-33 through 2-40 for OGP program structure.

2-4. ALIGNMENT. See Figure 2-2. Performs the operations necessary to place the system in, or return the system to, a state of instant readiness for launch following a startup or restart condition (initial and restart alignment subfunction), and following acceptance of a preparatory launch command (PLC) requiring platform realignment (retarget alignment subfunction).

2-4.1 Initial and Restart Alignment. The initial and restart alignment subfunction performs operations which cause:

a. Platform slewing to be accomplished in pitch, yaw, and roll to establish baseline platform position with respect to the platform roll gimbal stop and the local gravity vector.

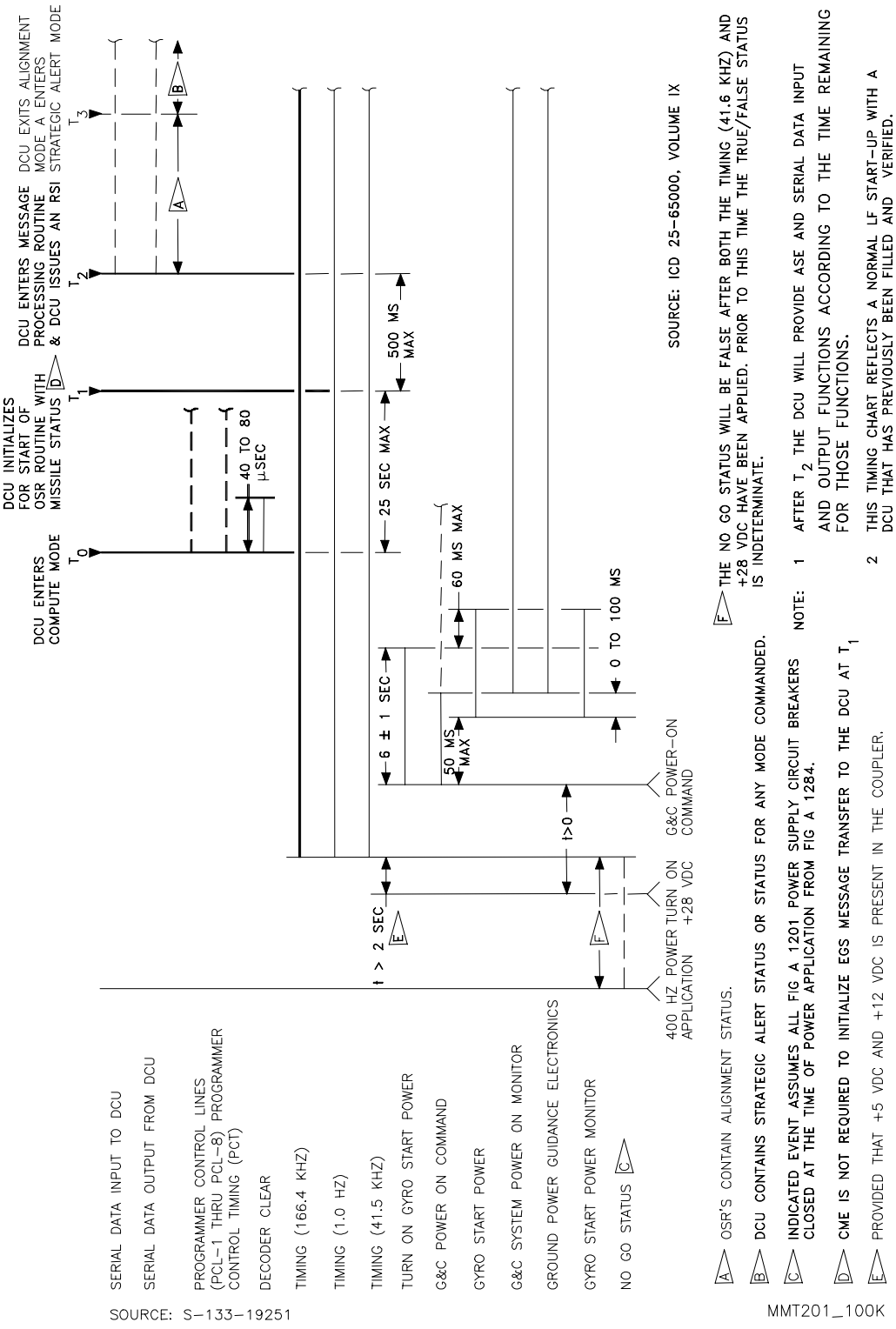


Figure 2-1. Startup Sequential Diagram (Sheet 1 of 2)

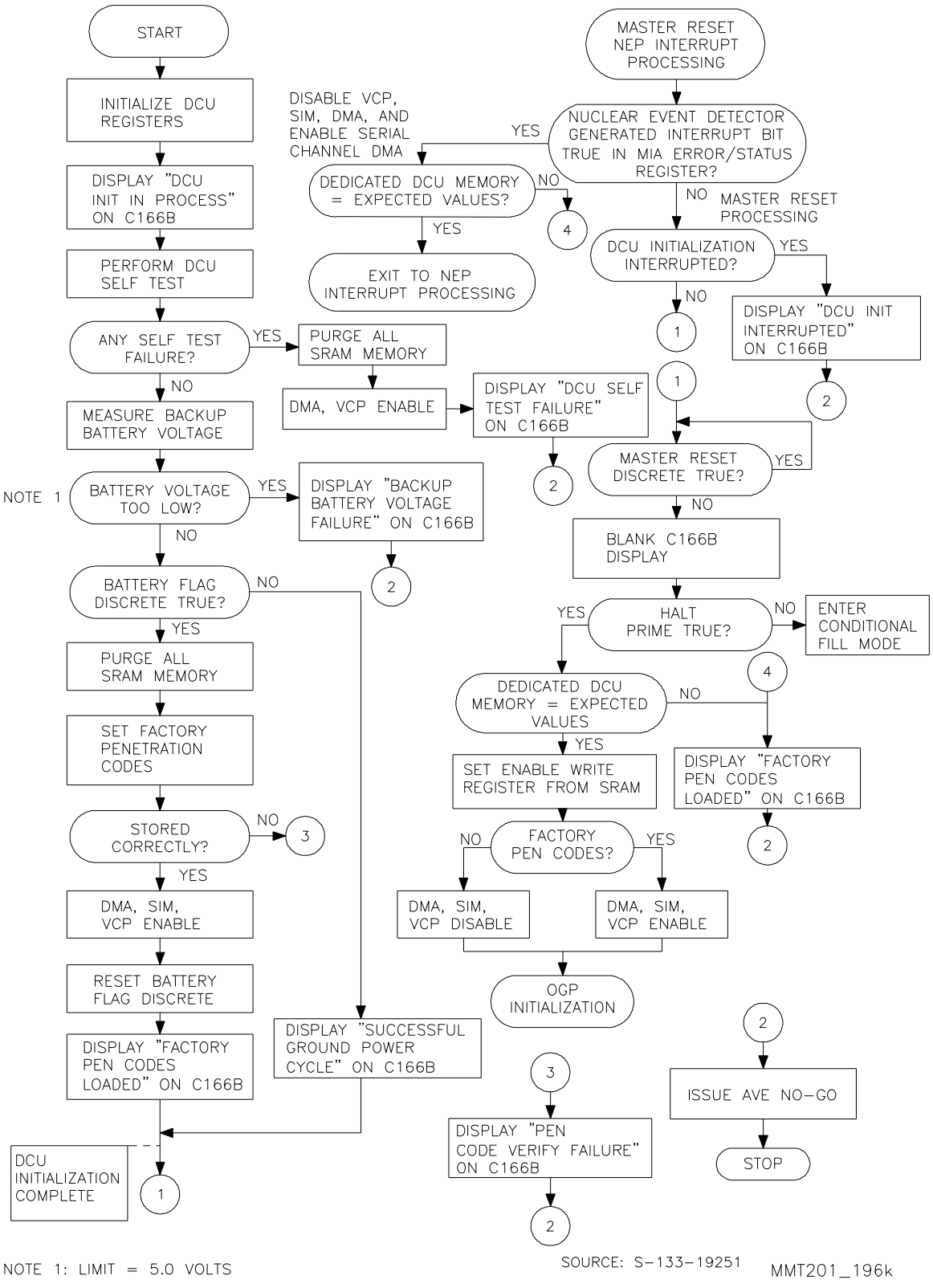


Figure 2-1. Startup Sequential Diagram (Sheet 2 of 2)

b. Alignment checks to be performed utilizing LD1 and LD4 rates to ensure positioning the gyrocompass assembly (GCA) relative to the stable platform to a specific optical electrical resolver (OER) null.

c. The GCA to be slewed to properly position it relative to the stable platform for the selected target azimuth.

d. Erection (platform leveled to LD No. 1) and alignment of the down-range axis of the platform to the selected target azimuth using a roll gimbal edge as an azimuth reference. This reference is used to maintain platform azimuth alignment.

e. Fuzing of the Reentry System as determined by the target selected for alignment.

f. The gimbal resolver registers to be initialized to allow for the accumulation of missile attitude excursions from the initial reference position.

g. Computation of pendulous integrating gyro accelerometer (PIGA) and platform stabilization gyro (G6B4) instrument biases.

h. Computation of the platform azimuth heading.

i. Monitoring of hostile environment flag.

j. Inertial instrument performance to be checked so that the operator can be advised of the missile operational status, and in the event of a failure, failure mode data to be generated to aid in maintenance.

2-4.2. Reentry System Fuzing. The reentry system (R/S) fuzing operation performs a prescribed set of operations to command the turn on of the R/S ground power, to transmit fuzing information to each reentry vehicle (R/V), and to verify the fuzing information when it is retransmitted from the R/S back to the DCU. The DCU controls the R/S fuzing operation through character outputs to the coupler unit in the OGE and one direct lines to the R/S. The coupler unit converts the character outputs from the DCU providing R/S ground power turn-on and transmitting the 36-bit fuzing information to the reentry system over the R/S input data line 1 and R/S input data line 2 lines. The reentry system then sets the R/S monitor ready signal true when it is ready to retransmit the 36-bit message back to the DCU via the coupler unit. The coupler unit receives the message from the R/S on the R/S output data line clocked by the R/S data 2 line. The coupler unit relays this information to the DCU through the multiplexer input lines. Finally, the DCU compares the 36-bit message it received with the message it has sent to determine if any errors occurred. If the comparison checks, the operation is repeated until all of the R/Vs in the

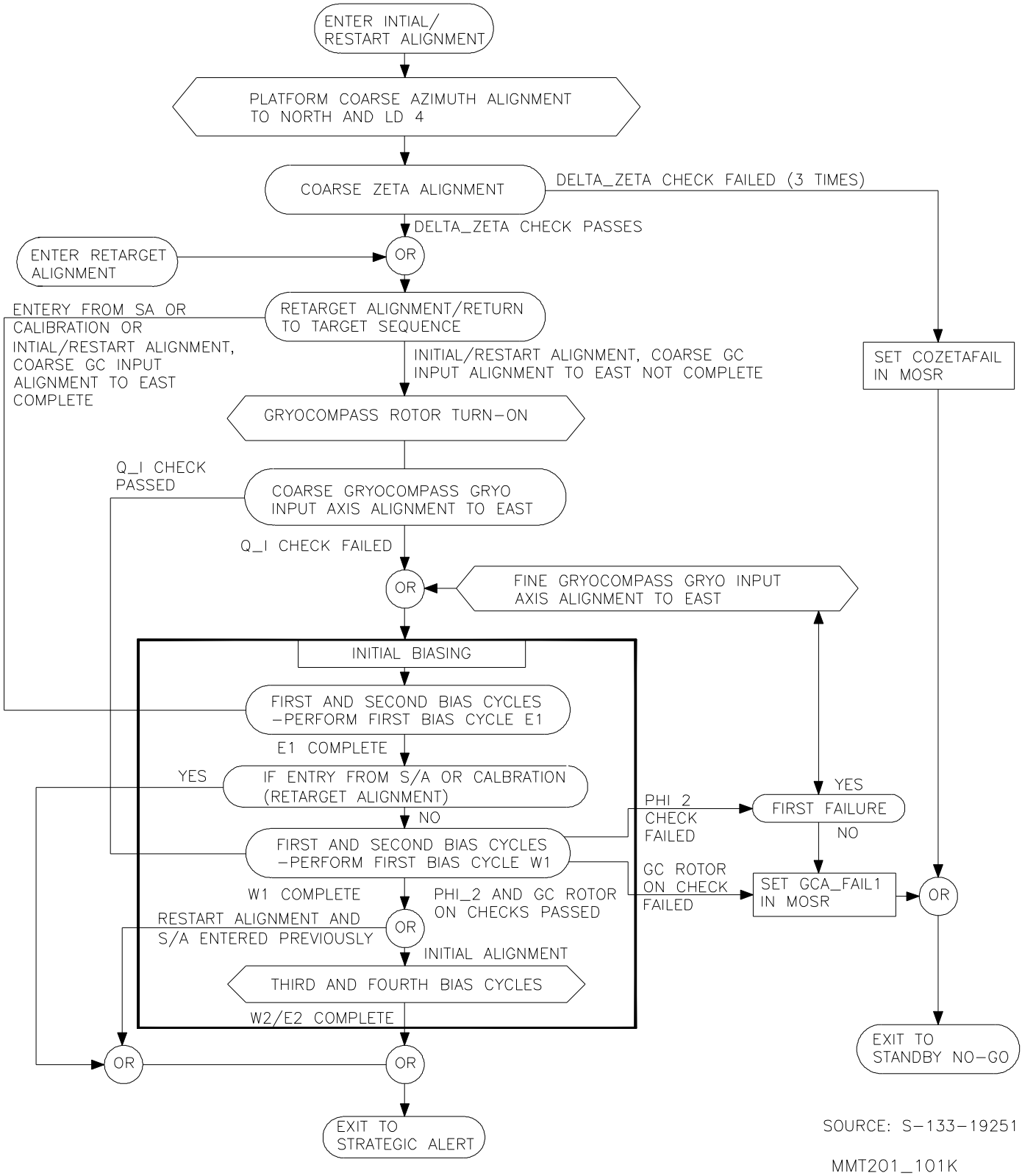


Figure 2-2. Initial/Restart Alignment and Retarget Alignment Sequence

R/S are fuzed. If the comparison fails, a second attempt is made to fuze the R/V. If the fuzing attempt fails the second time, depending on the conditions for the failure, proper system flags are set.

2-4.2.1. Conditions for Reentry System Fuzing. The R/S fuzing operation shall be initiated whenever any of the following conditions exist:

a. An active target exists and a partial tape fill or a restart alignment sequence is performed.

b. DCU acceptance of a preparatory launch command (PLC). A second PLC accepted by the DCU shall automatically restart the fuzing sequence with all R/Vs fuzed, as specified by the new PLC.

2-4.3. Retarget Alignment. The retarget alignment function consists of items c. through j. except for item g. of paragraph 2-4.1.

2-5. STRATEGIC ALERT. See Figure 2-41. Strategic Alert performs the operations necessary to maintain the system in a state of instant readiness for launch in a nonhostile environment (strategic alert biasing subfunction) or a hostile environment (strategic alert PIGA leveling subfunction).

2-5.1. Strategic Alert Biasing Function. See Figure 2-41. The strategic alert biasing function performs operations which cause:

a. The platform to be maintained in level (LD No. 1 reference) and aligned to a specific target azimuth (roll gimbal edge azimuth reference).

b. Tracking of missile attitude excursions from initial reference position.

c. Computation of PIGA and platform stabilization (G6B4) gyro instrument biases.

d. Computation of the platform azimuth heading.

e. Inertial instrument performance to be checked for missile operational status, and in the event of a failure, failure mode data to be generated to aid in maintenance.

f. Monitor for a hostile event.

2-5.2. Strategic Alert PIGA Leveling. (See Figure 2-42) The strategic alert PIGA leveling function performs operations which cause:

a. The platform is maintained in level and aligned to a specific target azimuth by calculating G6B4 gyro bias and platform attitude errors with the platform Y-axis caged to the Gyrocompass Pickoff Monitor and platform X and Z-axes in free inertial. Periodically, the gyro biases will be updated and the platform will be repositioned to correct the platform attitude errors.

b. Tracking of missile attitude excursions from the initial reference position.

c. Inertial instrument performance is checked for missile operational status.

2-6. CALIBRATION. Calibration performs the operations necessary to determine the following:

a. The misalignment angles about the level axes between the platform reference and platform alignment coordinate systems (Phi calibration subfunction).

b. Inertial measurement unit calibration subfunction.

(1) The elements of the velocity transformation matrix (Q matrix) which defines the relationship between the pendulous integrating gyro accelerometer (PIGA) coordinate system and the platform alignment coordinate system.

(2) The PIGA biases in PIGA coordinates.

(3) The error in orthogonality between the normals to level detector 1 and level detector 2.

c. The misalignment angle (Ø3) estimate between the gyrocompass input axis and the plane described by the normal to level detector 2 (perturbation self-alignment technique calibration subfunction).

d. If the performance of the platform servo loops has been degraded.

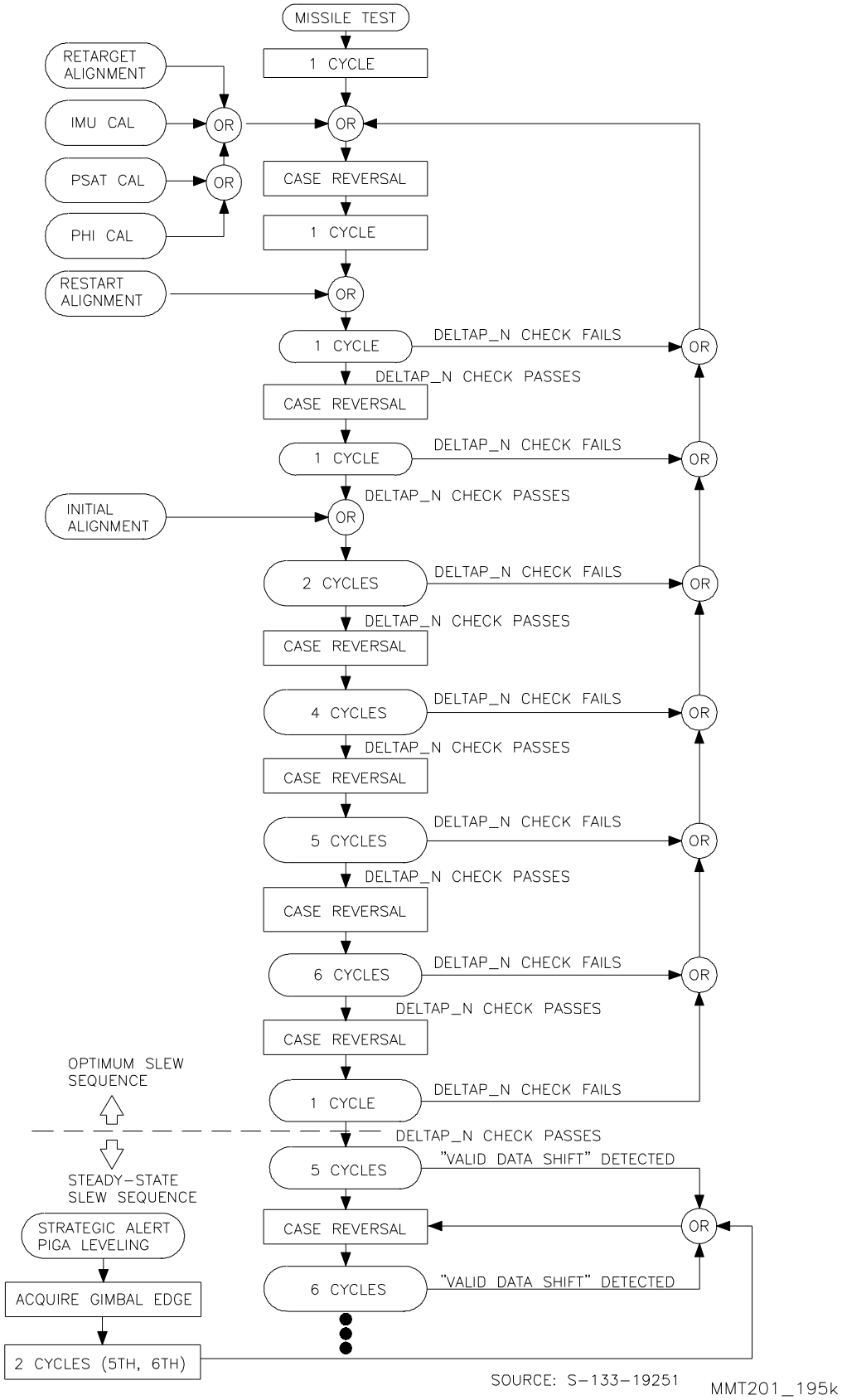


Figure 2-3. Gyrocompass Bias Cycle Sequence

2-6.1. Processing. Calibration shall perform Phi calibration, inertial measurement unit (IMU) calibration, and perturbation self-alignment technique (PSAT) calibration processing as specified below. During Phi calibration or IMU calibration, the IMU calibration/Phi calibration indicator shall be set. During PSAT calibration, the PSAT calibration indicator shall be set. If a hostile environment is detected the hostile event indicator shall be set true. High level seismic detection operations and DCU circumvention and circumvention reset processing shall be performed. If an execute launch command (ELC) or a preparatory launch command (PLCA sequence) is accepted while in calibration the strategic alert mode shall be entered within 15 minutes, 95 percent of the time, and within 20 minutes, 99 percent of the time.

2-6.2. Phi Calibration. Phi calibration shall be entered upon acceptance of a missile calibrate command (MCC) in strategic alert (biasing) indicating Phi calibration or when the Phi calibration is indicated by the Program Data. Refer to Figure 2-4 for a general description of the phi calibration sequence. The time required for each successful calibration sequence (i.e., removal from strategic alert, no portion repeated and return to strategic alert) shall not exceed 2.5 hours. The total time including a repeat shall not exceed 5.0 hours. Platform servo transient response test shall be performed at the end of phi calibration to determine if degraded performance in the platform servo loops exists.

2-6.2.1. Phi Matrix Determination. The phi matrix shall be determined by establishing a reference orientation so that the platform reference axes coincide with the platform alignment axes. PIGA pulse rates shall then be determined at the reference orientation and at seven different GCA positions. These data shall be used to calculate the rotation about the level axes relative to the reference position. A least squares sinusoidal fit shall then be calculated from the accumulated data resulting in parameters A_1 and A_2. Using these constants, a solution for the misalignment angle Phi matrix shall be determined for any azimuth angle.

2-6.2.2. Platform Servo Transient Response Test. The platform is tested to verify that the roll, yaw and pitch servo loops are operating properly. Torque disturbance voltages are applied to the X, Y and Z platform amplifiers and then the platform is checked for loss of control by checking the count in the gimbal resolver registers. If the count exceeds the limit the MOSR for IMU servo failure will be set and standby no-go will be entered.

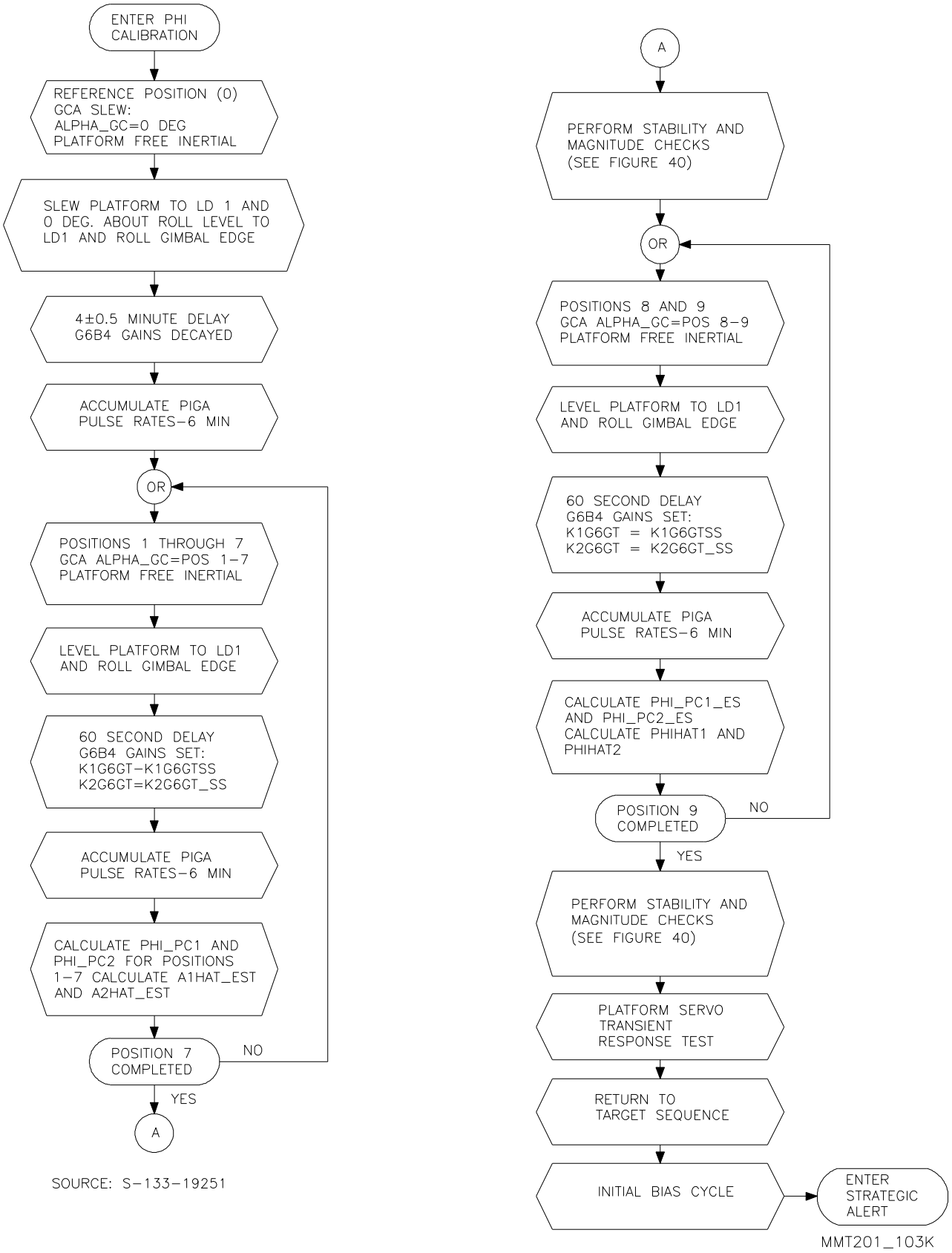


Figure 2-4. Phi Calibration

2-6.3. Inertial Measurement Unit Calibration. The inertial measurement unit (IMU) calibration subfunction consists of two IMU calibration segments. IMU calibration segment 1 contains a four (level detector) position calibration sequence. IMU calibration segment 2 contains a six-position bootstrap calibration sequence, utilizing gimbal edge held positions (each PIGA up and down). Refer to Figure 2-5 (IMU calibration) for a general description of the inertial measurement unit calibration sequence.

2-6.3.1. Inertial Measurement Unit Calibration Segment 1. Inertial measurement unit (IMU) calibration segment 1 shall be entered upon acceptance of an MCC in strategic alert (biasing). The IMU calibration advised MOSR bit shall be set true when entering IMU calibration segment 1. Figure 2-5A (IMU Calibration) presents a general description of the segment sequence. The time required for each successful calibration sequence (i.e., removal from strategic alert, no portion repeated and return to strategic alert) shall not exceed 2.5 hours. The total time including a repeat shall not exceed 5.0 hours.

2-6.3.2. Inertial Measurement Unit Calibration Segment 2. See Figure 2-5B. Inertial measurement unit (IMU) calibration segment 2 shall be entered upon acceptance of a MCC in strategic alert (biasing). The time required for each successful calibration sequence (i.e., removal from strategic alert, no portion repeated and return to strategic alert) shall not exceed 2.0 hours. The total time including a repeat shall not exceed 4.0 hours.

2-6.4. Perturbation Self-Alignment Technique Calibration. See Figure 2-6. Perturbation self-alignment technique (PSAT) calibration shall be entered upon acceptance of a self-alignment technique calibrate command (SATCC) in strategic alert (biasing) if GCA Failure No. 1, Low Level Seismic, and GCA/Platform Indexing Advised are false, and at least 12 bias cycles have been completed following either a platform slew during a return to target sequence, or entry to strategic alert biasing from PIGA Leveling. The PSAT calibration G6B4 earth rate correction and extended perturbation sequence shall be performed. PSAT calibration shall not exceed 5.7 hours.

2-6.4.1. PSAT Operations. PSAT operations will cause:

a. Gyrocompass scale factor check.

b. Determination of mass unbalance angle.

c. Platform stabilization gyro perturbation.

d. Input axis misalignment angle calculations.

e. Return to target sequence.

f. Initial bias cycle.

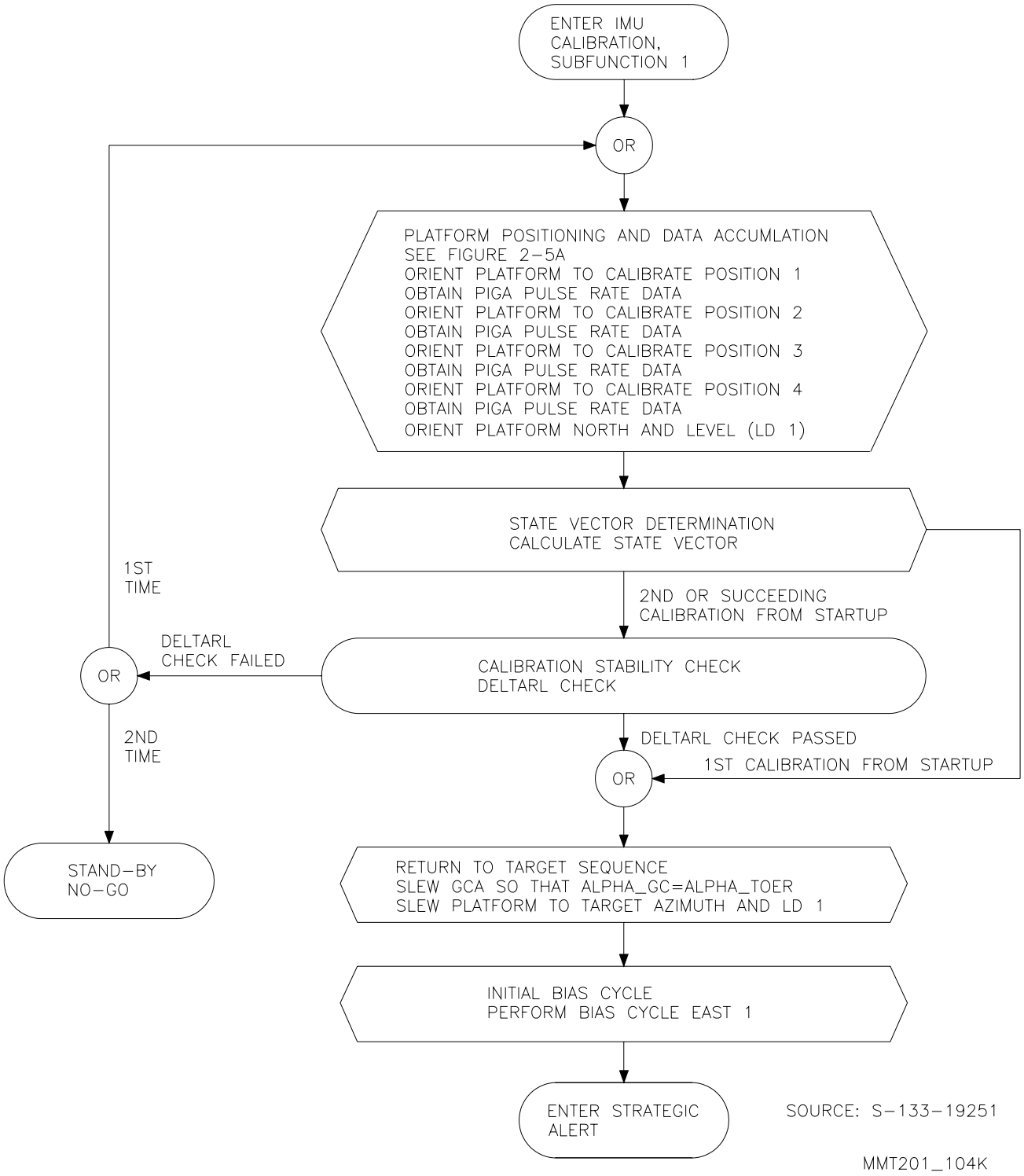
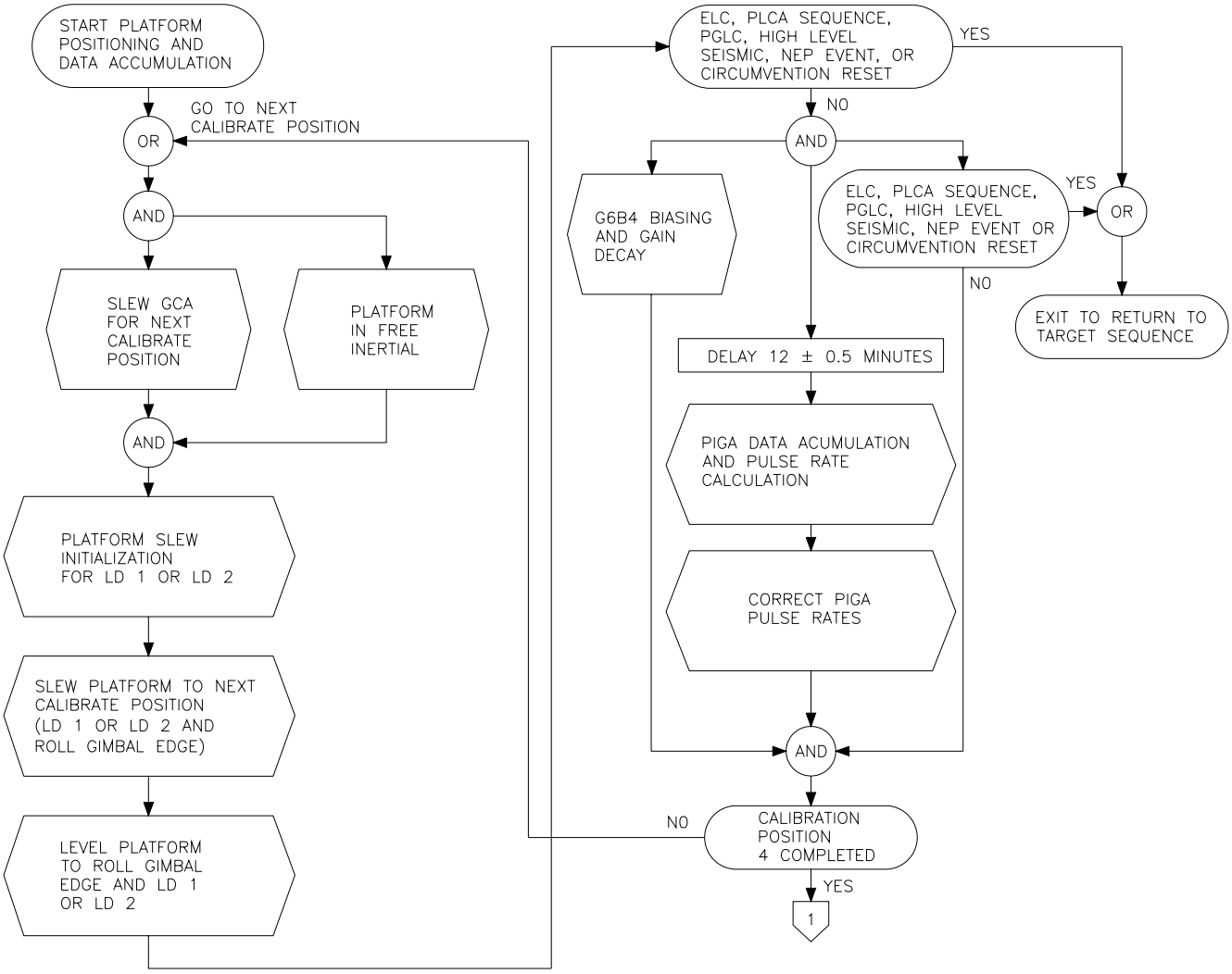


Figure 2-5. IMU Calibration Subfunction 1

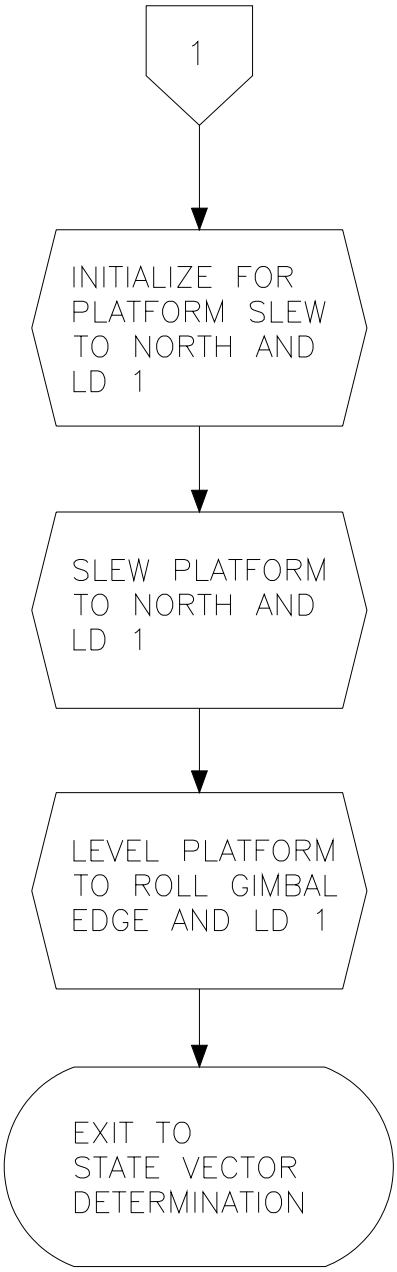


CALIBRATION POSITIONS

POSITION	ORIENTATION	LEVEL DETECTOR REFERENCE	PLATFORM ORIENTATION (PITCH, YAW, ROLL)
1	ALPHA_GC = 0 DEG	LD 1	(0 DEG, 0 DEG, 0 DEG)
2	ALPHA_GC = 166 DEG	LD 2	(−90 DEG, −14 DEG, 0 DEG)
3	ALPHA_GC = 194 DEG	LD 2	(−90 DEG, +14 DEG, 0 DEG)
4	ALPHA_GC = 0 DEG	LD 3	(+90 DEG, 0 DEG, 0 DEG)

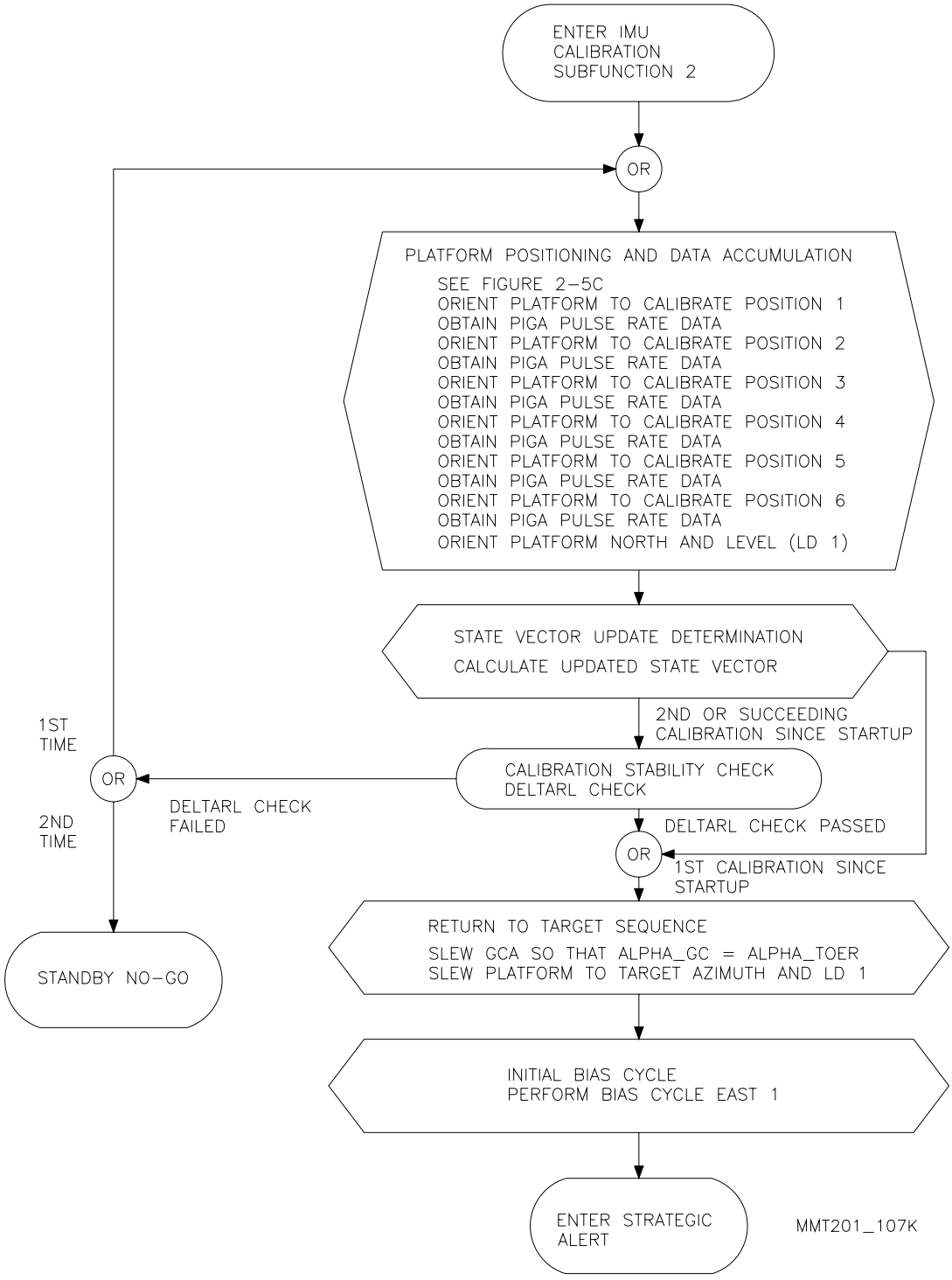
MMT201_105K

Figure 2-5A. Platform Positioning and Data Accumulation (Subfunction 1) (Sheet 1 of 2)



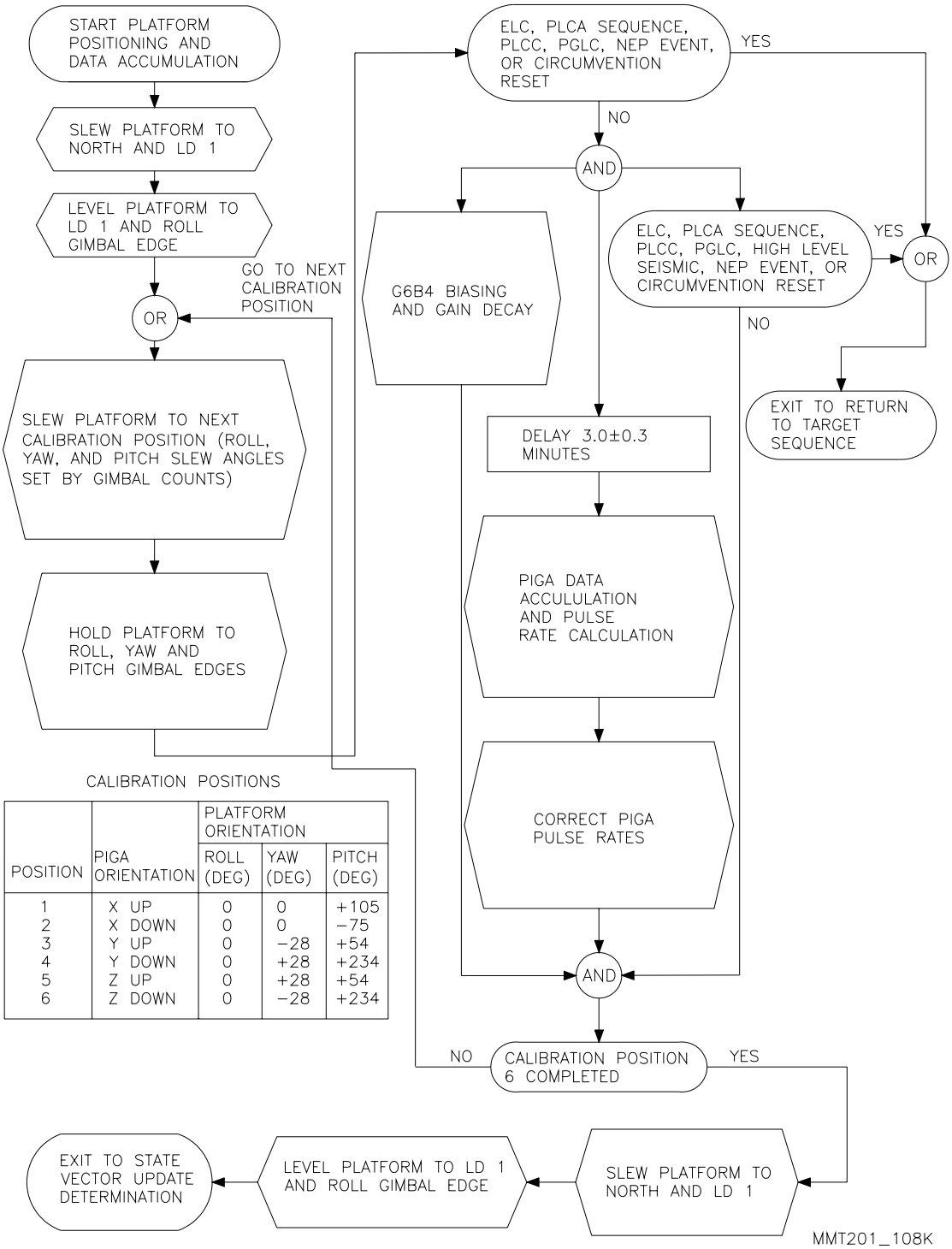
SOURCE: S-133-19251

Figure 2-5A. Platform Positioning and Data Accumulation (Subfunction 1) (Sheet 2 of 2)



SOURCE: S-133-19251

Figure 2-5B. IMU Calibration Subfunction 2



Source: S-133-19251

Figure 2-5C. Platform Positioning and Data Accumulation (Subfunction 2)

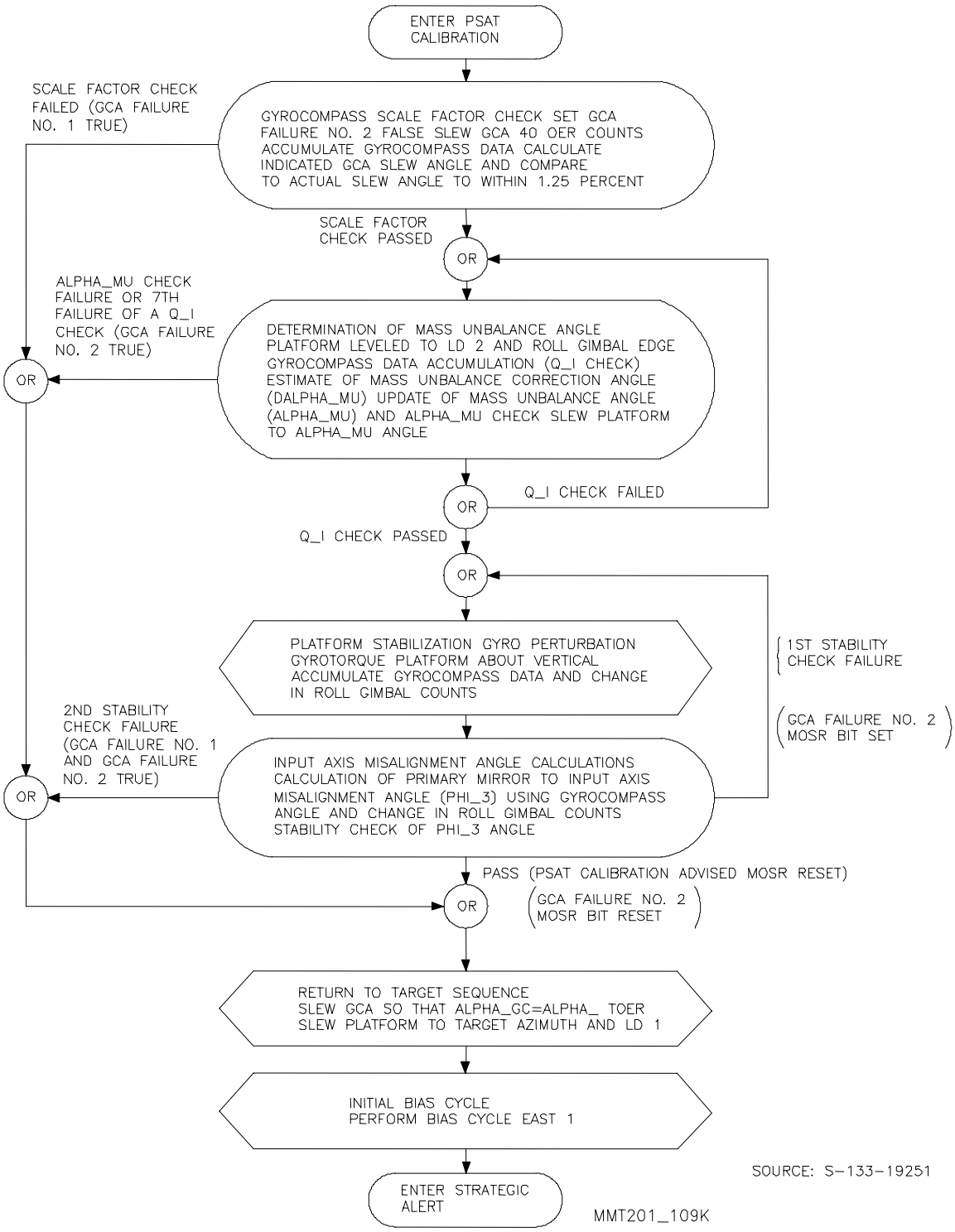


Figure 2-6. Perturbation Self-Alignment Technique Calibration Sequence

2-7. ENABLE STATES. The enable states performs the operations to test and arm the missile command signal decoder CSD(M), enable performance of the CSD(M) code change mode, transition to the appropriate state, and maintain system operation in the appropriate state. The enable states establishes and maintains the CSD(M) code change mode, enable test mode, enable state, disenabled commanded state, disenabled state and CSD(M) penetration mode (See Figure 2-7).

a. The CSD(M) code change mode function provides the logic necessary to enable a CSD(M) code change without entering the standby no-go Mode due to a CSD(M) off-home condition.

b. The enable test provides the logic necessary to step the CSD(M) to the test position and to verify that the device stepped as commanded.

c. The enabled state provides the logic which monitors the armed condition of the CSD(M). This subfunction co-exists with the launch modes and is the function which is mandatory for all active launch modes.

d. The disenable commanded state maintains the system in a transitory condition between the enabled state and the disenabled state and provides logic for monitoring the armed condition of the CSD(M).

e. The disenabled state provides the logic for maintaining the CSD(M) in the home position except during an enable test, during the CSD(M) code change mode, or during a CSD(M) penetration attempt. It also provides the logic to enable performance of an inhibit test or a CSD(M) code change. After acceptance of an enable command and following successful penetration of the CSD(M) to the armed condition, the system proceeds to the enabled state.

f. The CSD(M) penetration provides the logic necessary to step the CSD(M) to the armed position. It verifies that the CSD(M) armed as commanded, or if it did not arm, provides an appropriate indication to the launch control facility.

g. The CSD(M) reset sequence provides the logic for resetting the CSD(M) to the home position. The system then proceeds to the disenabled state.

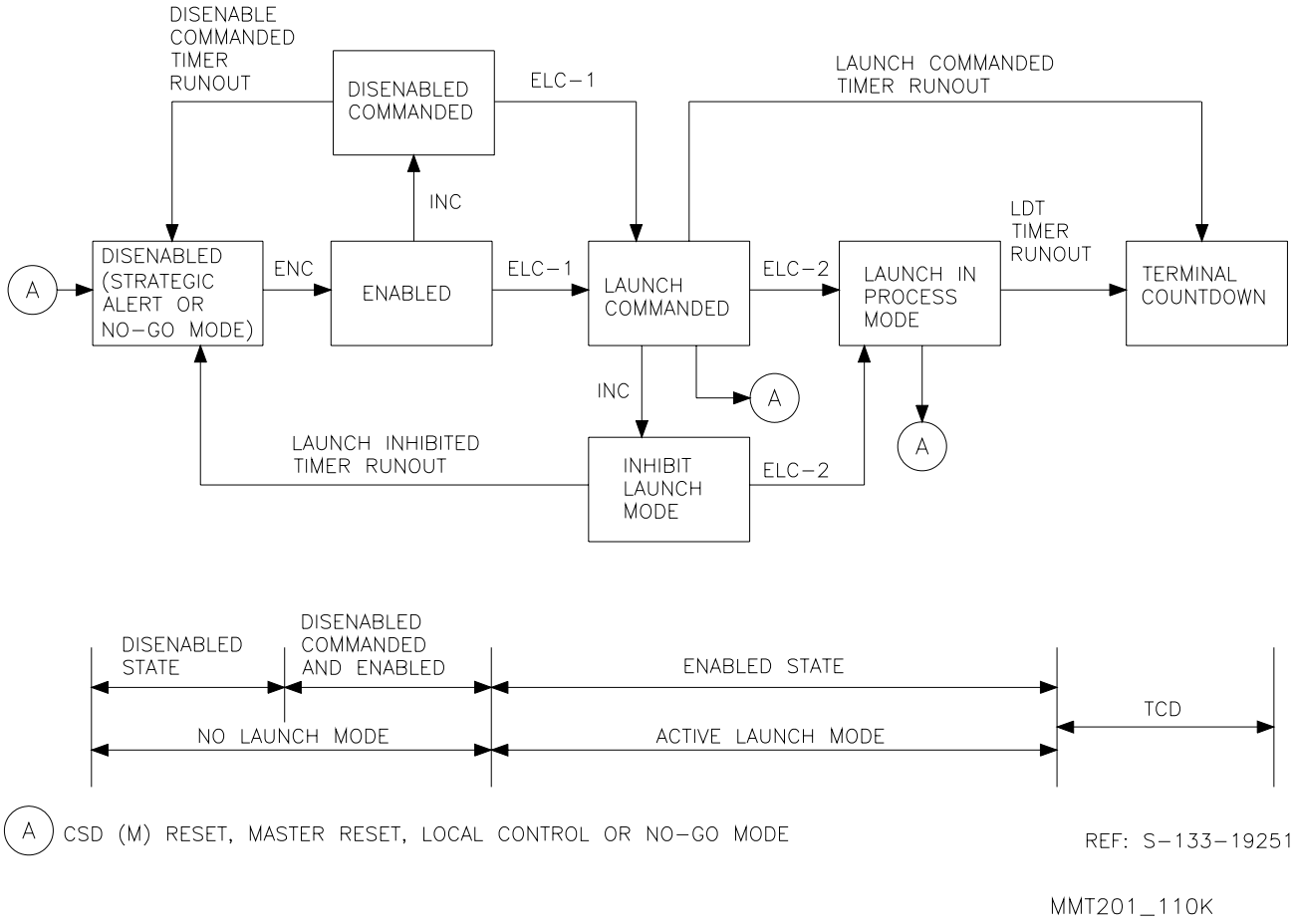


Figure 2-7. Launch and Enable States

2-7.1. <u>Command Signal Decoder (Missile) Code Change Mode</u>. The CSD(M) code change mode shall perform functions as follows:

a. When a false state occurs on CSD(M) home and a true state occurs on CSD(M) computer home monitor, this mode shall:

(1) Inhibit the system from entering the standby no-go mode due to a CSD(M) off home condition.

(2) Set the CSD(M) code change mode in the MOSR when the conditions of item a. above are determined to exist for two consecutive samples taken at least one second apart. The CSD(M) code change mode shall be reported in at least one MOSR response.

(3) The CSD(M) computer home monitor and the CSD(M) armed prime monitor shall be sampled at least once per second. If at least one sample of the CSD(M) computer home monitor is false and none of the CSD(M) armed prime monitor samples are false prior to terminating the CSD(M) code change mode, CSD(M) control failure shall be set in the MOSR. In addition, the standby no-go mode of no-go processing shall be initiated and commanded restarts via restart alignment initialization shall be inhibited.

b. Terminate the CSD(M) code change mode when CSD(M) home and CSD(M) computer home monitor are both true and cause the CSD(M) code change mode to be reset in the MOSR if it has been issued for at least one MOSR reply.

2-7.2. Enable Test. See Figure 2-8. When an ENTC is received while the CSD(M) computer home monitor is true, the CSD(M) reset command is false and the CSD(M) code change mode is not in process, enable test shall:

a. Initiate the CSD(M) penetration sequence by issuing character outputs in order to penetrate the CSD(M) to the test position. The character outputs shall be based on the ENTC penetration code. For the first enable test following entry into initial alignment (power turn-on, complete tape fill, or partial tape fill) or restart alignment (commanded or automatic), the ENTC penetration code shall be set to the operational test XYL code, 36276747_8. Providing that the first enable test was successful, the maintenance code, 25252525_8 shall be used for the second enable test and each succeeding enable test shall use the one's complement of the previous ENTC penetration code sent to the CSD(M). Otherwise, the operational test XYL code shall be used for subsequent enable tests until the test is successful. A "1" bit in the test code shall result in the issuance of the CSD(M) mark character output code. A "0" bit in the test code shall result in the issuance of the CSD(M) space character output code. The test penetration rate shall not be slower than that used to arm the CSD(M). After a delay of 58 to 100 msec from issuing a CSD(M) mark or CSD(M) space character output code, the CSD(M) mark or CSD(M) space shall be reset by issuing resets codes 15-1 through 15-7.

Note: There shall be a delay of 58 to 100 msec after the issuance of the resets specified above, before the issuance of the next CSD(M) mark or CSD(M) space.

b. CSD(M) drive enable shall be monitored at least once during the code transfer. CSD(M) drive enable failure shall be set in the MOSR if CSD(M) drive enable is false.

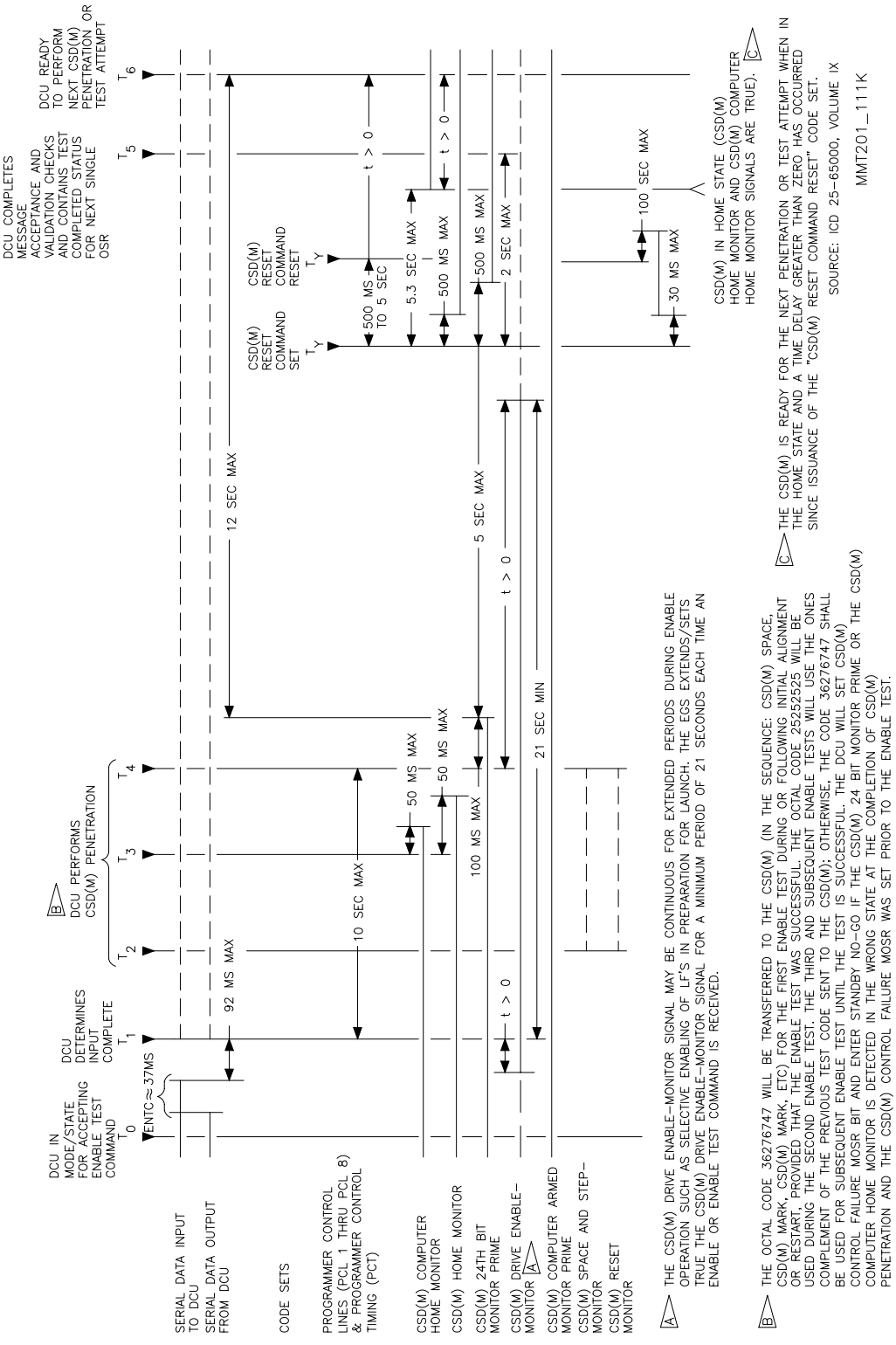


Figure 2-8. Enable Test Sequential Timing Diagram

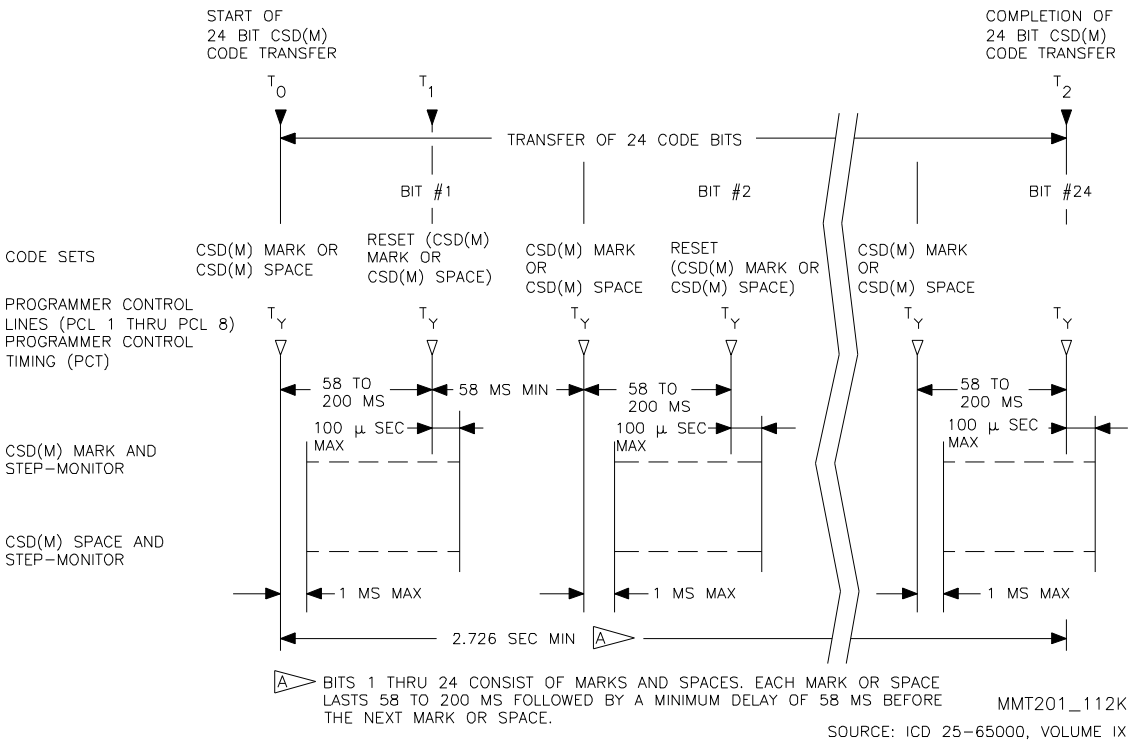


Figure 2-9. CSD(M) 24 Bit Code Transfer Sequential Timing Diagram

c. Upon completion of the CSD(M) penetration, and at least 100 msec after issuing the resets for the last CSD(M) mark or space in item a. The CSD(M) 24th bit monitor, the CSD(M) computer home monitor, and the CSD(M) armed prime monitor shall be monitored. If these inputs are in the true, false, and true states, respectively, the test was successful and CSD(M) control failure shall be reset in the MOSR. If the inputs are not in the specified states, CSD(M) control failure shall be set in the MOSR. If a circumvention reset did not occur during the penetration sequence and CSD(M) control failure had previously been set in the MOSR, entry to the stand no-go mode of no-go processing shall be initiated. If the CSD(M) armed prime monitor is false, restarts via restart alignment initialization shall be inhibited and standby no-go entered regardless of whether or not a circumvention reset occurred or if the CSD(M) control failure MOSR is set.

d. Cause CSD(M) reset command reset to be issued from 0.5 to 5.0 seconds after having caused the issuance of CSD(M) reset command set as specified in step c. above. If entry to local communications, standby no-go or restart occurs subsequent to issuing CSD(M) reset command set, the 0.5 to 5.0 second delay shall be 0.5 to 7.5 seconds.

e. Upon completion of the enable test, the test completed bit shall be set in the OSR. The true state shall be reported for one OSR response.

f. Terminate the enable test upon occurrence of any of the conditions specified below:

(1) Completion of all functions described above.

(2) Entry into the restart alignment. Cause the enable test to be truncated in an orderly manner by causing issuance of resets codes 15-1 through 15-7, and CSD(M) reset command set. Subsequently, after a delay of 0.5 to 5.0 seconds, cause CSD(M) reset command reset to be issued.

(3) Entry into standby no-go mode of no-go processing. Cause enable test to be truncated in an orderly manner by causing issuance of resets codes 15-1 through 15-7 and CSD(M) reset command set. Subsequently, after a delay of 0.5 to 5.0 seconds, cause CSD(M) reset command reset to be issued.

(4) Entry into local communications. Cause the enable test to be truncated in an orderly manner by causing issuance of resets codes 15-1 through 15-7 and CSD(M) reset command set. Subsequently, after a delay of 0.5 to 5.0 seconds, cause CSD(M) reset command reset to be issued.

2-7.3. Enabled State. Entry into the enabled state will occur upon:

a. Successful arming of the CSD(M) during the disenabled state, via an LF or all call addressed ENC, as determined by ENC address, which satisfies the requirements of remote communications. See Figures 2-10 and 2-11.

b. Receipt of an ELC during the disenable commanded state.

2-7.3.1. Entry Into the Enabled State. Entry into the enabled state shall:

a. Set enabled state in the system status.

b. Monitor CSD(M) armed prime monitor at least once each 5 seconds. If the CSD(M) armed prime monitor is true, CSD(M) control failure is set in the MOSR within 5 seconds of terminating the enabled state.

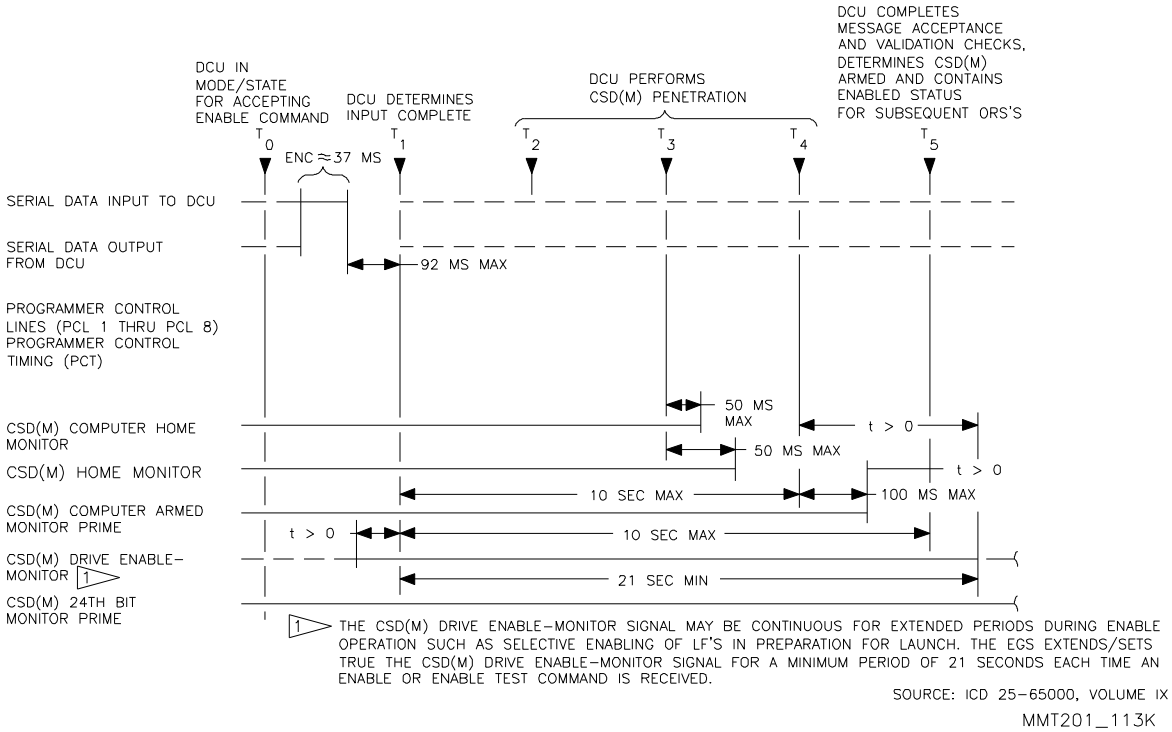


Figure 2.10. Enable Sequential Timing Diagram

c. Set improper command in the OSR if an INC is received with INC secure code 1 and 2 that is not identical to the prestored code; namely inhibit command code 1 and inhibit command code 2. Improper command shall be reported for a nominal period of 5 minutes.

d. Any memory locations dedicated to CSD(M) secure code storage shall be cleared.

2-7.3.2. Terminate the Enabled State. Terminate the enabled state upon occurrence of any of the conditions specified below:

a. Expiration of the Disenable Commanded Timer. Upon termination of the Disenable Commanded State, initiate Disenabled State processing.

b. Entry in local communications (initiate disenabled state processing).

c. Entry into standby no-go mode of no-go processing (initiate disenabled state processing).

d. Entry into the restart section of alignment (initiate disenabled state processing).

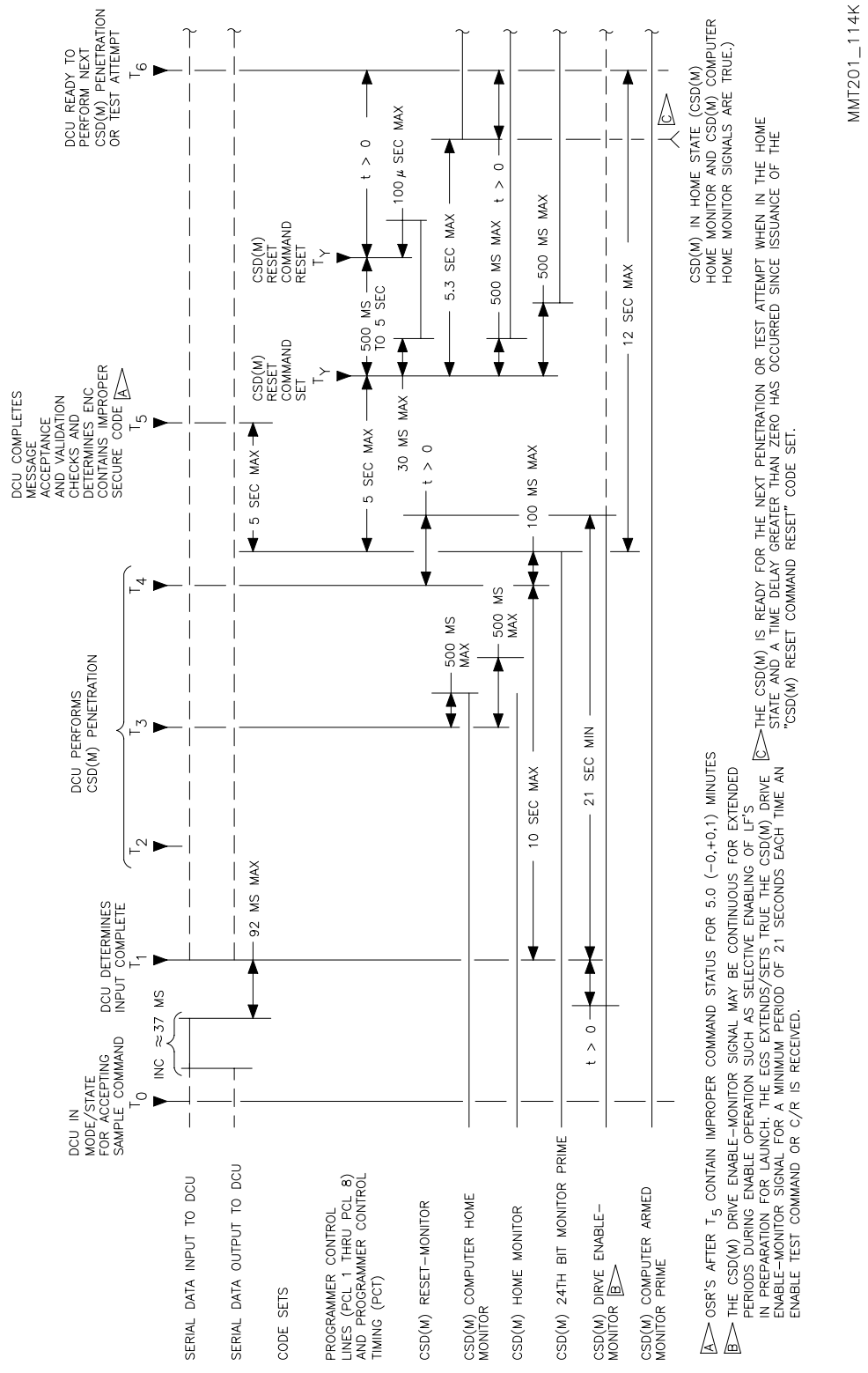


Figure 2-11. Improper Enable Command Sequential Timing Diagram

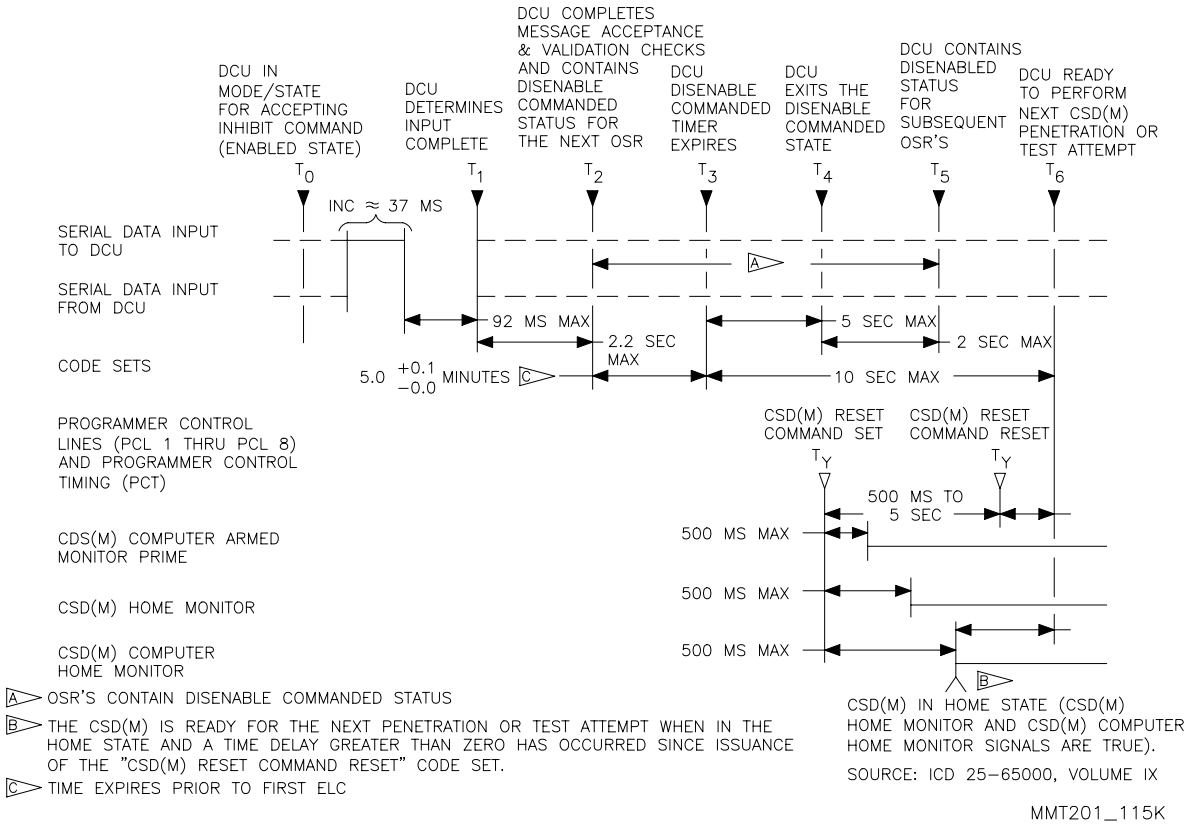


Figure 2-12. Disenable Sequential Timing Diagram

e. Detection of a true state on CSD(M) armed prime monitor (initiate disenabled state processing).

f. Expiration of the launch inhibited time during the launch inhibited mode (initiate disenabled state processing).

2-7.4. <u>Disenabled State</u>. Entry into the disenabled state shall occur within 5 seconds upon:

a. Detection of a true state on CSD(M) armed prime monitor while in enabled or disenabled commanded state.

b. Entry into local communications.

c. Expiration of the disenable commanded time during the disenable commanded state.

d. Expiration of the launch inhibited time during the launch inhibited mode.

e. Entry into standby no-go mode of no-go processing.

f. Entry into the initial and restart alignment subfunction of alignment.

2-7.4.1. Entry Into the Disenabled State. Entry into the disenabled state shall:

a. Cause issuance of resets codes 15-1 through 15-7, and CSD(M) reset command set and, after a delay of 0.5 to 5.0 seconds, cause issuance of CSD(M) reset command reset.

b. Set disenabled state in the OSR, and initiate CSD(M) home monitoring.

c. Cause SCS test inhibit indicator to be set false when the CSD(M) computer home monitor and CSD(M) home indicate home.

d. Suspend CSD(M) home monitoring during an arming or test penetration attempt and during the CSD(M) code change mode.

e. Perform the inhibit test by causing inhibit test to be set in the OSR response for 5.05 ± 0.05 minutes if an INC is received via remote communications, which contains INC secure code 1 and 2 identical to the prestored secure code 1 and 2. If the INC contains secure code 1 and 2 which are not identical to the prestored secure code 1 and 2, set improper command in the OSR for 5.05 ± 0.05 minutes. Terminate the inhibit test upon occurrence of any of the following conditions:

(1) Entry into local communications.

(2) Entry into initial and restart alignment subfunction of alignment.

(3) Entry into the standby-no-go mode, no-go processing.

(4) Performance of an enable test.

(5) Acceptance of an ENC via remote communications, and successful arming of the CSD(M).

(6) Exit from CSD(M) code change mode.

(7) The occurrence of a CSD(M) off home indication during CSD(M) home check.

f. Terminate the Disenabled State. Terminate the disenabled state upon receipt of an ENC via remote communication, and subsequent successful arming of the CSD(M).

2-7.5. Disenable Commanded State. Disenabled commanded state shall be entered and terminated as follows:

a. During the enabled state, when an INC is received via remote communications which contains INC secure code 1 and 2 identical to the prestored secure code 1 and 2, disenabled commanded state shall be entered and shall:

(1) Set disenable commanded state in the OSR.

(2) Set the disenable commanded time to 5.05 $\pm$ 0.05 minutes.

(3) Monitor CSD(M) armed prime monitor at least once each 5 seconds. If the input is true, CSD(M) control failure is set in the MOSR within 5 seconds of terminating the disenable commanded state.

b. Terminate the disenable commanded state upon occurrence of any of the following conditions:

(1) Expiration of the disenable commanded time (initiate disenabled state processing).

(2) Receipt of an ELC from remote communications, which satisfies the checks specified in enabled state processing.

(3) Entry into local communications (initiate disenabled state processing).

(4) Entry into standby no-go mode of no-go processing (initiate disenabled state processing).

(5) Entry into the restart section of alignment (initiate disenabled state processing).

(6) Detection of a true state on CSD(M) armed prime monitor (initiate disenabled state processing).

2-7.6. Command Signal Decoder (M) Penetration Sequence. See Figure 2-9.

a. When an ENC is accepted by remote communications, while a repeated CSD(M) penetration is in process or a CSD(M) reset is in process and a repeated CSD(M) penetration is required, the CSD(M) secure code shall be saved for subsequent use in the next repeated CSD(M) penetration sequence.

b. When an ENC is accepted by remote communications, while the CSD(M) Computer home monitor is true and a CSD(M) reset is not in process, this function shall:

(1) Issue character outputs in order to arm the CSD(M). The character outputs shall be successively determined by each bit in the CSD(M) secure code. A “1" bit in the CSD(M) secure code shall result in a CSD(M) mark character output code to be issued twice with 6.5 to 15 msec between issuances. A “0” bit in the CSD(M) secure code shall result in a CSD(M) space character output code to be issued twice with 6.5 to 15 msec between issuances. After a delay of 58 to 100 msec from issuing the second CSD(M) mark or CSD(M) space character output code, the CSD(M) mark or CSD(M) space shall be reset by issuing resets codes 15-1 through 15-7.

Note: There shall be a delay of 58 to 100 msec after the issuance of the resets specified above before the issuance of the next CSD(M) mark or CSD(M) space. The order of penetration via the CSD(M) secure code is from MSB to LSB.

(2) CSD(M) drive enable shall be monitored at least once during the code transfer. CSD(M) drive enable failure shall be set in the MOSR if CSD(M) drive enable is false.

(3) Upon completion of the code transfer, and at least 100 msec after issuing the reset for the last CSD(M) mark or space above, monitoring of the CSD(M) armed prime monitor shall be initiated. If the CSD(M) armed prime monitor is in the true state and a circumvention reset occurred during the code transfer, the CSD(M) shall be reset. The CSD(M) penetration sequence shall then be repeated one time starting with step 1., above, after the CSD(M) computer home monitor is true and: the CSD(M) home monitor is true. If the CSD(M) armed prime monitor is in the true state and a circumvention reset did not occur during the code transfer, the CSD(M) shall be reset and improper command status shall be reported in the OSR for 5.05 (±0.05) minutes.

(4) If the CSD(M) armed prime monitor is in the false state, set the IPD bit reported in an OSR.

(5) Upon completion of the CSD(M) penetration sequence, the CSD(M) secure code shall be erased from memory.

2-7.7. <u>Command Signal Decoder (M) Reset Sequence</u>. When it is required to reset the CSD(M), the following sequence shall be performed:

a. Issue the CSD(M) reset command set character output code.

b. Delay 0.5 to 5.0 seconds after item a. above and then issue the CSD(M) Reset command reset character output code. If entry to local communications, the standby no-go mode, or commanded restart occurs subsequent to item a. above, the 0.5 to 5.0 second delay shall be 0.5 to 7.5 seconds.

2-8. LAUNCH MODES. See Figure 2-7. When the system is operating in the remote communications mode, launch modes function performs the operations necessary to transition to the appropriate launch mode and maintain system operations in the appropriate launch mode. The various modes and their functions are:

a. The No Launch Mode subfunction is the normal mode of operation when a launch has not been initiated. It is the time period when no acceptable ELC has been received or is in effect. During local communications, the no launch mode is maintained.

b. The Launch Commanded Mode subfunction provides the logic necessary to allow a one vote launch. It is also a transitionary mode between the no launch mode and the launch in process mode on a two vote launch.

c. The Launch Inhibited Mode subfunction is a transitory mode and provides for transition between the launch commanded mode and the no launch mode. Further, it provides a specific time period during which an ELC may be accepted thus allowing transition to the launch in process mode.

d. The Launch In Process Mode subfunction is the primary mode of operation for a launch. It provides the logic necessary to allow a two-vote launch after a commanded time delay.

2-8.1. <u>No Launch Mode</u>. This function shall initiate, maintain, and terminate the no launch mode per the following:

a. When any one of the following conditions occurs, the no launch mode shall be initiated as specified below:

(1) Detection of a true state on CSD(M) armed prime monitor.

(2) Entry into the disenabled state.

(3) Expiration of the launch inhibited mode timer during the launch inhibited mode.

(4) Entry into the standby no-go mode.

(5) Entry into restart alignment initialization.

(6) Entry into initial alignment.

(7) Detection of a high altitude fuzing error.

(8) Detection of the local state.

b. After initiating the no launch mode, this function shall perform the following:

(1) Set no launch in the system status.

(2) Validate ELC(s) received via remote communications by performing the following processing and checks in the order specified (step (d) may be performed at any point before step (e)). This function shall discontinue validation of any ELC which fails to pass any of those checks, including any P-plug penetrations.

(a) Verify that the delta-t time is finite.

(b) Reset ELCNJKSAT and set ELC_LCP = 0 for telemetry.

(c) Verify that the LCP Identifier in the ELC is one of those shown in Table 2-1.

(d) Form the index, j, as follows:

$$j = LCP\_IDENT$$

(e) Form: $ELC\_N2(j) = ELC\_Z2 \oplus PPLUG\_2 \oplus RCODE\_2(j)$

(f) Verify that $ELC\_N2(j) + LCP\_K(j) - ELC\_K\_S = 0$. If the check passes, set ELCNJKSAT for telemetry.

Note: The value for ELC_K_S shall not be explicitly stored in memory. (The storing of its two's complement would meet this requirement.)

(g) Form: $ELC\_N1(j) = ELC\_Z1 \oplus PPLUG\_1 \oplus RCODE\_1(j)$

(h) Verify that $ELC\_N2(j) = ELC\_N1(j)$

(i) If any one of the checks in (c) through (h) above fails, set improper command status in the OSR for 5.05 ± 0.05 minutes.

(j) If all of the above checks pass, set ELC_LCP = j for telemetry and initiate the launch commanded mode.

Table 2-1. LCP Identifier

LCP IDENTIFIER	TRANSFER BITS		
	27	28	29
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1

c. Terminate the no launch mode upon the occurrence of any of the conditions specified below:

(1) Receipt of an ELC via remote communications, which passes all of the checks. Upon terminating the no launch mode, launch commanded mode processing shall be initiated.

(2) Entry into the critical no-go mode. All launch modes processing shall be terminated.

2-8.2. Launch Commanded Mode. This function shall initiate, maintain and terminate the launch commanded mode per the following:

a. When an ELC is received via remote communications, which satisfies the checks, this function shall initiate the launch commanded mode as specified below:

(1) Set launch commanded in the system status.

(2) Initialize the launch commanded mode timer and the launch commanded mode validation variable (LCMVV) as defined below. The launch commanded mode timer shall be rounded to the nearest 3.6 second increment.

(a) If LCF address time expired is not set in the MOSR (has not expired) and ALCC access is not allowed, the following shall be performed:

(1) The launch commanded mode timer shall be initialized with the one-vote launch time, the delta-t time from the last accepted PLC and the one-vote launch fixed time constant. In addition, the launch timer limit shall be initialized.

L_COM_TMR = KT + DELTA_T + LCTFIX_TYM
LTIM_LMT = LCTFIX_TYM

(2) The launch commanded mode validation variable (LCMVV) shall be initialized with the one-vote launch time modifier #2 (KA2).

(b) If LCF address time expired is set in the MOSR (has expired) or ALCC access is allowed, perform the following:

(1) If the delta-t time from the last accepted Preparatory Launch Command (PLC) is less than the minimum TCD time (see note), then the launch commanded mode timer shall be initialized with the one-vote launch time:

L_COM_TMR = KT

(2) If the delta-t time from the last accepted PLC is greater than or equal to the minimum TCD time (see note), the launch commanded mode timer shall be initialized as shown below:

L_COM_TMR = KT + DELTA_T - TCD_TYM

(3) The launch time limit shall be initialized.

LTIM_LMT = KT

(4) The launch commanded mode validation variable (LCMVV) shall be initialized with the one-vote launch time modifier #1 (KA).

Note: The minimum TCD time excludes the occurrence of one or more NEP events, multiple ground ordnance interlock decoder arming attempts and multiple CSD(G) penetrations.

b. After initiating the launch commanded mode, perform the following:

(1) Decrement the launch commanded mode timer by one every 180 msec until it expires upon initializing the timer.

(2) If all of the conditions noted below are satisfied, the total error in time of launch control contributed by this function shall not exceed ±6.0 seconds:

(a) The delta-t time is greater than the minimum TCD time plus the PIGA leveling control time.

(b) None of the following occurs during TCD:

(1) NEP events.

(2) Multiple ground ordnance interlock decoder arming attempts.

(3) Multiple CSD(G) arming attempts.

(c) The launch commanded mode timer was not initialized to (KT + DELTA_T + LCTFIX_TYM).

(3) The launch commanded mode validation variable shall be updated once every 3.6 seconds, as specified below, until the launch commanded mode timer expires. The updating process shall begin when the launch commanded mode timer becomes equal to or less than the launch time limit.

c. When the system is in strategic alert PIGA leveling mode and a GCA case reversal is not in process, the PIGA leveling control cycle shall be initiated 12 ± 1 seconds prior to the expected runout of the launch commanded mode timer or within 2 seconds if the 12 ± 1 seconds are not available.

d. If the launch commanded mode timer expires while in the launch commanded mode and all conditions for entry into terminal countdown have been satisfied, perform the following:

(1) Form the CSD(G) penetration code (K_DAM) as follows:

(a) Set j = LCP_IDENT (the LCP identifier of the ELC that caused the system to enter the launch commanded mode).

(b) KWP = ELC_N1(j) + LCP_K(j) – LCMVV

(c) K_DAM = (ELC_N1(j) + LCP_K(j) - LCMVV) $\oplus$ K_C

e. Validate ELC(s) received via remote communications by performing the following processing and checks in the order specified (step 4. may be performed at any point before 5.). This function shall discontinue validation

of any ELC which fails to pass any of those checks, including any P-Plug penetrations.

(1) Reset ELCNJKSAT and set ELC_LCP = 0 for telemetry.

(2) Verify that the LCP identifier is one of those shown in Table 2-1.

(3) Verify that the LCP identifier in the ELC received is different from the LCP identifier of the ELC that caused the system to enter the launch commanded mode.

(4) Perform the processing of 2-8.1.b.2(d) through 2-8.1.b.2(i) above.

(5) If all of the above checks pass, set ELC_LCP = j for telemetry and initiate the launch-in-process mode.

f. Validate INC(s) received via remote communications by performing the following processing and checks. If the checks are successful, terminate the launch commanded mode.

(1) Verify that inhibit command secure code 1 is identical to the prestored secure code 1.

(2) Verify that inhibit command secure code 2 is identical to the prestored secure code 2.

(3) If either of the above checks fail, set improper command status in the OSR for 5.05 ± 0.05 minutes.

(4) If both of the above checks pass, the launch inhibited mode shall be initiated.

g. Terminate the launch commanded mode upon occurrence of any of the following conditions:

(1) Detection of the Local State. Upon termination of the launch commanded mode, initiate no launch mode processing.

(2) Detection of a True State on CSD(M) Armed Prime Monitor. Upon termination of the launch commanded mode, initiate no launch mode processing.

(3) Entry into Initial or Restart Alignment Initialization. Upon termination of the launch commanded mode, initiate no launch mode processing.

(4) Entry into the standby no-go mode. Upon termination of the launch commanded mode, initiate no launch mode processing.

(5) Entry into the critical no-go mode. All launch modes processing shall be terminated.

(6) Detection of a High Altitude Fuzing error. Upon termination of the launch commanded mode, initiate no launch mode processing.

(7) Expiration of the Launch Commanded Timer and the Existence of the Strategic Alert Biasing Mode. Upon termination of the launch commanded mode, initiate terminal countdown processing. If the launch commanded timer expires before strategic alert biasing mode is entered and no high level seismic or NEP event occurrence has been detected, terminal countdown processing shall be entered as soon as the strategic alert biasing mode is achieved.

(8) Expiration of the Launch Commanded Timer and the Existence of Strategic Alert PIGA Leveling Mode and Completion of the PIGA Leveling Control Cycle. Upon termination of the launch commanded mode, initiate terminal countdown processing. If the launch commanded timer expires prior to entry into strategic alert and a high level seismic or NEP event occurrence has been detected, terminal countdown processing shall be entered as soon as the strategic alert PIGA leveling mode is achieved.

(9) Receipt of an Inhibit command that satisfies the checks above. Upon termination of the launch commanded mode, initiate launch inhibited mode processing.

(10) Receipt of an ELC that satisfies the checks above. Upon termination of the launch commanded mode, initiate launch-in-process mode processing.

2-8.3. Launch Inhibited Mode. This function shall initiate, maintain, and terminate the launch inhibited mode per the following (see Figure 2-13):

a. When an Inhibit Command (INC) is received via remote communications which satisfies the checks, this function shall initiate the launch inhibited mode as specified below:

(1) Set launch inhibited in the system status.

(2) Initialize the launch inhibited mode timer to 5.05 ±0.05 minutes.

b. After initiating the launch inhibited mode, this function shall perform the following:

(1) Decrement the launch inhibited mode timer.

(2) Validate new ELC(s).

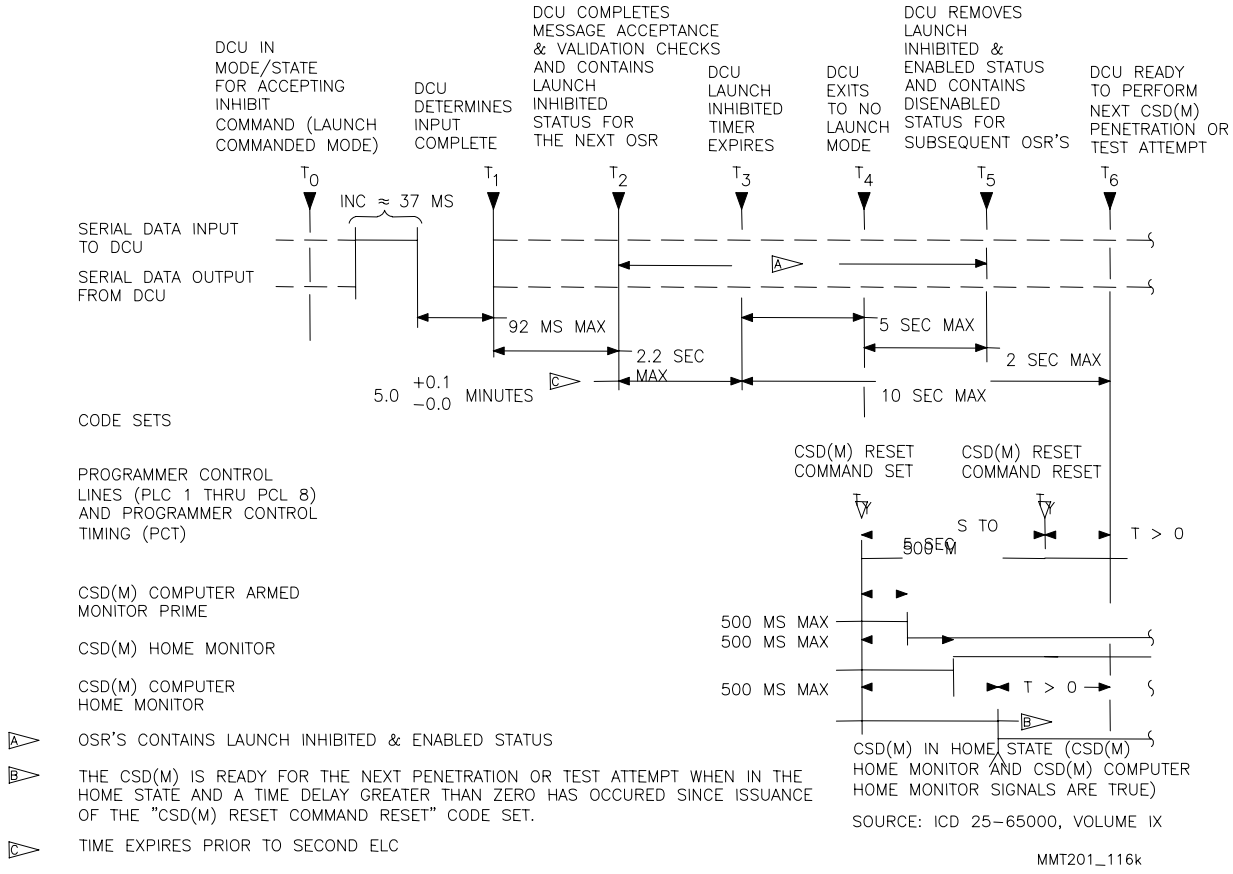


Figure 2-13. Inhibit Launch Sequence Timing Diagram

c. Terminate the launch inhibited mode upon the occurrence of any of the conditions specified below:

(1) Expiration of the Launch Inhibited Mode Timer. Upon termination of the launch inhibited mode, initiate no launch mode processing.

(2) Detection of a local state in Local or Remote Status Indicator. Upon termination of the Launch Inhibited Mode, Initiate No Launch Mode processing.

(3) Detection of a true state on CSD(M) Armed Prime Monitor. Upon termination of the Launch Inhibited Mode, initiate No Launch Mode processing.

(4) Entry into Initial or Restart Alignment Initialization. Upon termination of the Launch Inhibited Mode, Initiate No Launch Mode processing.

(5) Entry into the Standby No-Go Mode of No-Go Processing. Upon termination of the Launch Inhibited Mode, Initiate No Launch Mode processing.

(6) Entry into the Critical No-Go Mode of No-Go Processing. All Launch Modes processing shall be terminated.

(7) Detection of a High Altitude Fuzing Error. Upon termination of the Launch Inhibited Mode, initiate No Launch Mode processing.

(8) Receipt of an ELC that satisfies the checks of a valid ELC. Upon termination of the Launch Inhibited Mode, initiate Launch-in-Process Mode processing.

2.8.4. Launch-in-Process Mode. This function shall initiate, maintain, and terminate the launch-in-process mode per the following:

a. When an ELC is received via remote communications which satisfies the checks, this function shall initiate the launch-in-process mode as specified below:

(1) Set launch-in-process in the system status.

(2) Terminate launch commanded mode timer and launch commanded mode validation variable operations if they are in process.

(3) Initialize the launch-in-process timer as follows:

(a) If the Delta-t time from the last accepted PLC is less than the minimum TCD time (see note), the launch-in-process mode timer shall be set to zero.

(b) If the delta-t time from the last accepted PLC is greater than or equal to the minimum TCD time (see note), the launch-in-process mode timer shall be initialized as shown below:

L_LIPM_TMR = DELTA_T - TCD_TYM

Note: The minimum TCD time excludes the occurrence of one or more NEP events (NEPDETIND), multiple ground ordnance interlock decoder arming attempts and multiple CSD(G) penetrations.

b. After initiating the launch-in-process mode, this function shall perform the following:

(1) Decrement the launch-in-process mode timer by one every 180 msec.

(2) The total error in the time of launch control contributed by the G&C system, exclusive of flight, shall not exceed ± 0.5 seconds provided:

(a) The delta-t time is greater than the TCD time plus the PIGA leveling control cycle time plus 2 seconds.

(b) A NEP event(s) does not occur during the launch-in-process mode timer countdown.

(c) None of the following occurs during TCD:

(1) NEP events.

(2) Multiple ground ordnance interlock decoder arming attempts.

(3) Multiple CSD(G) arming attempts.

c. When the system is in the strategic alert PIGA leveling mode and a GCA case reversal is not in process, the PIGA leveling control cycle shall be initiated 12 ±1 seconds prior to the expected runout of the launch-in-process mode timer or within 2 seconds if the 12 ±1 seconds are not available.

d. If the launch-in-process mode timer expires while in the launch-in-process mode and all conditions for entry into terminal countdown have been satisfied, perform the following:

(1) Form the CSD(G) penetration code as follows:

(a) Set j = LCP_IDENT (the LCP identifier of the ELC that caused the system to enter the launch commanded mode).

(b) Set k = LCP_IDENT (the LCP identifier of the ELC that caused the system to enter the launch-in-process mode).

(c) Set m = |j - k|

(d) KWP = |ELC_N1(j) - ELC_N1(k)| ± K_M(m)

(e) K_DAM = (|ELC_N1(j) - ELC_N1(k)| ± K_M(m)) $\oplus$ K_C

e. Terminate the launch-in-process mode upon occurrence of any of the conditions specified below:

(1) Detection of the Local State. Upon termination of the launch-in-process mode, initiate no launch mode processing.

(2) Detection of a True State on CSD(M) Armed Prime Monitor. Upon termination of the launch-in-process mode, initiate no launch mode processing.

(3) Entry into Initial or Restart Alignment Initialization. Upon termination of the launch-in-process mode, initiate no launch mode processing.

(4) Entry into the Standby No-Go Mode. Upon termination of the launch-in-process mode, initiate no launch mode processing.

(5) Entry into the Critical No-Go Mode. All launch modes processing shall be terminated.

(6) Detection of a High Altitude Fuzing Error. Upon termination of the launch-in-process mode, initiate no launch mode processing.

(7) Expiration of the Launch-in-Process Timer and the Existence of the Strategic Alert Biasing Mode. Upon termination of the launch-in-process mode, initiate terminal countdown processing. If the launch-in-process timer expires before strategic alert biasing mode is entered and no high level seismic or NEP event occurrence has been detected, terminal countdown processing shall be entered within 0.18 seconds after the strategic alert biasing mode is achieved.

(8) Expiration of the Launch-in-Process Timer and the Existence of Strategic Alert PIGA Leveling Mode and Completion of the PIGA Leveling Control Cycle. Upon termination of the launch-in-process mode, initiate terminal countdown processing. If the launch-in-process timer expires prior to entry into strategic alert and high level seismic or NEP event occurrence has been detected, terminal countdown processing shall be entered within 0.18 seconds after the strategic alert PIGA leveling mode and control cycle is achieved.

2.8.5. P-Plug Sampling Sequence. To process an ELC, this function shall sample the P-Plug in accordance with the requirements and sequence specified below:

a. PPLUG discrete output #2 shall be issued.

b. The 24-bit P-plug Code 2 word shall be formed in the least significant bit positions of two DCU registers by combining the P-Plug data bits from P-Plug discrete input word register #1 and #2. The most significant eight bits shall be zero.

c. PPLUG discrete output #2 shall be reset.

d. The P-Plug Code 2 word shall remain in memory just long enough to form ELC_N2(j).

e. PPLUG discrete output #1 shall be issued.

f. The 24-bit P-Plug Code 1 word shall be formed in the least significant bit positions of two DCU registers by combining the P-Plug data bits from P-Plug discrete input word register #1 and #2. The most significant eight bits shall be zero.

g. PPLUG discrete output #1 shall be reset.

h. The P-Plug Code 1 word shall remain in memory just long enough to form ELC_N1(j).

2-9. TERMINAL COUNTDOWN. Terminal Countdown (TCD) performs the operations necessary to sequence the program through an orderly progression of events which will result in a successful launch.

a. The following functions are part of the OGP:

(1) Initialization.

(2) Calculate and Store Operations.

(3) SCS Arming Operations.

(4) CSD(G) Arming Operations.

(5) Ground Ordnance Interlock Decoder Arming Operations.

(6) Ground Ordnance Power-On Determination.

(7) TCD Validity Test.

(8) Transfer to the Flight Program.

b. The following functions are part of the OFP:

(1) Flight Control (F/C) Ground Power Application.

(2) Missile Battery Activation.

(3) Suspension System Activation.

(4) Removal of F/C and G&C Ground Power.

(5) Battery Ignition Test.

(6) Arming of Missile Ordnance Devices.

(7) Launcher Closure Removal.

(8) Critical Leads Disconnect.

(9) G&C Umbilical Release.

(10) First Stage Ignition.

2-9.1. Processing. Terminal countdown shall be initiated upon the occurrence of any of the conditions specified below:

a. Expiration of the launch commanded mode timer and the existence of the strategic alert biasing mode or entry into the strategic alert biasing mode after expiration of the launch commanded mode timer while in the launch commanded mode.

b. Expiration of the launch commanded mode timer and the existence of the strategic alert PIGA leveling mode and the completion of a PIGA leveling control cycle while in the launch commanded mode.

c. If the launch commanded mode timer expires during a non-strategic alert mode during which conditions occurred which require exit to the strategic alert PIGA leveling mode, then this function shall be initiated upon existence of the strategic alert PIGA leveling mode while in the launch commanded mode.

d. Expiration of the launch-in-process mode timer and the existence of the strategic alert biasing mode or entry into the strategic alert biasing mode after expiration of the launch-in-process mode timer while in the launch-in-process mode.

e. Expiration of the Launch-in-process mode timer and the existence of the strategic alert PIGA leveling mode and the completion of a PIGA leveling control cycle while in the launch-in-process mode.

f. If the launch-in-process mode timer runs out during a non-strategic alert mode during which conditions occurred which require exit to the strategic alert PIGA leveling mode, then this function shall be initiated upon existence of the strategic alert PIGA leveling mode while in the launch-in-process mode.

2-9.2. Initialization. The following operations shall be performed during terminal countdown initialization:

a. Update the OFP G6B4 gyro biases with the filtered G6B4 gyro biases.

b. Update the OFP gyrocompass bias.

c. The auxiliary status enable set character output code shall be issued at least twice within 290 msec of the start of the receipt of an interrogation to which no response will be made due to entering TCD. However, any reply being sent upon entry to TCD shall be completed. Remote communications shall then be terminated.

d. Issue a keep alive character output code at least twice every 1.4 seconds. The last issuance shall be within 40 msec of entry to the OFP.

e. Set the GCA slew controls word to stable.

f. Issue the resets codes 9-1 through 9-7 character output code at least twice.

g. Issue the critical status override set character output code at least twice prior to transferring the arming code to the CSD(G).

h. The stable platform shall be placed in the free inertial mode.

I. The gyrocompass shall be placed in the free inertial mode.

2-9.3. Sequence of Events. TCD shall perform the OGP portion of Figures 2-14, (Terminal Countdown Timing), Figure 2-43, (Terminal Countdown) and the following (also reference Table 2-2):

a. Perform the following computations/operations and store the resulting data for the OFP:

(1) Calculate target independent PIGA bias component PHIINVMAT.

(2) Calculate the Q'-Matrix.

(3) Compute the platform azimuth limit correction angle PHI_EPSLN.

(4) Calculate the computed target misalignment angle.

(5) Calculate the platform azimuth angle.

(6) Calculate the PIGA biases.

(7) Obtain the ratio of computer time to external precision time, subtract one from it and save the result.

(8) Reformat and save the current target number.

(9) Obtain launch point gravity and save it.

(10) Obtain the sine of astronomic latitude and save it.

(11) Obtain the warhead prearm code key and save it.

b. The following shall be performed:

(1) The CSD(G) reset command reset character output code shall be issued at least twice at least 400 msec before beginning the first CSD(G) penetration sequence. The SCS safe reset character output code shall be issued at least twice prior to arming the SCS. Critical circuits enable shall be set prior to and during SCS arming. The SCS arm set character output code shall be issued at least once every CIRTI interval prior to the CSD(G) penetration sequence for a period of at least 500 msec after the issuance of the second SCS arm set character output code, then issue the SCS arm reset character output code at least twice.

(2) The CSD(G) shall be penetrated as specified below (see Figure 2-15):

(a) Character output codes shall be issued in order to arm the CSD(G). The character outputs shall be successively determined by each bit in the most significant 20 bits of the 24-bit CSD(G) penetration code. A “1” bit in the penetration code shall result in the issuance of a CSD(G) mark. A ”0” bit in the penetration code shall result in the issuance of a CSD(G) space. The CSD(G) mark and space character output codes shall be issued at least once every CIRTI interval for 100 to 200 msec. Then the CSD(G) mark or space shall be reset by issuing the reset codes 15-9 through 15-15 character

output code at least once every CIRTI interval for a period of 100 to 200 msec prior to issuing the next CSD(G) mark or space. The maximum arming code bit rate shall be 5 bits per second and shall not be faster than the bit rate used during the CSD(G) sub-test. Critical circuits enable shall be set prior to and remain set during the issuance of any CSD(G) mark or space character output code. The order of penetration via the CSD(G) penetration code shall be from MSB to LSB.

(b) The CSD(G) 19th-bit monitor shall be sampled for a true indication at least 200 msec after the leading edge of the 20th CSD(G) output bit. If the monitor is true, TCD shall continue at step 3. below. If the monitor is not true following the first penetration attempt, the CSD(G) shall be reset as specified in item (c) below, and the penetration sequence shall be repeated one time, after which TCD shall be allowed to continue at step 3. below.

(c) To reset the CSD(G), the CSD(G) reset command set character output code shall be issued at least 2 seconds prior to beginning a repeated CSD(G) penetration sequence. CSD(G) reset command set shall then be issued once every CIRTI interval for a period of 96 to 200 msec. The CSD(G) reset command reset character output code shall then be issued at least twice.

(3) After all CSD(G) penetration attempts have been completed, the ground ordnance interlock decoder shall be armed per the following sequence:

(a) Reset critical circuits enable and issue resets codes 15-9 through 15-15 character output code at least twice after the last issuance of the ground ordnance interlock 2 set and ground ordnance interlock clear (test 1) character output codes.

(b) Issue ground ordnance interlock 1 set at least twice.

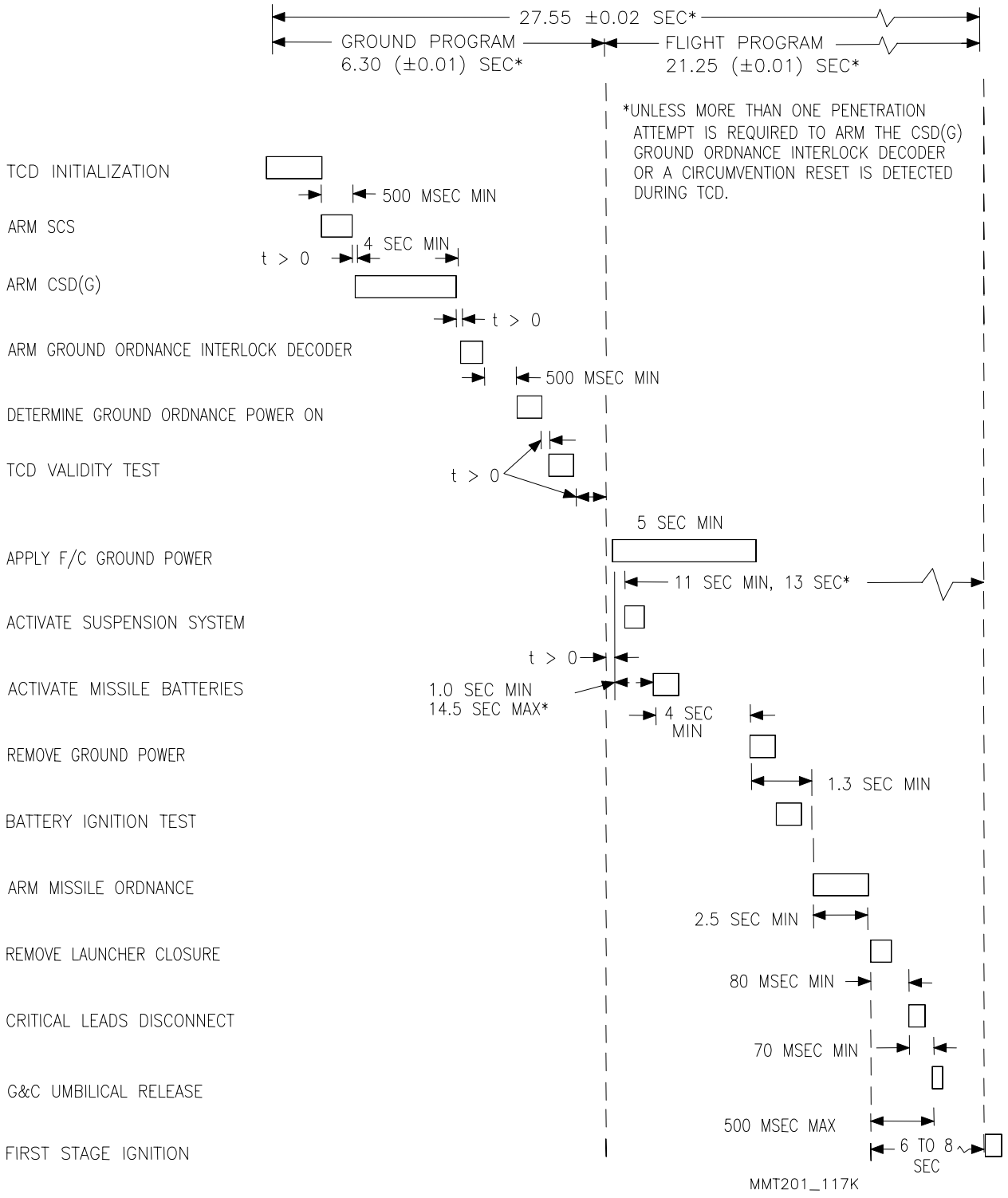
(c) Issue ground ordnance interlock 2 set at least twice after a minimum delay of 300 **µ**sec after issuing ground ordnance interlock 1 set in step (b) above.

(d) Set critical circuits enable true for at least 100 **µ**sec at least 50 **µ**sec after step (c) above and for the first arming attempt less than 400 msec after issuing the reset codes 15-9 through 15-15 character output code for the last output bit in the preceding CSD(G) penetration sequence.

(4) The ground ordnance power-on monitor shall be sampled at least 500 msec after the attempt to arm the ground ordnance interlock decoder. If the monitor is true, TCD shall be allowed to continue at step d. below. If the monitor is not true following the first arming attempt, the arming sequence of step 3. above shall be repeated one time after which TCD shall be allowed to continue at step d. below.

c. After all ground ordnance interlock decoder arming attempts and sampling of the ground ordnance power-on monitor are completed, a validity test shall be made to ensure that TCD was not entered erroneously. This shall be accomplished by verifying that the 24-bit constant (KWP) generated for use during OFP warhead prearm operations is correct. The expected correct constants shall not be stored in enable write protected memory (see note). If the check fails, TCD shall be terminated. If the check passes, transition shall be made to the OFP. If KWP is saved in a temporary memory location, it shall not remain in memory following successful completion of the above check.

Note: Storing the correct constant's two's complement would meet this requirement.



SOURCE: S-133-19251

Figure 2-14. Terminal Countdown Timing

Table 2-2. TCD Timing Sequence

TIME (SEC)	EVENT
0	TCD ENTRY INITIALIZATION
.56	COUPLER TEST RESET
.58	ARM SCS
.58	AUXILIARY STATUS ENABLE
.59	CRITICAL STATUS OVERRIDE
1.19	CSD(G) PENETRATION (FIRST MARK)
5.29	CSD(G) 19TH BIT MONITOR
5.60	ARM GROUND ORDNANCE INTERLOCK DECODER
5.60	GROUND ORDNANCE POWER ON
5.62	ARM LES
6.27	TCD VALIDITY TEST
6.3	FLIGHT PROGRAM ENTER
6.33	F/C AND NCU POWER ON
6.86	F/C ELECTRONICS POWER ON
7.35	BATTERY ACTIVATE
14.8	ACTIVATE SUSPENSION SYSTEM
14.91	REMOVE G&C GROUND POWER AND RESET F/C GROUND POWER
15.9	BATTERY TEST (FIRST STAGE NOZZLES - +6V AND -6V TEST)
16.44	ARM MISSILE ORDNANCE
19.8	REMOVE LAUNCHER CLOSURE
19.90	ACTIVATE DCU INTERNAL CRITICAL LEADS DISCONNECT
19.97	CRITICAL LEADS DISCONNECT (FROM OGE TO DCU)
19.97	RELEASE MGS UMBILICAL
19.98	RETRACT MGS UMBILICAL
27.55	FIRST STAGE IGNITION

NOTES: [1] INCLUDES APPROXIMATE TIME WITH MAJOR EVENTS LISTED (T=0 AT TCD ENTRY)

[2] TIMELINE ASSUMES NORMAL TCD WITH NO FAILURES, RE-ARM OR RE-PENETRATION ATTEMPTS.

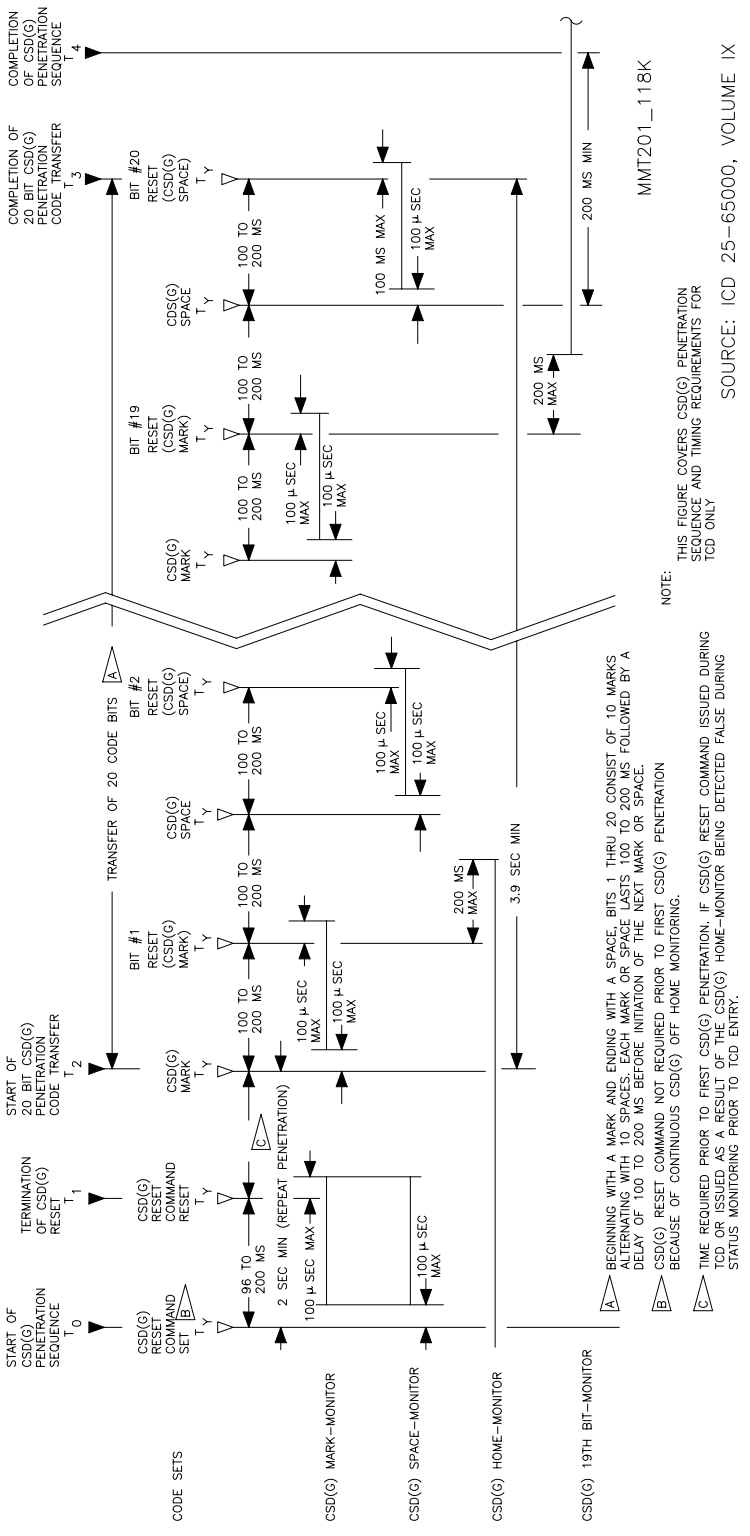


Figure 2-15. CSD(G) Penetration Sequential Timing Diagram

2-9.3.1. Flight Program TCD Sequence of Events. The Operational Flight Program will perform the sequence of events specified below. The TCD sequence of events steps d. through n. are mutually exclusive and occur in the order given.

a. Issue the keep alive character output code at least twice every 1.4 seconds until at least 800 msec after first stage ignition.

b. Monitor for the occurrence of a Circumvention Reset (C/R) by sampling the C/R indicator multiplexer status bit for a true state at least once every 11 msec with sampling beginning within 30 msec after entry to the OFP and lasting at least until G&C Umbilical Release is completed. When C/R is detected, recovery processing will be performed.

c. Issue the reset 9-1 through 9-7 character output code pair at least 70 msec after issuance of the second ground ordnance character output code pair for items e., f., and j. below, but prior to issuing the first character output code pair for the next item. In addition, critical circuits enable will be set prior to issuing any character output code pair specified in items e., f., i., j., and l. and will remain set at least until the reset 9-1 through 9-7 character output code pair is issued.

d. Issue the F/C and NCU ground power on command character output code pair at least one second prior to issuance of the first battery activate character output code pair. Issuance of any required ground ordnance character output code pairs will not occur for at least 1 second after or 40 msec before issuance of the F/C and NCU ground power on command character output code pair.

e. Issue the battery activate character output code pair at least twice with the issuance of the first code pair at least 1 second after issuance of the F/C and NCU ground power on command character output code pair and the issuance of the second code pair no later than 14.5 sec (time may be extended if C/R is detected) after issuance of the F/C and NCU ground power on command character output code pair. Issuance of the reset 9-1 through 9-7 character output code pair, as constrained in c. above, completes this step in the TCD sequence.

f. Issue the activate suspension system character output code pair at least twice with the issuance of both code pairs 11 to 13 sec (time may be extended if C/R is detected) prior to the issuance of the first stage ignition command. Issuance of both activate suspension system character output code pairs will not occur within 50 msec of issuance of any other required ground ordnance activation character output code pair. Issuance of the reset 9-1 through 9-7 character output code pair, as constrained in c. above, completes this step in the TCD sequence.

g. Issue the reset F/C and NCU ground power on command and remove G&C ground power character output code pairs a minimum of 4.0 sec after issuing the second battery activate character output code pair and prior to

performing the battery ignition test. The OFP will zero the stage I nozzle commands prior to issuing the reset F/C and NCU ground power on command character output code pair.

h. Perform the battery ignition test after performing item g. and before issuing any arm missile ordnance character output code pair. The test sequence will be as follows:

(1) Delay a minimum of 500 msec after issuing the reset F/C and NCU ground power on command and remove G&C ground power character output code pairs.

(2) Apply +6 volts of equivalent nozzle motion.

(3) Delay a minimum of 500 msec.

(4) Apply -6 volts of equivalent nozzle motion to the same nozzles as in step (2) above.

(5) Delay a minimum of 420 msec.

(6) Sample the voltage inputs for the same two nozzles as in step (2) above. A voltage of $\geq$ 2.56 volts on either nozzle is a go condition. If the voltage input sample is < 2.56 volts on both nozzles, the remaining portion of the launch sequence will be discontinued. Transition back to the OGP will be made with the Critical no-go identifier set equal to 13_8. The OFP will transfer control to a unique location in the OGP.

(7) Zero the equivalent nozzle motion commands upon completion of a successful battery ignition test.

i. Issue the arm missile ordnance character output code pair at least twice with the issuance of the first code pair at least 1.3 sec after issuance of the reset F/C and NCU ground power on command character output code pair and the issuance of the second code pair at least 2.5 sec prior to issuing any remove launcher closure character output code pair. The reset 9-1 through 9-7 character output code pair will not be issued for at least 2.5 sec after issuance of the second arm missile ordnance character output code pair. Issuance of the reset 9-1 through 9-7 character output code pair, as constrained in c. above, completes this step in the TCD sequence.

j. Issue the remove launcher closure character output code pair at least twice with the issuance of the first code pair at least 2.5 sec after issuance of the second arm missile ordnance character output code pair. In addition, the issuance of both remove launcher closure character output code pairs will occur 6 to 8 sec (time may be extended if C/R is detected) prior to the issuance of the first stage ignition command. Issuance of the reset 9-1

through 9-7 character output code pair, as constrained in c. above, completes this step in the TCD sequence.

k. Activate the DCU internal critical leads disconnect function.

l. Issue the G&C umbilical release character output code pair at least twice with the issuance of the first code pair at least 80 msec after issuance of the second remove launcher closure character output code pair and the issuance of the second code pair no later than 500 msec (time may be extended if C/R is detected) after issuance of the first remove launcher closure character output code pair.

m. Issue the reset 9-1 through 9-7 character output code pair 70 msec to one second (time may be extended if C/R is detected) following issuance of the second G&C umbilical release character output code pair.

n. Issue the first stage ignition command after an appropriate delay which will ensure the following minimum times are satisfied:

(1) A minimum of 11 sec between issuance of the second activate suspension system character output code pair and issuance of the first stage ignition command.

(2) A minimum of 6 sec between issuance of the second remove launcher closure character output code pair and issuance of the first stage ignition command.

2-9.4. Terminal Countdown Termination. Terminal countdown shall be terminated upon the occurrence of any of the conditions specified below:

a. Successful completion of the OGP portion of TCD. Flight processing shall then be entered with critical circuits enable on, MGSC servo enable on and MGSC command enable off.

b. Verification that TCD was not entered properly (TCD validity test). No-go processing shall be entered with the critical no-go identifier set to indicate that this error has occurred.

c. Master Reset. No-go processing shall be entered with the critical no-go identifier set to indicate that this error has occurred.

d. Critical no-go entered due to an executive fault.

e. Standby no-go entered due to an absolute PIGA bias failure in TCD.

2-10. MISSILE TEST. The Missile Test Function (See Figure 2-44) performs the launch facility and missile hardware test processes listed below to permit recognition of malfunctions which would prevent a successful launch and flight. A missile test consists of the following:

a. Missile Test Initiating Conditions

b. Command Signal Decoder (Ground) Test

c. Safety Control Switch Arm Test

d. Ground Ordnance Discretes Test

e. Chaff Motor Speed Command Control Test

f. Flight Control Ground Power Turn-on Test, Stage 1 Nozzles Null and Stage 2 Closed Position Control

g. Missile Ordnance Discretes Test

h. Propulsion System Rocket Engine Control Test

I. Downstage Control System Test

j. Flight Control Ground Power Removal

k. Circumvention Reset Detection

l. Circumvention Reset System Test

m. Safety Control Switch Test

n. Nuclear Event Detectors Test

o. DCU Self Test

p. Exit Processing

q. Exit Conditions

2-10.1. Processing. Missile test shall be performed following acceptance of a Missile Test Command (MTC) from local communications or remote communications. The detailed test processes are described in the following paragraphs and shall be performed subject to the conditions specified below:

a. Missile test shall not exceed 38 seconds in duration. The sub-tests which require flight control ground power shall be completed within 18.5 seconds after flight control ground power turn on.

b. Except as specifically otherwise required, the Keep-Alive character output code shall be issued at least twice every 1.4 seconds during missile test.

2-10.2. Missile Test Initiating Conditions. Missile test shall be initiated by performing the following:

a. Local communications and remote communications shall be terminated.

b. If CSD(M) reset is in process, missile test shall ensure that the CSD(M) reset signal does not remain true set longer than 5 seconds by issuing CSD(M) reset command reset character output code, and shall ensure that the CSD(M) reset signal remain true set for at least 0.5 sec if missile test was entered with this signal true set.

c. The auxiliary status enable set character output code shall be issued within 290 msec of the start of receipt of an interrogation to which a response is not made and shall be issued at least once every 15 seconds.

d. A missile test indication shall be issued at least once by sending data readout initiate followed by data readout 7 character output codes.

e. Set Excitation Voltage Scale Factor = 1.0.

f. The stable platform shall be placed in the free inertial mode by performing the processing specified in Initialization - Free Inertial and Free Inertial.

g. The gyrocompass shall be placed in the free inertial mode by bypassing the processing of Gyrocompass Gyro Torquing and Biasing.

2-10.3. Command Signal Decoder (Ground) Test. Whenever an encrypted missile test command is accepted via remote communications, this test shall verify that the command signal decoder (ground) can be stepped to the 19th bit position utilizing the CSD(G) test code. The test processes shall be as follows:

a. Critical circuits enable shall be set to begin this test.

b. The CSD(G) shall be stepped to the 19th bit position by issuing character output codes that correspond to the one and zero bits of the CSD(G) test code as follows:

(1) If a one bit exists in the CSD(G) test code, a CSD(G) mark shall be issued.

(2) If a zero bit exists in the CSD(G) Test Code, a CSD(G) Space shall be issued.

(3) The CSD(G) mark and CSD(G) space character output codes shall be issued at least once every 10 msec for 100 to 200 msec.

(4) Then, the CSD(G) mark and CSD(G) space shall be reset by issuing the reset codes 15-9 through 15-15 character output code. Subsequently, a delay of 100 to 200 msec shall be allowed before issuing the next CSD(G) mark or CSD(G) space.

(5) The stepping rate shall be 5 bits per second, maximum, and it shall not be less than the rate utilized in terminal countdown.

c. Upon executing the reset codes for the 19th bit, delay 200 msec minimum and verify the following:

(1) The CSD(G) home is false.

(2) The CSD(G) 19th bit monitor is true.

d. The 20th bit of the CSD(G) test code shall be issued.

e. Delay at least 2 seconds minimum and verify the following:

(1) The CSD(G) home is true.

(2) The CSD(G) 19th bit monitor is false.

f. Failure to verify the status of the CSD(G) in step e. above shall result in another reset attempt as follows:

(1) Issue the CSD(G) reset command set character output code followed by the issuance of the CSD(G) reset command reset character output code within 148 ± 52 msec.

(2) Repeat step e. above following execution of the CSD(G) reset command reset and proceed to step g. below

g. The CSD(G) test results shall be processed as follows:

(1) The Critical no-go section of no-go processing shall be initiated after setting the critical no-go identifier if the CSD(G) 19th bit monitor is true in step f.2 above.

(2) CSD(G) test failure shall be set in the MOSR and missile test discontinued if the results of steps c. or e. above or the CSD(G) home monitor of step f.2 above is incorrectly indicated.

h. The CSD(G) test code shall not remain in memory upon exit of this test. except for exit to critical no-go. Critical circuits enable shall also be reset.

2-10.4. <u>Safety Control Switch Arm Test</u>. The Safety Control Switch (SCS) arm test shall verify that the SCS arm decoder flip-flop in the coupler unit is not in the true state by performing the following functions:

a. Critical circuits enable shall be set for a minimum duration of 500 msec.

b. Obtain the status of the SCS armed monitor and the following action shall result:

(1) Missile test shall be discontinued and Missile Test Exit processing shall be performed if a true state is detected.

(2) Detection of a false state shall permit the conductance of the Ground Ordnance Discretes Test.

(3) Critical Circuits Enable shall be reset.

2-10.5. Ground Ordnance Discretes Test. The ground ordnance discretes test shall verify that all ground ordnance circuits and safety provisions are functioning properly. The following test functions shall be executed upon the successful completion of the safety control switch arm test. The responses to verification failures discussed below are shown in step h.

a. The ground ordnance test enable set character output code shall be issued to begin this test and it shall be reset by issuing the ground ordnance test enable reset character output code when this test is concluded.

b. The ground ordnance interlock decoder shall be set by performing the sequence specified below:

(1) Issue the critical circuits enable false and issue ground ordnance interlock 1 set character output code. This command shall be reset by issuing of ground ordnance interlock 1 reset character output code between the setting and resetting of the ground ordnance interlock decoder.

(2) Delay more than 300 microseconds, and issue ground ordnance interlock 2 set character output code.

(3) Delay more than 50 microseconds, and issue critical circuits enable. Obtain the FOIO Ordnance Enable Register data and verify that the read is the same as the write issued.

c. Delay at least 50 msec following the completion of step b. above and verify that the responses of ground ordnance discretes commands and responses occur when each of the commands is issued. This iterating sequence shall consist of the following:

(1) Issue an ordnance command one at a time as specified below:

(a) For N/A* listed command, a command shall not be issued.

(b) Issue activate suspension system, battery activate, arm missile ordnance devices, remove launcher closure, and G&C umbilical release character output codes.

(c) Issue stage 1 Ignition. Obtain the FOIO ordnance commands register data and verify that the response is correct.

(2) Obtain the ground ordnance discrete responses as follows:

(a) Obtain responses within the time frame defined by ground ordnance discrete timing, except responses for N/A* listed command shall be obtained after a delay of at least 50 msec following completion of step b.

(b) Obtain the UIO discrete input monitors #1.

(3) Upon obtaining the responses, the following shall be performed:

(a) For activate suspension system, battery activate, arm missile ordnance devices, remove launcher closure, and G&C umbilical release, reset the command within 120 msec by issuing reset 9-1 through 9-7 character output code, delay at least 300 microseconds and issue the next command.

(b) Reset stage 1 ignition within 120 msec of its issuance. Obtain the FOIO ordnance commands register data and verify that the response is correct.

d. Verify that Any Ground Ordnance Driver On Monitor is false and the ground ordnance power on monitor is true at least 120 msec following the execution of and during the presence of the G&C umbilical release command.

e. When both steps c. and d. above have been completed and at least 2.5 seconds have elapsed since the completion of step b.3 above, the ground ordnance interlock decoder shall be reset as follows:

(1) Issue the ground ordnance interlock clear character output code.

(2) Delay at least 300 microseconds and issue reset 15-9 through 15-15 character output code.

f. Delay at least 100 msec following the execution of step e.1 above and verify that all ground ordnance monitors are false during the presence of each ordnance command. Upon resetting the last ordnance command, delay at least 50 microseconds and issue the ground ordnance test enable reset character output code and set the critical circuits enable false. Obtain the

FOIO ordnance enable register data and verify that the read is the same as the write issued.

g. Except for incorrect responses of the ordnance command register and the ordnance enable register, any incorrect responses obtained in steps c., d. and f. above and the following actions shall be taken:

(1) The ground ordnance discretes test failure MOSR shall be set.

(2) The ground ordnance alarm set character output code shall be issued prior to the exit of missile test in the absence of a circumvention reset.

h. Any incorrect responses obtained for the ordnance command register in steps c.1.(c) or c.3.(b) above, or the ordnance enable register in steps b.3 or f above, shall set the computer failure MOSR bit as an alarm.

I. The ground ordnance alarm reset character output code shall be issued and the ground ordnance discretes test failure MOSR shall be reset upon successful completion of the test.

2-10.6. Chaff Motor Speed Command Control Test. The Chaff Motor Speed (CMS) command control test shall be performed in the absence of flight control ground power. The CMS command control test shall verify that the CMS control circuitry can respond properly when commanded by the computer by performing chaff motor speed (CMS) command and response.

2-10.6.1. Chaff Motor Speed (CMS) Command and Response. The following shall be performed:

a. Set Chaff Motor Speed (CMS) command to -5 (volts).

b. Issue Flight Control Select/Event Markers commands in test pattern. Obtain the flight control select/event markers and verify correct read back response to test pattern. Set the computer failure MOSR as an alarm for any incorrect responses.

c. Unmask thrust vector control (TVC) initiate interrupt.

d. Perform the processing of chaff motor speed (CMS) command control when TVC initiate interrupt occurs, as long as ADC cycle select is 11_2.

e. Obtain the Stage Auxiliary Monitor 2 at 305 ± 45 msec after performing steps a., b., and c. above, and perform the following:

(1) Set STGAUX2V = STGAUXMON2(bits 0 thru 11) and IDTAGSA2V = STGAUXMON2(bits 12 thru 15).

(2) The processing of analog to digital converter (ADC) output compensation shall be performed.

(3) Set CMSV = {ADCSC (obtained for STGAUX2V)/204.8} (volts).

(4) Verify CMSV = -3.6175 ± .2 volts. Set the computer failure MOSR as an alarm for an incorrect response.

(5) Verify the ID tag is 3. Set the computer failure MOSR as an alarm for an incorrect response.

f. Set chaff motor speed (CMS) command to +5 (volts).

g. Obtain the stage auxiliary monitor 2 at 305 ± 45 msec after performing step f. above, and perform the following:

(1) Set STGAUX2V = STGAUXMON2(bits 0 thru 11) and IDTAGSA2V = STGAUXMON2(bits 12 thru 15).

(2) The processing of ADC output compensation shall be performed.

(3) Set CMSV = {ADCSC (obtained for STGAUX2V)/204.8} (volts).

(4) Verify CMSV = +3.6175 ± .2 volts. Set the computer failure MOSR as an alarm for an incorrect response.

(5) Verify the ID Tag (IDTAGSA2V) is 3. Set the Computer Failure (COMPUTER_F) MOSR as an alarm for an incorrect response.

h. Mask TVC Initiate (TVCININT) interrupt.

2-10.6.2. Chaff Motor Speed (CMS) Command Control. The analog voltage is provided by circuitry in the DCU which averages the Pulse Width Modulated (PWM) signal commanded by Missile Test via the TVC AES Stage 1, Nozzle 1. In order to have the required analog voltage accuracy, the analog Chaff Motor Speed output voltage is read by Missile Test via the Stage Auxiliary Monitor 2. The CMS output voltage is compared to the desired analog voltage, and TVC AES Stage 1, Nozzle 1 is adjusted to drive the CMS output to the desired analog voltage in the required time. The chaff motor speed command control processing is shown in block diagram form in Figure 2-16 and is processed every 2 msec during post boost. The processing utilizes the TVC AES Stage 1, Nozzle 1 register to form a PWM command to the FOIO analog chaff motor speed module. The CMS output from this module is read back from Stage Auxiliary Monitor 2 and is combined with the chaff motor command to close the loop. Since the CMS is sampled once in every 4 (500 microsecond) interrupts and 2 msec filtering is desired, every sample is processed in post boost.

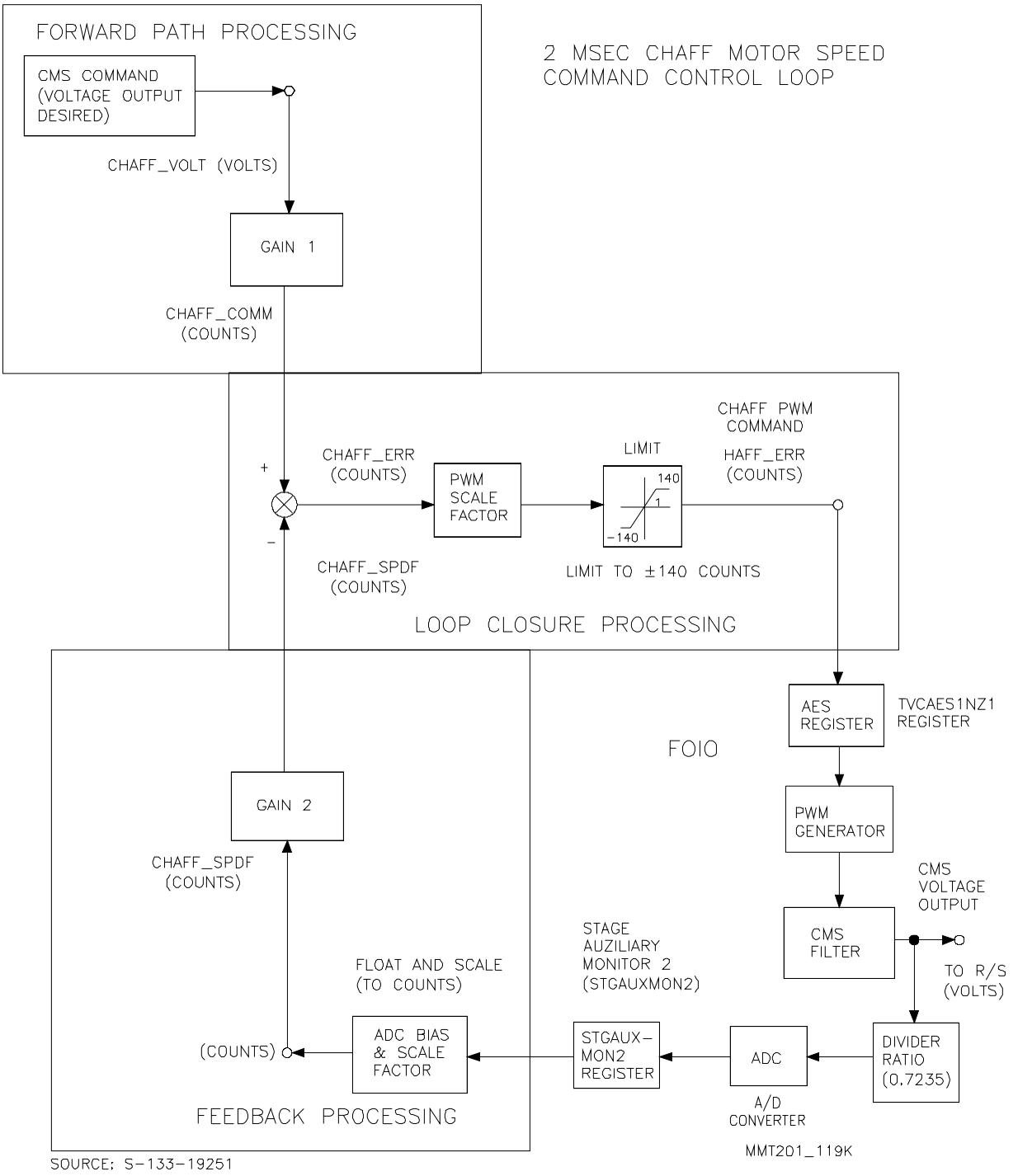


Figure 2-16. Chaff Motor Speed Command Control Loop Processing

2-10.7. Flight Control Ground Power Turn-on Test, Stage 1 Nozzles Null and Stage 2 Injectors Closed Position Control. The flight control ground power turn-on test ensures that Flight Control (F/C) and Nozzle Control Unit (NCU) ground power can be applied to the missile to permit the conductance of flight control power dependent tests which allows the recognition of critical failures pertinent to flight mission success. The stage 1 nozzles are controlled to null (except during the downstage actuator response test for the stage 1 nozzles) and the stage 2 injectors are controlled to the closed position (except during the downstage actuator response test for the stage 2 injectors), for the period during which flight control ground power is applied. The following shall be performed:

a. Flight control ground power turn-on test processing.

b. Stage 1 nozzles null control processing.

c. Stage 2 injectors closed position control processing.

2-10.7.1. Flight Control Ground Power Turn-on Test. The F/C and NCU ground power application sequence shall be as follows:

a. Perform the following:

(1) Issue Thrust Vector Control (TVC) Actuator Error Signal (AES) commands of 0 for all stage 1, stage 2, stage 3, and PBPS, TVC and AES Commands.

(2) Obtain the read back of all stage 1, stage 2, stage 3, and PBPS, TVC and AES commands issued in step a.1. and verify for each command read back is 0.

(3) Set the computer failure MOSR as an alarm for any incorrect responses obtained in step a.2.

(4) The following sequential steps shall be performed:

(a) Set TVC_CMD_4 a minimum of 4 msec before flight control ground power turn on of step b. below, as shown below:

(b) Issue flight control select/event markers command test pattern a minimum of 4 msec before flight control ground power turn on of step b. below. Obtain the flight control select/event markers and verify correct read back response test pattern. Set the computer failure MOSR as an alarm for any incorrect responses.

(c) Unmask (enable) TVC Initiate interrupt a minimum of 2 msec before flight control ground power turn on of step b. below and within 2 msec after performing step (b) above. Keep TVC Initiate interrupt unmasked until a minimum of 300 msec after flight control ground power turn off and then it shall be masked.

(d) Perform the processing of Thrust Vector Control when TVC Initiate interrupt occurs.

(e) The Stage 2 actuator error signal commands shall be set at least one time to minus 28 counts (minus 20% PWM) when the ID Tag of the Position Feedback register is either 0, 1, 2 or 3. (Note: this will occur within one msec after performing step (c) above.)

b. Issue the F/C ground power set character output code in accordance with the conditions specified in Flight Control Ground Power On/Off Cycle.

c. Verify that the Stage 2-3 Hydraulic Power Monitor is in the following state:

(1) True set 175 ± 25 msec following execution of step b. above.

(2) False set 1.5 sec minimum following execution of step b. above.

d. Set the F/C power failure bit in the MOSR as an alarm, if the specific responses of step c. cannot be obtained.

2-10.7.2. Stage 1 Nozzles Null Control. The stage 1 nozzles shall be controlled to null, except during the downstage actuator response test for the stage 1 nozzles, for the period that TVC initiate interrupt is unmasked as specified in flight control power turn-on test above. Stage 1 nozzles control shall depend on which stage is selected by the ADC cycle select. Whenever ADC cycle select does not select stage 1, the stage 1 nozzles shall be controlled to null as specified in stage 1 nozzles null control at 8 milliseconds rate. Otherwise, whenever ADC cycle select does select stage 1, except during the downstage actuator response test for the stage 1 nozzles, stage 1 nozzles shall be controlled as specified in stage 1 nozzles null control at 2 milliseconds rate.

2-10.7.2.1. Stage 1 Nozzles Null Control at 2 Milliseconds Rate. The following steps shall be performed:

a. Set TVC_CMD_4 to 0.0 (degrees).

b. Issue flight control select/event markers commands shown in test pattern. Obtain the flight control select/event markers and verify correct read back

response to test pattern. Set the computer failure MOSR as an alarm for any incorrect responses.

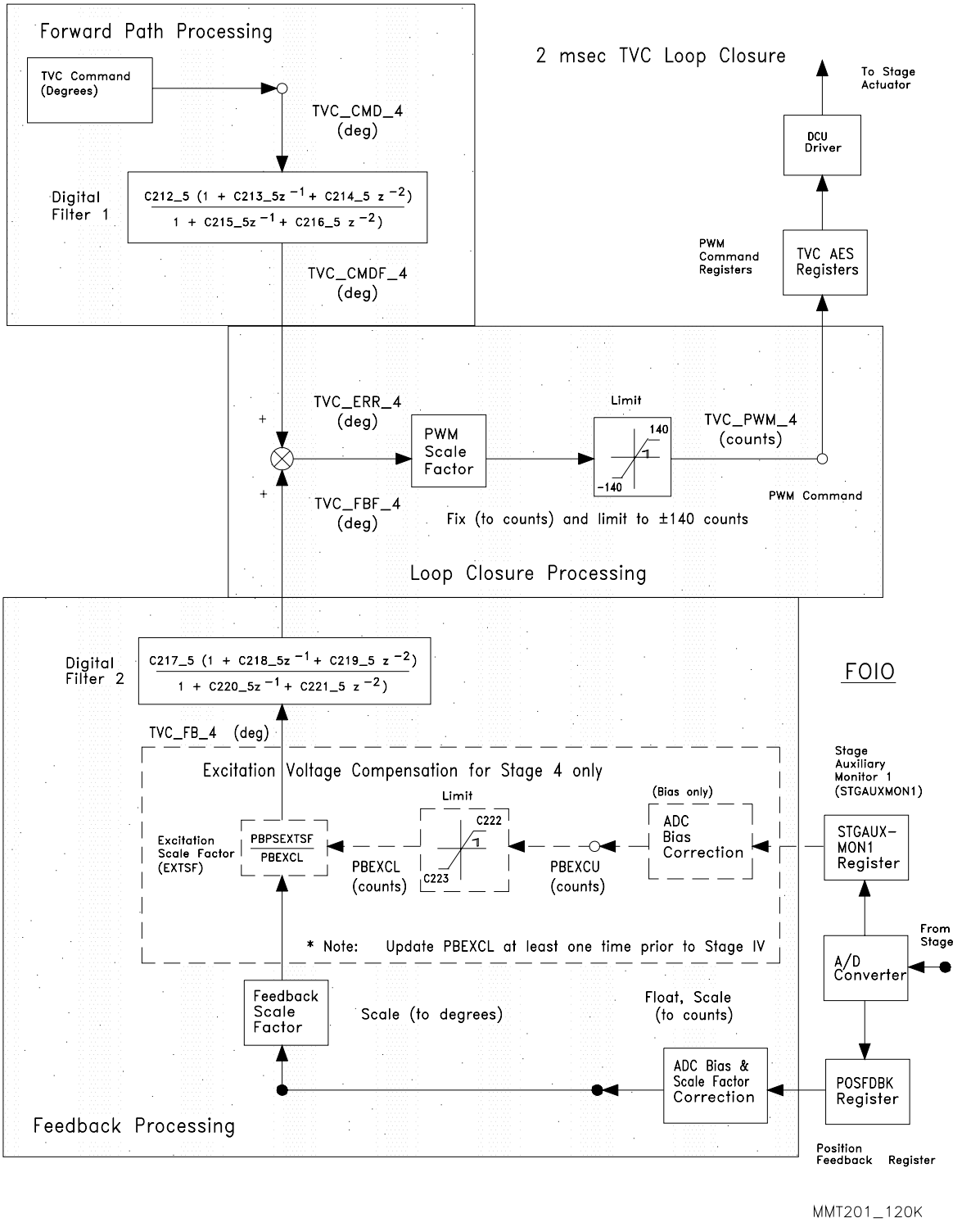
c. Perform the processing of Thrust Vector Control when TVC Initiate interrupt occurs.

d. At least once, obtain the position feedback for a minimum of five consecutive interrupts, and verify the ID tag cycles (i.e. numerically increments by one, modulo 4, with each consecutive sample) through 0, 1, 2, 3, and 0. Set the computer failure MOSR as an alarm for an incorrect response.

2-10.7.2.2. Stage 1 Nozzles Null Control at 8 Milliseconds Rate. The processing of thrust vector control for stage 1 nozzles nulling when stage 1 is not selected shall be performed.

2-10.7.3. Stage 2 Injectors Closed Position Control. The stage 2 injectors shall be controlled to the closed position except when ADCCYCSEL does select stage 2. The stage 2 actuator error signal commands shall be set to minus 28 counts (minus 20% PWM).

2-10.7.4. Thrust Vector Control. The thrust vector control processing is described below. For the NS20A, the thrust vector control was an automatic function provided by analog circuits in the P92A3. The NS20A supplied thrust vector position commands in terms of volts to the P92A3. The P92A3 measured the actuator position in terms of volts and supplied a pulse width modulated (PWM) signal to the actuator servo valve to move the actuator. For the GRP NS50A, the analog compensation supplied by the P92A3 is duplicated with digital processing at a nominal two msec rate in the GRP Operational Ground Program. The DCU converts the digital signal to a PWM signal. A block diagram of the GRP Operational Ground Program TVC loop closure processing is shown in TVC Loop Closure Processing (Figure 2-17). Depending on the stage selection and the cycle select code in effect, the DCU sequence of 500 microsecond interrupts for a particular 2 msec cycle is as follows: actuator 1, 2, 3, 4 for stage 1, or actuator 1, 2, 3, 4 for stage 2, or actuator 1, 2, 3, 4 for stage 3, or Pitch, Pitch, Yaw, Yaw for the post boost actuators. Since the post boost actuators are sampled twice in every 4 (500 microsecond) interrupts and 2 msec filtering is desired, only every other sample is processed in post boost. The general timing of the OGP TVC Interrupt processing is shown in TVC Interrupt Processing (Figure 2-18). The coefficients for digital filter 1 and digital filter 2 of TVC Loop Closure Processing are provided by the Flight Program Constants.



SOURCE: S-133-19251

Figure 2-17. TVC Loop Closure Processing

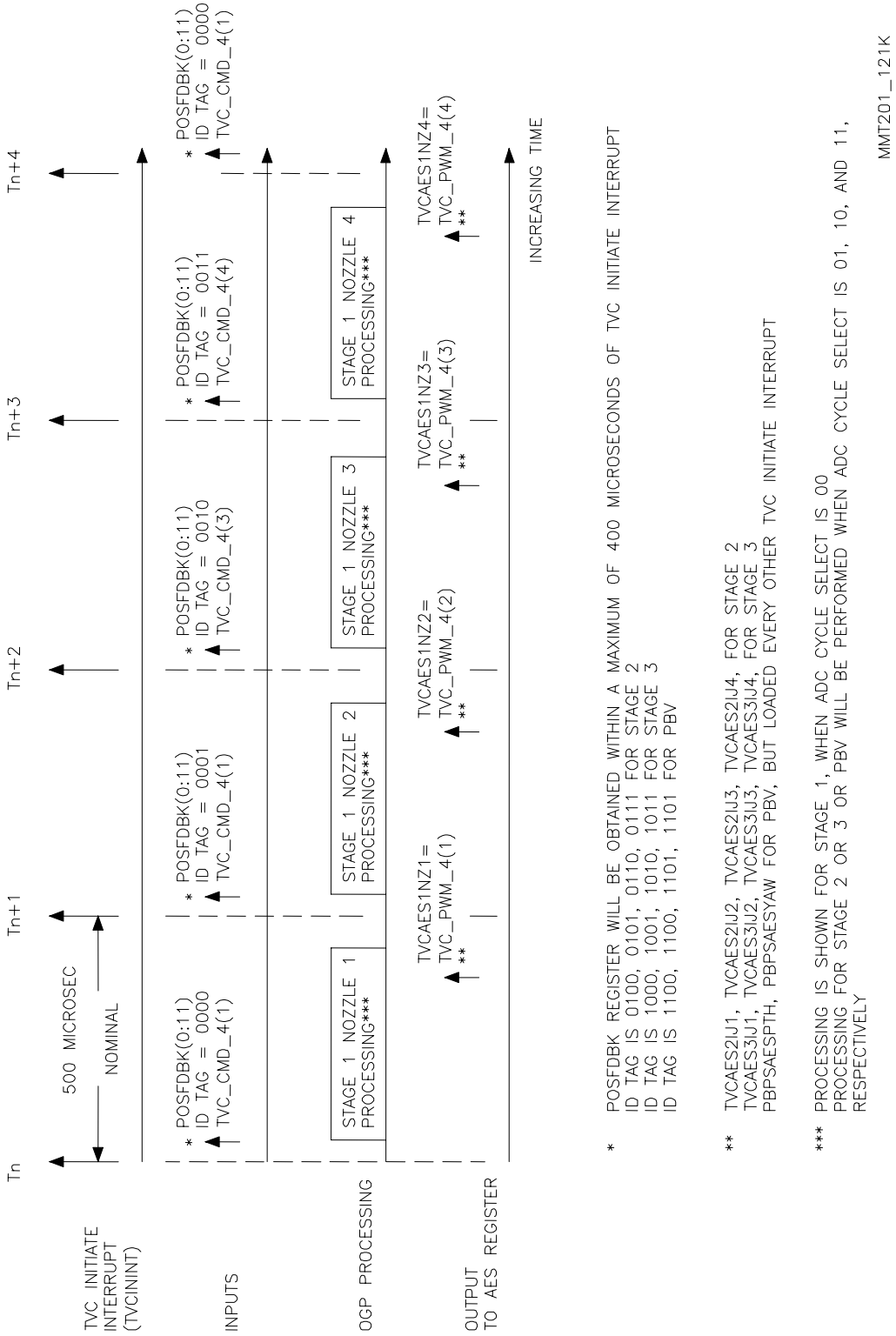


Figure 2-18. TVC Interrupt Processing

2-10.7.5. Thrust Vector Control for Stage 1 Nozzles Nulling When Stage 1 Is Not Selected. During the parts of Missile Test when Stage 1 is not being tested, the Stage 1 TVC loops are closed at a nominal 8 msec rate in the GRP Ground Program. Since the purpose is to just maintain the Stage 1 nozzles near null, a simple loop closure for each actuator using the actuator feedback with a low gain as the error function is adequate. This provides TVC control loop nulling and attenuates the inherent nozzle/actuator oscillations while on the ground.

2-10.8. Missile Ordnance Discretes Test. The Missile Ordnance Discretes Test shall start at a minimum of 5.55 seconds after the issuance of the F/C Ground Power Set character output command. The Missile Ordnance Discretes Test verifies that all flight mandatory ordnance discrete circuits and missile ordnance safety provisions are in the flight ready condition. The verification process shall consist of the following functions:

a. Initialize Fault Data Word 2 and Fault Data Word 3 to the no fault state.

b. Ordnance Enable (Missile) and R/S Ordnance Enable shall be reset, then perform the following:

(1) Obtain the FOIO Ordnance Enable Register. Verify that the read is the same as the write issued.

(2) Obtain the UIO Discrete Output Register. Verify that the read is the same as the write issued.

(3) Set the Computer Failure MOSR as an alarm for any incorrect responses obtained in steps 1. and 2.

c. Sequentially issue each of the Test Commands listed in Table 2-3 through Table 2-6. Verify that the read back matches the write command. Set the computer failure MOSR as an alarm for alarm for any incorrect responses.

d. Delay greater than 0.0 MSEC and issue the appropriate Ordnance Enable (Ordnance Enable (Missile) for downstage and PBPS, R/S Ordnance Enable for the R/S). Verify that the read back matches the write command. Set the Computer Failure MOSR as an alarm for any incorrect responses.

e. Obtain the discrete input responses in Table 2-7 through Table 2-11 in accordance with the Missile Ordnance Discrete Timing in Figure 2-19. Save the responses in Fault Data Word 2 and Fault Data Word 3.

f. Verify a false response at the PSRE Valve Fault Monitor.

g. Reset the command by resetting the appropriate Ordnance Enable within

20 msec of obtaining the discrete input response. Verify that the read back matches the write command. Set the Computer Failure MOSR as an alarm for any incorrect responses.

h. Obtain discrete input response to verify all downstage PBPS, and R/S ordnances are reset.

i. Issue Reset All PBPS and Downstage Ordnances Command and Rest All R/S Ordnances Command.

j. Repeat this iteration for each command until all commands have been processed.

k. Process incorrect responses as follows:

(1) A Downstage Discretes Failure MOSR shall be reported if any of the discrete response bits of Downstage Ordnance Discretes failed to respond true upon command.

(2) The R/S Discretes Failure MOSR shall be reported if any of the discrete response bits of Reentry System Discretes except R/S Prearm failed to respond true upon command.

(3) The PSRE Discretes Failure MOSR shall be reported if any of the discrete response bits of Propulsion System Rocket Engine Discretes failed to respond true upon command.

(4) The Control and Discretes Unit Failure MOSR shall be reported if any ordnance discrete response bits responded true either more than once or in an out-of-sequence manner or the ordnance discrete response bits of Ordnance Hazardous Current Discretes failed to respond properly. The Control and Discretes Unit Failure MOSR shall be reported if R/S Prearm bit responded true, and for this failure, if the R/S Configuration is MK12 (value is 1 to 12) it is only an alarm condition and if the R/S Configuration is MK12A (value is 13 to 24) Standby No-Go shall be entered at the end of Missile Test. The Control and Discretes Unit Failure MOSR shall be reported if any of the discrete response bits of Downstage Ordnance Discretes failed to respond false upon command. The Control and Discretes Unit Failure MOSR shall be reported if any of the discrete response bits of Reentry System Discretes failed to respond false upon command. The Control and Discretes Unit Failure MOSR shall be reported if any of the discrete response bits of Propulsion System Rocket Engine Discretes failed to respond false upon command.

(5) The Control and Discretes Unit Failure MOSR shall be reported if the PSRE Valve Fault Monitor responded true during step f. above. If R/S Configuration is MK12, any failure specified in this paragraph for only R/S Prearm and R/S Ordnance Enable true set shall be set as an alarm.

(6) The Computer Failure MOSR shall be reported as an alarm, if any of the ordnance discrete response bits of Ordnance Spares Discretes failed to respond properly.

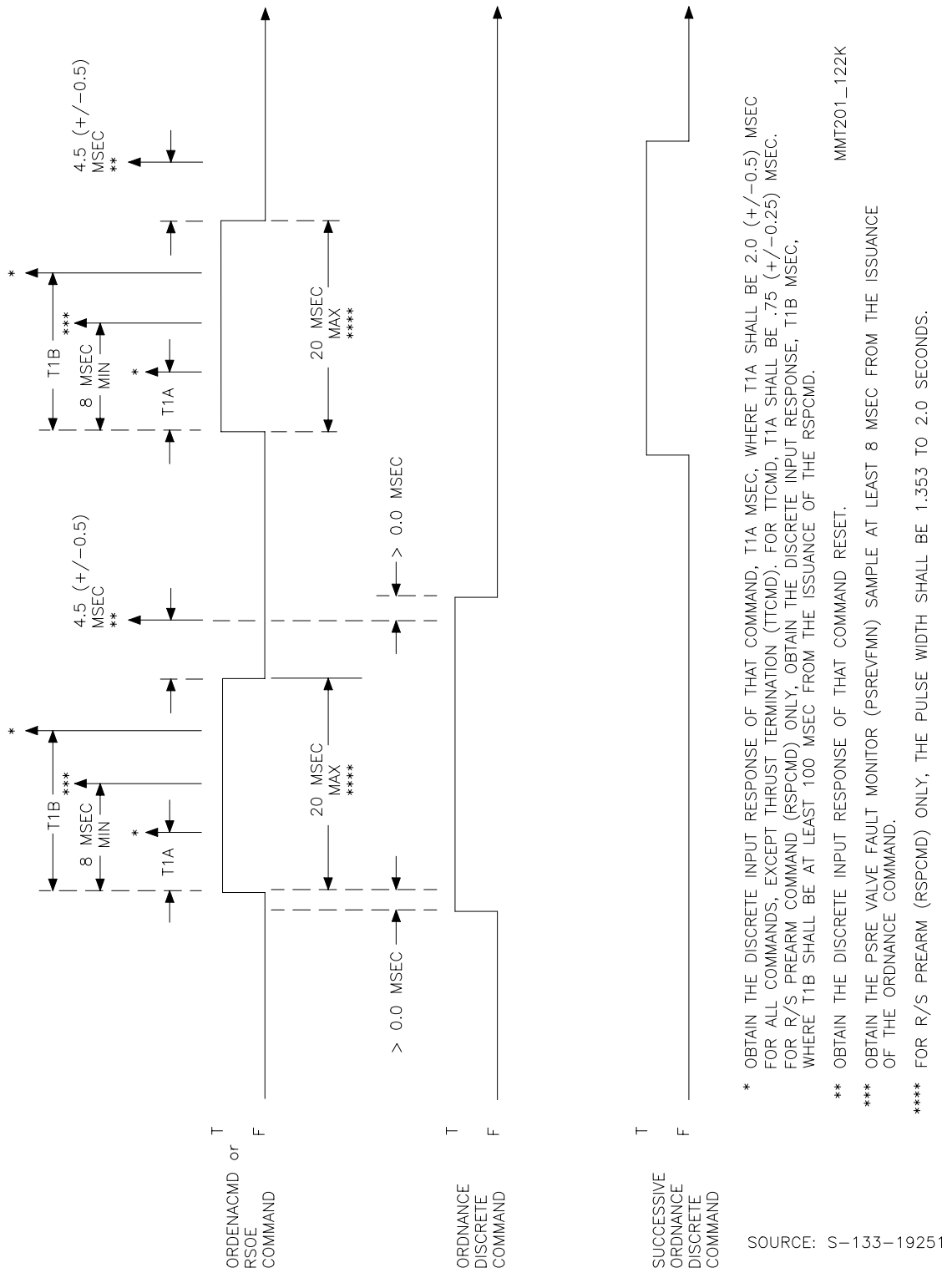


Figure 2-19. Missile Ordnance Discrete Timing

Table 2-3. Missile Ordnance Discrete Test Commands Format 1

DISCRETE COMMANDS SYMBOL	FUNCTION	(FOIO) ORDNANCE COMMANDS REGISTER (ORDCMDS) (0221) BIT *															
		0	1	STG1IG 2	STG12CMD 3	GG12CMD 4	DOSP1CMD 5	DOSP2CMD 6	STG23CMD 7	GG34CMD 8	TTCMD 9	S3EDCMD 10	S3MDCMD 11	PBPSOS1CMD 12	PBPSOS2CMD 13	PSREPOCMD 14	PSREPPCMD 15
N/A	Reset all PBPS & Downstage Ordnances command (None)	x	x	0	0	0	0	0	0	0	0	0	0	0	0	0	0

* x bits (0-1) shall be commanded 0. During read back of this register, PBPSOS1RB, PBPSOS2RB, DOSP1RB and DOSP2RB shall be masked.

Table 2-3. Missile Ordnance Discrete Test Commands Format 1

DISCRETE COMMANDS SYMBOL	FUNCTION	(FOIO) ORDNANCE COMMANDS REGISTER (ORDCMDS) (0221) BIT *															
		0	1	STG1IG 2	STG12CMD 3	GG12CMD 4	DOSP1CMD 5	DOSP2CMD 6	STG23CMD 7	GG34CMD 8	TTCMD 9	S3EDCMD 10	S3MDCMD 11	PBPSOS1CMD 12	PBPSOS2CMD 13	PSREPOCMD 14	PSREPPCMD 15
N/A	Reset all PBPS & Downstage Ordnances command (None)	x	x	0	0	0	0	0	0	0	0	0	0	0	0	0	0

* x bits (0-1) shall be commanded 0. During read back of this register, PBPSOS1RB, PBPSOS2RB, DOSP1RB and DOSP2RB shall be masked.

Table 2-4. Missile Ordnance Discrete Test Commands Format 2

DISCRETE COMMANDS SYMBOL	FUNCTION	(FOIO) ORDNANCE COMMANDS REGISTER (ORDCMDS) (0221) BIT *															
		0	1	2 STG1IG	3 STG12CMD	4 GG12CMD	5 DOSP1CMD	6 DOSP2CMD	7 STG23CMD	8 GG34CMD	9 TTCMD	10 S3EDCMD	11 S3MDCMD	12 PBPSOS1CMD	13 PBPSOS2CMD	14 PSREPOCMD	15 PSREPPCMD
STG12CMD	1-2 Staging	x	x	0	1	0	0	0	0	0	0	0	0	0	0	0	0
GG12CMD	Gas Gen 1 and 2	x	x	0	0	1	0	0	0	0	0	0	0	0	0	0	0
STG23CMD	2-3 Staging	x	x	0	0	0	0	0	1	0	0	0	0	0	0	0	0
GG34CMD	Gas Gen 3 and 4	x	x	0	0	0	0	0	0	1	0	0	0	0	0	0	0
TTCMD	Thrust Termination	x	x	0	0	0	0	0	0	0	1	0	0	0	0	0	0
S3EDCMD	Stage 3 Elect Discon	x	x	0	0	0	0	0	0	0	0	1	0	0	0	0	0
S3MDCMD	Stage 3 Mech Discon	x	x	0	0	0	0	0	0	0	0	0	1	0	0	0	0
PSREPOCMD	PSRE Prop Outlet	x	x	0	0	0	0	0	0	0	0	0	0	0	0	1	0
PSREPPCMD	PSRE Prop Pres	x	x	0	0	0	0	0	0	0	0	0	0	0	0	0	1

* x bits (0-1) shall be commanded 0. During read back of this register, PBPSOS1RB, PBPSOS2RB, DOSP1RB, DOSP2RB shall be masked.

Table 2-5. Missile Ordnance Test Commands Format 3

DISCRETE COMMANDS SYMBOL	FUNCTION	(UIO) R/S DISCRETE OUTPUT REGISTER (RSDOREG) (0184) BIT *															
		0	1	RSPCMD 2	RSSMCMD 3	RS12CMD 4	RS11CMD 5	RS10CMD 6	RS9CMD 7	RS8CMD 8	RS7CMD 9	RS6CMD 10	RS5CMD 11	RS4CMD 12	RS3CMD 13	RS2ABCMD 14	RS1CMD 15
N/A	Reset all R/S Ordnances command (None)	x	x	0	0	0	0	0	0	0	0	0	0	0	0	0	0

* x bits (0-1) shall be commanded 0.

Table 2-6. Missile Ordnance Test Commands Format 6

DISCRETE COMMANDS SYMBOL	FUNCTION	(UIO) R/S DISCRETE OUTPUT REGISTER (RSDOREG) (0184) BIT *															
		0	1	RSPCMD 2	RSSMCMD 3	RS12CMD 4	RS11CMD 5	RS10CMD 6	RS9CMD 7	RS8CMD 8	RS7CMD 9	RS6CMD 10	RS5CMD 11	RS4CMD 12	RS3CMD 13	RS2ABCMD 14	RS1CMD 15
RS11CMD	R/S No. 11	x	x	0	0	0	1	0	0	0	0	0	0	0	0	0	0
RS10CMD	R/S No. 10	x	x	0	0	0	0	1	0	0	0	0	0	0	0	0	0
RS9CMD	R/S No. 9	x	x	0	0	0	0	0	1	0	0	0	0	0	0	0	0
RS8CMD	R/S No. 8	x	x	0	0	0	0	0	0	1	0	0	0	0	0	0	0
RS7CMD	R/S No. 7	x	x	0	0	0	0	0	0	0	1	0	0	0	0	0	0
RS6CMD	R/S No. 6	x	x	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Table 2-6. Missile Ordnance Test Commands Format 6 (Continued)

DISCRETE COMMANDS SYMBOL	FUNCTION	(UIO) R/S DISCRETE OUTPUT REGISTER (RSDOREG) (0184) BIT *															
		0	1	2 RSPCMD	3 RSSMCMD	4 RS12CMD	5 RS11CMD	6 RS10CMD	7 RS9CMD	8 RS8CMD	9 RS7CMD	10 RS6CMD	11 RS5CMD	12 RS4CMD	13 RS3CMD	14 RS2ABCMD	15 RS1CMD
RS5CMD	R/S No. 5	x	x	0	0	0	0	0	0	0	0	0	1	0	0	0	0
RS4CMD	R/S No. 4	x	x	0	0	0	0	0	0	0	0	0	0	1	0	0	0
RS3CMD	R/S No. 3	x	x	0	0	0	0	0	0	0	0	0	0	0	1	0	0
RS2ABCMD	R/S No. 2 (A,B)	x	x	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RS1CMD	R/S No. 1	x	x	0	0	0	0	0	0	0	0	0	0	0	0	0	1

* x bits (0-1) shall be commanded 0.

Table 2-7. Downstage Ordnance Discretes

DISCRETE RESPONSE BITS	FUNCTION
GG1MN, GG2MN	Gas Generators 1 and 2
STG2IMN, STG12MN	Stage 2 Ignition and 1-2 Separation
STG3IMN, STG23MN	Stage 3 Ignition and 2-3 Separation
GG3MN, GG4MN	Gas Generators 3 and 4
TTAMN, TTBMN	Thrust Termination A and B

Table 2-8. Reentry System Discretes

DISCRETE RESPONSE BITS	FUNCTION
RS4MN	R/S 4
RS5MN	R/S 5
RS9MN	R/S 9
RS10MN	R/S 10
RS6MN	R/S 6
RS3MN	R/S 3
RS7MN	R/S 7
RS2AMN, RS2BMN	R/S 2A and 2B
RS1MN	R/S 1
RS11MN	R/S 11
RS8MN	R/S 8
RS12MN	R/S 12
RSPMN	R/S Prearm

Table 2-9. Propulsion System Rocket Engine Discretes

DISCRETE RESPONSE BITS	FUNCTION
PBPSPPMN	PSRE Propellant Pressure
PBPSPOMN	PSRE Propellant Outlet
S3EDMN	Stage 3/PSRE Electrical Disconnect
S3MDMN	Stage 3/PSRE Mechanical Disconnect

Table 2-10. Ordnance Hazardous Current Discretes

DISCRETE RESPONSE BITS	FUNCTION
ORDHZ1MN	Ordnance Hazardous Current Monitor No. 1
ORDHZ2MN	Ordnance Hazardous Current Monitor No. 2
RSHZ1MN	R/S Ordnance Hazardous Current Monitor No. 1
RSHZ2MN	R/S Ordnance Hazardous Current Monitor No. 2

Table 2-11. Ordnance Spares Discretes

DISCRETE RESPONSE BITS	FUNCTION
DOSP1MN	Downstage Ordnance Spare No. 1
DOSP2MN	Downstage Ordnance Spare No. 2
PBPSOS1MN	PBPS Ordnance Spare No. 1
PBPSOS2MN	PBPS Ordnance Spare No. 2

2-10.9. Propulsion System Rocket Engine Control Test. The Propulsion System Rocket Engine (PSRE) Control Test shall start at a minimum of 1.50 seconds after the issuance of the F/C Ground Power Set character output code in the Flight Control Ground Power Turn-on Test. The Propulsion System Rocket Engine (PSRE) Control Test shall be comprised of the PSRE Actuator Response and Transducer Excitation Enable Control Test and the PSRE Valve Control Test.

2-10.9.1. Propulsion System Rocket Engine Actuator Response and Transducer Excitation Enable Control Test. The PSRE Actuator Response Test verifies that the axial engine pitch and yaw actuators will respond to extend and retract deflection commands with a minimum deflection rate equivalent to 4 deg per second, nominal-voltage (29 volts), non-firing, non-pressurized silo condition. The general test sequence is shown in Figure 2-20. Detection of a failure during these tests will set the appropriate fault bit(s) in Fault Data Word 5 and will set the PSRE Control Failure MOSR. The Transducer Excitation Enable Control Test portion (steps o. through q. below) verifies that no voltage excitation is present when the Transducer Excitation Enable command is false (off). Detection of a failure during this test will set the Computer Failure MOSR. The Pitch and Yaw Actuator Null (step c. below), Extend Rate (f.2.), Deflected Position Steady State (f.4.) and Retract Rate (I.) Position Feedback data samples shall be saved into the Missile Test IPDR Buffer. The following test steps shall be performed:

a. Assure that Fault Data Word 5 is initialized one time only prior to the performance of step d.

b. Perform the following:

(1) For I=1 to 2, set TVC_CMD_4(I) = 0.0 deg, where TVC_CMD_4(1) is pitch command and TVC_CMD_4(2) is yaw command.

(2) Issue Flight Control Select/Event Markers command test pattern 1 of Table 2-13. The Stage 2 actuator error signal commands shall be set at least one time to minus 28 counts (minus 20% PWM) when the ID Tag of the Position Feedback register is either 12 or 13. Obtain the Flight Control Select/Event Markers and verify correct readback response to test pattern. Set the Computer Failure MOSR as an alarm for any incorrect responses. (Note: During the PSRE Actuator Response Test the Stage 1 Actuator Nozzles and the Stage 2 Injectors are also being controlled).

(3) Perform the processing of Thrust Vector Control when TVC Initiate interrupt occurs.

(4) If Tranducer Excitation Enable bite was not previously set for 100 msec, perform the following:

(a) Delay a minimum of 100 msec.

(b) Perform Excitation Voltage Compensation.

c. If Tranducer Excitation Enable bit was not previously set for 100 msec, perform the following:

(1) Delay .98 sec minimum following the TVC Initiate interrupt that commences Thrust Vector Control processing of the command set in step b.1 and obtain one position feedback sample for each of the two (pitch and yaw) PSRE actuator position feedbacks.

(2) Each Position Feedback shall be processed, scaled, and compensated:

(3) Save POSFDBKVV into scaled and compensated feedback variables listed in step (a) below for pitch, or step (b) below for yaw as follows:

(a) if IDTAGV = 12, set VPITCHN = POSFDBKVV

(b) if IDTAGV = 13, set VYAWN = POSFDBKVV

d. Perform the following:

(1) Set the pitch null error bit(s) in Fault Data Word 5 if VPITCHN $\neq$ 0.0 ± 0.832 (arc) degrees.

(2) Set the yaw null error bit(s) in Fault Data Word 5 if VYAWN $\neq$ 0.0 ± 0.832 (arc) degrees.

(3) Set the fault monitor null error bit(s) in Fault Data Word 5 if PBPS Actuator Fault Monitor = true.

(4) Set the Computer Failure MOSR as an alarm if the two ID Tag samples obtained in step c.2.(a) above, one is not 12 and the other is not 13.

e. For I=1 to 2, set TVC_CMD_4(I) = 6.552 deg, where TVC_CMD_4(1) is pitch command and TVC_CMD_4(2) is yaw command.

f. Obtain an extend-rate sample and a deflected-position sample of each actuator feedback and the PBPS actuator fault monitor as follows:

(1) Delay 100 ± 80 msec following the TVC Initiate interrupt that commences Thrust Vector Control processing of the command set in step e. and obtain a sample of the PBPS Actuator Fault Monitor.

(2) Delay 1.50 ± 0.01 sec following the TVC Initiate interrupt that commences Thrust Vector Control processing of the command set in step e. and obtain one position feedback extend-rate sample for each of the two (pitch and yaw) PSRE actuator position feedbacks. Each position feedback shall be processed, scaled, and compensated.

(a) If IDTAGV = 12, set VPITCHE = POSFDBKVV

(b) If IDTAGV = 13, set VYAWE = POSFDBKVV

(c) Set the Computer Failure MOSR as an alarm if the two ID Tag samples obtained in step f.2.(a) above, one is not 12 and the other is not 13.

(3) Delay a minimum of 2.59 sec following the TVC Initiate interrupt that commences Thrust Vector Control processing of the command set in step e. and obtain a sample of the PBPS Actuator Fault Monitor.

(4) Delay a minimum of 2.59 sec following the TVC Initiate interrupt that commences Thrust Vector Control processing of the command set in step e. and obtain one position feedback deflected-position sample for each of the two (pitch and yaw) PSRE actuator position feedbacks. Feedback shall be processed, scaled, and compensated.

(a) If IDTAGV = 12, set VPITCHS = POSFDBKVV

(b) If IDTAGV = 13, set VYAWS = POSFDBKVV

(c) Set the Computer Failure MOSR as an alarm if the two ID Tag samples obtained in step f.4(a) above, one is not 12 and the other is not 13.

g. Set the actuator extend rate error bit(s) and the deflected steady state position error bit(s) in Fault Data Word 5 if any of the samples obtained in step f. satisfies the following:

(1) VPITCHE - VPITCHN $\neq$ -8.944 ± 4.368 degrees, set pitch extend rate error.

(2) VYAWE - VYAWN $\neq$ -8.944 ± 4.368 degrees, set yaw extend rate error.

(3) PACTFLTMON of step f.1. = false, set fault monitor extend rate error.

(4) VPITCHS $\neq$ -6.552 ± 1.144 degrees, set pitch deflected position error.

(5) VYAWS $\neq$ -6.552 ± 1.144 degrees, set yaw deflected position error.

(6) PACTFLTMON of step f.3. = true, set fault monitor deflected position error.

h. Set TVC_CMD_4(2) = 0.0 deg.

i. Obtain a retract-rate sample of the yaw actuator feedback and a sample of the PBPS actuator fault monitor as follows:

(1) Delay 100 ± 80 msec following the TVC Initiate interrupt that commences Thrust Vector Control processing of the command set in step h. and obtain a sample of the PBPS Actuator Fault Monitor.

(2) Delay 1.50 ± 0.01 sec following the TVC initiate interrupt that commences Thrust Vector Control processing of the command set in step h. and obtain one Position Feedback retract-rate sample of the yaw actuator position feedback. The position feedback shall be processed, scaled & compensated.

(a) If IDTAGV = 13, set VYAWR = POSFDBKVV

j. Set the actuator yaw retract rate error bit(s) in Fault Data Word 5 if any of the samples obtained in step i. satisfies the following:

(1) VYAWR - VYAWS $\neq$ 8.944 ± 4.368 degrees, set yaw retract rate error.

(2) PACTFLTMON of step i. = false, set fault monitor yaw retract rate error.

k. Assure that a minimum of 2.59 sec have elapsed from the setting of the thrust vector command in step h. and set TVC_CMD_4(1) = 0.0 deg.

l. Obtain a retract-rate sample of the pitch actuator feedback and a sample of the PBPS actuator fault monitor as follows:

(1) Delay 100 ± 80 msec following the TVC Initiate interrupt that commences Thrust Vector Control processing of the command set in step k. and obtain a sample of the PBPS Actuator Fault Monitor.

(2) Delay 1.50 ± 0.01 sec following the TVC Initiate interrupt that commences Thrust Vector Control processing of the command set in step k. and obtain one Position Feedback retract-rate sample of the pitch actuator position feedback. The position feedback shall be processed, scaled and compensated.

(a) If IDTAGV = 12, set VPITCHR = POSFDBKVV

m. Set the actuator pitch retract rate error bit(s) in Fault Data Word 5 if any of the samples obtained in step l. satisfies the following:

(1) VPITCHR - VPITCHS $\neq$ 8.944 ± 4.368 degrees, set pitch retract rate error.

(2) PACTFLTMON of step l. = false, set fault monitor pitch retract rate error.

n. Any of the following fault data bits, saved in Fault Data Word 5, if set, shall set the PSRE Control Failure MOSR:

Fault Data Bits	PSRE Control Failure MOSR
Yaw null error	Set
Pitch null error	Set
Fault monitor null error	-
Yaw extend rate error	Set
Pitch extend rate error	Set
Fault monitor extend rate error	-
Yaw deflected position error	Set
Pitch deflected position error	Set
Fault monitor deflected position error	-
Yaw retract rate error	Set
Fault monitor yaw retract rate error	-
Pitch retract rate error	Set
Fault monitor pitch retract rate error	-

o. Issue Flight Control Select/Event Markers command shown in Test Pattern 2 of Table 2-12. Obtain the Flight Control Select/Event Markers and verify correct readback response to test pattern. Set the Computer Failure MOSR as an alarm for any incorrect responses.

p. Delay a minimum of 100 msec after the command issuance of step o. above, and obtain the Stage Auxiliary Monitor 1, and perform the following:

(1) Set IDTAGSA1V = STGAUXMON1(12:15), and set STGAUX1V = STGAUXMON1(0:11).

(2) STGAUX1V shall be floated and compensated for ADC bias by performing ADC Output Compensation (Note: set ADCU=STGAUX1V). The result shall be the PBV Measured Transducer Excitation Voltage Compensated for ADC Bias (PBEXCU) (Note: set PBEXCU = ADCBC).

(3) Calculate the transducer excitation voltage (in volts) as follows: PBEXCU = PBEXCU / 204.8 (volts)

q. Set the Computer Failure MOSR as an alarm if PBEXCU $\geq$0.95 volts.

r. Set TVC_CMD_4(3) = 0.0 deg and TVC_CMD_4(4) = 0.0 deg. Issue Flight Control Select/Event Markers command shown in test pattern 3 of Table 2-12. Obtain the Flight Control Select/Event Markers (FCSELEMRB) and verify correct readback response to test pattern. Set the Computer Failure MOSR as an alarm for any incorrect responses.

2-10.9.2. Propulsion System Rocket Engine Valve Control Test. The PSRE valve control test shall verify that the correct valve monitor responses result from each attitude control commands and from the axial engine control commands. Fault Data Word 6 shall be initialized prior to its utilization as data storage. Detection of a failure during these tests shall set the appropriate fault bit(s) in Fault Data Word 6.

2-10.9.2.1. Attitude Control Commands. Each attitude control command and valve monitor response shall be verified to function properly by performing the following iterating sequence:

a. Issue each attitude control command of Table 2-13.

b. Read the (FOIO) PBPS Axial/Attitude Register following each command issued in step a. above. Verify that the read is the same as the write issued. Set the Computer Failure MOSR as an alarm for any incorrect responses obtained.

c. Delay between 15 to 20 msec following each command issued in step a. above, then read the FOIO PBPS Valve Status Register. Verify correct read back response.

2-10.9.2.2. Axial Engine Control Commands. There are two groups of commands which shall be applied sequentially to verify the flightworthy status of the axial engine valve. The following sequences shall be executed:

a. Execute command group 1 specified in Table 2-14.

b. Read the (FOIO) PBPS Axial/Attitude Register following the command issued in step a. above. Verify that the read is the same as the write issued. Set the Computer Failure MOSR as an alarm for any incorrect responses obtained.

c. Delay 88 ± 3 msec following the command issued in step a. above, then read the FOIO PBPS Valve Status Register. Verify correct read back response.

d. Execute command group 2 specified in Table 2-14.

e. Read the (FOIO) PBPS Axial/Attitude Register following the command issued in step d. above. Verify that the read is the same as the write issued.

Set the Computer Failure MOSR as an alarm for any incorrect responses obtained.

f. Delay 45 ± 5 msec following the command issued in step d. above, then read the FOIO PBPS Valve Status Register. Verify correct read back response.

2-10.9.2.3. Attitude and Axial Engine Valve Responses. Whenever any of the discrete monitor responses disagrees with the expected responses, the following action shall result:

a. The PSRE Control Failure MOSR shall be set.

b. The discrete monitor which failed to respond correctly shall be saved in Fault Data Word 6.

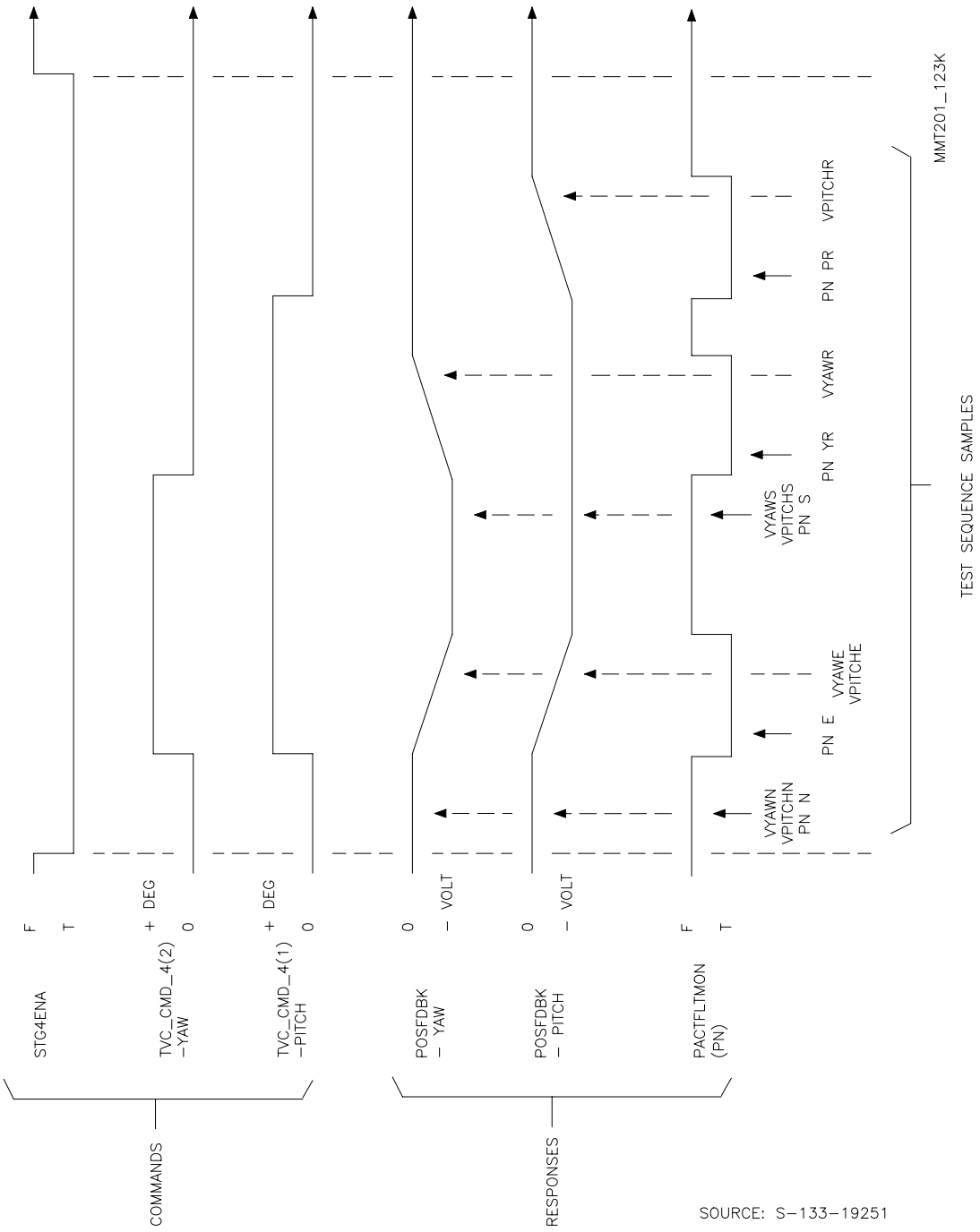


Figure 2-20. PSRE Actuator Response Test

Table 2-12. Flight Control Select/Event Markers Commands for PSRE Actuator Response Test

SYMBOL	FUNCTION	FLIGHT CONTROL SELECT/EVENT MARKERS (020E) BIT(S)	TEST PATTERN *	TEST PATTERN *	TEST PATTERN *
			1	2	3
N/A		0-3	x	x	x
N/A		4	x	x	x
EVNTMARKER	Event Marker #1 - MSB	5	0	0	0
EVNTMARKER	Event Marker #2	6	1	1	0
EVNTMARKER	Event Marker #3	7	0	0	0
EVNTMARKER	Event Marker #4 - LSB	8	0	0	0
TRNDUCXENA	Transducer Excitation Enable	9	1	0	0
ADCCYCSEL	ADC Cycle Select - MSB	10	1	1	0
ADCCYCSEL	ADC Cycle Select - LSB	11	1	1	0
STG1ENA	Stage 1 Command Enable	12	1	1	1
STG2ENA	Stage 2 Command Enable	13	1	1	1
STG3ENA	Stage 3 Command Enable	14	0	0	0
STG4ENA	PBPS Actuator Command Enable	15	1	0	0
* x bits (0-4) are unassigned and shall be commanded 0.					

Table 2-13. PSRE Attitude Valve Control Commands

FUNCTION	PSRE VALVE DISCRETE COMMANDS	(FOIO) PBPS AXIAL/ATTITUDE REGISTER (PBPSAXATT) (0212) BIT *												
		0-3	4	5 AXENGINON	6 YAWATT1CMD	7 YAWATT2CMD	8 PCHATT1CMD	9 PCHATT2CMD	10 PCHATT3CMD	11 PCHATT4CMD	12 ROLATT1CMD	13 ROLATT2CMD	14 ROLATT3CMD	15 ROLATT4CMD
Roll 4	ROLATT4CMD	x	x	0	0	0	0	0	0	0	0	0	0	1
None (all PBPS axial and attitude valve commands off)		x	x	0	0	0	0	0	0	0	0	0	0	0
Roll 3	ROLATT3CMD	x	x	0	0	0	0	0	0	0	0	0	1	0
None		x	x	0	0	0	0	0	0	0	0	0	0	0
Roll 2	ROLATT2CMD	x	x	0	0	0	0	0	0	0	0	1	0	0
None		x	x	0	0	0	0	0	0	0	0	0	0	0
Roll 1	ROLATT1CMD	x	x	0	0	0	0	0	0	0	1	0	0	0
None		x	x	0	0	0	0	0	0	0	0	0	0	0
Pitch 4	PCHATT4CMD	x	x	0	0	0	0	0	0	1	0	0	0	0
None		x	x	0	0	0	0	0	0	0	0	0	0	0
Pitch 3	PCHATT3CMD	x	x	0	0	0	0	0	1	0	0	0	0	0
None		x	x	0	0	0	0	0	0	0	0	0	0	0
Pitch 2	PCHATT2CMD	x	x	0	0	0	0	1	0	0	0	0	0	0
None		x	x	0	0	0	0	0	0	0	0	0	0	0
Pitch 1	PCHATT1CMD	x	x	0	0	0	1	0	0	0	0	0	0	0
None		x	x	0	0	0	0	0	0	0	0	0	0	0
Yaw 2	YAWATT2CMD	x	x	0	0	1	0	0	0	0	0	0	0	0
None		x	x	0	0	0	0	0	0	0	0	0	0	0
Yaw 1	YAWATT1CMD	x	x	0	1	0	0	0	0	0	0	0	0	0
None		x	x	0	0	0	0	0	0	0	0	0	0	0

* x bits (0-4) shall be commanded 0.

Table 2-14. PSRE Axial Valve Control Commands

COMMAND GROUP	PSRE VALVE DISCRETE COMMANDS	(FOIO) PBPS AXIAL/ATTITUDE REGISTER (PBPSAXATT) (0212) BIT *												
		0-3	4	5 AXENGINON	6 YAWATT1CM	7 YAWATT2CM	8 PCHATT1CMD	9 PCHATT2CMD	10 PCHATT3CMD	11 PCHATT4CMD	12 ROLATT1CMD	13 ROLATT2CMD	14 ROLATT3CMD	15 ROLATT4CMD
1	AXENGINON	x	x	1	0	0	0	0	0	0	0	0	0	0
2	None (all off)	x	x	0	0	0	0	0	0	0	0	0	0	0
* x bits (0-4) shall be commanded 0.														

2-10.10. Downstage Control System Test. The Downstage Control System Test shall start at a minimum of 1.50 seconds after the issuance of the F/C Ground Power Set character output code in 2-10.7.1. The Downstage Control System test shall verify that all downstage control actuators respond properly when commanded by the computer and that both roll control systems, stages 2 and 3, perform as required. This test shall be conducted for each stage and shall be completed regardless of test failures which may occur. The tests shall be as follows:

2-10.10.1. Downstage Actuator Response Test. This test verifies hardware performance characteristics equivalent to those specified by the following: (1) test for the following minimum combined rates when all actuators for the given stage are rate limited: 80 deg/sec for Stage 1, 6 inches/sec for Stage 2, 4.5 inches/sec for Stage 3, (2) test for the following minimum rates of each actuator of the given stage when moving individually: 20 deg/sec for Stage 1, 1.5 inches/sec for Stage 2, 1.125 inches/sec for Stage 3, (3) test each actuator for the following static accuracy at the no load null and half-scale command positions for each servo loop: ± 10% gain variation, and ± 0.0176 inches bias, for Stage 1, ± 10% gain variation, and ± 0.0075 inches bias, for Stage 2, ± 10% gain variation, and ± 0.0075 inches bias, for Stage 3, (4) assure that each 35 radian/second command line filter and servo loop gain provide the following minimum gain/phase margin: 10 db gain margin, and 30 degrees phase margin for Stage 1, 10 db gain margin, and 30 degrees phase margin for Stage 2, 10 db gain margin, and 30 degrees phase margin for Stage 3, (5) perform Fault Isolation Monitor check during steady state check and store results in a fault data word. The test sequence per stage is shown in Figure 2-21. Fault Data Word 4 will be initialized prior to its utilization as data storage. Detection of a failure during

these tests will set the appropriate fault bit(s) in Fault Data Word 4 and will set the Downstage Control Failure MOSR. The Stage 1 Nozzles 1, 2, 3, and 4 Null - first sample only (step c. below), Rate (h.), Steady State (j) and Lag (m.1.(a)) Position Feedback data samples shall be saved into the Missile Test IPDR Buffer. The Stage 2 Injectors 1, 2, 3, and 4 Null - first sample only (step c. below), Rate (h.), Steady State (j.) and Lag (m.1.(a)) Position Feedback data samples shall be saved into the Missile Test IPDR Buffer. The Stage 3 Injectors 1, 2, 3, and 4 Null - first sample only (step c. below), Rate (h.) Steady State (j.) and Lag (m.1.(a)) Position Feedback data samples shall be saved into the Missile Test IPDR Buffer. The following steps shall be performed for each stage (Stages 1, 2 and 3):

a. Assure that Fault Data Word 4 is initialized one time only prior to the performance of step d.

b. Perform the following:

(1) The appropriate stage shall be selected and controlled (see Figure 2-21, for reference only) as follows:

(a) Set [TVC_CMD_4] = [0]

(b) Perform step (1) below for Stage 1 Actuator Response Test, or step (2) below for Stage 2 Actuator Response Test, or step (3) below for Stage 3 Actuator Response Test.

(1) Issue Flight Control Select/Event Markers command shown in test pattern 1 of Table 2-15. The Stage 2 actuator error signal commands shall be set at least one time to minus 28 counts (minus 20% PWM) when the ID Tag of the Position Feedback register is either 0, 1, 2 or 3. Obtain the Flight Control Select/Event Markers and verify correct readback response to test pattern 1. Set the Computer Failure MOSR as an alarm for any incorrect responses. (Note: During the Stage 1 Actuator Response Test, the Stage 2 Injectors are also being controlled).

(2) Issue Flight Control Select/Event Markers command shown in test pattern 2 of Table 2-15. Obtain the Flight Control Select/Event Markers and verify correct readback response to test pattern. Set the Computer Failure MOSR as an alarm for any incorrect responses. (Note: During the Stage 2 Actuator Response Test, the Stage 1 Nozzles are also being controlled).

(3) Issue Flight Control Select/Event Markers command shown in test pattern 3 of Table 2-18. The Stage 2 actuator error signal commands shall be set at least one time to minus 28 counts (minus 20% PWM) when the ID Tag of the Position Feedback register is either 8, 9, 10 or 11. Obtain the Flight Control Select/Event Markers and verify correct readback response to test pattern 3. Set the Computer Failure MOSR as an alarm for any incorrect responses. (Note: During the Stage 3 Actuator Response Test, the Stage 1 Nozzles and the Stage 2 Injectors are also being controlled).

(c) Perform the processing of Thrust Vector Control when TVC Initiate interrupt occurs.

c. Obtain the Fault Monitor of the stage selected and a 17 sample steady state null feedback voltage average for each of the four actuator position feedbacks selected as follows:

(1) Obtain 17 Position Feedback samples for each of the four actuator position feedbacks selected after successive TVC Initiate interrupts and obtain a sample of the Fault Monitor of the stage selected at least 270 msec following step b.1.(b).

(2) Process and save POSFDBKVV into compensated feedback voltage variables listed in step (a) below for Stage 1, or step (b) below for Stage 2, or step (c) below for Stage 3, based on IDTAGV, as follows:

(a) if IDTAGV = 0, set V11(i) = POSFDBKVV (Stage 1 Nozzle 1), or
if IDTAGV = 1, set V12(i) = POSFDBKVV (Stage 1 Nozzle 2), or
if IDTAGV = 2, set V13(i) = POSFDBKVV (Stage 1 Nozzle 3), or
if IDTAGV = 3, set V14(i) = POSFDBKVV (Stage 1 Nozzle 4), where i=1 to 17.

(b) if IDTAGV = 7, set V21(i) = POSFDBKVV (Stage 2 Pintle 4), or
if IDTAGV = 6, set V22(i) = POSFDBKVV (Stage 2 Pintle 3), or
if IDTAGV = 5, set V23(i) = POSFDBKVV (Stage 2 Pintle 2), or
if IDTAGV = 4, set V24(i) = POSFDBKVV (Stage 2 Pintle 1),
where i=1 to 17.

(c) if IDTAGV = 11, set V31(i) = POSFDBKVV (Stage 3 Pintle 4), or
if IDTAGV = 10, set V32(i) = POSFDBKVV (Stage 3 Pintle 3), or
if IDTAGV = 9, set V33(i) = POSFDBKVV (Stage 3 Pintle 2), or
if IDTAGV = 8, set V34(i) = POSFDBKVV (Stage 3 Pintle 1),
where i=1 to 17.

(3) Get the feedback voltage average by performing step (a) below for Stage 1 Actuator Response Test, or step (b) below for Stage 2 Actuator Response Test, or step (c) below for Stage 3 Actuator Response Test.

(a) set V11_AVGN, V12_AVGN, V13_AVGN, V14_AVGN to the average of [V11], [V12], [V13], and [V14] for I=1 to 17, respectively.

(b) set V21_AVGN, V22_AVGN, V23_AVGN, V24_AVGN to the average of [V21], [V22], [V23], and [V24] for I=1 to 17, respectively.

(c) set V31_AVGN, V32_AVGN, V33_AVGN, V34_AVGN to the average of [V31], [V32], [V33], and [V34] for I=1 to 17, respectively.

d. Preform step 1. below for Stage 1 Actuator Response Test, or step 2. below for Stage 2 Actuator Response Test, or step 3. below for Stage 3 Actuator Response Test.

(1) Set a null error bit for Stage 1 in Fault Data Word 4 if any of the averages obtained in step c. are not within the following:

V11_AVGN = 0 ± .51154 volts, V12_AVGN = 0 ± .51154 volts,
V13_AVGN = 0 ± .51154 volts, V14_AVGN = 0 ± .51154 volts.

Set the Computer Failure MOSR as an alarm if five successive samples of the IDTAGV obtained in step c.1 above do not cycle through 0, 1, 2, 3, 0, 1, 2, 3, starting at any one of these numbers (0, or 1, or 2 or 3). Set a Downstage Fault Monitor Error bit in Fault Data Word 4 if a false state is not obtained for the Stage 1 Fault Monitor in step c.1.

(2) Set a null error bit for Stage 2 in Fault Data Word 4 if any of the averages obtained in step c. are not within the following:

V21_AVGN =-.114 ± .342 volts, V22_AVGN =-.114 ± .342 volts,
V23_AVGN =-.114 ± .342 volts, V24_AVGN =-.114 ± .342 volts.

Set the Computer Failure MOSR as an alarm if five successive samples of the IDTAGV obtained in step c.1 above do not cycle through 4, 5, 6, 7, 4, 5, 6, 7, starting at any one of these numbers (4, or 5, or 6 or 7). Set a Downstage Fault Monitor Error bit in Fault Data Word 4 if a false state is not obtained for the Stage 2 Fault Monitor in step c.1.

(3) Set a null error bit for Stage 3 in Fault Data Word 4 if any of the averages obtained in step c. are not within the following:

V31_AVGN =-.114 ± .342 volts, V32_AVGN =-.114 ± .342 volts,
V33_AVGN =-.114 ± .342 volts, V34_AVGN =-.114 ± .342 volts.

Set the Computer Failure MOSR as an alarm if five successive samples of the IDTAGV obtained in step c.1 above do not cycle through 8, 9, 10, 11, 8, 9, 10, 11, starting at any one of these numbers (8, or 9, or 10 or 11). Set a Downstage Fault Monitor Error bit in Fault Data Word 4 if a false state is not obtained for the Stage 3 Fault Monitor in step c.1.

e. Perform step 1. Below for Stage 1 Actuator Response Test, or step 2. below for Stage 2 Actuator Response Test, or step 3. below for Stage 3 Actuator Response Test.

(1) Set TVC_CMD_4(I) = -4.032 (degrees), where I = 1, 2, 3, 4. All commands shall be set prior to their use in Thrust Vector Control processing and within a two msec period.

(2) Set TVC_CMD_4(I) = 2.16 (degrees), where I = 1, 2, 3, 4. All commands shall be set prior to their use in Thrust Vector Control processing and within a two msec period.

(3) Perform the following sequence of steps:

(a) Issue Flight Control Select/Event Markers command. Obtain the Flight Control Select/Event Markers and verify correct readback response. Set the Computer Failure MOSR as an alarm for any incorrect responses.

(b) Set TVC_CMD_4(I) = 1.72546 (degrees), where I = 1, 2, 3, 4. All commands shall be set prior to their use in Thrust Vector Control processing and within a two msec period.

(c) Delay a minimum of 80 msec after step (b) and obtain four Position Feedback samples after successive TVC Initiate interrupts. Each Position Feedback shall be processed as follows:

(1) Set IDTAAGV = POSFDBK(12:15), and POSFDBKV = POSFDBK(0:11).

(2) The processing of ADC Output Compensation shall be performed for POSFDBKV.

(3) Get the compensated feedback voltage by performing the following calculation:

POSFDBKVV = {ADCSC (obtained for POSFDBKV) / 204.8} (volts)

(d) Set the Computer Failure (COMPUTER_F) as an alarm if any of the four POSFDBKVV of step (c)(3) above is not within the following:

POSFDBKVV > -0.9 volts

(e) Issue Flight Control Select/Event Markers command.

(f) Obtain the Flight Control Select/Event Markers and verify correct readback response to test pattern 3 of Table 2-16. Set the Computer Failure MOSR as an alarm for any incorrect responses.

f. Perform step 1. below for Stage 1 Actuator Response Test, or step 2. below for Stage 2 Actuator Response Test, or step 3. below for Stage 3 Actuator Response Test.

(1) Sample the Stage 1 Fault Monitor for a true state between 20 and 30 msec following the setting of the commands in step e.1.

(2) Sample the Stage 2 Fault Monitor for a true state between 20 and 30 msec following the setting of the commands in step e.2.

(3) Sample the Stage 3 Fault Monitor for a true state between 20 and 30 msec following the setting of the commands in step e.3.

g. Perform step 1. below for Stage 1 Actuator Response Test, or step 2. below for Stage 2 Actuator Response Test, or step 3. below for Stage 3 Actuator Response Test.

(1) Set a Downstage Fault Monitor Error bit in Fault Data Word 4 if a true state is not obtained for the Stage 1 Fault Monitor in step f.1.

(2) Set a Downstage Fault Monitor Error bit in Fault Data Word 4 if a true state is not obtained for the Stage 2 Fault Monitor in step f.2.

(3) Set a Downstage Fault Monitor Error bit in Fault Data Word 4 if a true state is not obtained for the Stage 3 Fault Monitor in step f.3.

h. Perform step 1. below for Stage 1 Actuator Response Test, or step 2. below for Stage 2 Actuator Response Test, or step 3. below for Stage 3 Actuator Response Test.

(1) Get the combined actuator rate voltage as follows:

(a) Obtain one voltage sample of each of the four actuator Position Feedback at 76 ± 1.5 msec following the TVC Initiate interrupt that commences Thrust Vector Control processing of the command set in step e.1.

(b) Process and save POSFDBKVV into compensated feedback voltage variables listed below, based on IDTAGV, as follows:

if IDTAGV = 0, set V11(18) = POSFDBKVV
(Stage 1 Nozzle 1), or
if IDTAGV = 1, set V12(18) = POSFDBKVV
(Stage 1 Nozzle 2), or
if IDTAGV = 2, set V13(18) = POSFDBKVV
(Stage 1 Nozzle 3), or
if IDTAGV = 3, set V14(18) = POSFDBKVV
(Stage 1 Nozzle 4).

(c) Calculate the Combined Actuator Rate Voltage for Stage 1 (VCARSTG1) as follows:

VCARSTG1 = V11(18) + V12(18) + V13(18) + V14(18)

(2) Get the combined actuator rate voltage as follows:

(a) Obtain one voltage sample of each of the four actuator Position Feedback at 76 ± 1.5 msec following the TVC Initiate interrupt that commences Thrust Vector Control processing of the command set in step e.2.

(b) Process and save POSFDBKVV into compensated feedback voltage variables listed below, based on IDTAGV, as follows:

if IDTAGV = 7, set V21(18) = POSFDBKVV
(Stage 2 Pintle 4), or
if IDTAGV = 6, set V22(18) = POSFDBKVV
(Stage 2 Pintle 3), or
if IDTAGV = 5, set V23(18) = POSFDBKVV
(Stage 2 Pintle 2), or
if IDTAGV = 4, set V24(18) = POSFDBKVV
(Stage 2 Pintle 1).

(c) Calculate the Combined Actuator Rate Voltage for Stage 2 (VCARSTG2) as follows:

VCARSTG2 = V21(18) + V22(18) + V23(18) + V24(18)

(3) Get the combined actuator rate voltage as follows:

(a) Obtain one voltage sample of each of the four actuator Position Feedback at 76 ± 1.5 msec following the command set in step e.3(e) above.

(b) Process and save POSFDBKVV into compensated feedback voltage variables listed below, based on IDTAGV, as follows:

if IDTAGV = 11, set V31(18) = POSFDBKVV
(Stage 3 Pintle 4), or
if IDTAGV = 10, set V32(18) = POSFDBKVV
(Stage 3 Pintle 3), or
if IDTAGV = 9, set V33(18) = POSFDBKVV
(Stage 3 Pintle 2), or
if IDTAGV = 8, set V34(18) = POSFDBKVV
(Stage 3 Pintle 1).

(c) Calculate the Combined Actuator Rate Voltage for Stage 3 (VCARSTG3) as follows:

VCARSTG3 = V31(18) + V32(18) + V33(18) + V34(18)

i. Perform step 1. below for Stage 1 Actuator Response Test, or step 2. below for Stage 2 Actuator Response Test, or step 3. below for Stage 3 Actuator Response Test.

(1) Set an Actuator Rate Error bit in Fault Data Word 4 if the results of step h.1.(d) above is not within the following:

$$6.942308 \leq |\text{VCARSTG1}| \leq 37.12308 \text{ (volts)}$$

(2) Set an Actuator Rate Error bit in Fault Data Word 4 if the results of step h.2.(d) above is not within the following:

$$10.716 \leq |\text{VCARSTG2}| \leq 38.912 \text{ (volts)}$$

(3) Set an Actuator Rate Error bit in Fault Data Word 4 if the results of step h.3.(d) above is not within the following:

$$14.82 \leq |\text{VCARSTG3}| \leq 38.912 \text{ (volts)}$$

j. Obtain the Fault Monitor of the stage selected and a 17 sample steady state extended feedback voltage average for each of the four actuator feedbacks selected as follows:

(1) Obtain 17 Position Feedback samples for each of the four actuator feedbacks selected after successive TVC Initiate interrupts beginning 274.5 ± 4 msec following step e.1. for Stage 1 Actuator Response Test, or step e.2. for Stage 2 Actuator Response Test, or step e.3(e). for Stage 3 Actuator Response Test.

(2) Process and save POSFDBKVV into compensated feedback voltage variables listed in step (a) below for Stage 1 Actuator Response Test, or step (b) below for Stage 2 Actuator Response Test, or step (c) below for Stage 3 Actuator Response Test, based on IDTAGV, as follows:

(a) if IDTAGV = 0, set V11(I) = POSFDBKVV (Stage 1 Nozzle 1), or
if IDTAGV = 1, set V12(I) = POSFDBKVV (Stage 1 Nozzle 2), or
if IDTAGV = 2, set V13(I) = POSFDBKVV (Stage 1 Nozzle 3), or
if IDTAGV = 3, set V14(I) = POSFDBKVV (Stage 1 Nozzle 4),
where I=19 to 35.

(b) if IDTAGV = 7, set V21(I) = POSFDBKVV

(Stage 2 Pintle 4), or
if IDTAGV = 6, set V22(I) = POSFDBKVV
(Stage 2 Pintle 3), or
if IDTAGV = 5, set V23(I) = POSFDBKVV
(Stage 2 Pintle 2), or
if IDTAGV = 4, set V24(I) = POSFDBKVV
(Stage 2 Pintle 1),
where I=19 to 35.

(c) if IDTAGV = 11, set V31(I) = POSFDBKVV
(Stage 3 Pintle 4), or
if IDTAGV = 10, set V32(I) = POSFDBKVV
(Stage 3 Pintle 3), or
if IDTAGV = 9, set V33(I) = POSFDBKVV
(Stage 3 Pintle 2), or
if IDTAGV = 8, set V34(I) = POSFDBKVV
(Stage 3 Pintle 1),
where I=19 to 35.

(3) Get the steady state extended feedback voltage average by performing step (a) below for Stage 1 Actuator Response Test, or step (b) below for Stage 2 Actuator Response Test, or step (c) below for Stage 3 Actuator Response Test.

(a) set V11_AVGE, V12_AVGE, V13_AVGE, V14_AVGE to the average of [V11], [V12], [V13], and [V14] for I=19 to 35, respectively.

(b) set V21_AVGE, V22_AVGE, V23_AVGE, V24_AVGE to the average of [V21], [V22], [V23], and [V24] for I=19 to 35, respectively.

(c) set V31_AVGE, V32_AVGE, V33_AVGE, V34_AVGE to the average of [V31], [V32], [V33], and [V34] for i=19 to 35, respectively.

k. Perform step 1. below for Stage 1 Actuator Response Test, or step 2. below for Stage 2 Actuator Response Test, or step 3. below for Stage 3 Actuator Response Test. Set a Downstage Fault Monitor error bit in Fault Data Word 4 if a false state is not obtained for the appropriate stage monitor.

(1) Set a Steady State Extended Error bit in Fault Data Word 4 if any of the averages obtained in step j.3.(a) are not within the following:

V11_AVGE = 4.60385 ± .438462 volts,
V12_AVGE = 4.60385 ± .438462 volts,

V13_AVGE = 4.60385 ± .438462 volts,
V14_AVGE = 4.60385 ± .438462 volts.

(2) Set a Steady State Extended Error bit in Fault Data Word 4 if any of the averages obtained in step j.3.(b) are not within the following:

V21_AVGE = -4.788 ± .456 volts, V22_AVGE = -4.788 ± .456 volts,
V23_AVGE = -4.788 ± .456 volts, V24_AVGE = -4.788 ± .456 volts.

(3) Set a Steady State Extended Error bit in Fault Data Word 4 if any of the averages obtained in step j.3.(c) are not within the following:

V31_AVGE = -7.676 ± .76 volts, V32_AVGE = -7.676 ± .76 volts,
V33_AVGE = -7.676 ± .76 volts, V34_AVGE = -7.676 ± .76 volts.

l. Perform step 1. below for Stage 1 Actuator Response Test, or step 2. below for Stage 2 Actuator Response Test, or step 3. below for Stage 3 Actuator Response Test.

(1) Commence increments on one to four thrust vector commands of step e.1. to zero degree at a rate of 32 deg/sec, consisting of 63 increments of .064 degree within each successive two msec period. The command shall be set prior to its use in Thrust Vector Control processing.

(2) Commence decrements on one to four thrust vector commands of step e.2. to zero degree at a rate of 34.286 deg/sec, consisting of an initial decrement of .034268 degree, followed by 31 decrements of .068572 degree within each successive two msec period. The command shall be set prior to its use in Thrust Vector Control processing.

(3) Commence decrements on one to four thrust vector commands of step e.3.(b) to zero degree at a rate of 20.3 deg/sec, consisting of an initial decrement of .02026 degree, followed by 42 decrements of .0406 degree within each successive two msec period. The command shall be set prior to its use in Thrust Vector Control processing.

m. Perform step 1. below for Stage 1 Actuator Response Test, or step 2. below for Stage 2 Actuator Response Test, or step 3. below for Stage 3 Actuator Response Test.

(1) When the incrementing command of step l.1. is set to zero degree, perform the following:

(a) Obtain a sample of the actuator Position Feedback associated with the increment command output of step l.1. (i.e. if nozzle 1 command is incrementing, obtain the sample which has IDTAG = 0, etc...) during the 0.25 msec period after the TVC Initiate Interrupt that commences Thrust Vector Control processing of the zero degree command and perform the following:

(1) Process and save the compensated feedback voltage based on IDTAGV associated with the increment command output of step l.1., as follows:

if IDTAGV = 0, set V11(i) = POSFDBKVV (Stage 1 Nozzle 1), or
if IDTAGV = 1, set V12(i) = POSFDBKVV (Stage 1 Nozzle 2), or
if IDTAGV = 2, set V13(i) = POSFDBKVV (Stage 1 Nozzle 3), or
if IDTAGV = 3, set V14(i) = POSFDBKVV (Stage 1 Nozzle 4), where I=36.

(b) Obtain a sample of the actuator Position Feedback associated with the increment command output of step l.1. (i.e. if nozzle 1 command was incremented, obtain the sample which has IDTAG = 0, etc...) during the 0.25 msec period following the fourth TVC Initiate Interrupt occurring after step (a) above and perform the following:

(1) Process and save the compensated feedback voltage based on IDTAGV associated with the increment command output of step l.1, as follows:
if IDTAGV = 0, set V11(i) = POSFDBKVV (Stage 1 Nozzle 1), or
if IDTAGV = 1, set V12(i) = POSFDBKVV (Stage 1 Nozzle 2), or
if IDTAGV = 2, set V13(i) = POSFDBKVV (Stage 1 Nozzle 3), or
if IDTAGV = 3, set V14(i) = POSFDBKVV (Stage 1 Nozzle 4), where i=37.

(c) Set V11_LAG, V12_LAG, V13_LAG, V14_LAG to the average of [V11], [V12], [V13], and [V14] for i=36 to 37, respectively.

(2) When the decrementing command of step l.2. is set to zero degree, perform the following:

(a) Obtain a sample of the actuator Position Feedback associated with the decrement command output of step l.2. (i.e. if pintle 4 command is decrementing, obtain the sample which has IDTAG = 7, etc...) during the 0.25 msec period after the TVC Initiate Interrupt that commences Thrust Vector Control processing of the zero degree command and perform the following:

(1) Process and save the compensated feedback voltage based on IDTAGV associated with the decrement command output of step l.2., as follows:

if IDTAGV = 7, set V21(i) = POSFDBKVV (Stage 2 Pintle 4), or
if IDTAGV = 6, set V22(i) = POSFDBKVV (Stage 2 Pintle 3), or
if IDTAGV = 5, set V23(i) = POSFDBKVV (Stage 2 Pintle 2), or
if IDTAGV = 4, set V24(i) = POSFDBKVV (Stage 2 Pintle 1),
where I=36.

(b) Obtain a sample of the actuator Position Feedback associated with the decrement command output of step l.2. (i.e. if pintle 4 command was decremented, obtain the sample which has IDTAG = 7, etc...) during the 0.25 msec period following the fourth TVC Initiate Interrupt occurring after step (a) above and perform the following:

(1) Process and save the compensated feedback voltage based on IDTAGV associated with the decrement command output of step l.2., as follows:
if IDTAGV = 7, set V21(i) = POSFDBKVV (Stage 2 Pintle 4), or
if IDTAGV = 6, set V22(i) = POSFDBKVV (Stage 2 Pintle 3), or
if IDTAGV = 5, set V23(i) = POSFDBKVV (Stage 2 Pintle 2), or
if IDTAGV = 4, set V24(i) = POSFDBKVV (Stage 2 Pintle 1),
where I=37.

(c) Set V21_LAG, V22_LAG, V23_LAG, V24_LAG to the average of [V21], [V22], [V23], and [V24] for i=36 to 37, respectively.

(3) When the decrementing command of step i.3. is set to zero degree, perform the following:

(a) Obtain a sample of the actuator Position Feedback associated with the decrement command output of step i.3. (i.e. if pintle 4 command is decrementing, obtain the sample which has IDTAG = 11, etc...) during the 0.25 msec period after the TVC Initiate Interrupt that commences Thrust Vector Control 2-10.7.4 processing of the zero degree command and perform the following:

(1) Save the compensated feedback voltage based on IDTAGV associated with the decrement command output of step i.3., as follows:

if IDTAGV = 11, set V31(I) = POSFDBKVV (Stage 3 Pintle 4), or
if IDTAGV = 10, set V32(I) = POSFDBKVV (Stage 3 Pintle 3), or
if IDTAGV = 9, set V33(I) = POSFDBKVV (Stage 3 Pintle 2), or
if IDTAGV = 8, set V34(I) = POSFDBKVV (Stage 3 Pintle 1), where I=36.

(b) Obtain a sample of the actuator Position Feedback associated with the decrement command output of step i.3. (i.e. if pintle 4 command is decrementing, obtain the sample which has IDTAG = 11, etc...) during the 0.25 msec period following the fourth TVC Initiate Interrupt occurring after step (a) above and perform the following:

(1) Save the compensated feedback voltage based on IDTAGV associated with the decrement command output of step i.3., as follows:

if IDTAGV = 11, set V31(I) = POSFDBKVV (Stage 3 Pintle 4), or
if IDTAGV = 10, set V32(I) = POSFDBKVV (Stage 3 Pintle 3), or
if IDTAGV = 9, set V33(I) = POSFDBKVV (Stage 3 Pintle 2), or
if IDTAGV = 8, set V34(I) = POSFDBKVV (Stage 3 Pintle 1), where I=37.

(c) Set V31_LAG, V32_LAG, V33_LAG, V34_LAG to the average of [V31], [V32], [V33], and [V34] for I=36 to 37, respectively.

n. Perform step 1. below for Stage 1 Actuator Response Test, or step 2. below for Stage 2 Actuator Response Test, or step 3. below for Stage 3 Actuator Response Test.

(1) Set the actuator lag error bits in Fault Data Word 4 if any of the samples obtained in step m.1 is not within the following:

V11_LAG = 1.534615 ± .511538 volts,
V12_LAG = 1.534615 ± .511538 volts,
V13_LAG = 1.534615 ± .511538 volts,
V14_LAG = 1.534615 ± .511538 volts.

(2) Set the actuator lag error bits in Fault Data Word 4 if any of the samples obtained in step m.2. is not within the following:

V21_LAG = -2.812 ± .836 volts, V22_LAG = -2.812 ± .836 volts,
V23_LAG = -2.812 ± .836 volts, V24_LAG = -2.812 ± .836 volts.

(3) Set the actuator lag error bits in Fault Data Word 4 if any of the samples obtained in step m.3. is not within the following:

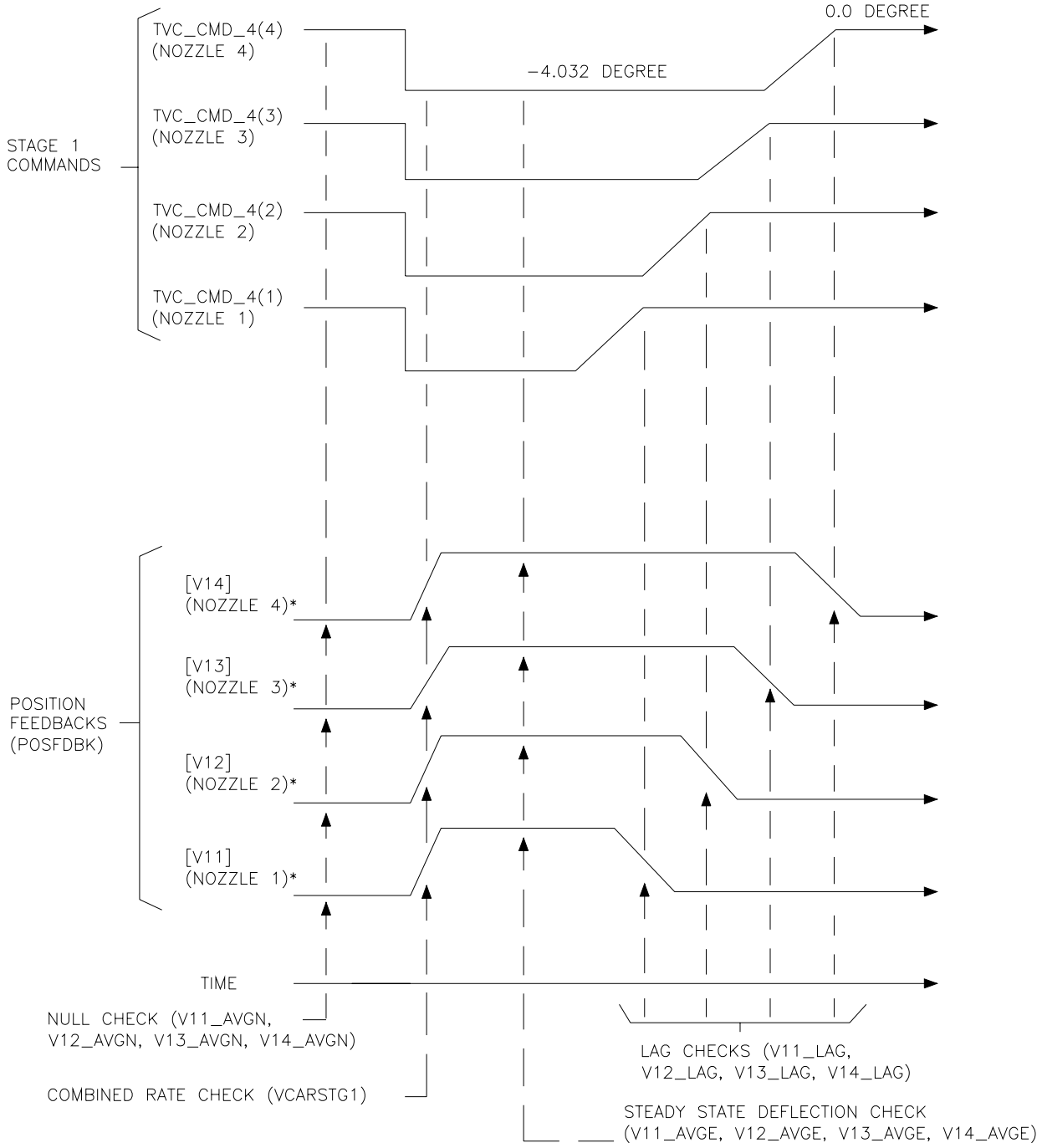
V31_LAG = -2.964 ± .76 volts, V32_LAG = -2.964 ± .76 volts,
V33_LAG = -2.964 ± .76 volts, V34_LAG = -2.964 ± .76 volts.

o. Repeat steps I. through n. for each of the respective commands, before proceeding to step p.

p. Repeat steps b. through o. for each stage (Stage 1, 2, and 3). Issue Flight Control Select/Event Markers command shown in test pattern 5 of Table 2-15. Obtain the Flight Control Select/Event Markers and verify correct readback response to test pattern 5 of Table 2-15. Set the Computer Failure MOSR as an alarm for any incorrect responses. The Stage 2 actuator error signal commands shall be set at least one time to minus 28 counts (minus 20% PWM) when the ID Tag of the Position Feedback register is either 0, 1, 2 or 3. Upon completion of this test any of the following fault data bits, saved in Fault Data Word 4, if set, shall set the Downstage Control Failure MOSR as follows:

Fault Data	Downstage Control Failure MOSR
Null error bit for any stage	Set
Downstage Fault monitor error bit for any stage	-
Actuator Rate error bit for any stage	Set
Steady State Extended error bit for any stage	Set
Lag error bit for any stage and any actuator	Set

q. If the Downstage Actuator Response Test (all steps above) does not complete, set Computer Failure MOSR alarm.



* NOZZLE 1 = IDTAGV 0, NOZZLE 2 = IDTAGV 1, NOZZLE 3 = IDTAGV 2, NOZZLE 4 = IDTAGV 3

SOURCE: S−133−19251

MMT201_176k

Figure 2-21. Downstage Actuator Test Sequence (Sheet 1 of 3)

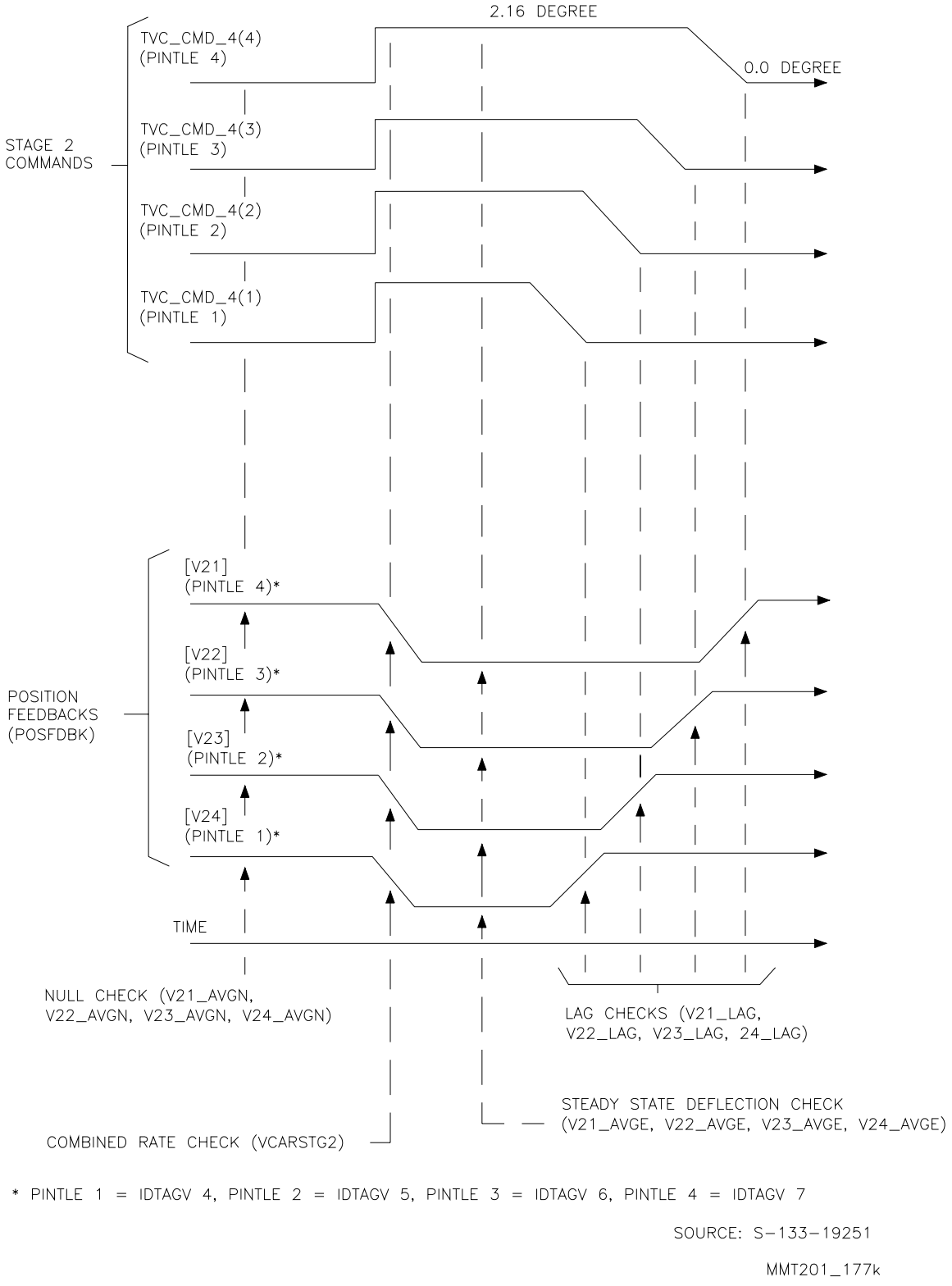
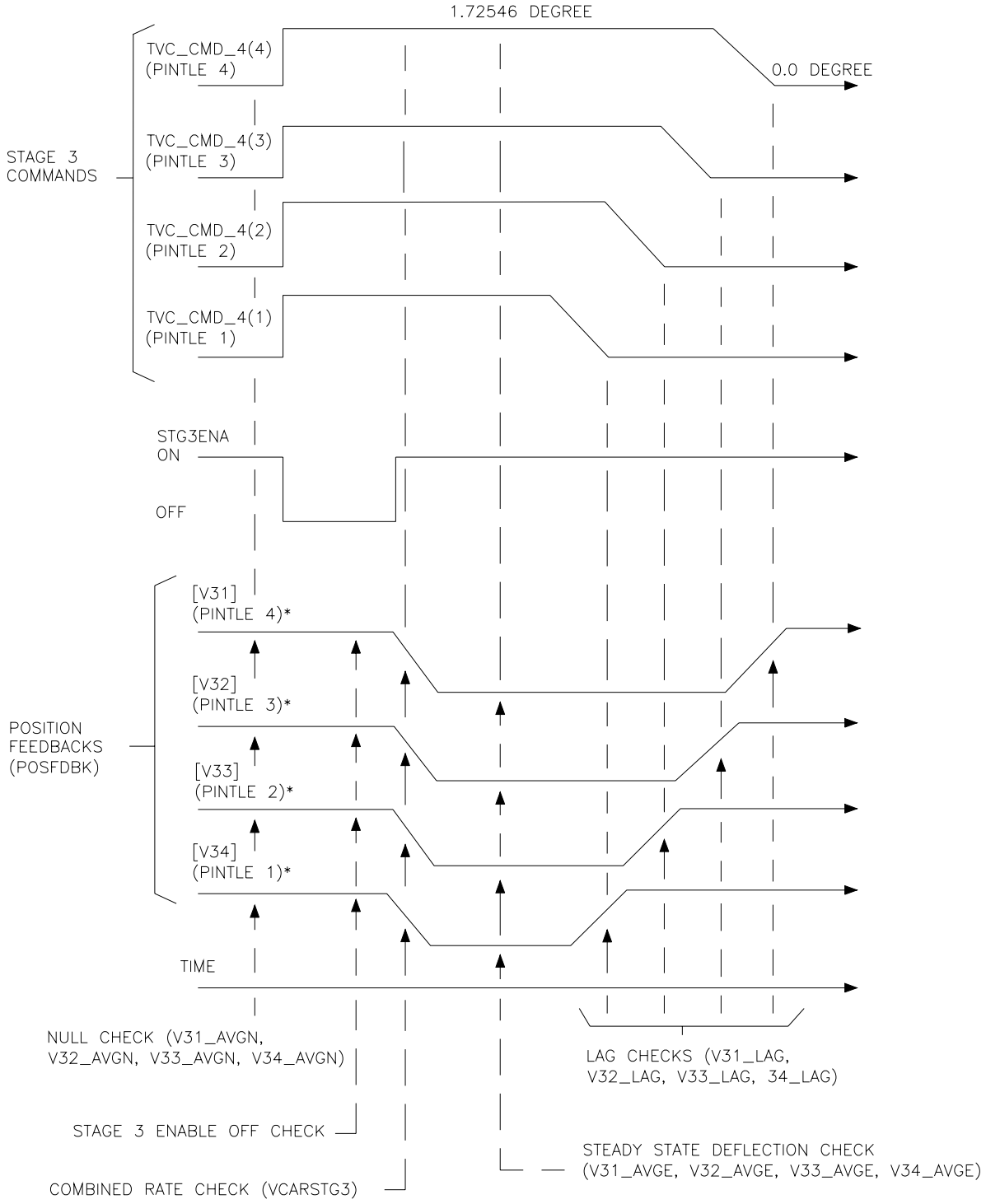


Figure 2-21. Downstage Actuator Test Sequence (Sheet 2 of 3)



* PINTLE 1 = IDTAGV 8, PINTLE 2 = IDTAGV 9, PINTLE 3 = IDTAGV 10, PINTLE 4 = IDTAGV 11

SOURCE: S-133-19251

MMT201_178k

Figure 2-21. Downstage Actuator Test Sequence (Sheet 3 of 3)

Table 2-15. Flight Control Select/Event Markers Commands for Downstage Actuator Response Test

SYMBOL	FUNCTION	FLIGHT CONTROL SELECT/ EVENT MARKERS (020E) BIT(S)	TEST PAT-TERN *	TEST PAT-TERN *	TEST PAT-TERN *	TEST PAT-TERN *	TEST PAT-TERN *
			1	2	3	4	5
N/A		0-3	x	x	x	x	x
N/A		4	x	x	x	x	x
EVNTMARKER	Event Marker #1 - MSB	5	0	0	0	0	0
EVNTMARKER	Event Marker #2	6	0	0	0	0	0
EVNTMARKER	Event Marker #3	7	0	1	1	0	0
EVNTMARKER	Event Marker #4 - LSB	8	1	0	1	0	0
TRNDUCXENA	Transducer Excitation Enable	9	0	0	0	0	1
ADCCYCSEL	ADC Cycle Select - MSB	10	0	0	1	0	0
ADCCYCSEL	ADC Cycle Select - LSB	11	0	1	0	0	0
STG1ENA	Stage 1 Command Enable	12	1	1	1	1	1
STG2ENA	Stage 2 Command Enable	13	1	1	1	1	1
STG3ENA	Stage 3 Command Enable	14	0	0	1	0	0
STG4ENA	PBPS Actuator Command Enable	15	0	0	0	0	0
* x bits (0-4) are unassigned and shall be commanded 0.							

2-10.10.2. Roll Valves Test. The Stages 2 and 3 Roll Valves Test consist of obtaining valve responses of clockwise movements when commanded with a clockwise command and counterclockwise movement when commanded with a counterclockwise command. The absence of both Stage 2 and Stage 3 roll control commands result in no indicated roll valve movement. If any of the responses are incorrect, the appropriate Stage 2 Roll Control Failure and/or Stage 3 Roll Control Failure MOSR are set. The following steps shall be performed for each stage:

a. The following shall be performed:

(1) The appropriate stage shall be selected and controlled as follows:

(a) Set [TVC_CMD_4] = [0]

(b) Perform step (1) below for Stage 2 Roll Valves Test, or step (2) below for Stage 3 Roll Valves Test.

(1) Issue Flight Control Select/Event Markers command shown in test pattern 1 of Table 2-16. Obtain the Flight Control Select/Event Markers and verify correct readback response to test pattern 1. Set the Computer Failure) MOSR as an alarm for any incorrect responses. (Note: During the Stage 2 Roll Valves Test, Stage 1 Nozzles and Stage 2 Injectors are also being controlled).

(2) Issue Flight Control Select/Event Markers command shown in test pattern 2 of Table 2-16. The Stage 2 actuator error signal commands shall be set to minus 28 counts (minus 20% PWM). Obtain the Flight Control Select/Event Markers and verify correct readback response to test pattern 2. Set the Computer Failure MOSR as an alarm for any incorrect responses. (Note: During the Stage 3 Roll Valves Test, Stage 1 Nozzles, Stage 2 Injectors, and Stage 3 Injectors are being controlled).

(c) Perform the processing of Thrust Vector Control when TVC Initiate interrupt occurs.

(2) Issue a roll command clockwise or counterclockwise by performing step (a) below for Stage 2 Roll Valves Test, or step (b) below for Stage 3 Roll Valves Test.

(a) Command Stage 2 roll clockwise by setting true Stage 2 Plus Roll (CW) and setting false Stage 2 Minus Roll (CCW), or

counterclockwise by setting true Stage 2 Minus Roll (CCW) and setting false Stage 2 Plus Roll (CW). Obtain the Stage 2 Roll Command. Verify that the appropriate commands are set and reset. Set the Computer Failure MOSR as an alarm for any incorrect responses.

(b) Command Stage 3 roll clockwise by setting true Stage 3 Plus Roll (CW) and setting false Stage 3 Minus Roll (CCW), or counterclockwise by setting true Stage 3 Minus Roll (CCW) and setting false Stage 3 Plus Roll (CW). Obtain the Stage 3 Roll Command. Verify that the appropriate commands are set and reset. Set the Computer Failure MOSR as an alarm for any incorrect responses.

b. Upon issuance of a roll command in step a.2, perform step 1. below for Stage 2 Roll Valves Test, or step 2. below for Stage 3 Roll Valves Test.

(1) The Stage Auxiliary Monitor 1 and the Stage Auxiliary Monitor 2 responses shall be obtained after a delay of 79 msec minimum.

(2) The Stage Auxiliary Monitor 1 response shall be obtained after a delay of 152.5 ± 2.5 msec.

c. Process and verify the roll response in step b. above / step h. below.

(1) Verify the following roll response:

(a) S2ROL1V < ±3 volts, for Stage 2 CCW roll and
(b) S2ROL2V < ±3 volts, for Stage 2 CCW roll, or
(c) S2ROL1V > ±6 volts, for Stage 2 CW roll and
(d) S2ROL2V > ±6 volts, for Stage 2 CW roll, or
(e) S3ROLV > ±3 volts, for Stage 3 CW roll, or
(f) S3ROLV < -3 volts, for Stage 3 CCW roll

(2) Verify IDTAGSA1V = 1 for Stage 2 Roll 1 Position Feedback and IDTAGSA2V = 1 for Stage 2 Roll 2 Position Feedback, or IDTAGSA1V = 2 for Stage 3 Roll Position Feedback. Set the Computer Failure MOSR as an alarm for any incorrect responses.

d. Set the following Roll Control Failure if the roll response in step c.1 is not within the specified limits:

(1) Set the Stage 2 Roll Control Failure MOSR if step c.1.(a), c.1.(b), c.1.(c), or c.1.(d) is beyond specified limits.

(2) Set the Stage 3 Roll Control Failure MOSR if step c.1.(e) or c.1.(f) is beyond specified limits.

e. Reset to false the roll command that has been set true in step a.2 above / step h. below. Obtain the Stage 2 Roll Command for Stage 2 Roll Valves Test, or the Stage 3 Roll Command for Stage 3 Roll Valves Test. Verify that the appropriate commands are reset. Set the Computer Failure MOSR as an alarm for any incorrect responses. Upon issuance of the reset command, perform step 1. below for Stage 2 Roll Valves Test, or step 2. below for Stage 3 Roll Valves Test.

(1) The Stage Auxiliary Monitor 1 and the Stage Auxiliary Monitor 2 responses shall be obtained after a delay of 45 ± 6 msec.

(2) The Stage Auxiliary Monitor 1 response shall be obtained after a delay of 152.5 ± 2.5 msec for Stage 3 Roll Feedback.

f. For Stage 3 Roll Valves Test only, process the roll response and verify S3ROLV = 0.0 ± 1.2 volts.

g. Set the Stage 3 Roll Control Failure MOSR if step f. is beyond specified limits.

h. Set true the previously false set roll command and set false the previously true set roll command of step a.2 of the stage under test. For Stage 2 Roll Valves Test, obtain the Stage 2 Roll Command, verify that the appropriate commands are set and reset, and set the Computer Failure MOSR as an alarm for any incorrect responses. For Stage 3 Roll Valves Test, obtain the Stage 3 Roll Command, verify that the appropriate commands are set and reset, and set the Computer Failure MOSR as an alarm for any incorrect responses. Upon issuance of the roll command, perform step 1. below for Stage 2 Roll Valves Test, or step 2. below for Stage 3 Roll Valves Test.

(1) The Stage Auxiliary Monitor 1 and the Stage Auxiliary Monitor 2 responses shall be obtained after a delay of 45 ± 6 msec.

(2) The Stage Auxiliary Monitor 1 response shall be obtained after a delay of 152.5 ± 2.5 msec.

i. Repeat steps c., d., e., f., g., and h. After all (CW and CCW) Stage 2 and Stage 3 Roll Commands have been tested and the final iteration step g. is done, perform step j.

j. Issue Flight Control Select/Event Markers command shown in test pattern 3 of Table 2-16. Obtain the Flight Control Select/Event Markers and verify correct readback response to test pattern. Set the Computer Failure MOSR

as an alarm for any incorrect responses. The Stage 2 actuator error signal commands shall be set at least one time to minus 28 counts (minus 20% PWM) when the ID Tag of the Position Feedback register is either 0, 1, 2 or 3, and exit this test.

Table 2-16. Flight Control Select/Event Markers Commands for Stage 2 and 3 Roll Valves Test

SYMBOL	FUNCTION	FLIGHT CONTROL SELECT/ EVENT MARKERS (020E) BIT(S)	TEST PAT-TERN * 1	TEST PAT-TERN * 2	TEST PAT-TERN * 3
N/A		0-3	x	x	x
N/A		4	x	x	x
EVNTMARKER	Event Marker #1 - MSB	5	0	0	0
EVNTMARKER	Event Marker #2	6	1	0	0
EVNTMARKER	Event Marker #3	7	0	1	0
EVNTMARKER	Event Marker #4 - LSB	8	0	0	0
TRNDUCXENA	Transducer Excitation Enable	9	0	0	0
ADCCYCSEL	ADC Cycle Select - MSB	10	0	1	0
ADCCYCSEL	ADC Cycle Select - LSB	11	1	0	0
STG1ENA	Stage 1 Command Enable	12	1	1	1
STG2ENA	Stage 2 Command Enable	13	1	1	1
STG3ENA	Stage 3 Command Enable	14	0	1	0
STG4ENA	PBPS Actuator Command Enable	15	0	0	0
* x bits (0-4) are unassigned and shall be commanded 0.					

2-10.11. Flight Control Ground Power Removal. The F/C Ground Power Reset character output code shall be commanded in accordance with F/C Power ON/OFF Cycle.

2-10.12. Circumvention Reset Detection. After completion of all Missile Test sub-tests, except for Circumvention Reset System Test, the Circumvention Reset Indicator shall be monitored to determine if a circumvention reset event occurred. The following action shall result:

a. Circumvention Reset Indicator sensed in the false state shall cause the Circumvention Reset System Test to be performed.

b. Circumvention Reset Indicator sensed in the true state shall cause Missile Test Exit Processing and the Missile Test recovery processing of Circumvention Reset/Nuclear Detection and Recovery to be performed.

2-10.13. Circumvention Reset System Test. The Circumvention Reset System Test shall verify that that the system is capable of recovering from a simulated circumvention reset event by the performance of the following sub-paragraphs:

2-10.13.1 Circumvention Reset System Test. After all other Missile Test sub-tests, the Circumvention Reset (C/R) System Test shall be performed as follows:

a. Assure that the following items are initiated prior to executing the Circumvention Reset (C/R) Test Initiate command:

(1) Set CO Code Interface Test true by issuing Ground Ordnance Interlock Clear (Test 1) and another character output code which is not the reset for Ground Ordnance Interlock Clear (Test 1).

(2) AVE No-Go Set shall be issued.

(3) Coupler No-Go Set shall be issued.

(4) Coupler Test Set shall be issued prior to the initiation of the AVE No-Go and the Coupler No-Go commands.

(5) Multiplexer Status Set selected is not A, B, or F.

b. Issue the C/R Test Initiate command.

c. Allow at least 18 msec from the execution of step b. and sample the Circumvention Reset Indicator for a true state, without issuing the Status Set A command.

d. Issue the Status Set F command following a minimum delay of 31 msec from the execution of step b. and interrogate the following monitors as specified:

(1) Coupler Test false.

(2) Critical Status Override true.

(3) AVE No-Go false.

(4) Coupler No-Go false.

(5) CO Code Interface Test false.

e. Issue the Status Set H command following a minimum delay of 31 msec from the execution of step b. and interrogate the CSD(M) Drive Enable for a true state.

f. Any incorrect responses obtained shall be processed as follows:

(1) The G&C Coupler Control Monitor Failure MOSR shall be reported if the results of step c. and d. 1. through d. 4. are not in the states specified.

(2) The Programmer Group Failure MOSR shall be reported if the result of step d. 5. is true.

(3) The CSD(M) Drive Enable Failure MOSR shall be reported if the result of step e. is false.

g. The following operations shall be performed prior to exit from Missile Test:

(1) Issue the reset for Circumvention Reset Test Initiate.

(2) Issue the AVE No-Go Reset and Coupler No-Go Reset.

(3) Issue the Coupler Test Reset after step g. 2. has been performed.

(4) Issue the Critical Status Override Reset.

(5) Issue the Circumvention Reset Indicator Reset.

(6) Issue the Auxiliary Status Enable Set within 380 msec after issuing the Circumvention Reset Test Initiate code, unless the DCU is ready to receive an input message within 56 msec after issuing the Circumvention Reset Test Initiate code.

(7) Reissue the Ground Ordnance Alarm Set if the Ground Ordnance Alarm was true prior to initiating the Circumvention Reset System Test, and was true as a result of a Ground Ordnance Discretes Test Failure occurring after the last acceptance of the Missile Test Command.

2-10.14. Safety Control Switch Test in Missile Test. This test shall arm and reset the Safety Control Switch (SCS) during Remote Missile Test. The following test shall be bypassed if Missile Test is performed during the Local Communications mode. The following functions shall be performed:

a. Assure that the CSD(M) Home Monitor and CSD(G) Home monitor are true and that the Programmer Group Monitor Failure is false.

b. Issue Critical Circuits Enable.

c. Issue SCS Safe Reset followed by SCS Arm Set.

d. After a delay of at least 500 msec after issuing SCS Arm Set (item c. above) issue SCS Arm Reset.

e. Monitor SCS Armed status. If true, cause SCS Armed to be set in the MOSR.

f. Reset Critical Circuits Enable.

g. After a delay of at least 2.4 seconds after issuing SCS Arm Set (step c. above) issue SCS Safe Set.

h. After a delay of at least 500 msec after issuing SCS Safe Set (step g. above) issue SCS Safe Reset.

2-10.15. Nuclear Event Detectors Test. The following shall be performed to verify that the DCU and MGSC radiation detectors are functioning properly and can provide a nuclear event detection indication to the DCU and that the DCU nuclear event recovery logic is working correctly:

a. Initiate each of the two DCU Nuclear Event Detectors one at a time and verify that activation of each Nuclear Event Detector (NED) results in an DCU Nuclear Environment Protection (NEP) Interrupt. If either one of the interrupts do not occur, set the Nuclear Event Detector Failure MOSR, as an alarm. Reset the NEP Detector Test bits in the UIO Discrete Output Register within ten msec after setting them true and prior to initiating the next NED test signal.

b. Issue a MGSC NED Test Command to the MGSC via the DCU/MGSC serial channel and verify that it results in a DCU NEP Interrupt. If the DCU NEP Interrupt does not occur, set the Nuclear Event Detector Failure bit MOSR as an alarm. Reissue Level Detector 1 to the MGSC via the DCU/MGSC serial channel within ten msec after issuing the MGSC NED Test Command.

c. If all three tests of the NEDs in steps a. and b., above, fail to result in a NEP Interrupt, discontinue the remainder of NED Test and enter standby no-go at the end of Missile Test. If Missile Test was entered from standby no-go, discontinue the remainder of the NED Test. Otherwise, set the DCU internal Critical Leads Disconnect discrete true, to simulate flight mode, and perform the following:

(1) Initialize the following interfaces as specified below:

(a) DCU UIO Module - Issue RS Ordnance Enable.

(b) DCU FOIO Module - Issue PIOs to set the following bits true in the FOIO registers:

(1) Critical Circuits Enable.

(2) Ordnance Downstage Spare No. 1.

(c) MGSC - Issue ADC Spare Channel Select for XY-YZ Gyro Caging Pickoff via the DCU to MGSC serial channel. Note: Do not initiate any further DCU to MGSC serial channel transfers prior to performing step c. 5. (b), below.

(2) Verify that the interfaces in step c. 1, above, have been initialized correctly as follows:

(a) Read back the R/S Ordnance Enable bit of the UIO Discrete Output Register, the Critical Circuits Enable bit of the FOIO Ordnance Enable register, and the Ordnance Downstage Spare No. 1 bit of the FOIO Ordnance Commands register, and verify that they are all true. If any bit is false, set the Computer Failure MOSR as an alarm.

(b) Read back MGSC to DCU serial channel word 17 and verify that XY-YZ Gyro Caging Pickoff ADC Spare Channel is selected. If it is incorrect, set the IMU Servo Failure MOSR as an alarm.

(3) Initiate one of the NEDs successfully tested in steps a. or b., above, after performing step c. 2. (b), above, and prior to or with the next serial channel transfer from the DCU to the MGSC.

(4) Verify that the NEP Time Done Interrupt occurs after the NEP Interrupt, with a delay that is equal (± 30 microseconds) to the NEP timer value stored as part of the Flight Program Constants Tape data and loaded into the dedicated DCU NEP Timer Register during OGP Initialization + 10 microseconds. If the check fails, set the NED Failure MOSR as an alarm. After the NEP Time Done Interrupt occurred or should have occurred, issue a PIO to reset the following bits in the UIO Discrete Output Register:

(1) UIO Module NEP Detector Test false.

(2) Power Supply Driver Module NEP Detector Test false.

(5) After the NEP Time Done Interrupt check in 4, above, is completed, verify that the following interfaces are reset as specified below:

(a) Read back the R/S Ordnance Enable bit of the UIO Discrete Output register, the Critical Circuits Enable bit of the FOIO Ordnance Enable register, and the Ordnance Downstage Spare No. 1 bit of the FOIO Ordnance Commands register, and verify that they are all false. If any bit is true, set the NED Failure MOSR as an alarm. If all bits are true, set the NED Failure MOSR, and enter Standby no-go at the end of Missile Test.

(b) Prior to the next DCU to MGSC serial channel transfer, read back MGSC to DCU serial channel word 17 and verify that Roll Gimbal (Z) Demod Pickoff ADC Spare Channel is selected. If it is incorrect, set the NED Failure MOSR as an alarm.

(6) After the checks in 5, above, are performed restore DCU and MGSC digital interfaces to their pre-NEP states, as follows:

(a) UIO - Issue a PIO to set/reset the following bits in the UIO Discrete Output register:

(1) RS Ordnance Enable false.

(2) Compute Mode Indicator true.

(3) MGSC Servo Enable true.

(b) FOIO - Issue PIOs to reset the following bits in the FOIO registers:

(1) Ordnance Enable register, Critical Circuits Enable false.

(2) Ordnance Commands register, Ordnance Downstage Spare No. 1 false.

(3) Flight Control SELECT/EVENT marks register - all bits false

(c) Flight Control Select/Event Markers register - all bits false.

(d) MGSC - Issue the following via the serial channel from the DCU to the MGSC:

(1) Level Detector 1.

(2) Restore ADC Spare Channel Select to the last value prior to Missile Test.

(e) UIO - Restore the following UIO registers to their bit settings prior to the NED test.

(1) UIO Interrupt Mask Register.

(2) UIO Interrupt Enable/Disable.

(7) Reset the DCU internal Critical Leads Disconnect discrete.

d. If steps a., b., c. 4, c. 5. (a) and c. 5. (b), above, are all successfully completed, reset the NED Failure MOSR.

2-10.16. DCU Self Test. The following DCU Self Test functions shall be performed during Missile Test prior to Flight Control Ground Power Turn-on Test or after Flight Control Ground Power Removal. A failure in any of the following subtests except Critical Leads Disconnect subtest shall be indicated by storing a unique code in Self Test Failure Status to indicate the type of failure that occurred.

2-10.16.1. DCU CPU Subtest. The CPU subtest in DCU ROM memory shall be performed, with the following exceptions:

a. If a CPU subtest failure is detected, the DCU Self Test Failure Display Character Output shall not be issued and the Stop Mode shall not be entered.

b. If a CPU subtest failure is detected, the Computer Failure MOSR shall be set in the MOSR and standby no-go shall be entered at the end of Missile Test.

2-10.16.2. DCU Memory Subtest. The Memory subtest in DCU ROM memory shall then be performed, with the following exceptions:

a. If a Memory subtest failure is detected, the DCU Self Test Failure Display Character Output shall not be issued and the Stop Mode shall not be entered.

b. If a memory subtest failure is detected, the computer failure MOSR shall be set and standby no-go shall be entered at the end of missile test.

2-10.16.3. Deleted.

2-10.16.4. Critical Leads Disconnect Subtest. Provided that missile test was entered from Strategic Alert Biasing, the operation of the DCU internal Critical Leads Disconnect function shall be verified by performing the following sequence. If missile test was entered from standby no-go, the following test shall not be performed. During the test below, the Enable Write signal shall be enabled only during that portion of time devoted to the transfer of data to write protected memory.

a. Withhold the issuance of Keep Alive character output codes.

b. Verify that the Enable Write signal from the OGE is operating correctly by performing the following sequence 1.25 ± 0.05 seconds after the last issuance of the Keep Alive character output code (step a. above) and prior to setting the DCU internal Critical Leads Disconnect discrete true (step c. below).

(1) Issue the Enable Write Set character output code to allow storage of data in write-protected DCU memory.

(2) Attempt to store data to write-protected memory.

(3) If write-protected memory was altered, restore the original value. If write-protected memory was not altered, set the G&C Coupler Control Monitor Failure bit in the MOSR as an alarm.

(4) Issue the Enable Write Reset character output code.

c. Set the DCU internal Critical Leads Disconnect discrete true and issue the Enable Write Set character output code 1.35 ± 0.05 seconds after the last issuance of the Keep Alive character output code.

d. Attempt to store data to write protected memory. The resulting fault interrupt due to attempting to store in write-protected memory shall be masked or ignored.

e. If write protected memory was altered, restore the original value and set the Computer Failure MOSR as an alarm.

f. Issue the Enable Write Reset character output code.

g. Sample the Hardware Disable Discrete Monitor Feedback, Current GCA Mode Controls, Current PIGA Mode Controls, and Current Platform Mode Controls via the MGSC to DCU serial channel at least 1.65 ± 0.05 seconds after the last issuance of the Keep Alive character output code. If the current PIGA Mode Controls and/or the Current Platform Mode Controls are not set

to stable and/or the Current GCA Mode Controls is not set to Disable, set the IMU Servo Failure MOSR as an alarm. If Disable Discretes is detected false, set the G&C Coupler Control Monitor Failure bit in the MOSR as an alarm.

h. Resume issuance of Keep Alive character output codes 1.65 ± 0.05 seconds after issuance of the last Keep Alive character output code, and issue the Disable Discretes and Startup Indicator Reset character output code. Issue the Keep Alive character output code at least twice prior to step i. below.

i. Set the DCU internal Critical Leads Disconnect discrete false after resuming the issuance of Keep Alive character output codes.

j. If a Master Reset Interrupt occurs during Critical Leads Disconnect subtest, set the Computer Failure MOSR, terminate Missile Test, and perform Restart Alignment.

2-10.17. Exit Processing. A successful Missile Test shall result in the reset of all MOSR(s) applicable to Missile Test, except the SCS Armed MOSR will be reported for one MOSR for a successful SCS Test in Missile Test. An unsuccessful Missile Test is indicated by the setting of the various MOSR(s). In either case, any MOSR bit(s) shall not be altered as a result of bypassing the entire subtest(s) which normally sets/resets the MOSR bit(s). The following functions shall be performed and the applicable mode entered as defined in Exit Conditions.

a. The Test Complete indicator shall be set for one OSR.

b. The Auxiliary Status Enable Reset character output code shall be issued after acceptance of, but before response to, the first addressed interrogation except for RDIs during RDC In Process Mode to which a response will be made upon completion of a remote Missile Test.

c. Missile Test Timer shall be set for 30 minutes.

d. The LCF Address Time shall be reset to its minimum value.

2-10.17.1. Exit Conditions. Transition to another mode shall occur when conditions defined below exist.

a. Exit to critical no-go when the specific conditions specified in the CSD-G Test occur in the absence of a detected circumvention reset.

b. Exit to standby no-go as follows:

(1) Occurrence of CSD(G) Test Failure, or SCS Armed during SCS Arm Test, or Ground Ordnance Test Failure, in any combination, in the absence of a detected circumvention reset.

(2) Unless specifically excepted, exit to standby no-go upon occurrence of PSRE Control Failure, or Control and Discretes Unit Failure, or Downstage Discretes Failure, or R/S Discretes Failure, or PSRE Discretes Failure, or Downstage Control Failure, or Stage 2 Roll Control Failure, or Stage 3 Roll Control Failure, in any combination, without a F/C Power Failure and in the absence of a detected circumvention reset.

(3) Occurrence of Computer Failure as specified in DCU Self Test, or specified NED failure, in any combination.

(4) Missile test was entered from the standby no-go mode.

c. Exit to Initialization, upon occurrence of Master Reset in Missile Test.

d. Exit to Strategic Alert Biasing at the completion of Missile Test, or completion of CSD(G) Test where Circumvention Reset is detected if Missile Test entry was from Strategic Alert Biasing, and if steps a., b., or c., above, did not occur. Missile Test MOSR(s) that true set during the Missile Test in which a non-test circumvention reset (C/R) occurred, except the SCS Armed MOSR, shall not be reset during the test.

2-11. SENSITIVE COMMAND NETWORK TEST. SCNT shall perform the processing listed below to permit recognition of malfunctions within launch facility hardware which are not normally exercised during other modes and states. The SCN test command message is accepted by the PG and transferred to the DCU. Two separate portions of the SCNT are controlled by the PG and DCU. If the LF is reporting outer or inner security violated, there must be a 5.1 minute delay between SCNT commands, to clear security violations provided the source of violation is no longer present. SCNT can be commanded remotely at any time, but if the DCU is down or in local, only the electronic ground system test (d. below) is performed. The tests which are performed by SCNT are described in the following paragraphs with the order of performance shown in Figure 2-22 and 2-23.

a. CSD(M) drive enable check.

b. Coupler test.

c. No-go test.

d. Electronic ground system test.

e. UHF radio test.

f. Critical status override test.

g. Keep alive test.

h. Safety control switch test.

i. Launch in process and test complete

2-11.1. Command Signal Decoder (M) Drive Enable Check. SCNT shall:

a. Cause CSD(M) drive enable to be monitored.

b. If CSD(M) drive enable is true, cause CSD(M) drive enable failure to be set in the MOSR.

c. If CSD(M) drive enable is false, cause CSD(M) drive enable failure to be reset in the MOSR.

2-11.2. Coupler Test. The coupler test set character output code shall be issued prior to setting any no-go or inhibiting keep alive character output codes. All no-gos shall be reset and issuance of keep alive codes resumed prior to issuing coupler test reset. If no failures occur, the G&C coupler control monitor failure MOSR shall be reset. The coupler test shall be completed within 40 seconds of acceptance of the SCNT command.

2-11.3. No-Go Test. SCNT shall cause the following sequence to be performed:

a. Issue coupler test set.

b. Issue AVE no-go set and coupler no-go set.

c. Monitor AVE no-go and coupler no-go.

d. If AVE no-go and coupler no-go are not both true and circumvention reset is not true, cause G&C coupler control monitor failure to be set in the MOSR, and cause entry into the standby no-go mode.

e. If both AVE no-go and coupler no-go are true, cause G&C coupler control monitor failure to be reset in the MOSR.

f. Issue AVE no-go reset and coupler no-go reset.

g. Issue coupler test reset.

2-11.4. Electronic Ground System (EGS) Test. The EGS controlled portion of the SCNT verifies the operation of UHF radio processing, security system violation reporting, SDU

alarm processing, and programmer group alarm and no-go monitoring circuits. The SCNT command received by the DCU causes the DCU to issue the start SCNT character output (CO) to the C604 coupler. This is decoded and then transmitted to the programmer group. The start SCNT command resets the SCNT timer to begin the 40 second SCNT count and inhibits alarms and no-go's. The SCNT signal flow is shown in Figure 2-23.

2-11.4.1 UHF Radio. The DCU also issues CO's for ALCC access and clear text allowed which then causes the programmer group to command UHF Radio SCNT. The UHF radio responds to this command by generating a UHF radio test message which is monitored by the DCU during SCNT. Radio mode and radio data present will be reported if the test was successful.

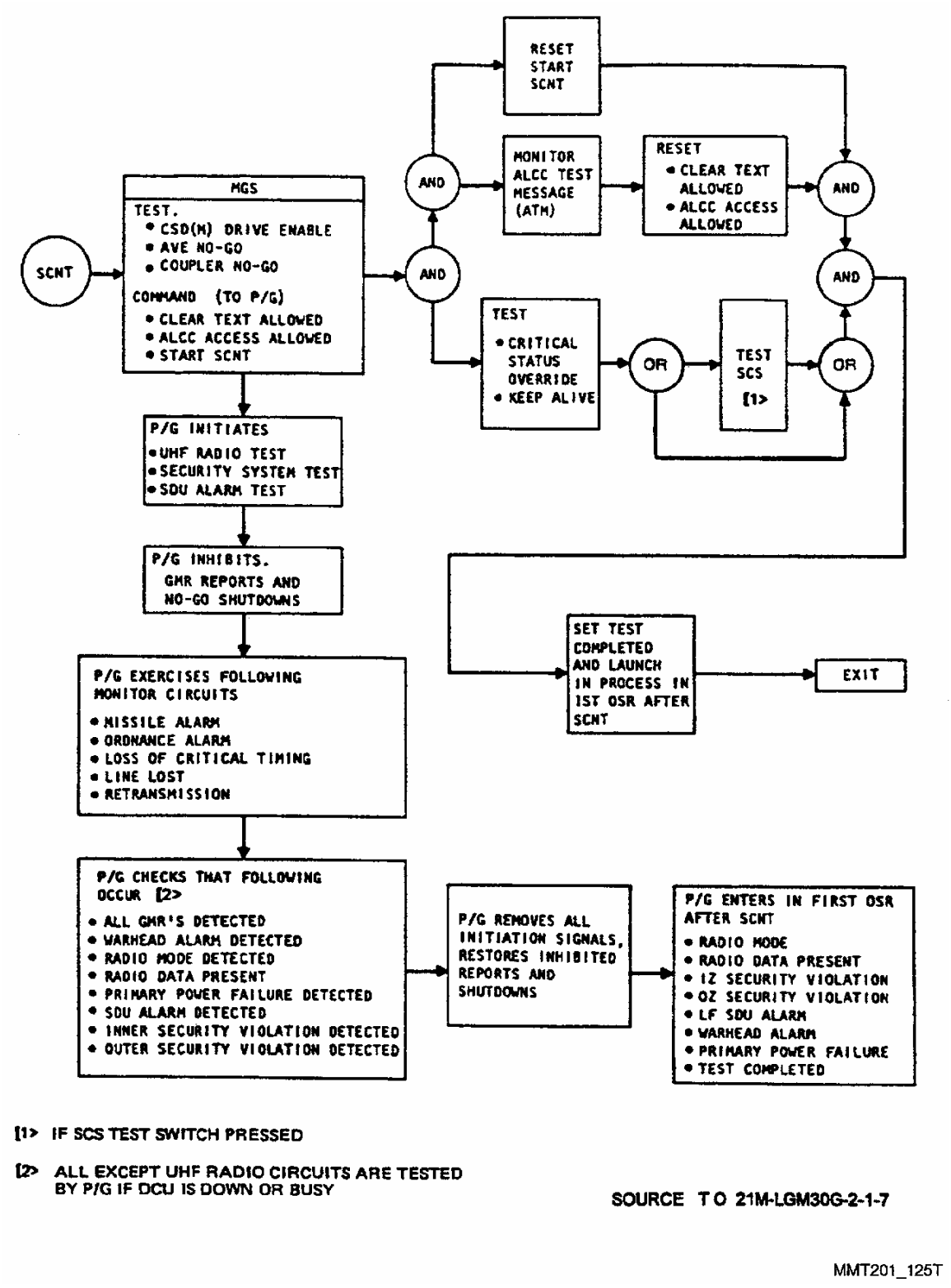


Figure 2-22. SCN Test

2-11.4.2. SDU and Security System. The programmer group also causes the SDU to generate an SDU alarm and the security system to issue inner and outer security violated as part of SCNT. The programmer group receives these alarms and processes them so that they can be reported in the OSR.

2-11.4.3. Programmer Group Monitoring, Alarms and No-Gos. SCNT verifies the operation of the no-go and alarm monitors in the programmer group A6 drawer. Each monitor receives a simulated fault while its output is checked to verify its presence. The inhibit alarm and no-go prevents normal processing during this operation. If any fault or no-go is absent the LF fault or no-go will be reported in the OSR. See block diagrams in Section VIII for alarm and no-go monitors which are tested during SCNT.

2-11.5. Ultra High Frequency Radio Test. SCNT shall perform the following:

a. The ALCC access allowed set and clear text allowed set character output codes shall be issued within 5 msec after issuing the start SCNT set character output.

b. Check at least every 200 msec for a Radio Test Message consisting of the ALCC test message (ATM) has been transferred to the DCU within 200 msec to 5 seconds after issuing the start SCNT set character output.

c. If the ATM received indicator is not true set 5.5 ± 2 seconds after issuance of start SCNT set character output, cause UHF radio test failure to be set in the MOSR.

d. If the ATM received indicator is true set within the time specified in c. above, cause UHF radio test failure to be reset in the MOSR.

e. The ALCC access allowed reset character output shall be issued within 200 msec of setting the ATM received indicator true (will be set true only providing that this is the first ATM processed during the current UHF radio test).

f. The ALCC access allowed and clear text allowed signals shall be restored to the states they were in prior to the test within 2.5 seconds after setting the ATM received indicator true, or within 9.0 seconds of issuance of start SCNT set character output after determining that a test failure occurred.

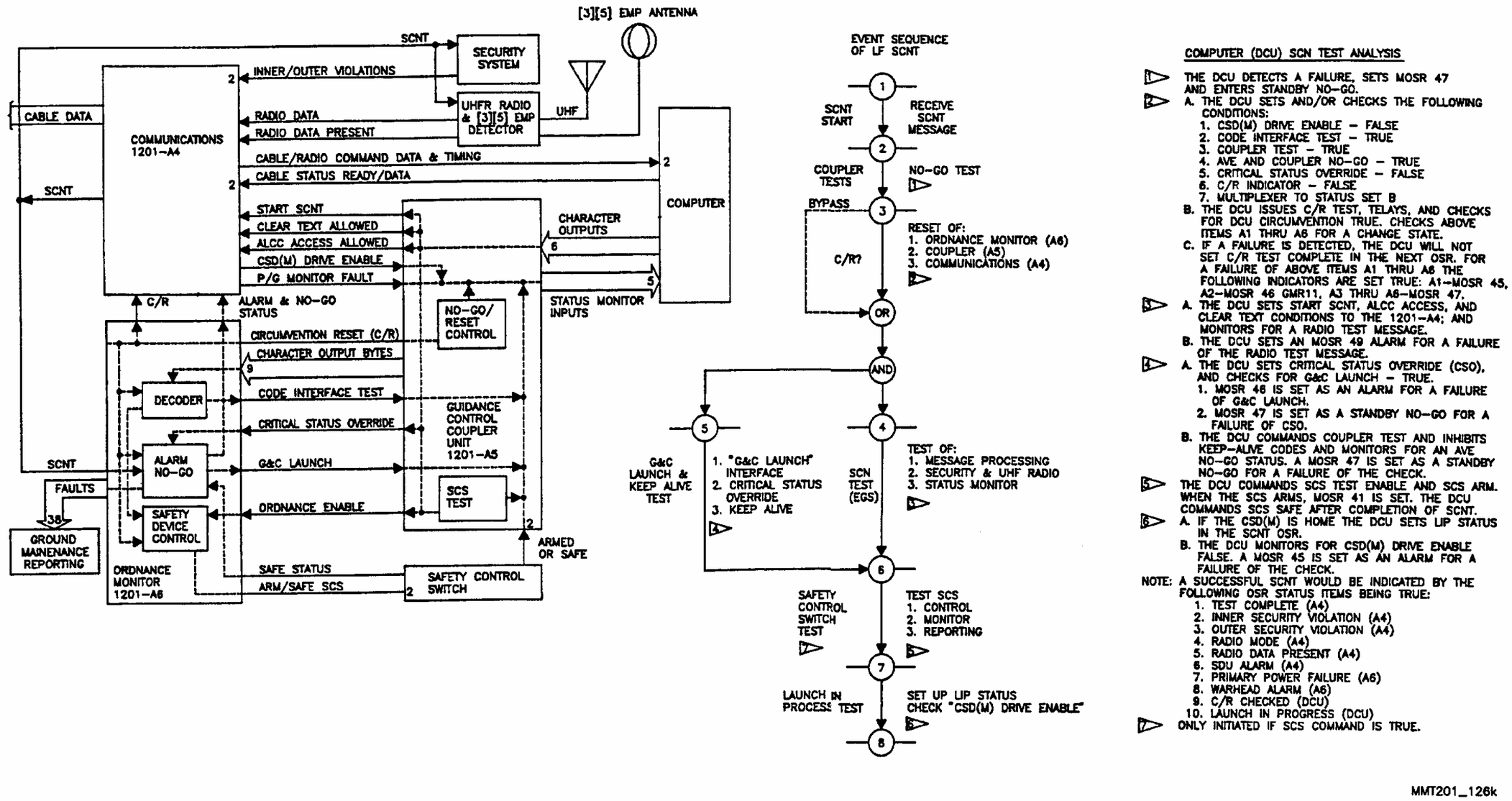


Figure 2-23. SCNT Signal Flow

2-11.6. Critical Status Override Test. SCNT shall perform the following sequence:

a. Issue critical status override set.

b. Monitor critical status override.

c. If critical status override and circumvention reset are false, cause G&C coupler control monitor failure to be set in the MOSR within 10 seconds and cause entry into the standby no-go mode within 5 seconds.

d. Issue critical status override reset.

2-11.7. Keep Alive Test. SCNT shall perform the following sequence.

a. Issue coupler test set.

b. Inhibit issuance of keep alive codes.

c. After a minimum delay of 3.15 seconds, following step b. monitor AVE no-go.

d. If AVE no-go is false and circumvention reset is false, cause G&C coupler control monitor failure to be set in the MOSR and cause entry into the standby no-go mode.

e. Issue in the following order, keep alive code, AVE no-go reset, and coupler test reset.

f. Cause resumption of the issuance of normal keep alive codes.

2-11.8. Safety Control Switch Test. The Safety Control Switch (SCS) test shall be performed if SCS Test Command is true, P/G Monitor Failure is false, CSD(G) Home is true, CSD(M) is home and CSD(M) is not being penetrated. In addition, whenever the SCS test is performed, the Cirtical N-Go Identifier shall be reset to indicate a non-critical no-go condition. The SCNT shall start SCS Test when at least 3.5 seconds have elapsed since issuing the Start SCNT Set character output and shall be completed within 38.5 seconds after the Start SCNT Set character output. The SCNT shall perform the following:

a. Issue SCS Safe Reset and SCS Test Enable Set followed by SCS Arm Set.

b. After a delay of at least 500 milliseconds after issuing SCS Arm Set, issue SCS Arm Reset, SCS Test Enable Reset, and SCS Test Command Reset.

c. Monitor SCS Armed Monitor at least 500 msec after step a. above. If true, set SCS Armed in the MOSR.

d. Issue SCS Safe Set after a delay of at least 2.4 seconds after issuing SCS Arm Set (item a above).

e. Issue SCS Safe Reset after a delay of at least 500 milliseconds after issuing SCS Safe Set (item d above).

2-11.9. Launch In Process and Test Complete Subfunction. SCNT shall cause launch in process and test completed to be issued for the first operational status reply (OSR) that occurs more than 40.09 (-0.00. ±0.05) seconds after issuing the start SCNT set character output if the following conditions are met:

a. CSD(M) Armed Prime Monitor is true, CSD(M) is not being penetrated, and CSD(M) code is not being changed.

b. CSD(M) home monitor is true.

c. System was not transitioned to local after the 40.09 (-0.00. ±0.05) seconds had elapsed.

Programmer group failure is reset in the MOSR if it is set.

2-11.10. Termination. SCNT shall be terminated upon occurrence of any of the conditions specified below:

a. Occurrence of a master reset. Issue in Critical Status Override Reset character output code and resume issuance of keep alive codes.

b. Entry into the terminal countdown mode. Issue the Coupler Test Reset character output code reset and resume issuance of keep alive codes.

c. Detection of circumvention reset or an NEP Event. Resume issuance of keep alive codes.

d. Acceptance of a missile calibrate command during standby no-go or acceptance of a SAT calibrate command during strategic alert with the GCA failure no. 1 MOSR bit set. Issue in order start SCNT reset and keep alive, coupler no-go reset, AVE no-go reset and coupler test reset character output codes, and resume issuance of keep alive codes.

e. Detection of a fault which warrants entry into the critical no-go mode of no-go processing.

f. Completion of the sensitive command network test.

2-12. COMPUTER MEMORY SECURITY CHECK. The Arithmetic checksum subfunction, the CMSC sum calculation subfunction, and the CMSC sum display subfunction shall be performed to verify a proper DCU load, calculating and displaying a Computer Memory Security Check (CMSC) sum of the DCU computer memory.

a. The Arithmetic Checksum subfunction computes an arithmetic checksum of the program and constant memory contents. After two consecutive multiplexer samples indicate an "Advance" command from the C-MON, this subfunction displays CMSC in Process (Readout 15) and then arithmetically adds all ROM, and all SRAM memory below the Enable Write Boundary Address to generate a 32-bit checksum value. If the sum is not equal to zero, Memory Checksum Error (Readout 0) and AVE No-Go shall be initiated.

b. The CMSC sum calculation subroutine shall perform the logic and arithmetic operations to compute a CMSC sum. The CMSC sum shall be derived by operating on all DCU and P-Plug words in a specific order. The locations containing the Screen word, S(s), shall be overwritten with zeros before the P-Plug words are read into DCU memory. The subroutine shall insure that the two P-Plug words are not in memory at the same time during the CMSC calculation, and the P-Plug words shall be overwritten as soon as the calculations using them are completed. After completing the CMSC calculation, the memory locations containing Control Words C(a) and C(b) and Screen Word S(f) shall be overwritten by zeros before proceeding.

c. The CMSC sum display subfunction shall output a blinking CMSC in Process (Readout 15) to the C-MON to indicate readiness to read out the CMSC. In response to an "Advance" command from the C-MON, the first hexadecimal digit is read out as Readout 0 through Readout 15. This process is repeated until all 8 digits of the CMSC have been read out. The readout of the CMSC can be repeated one time if desired.

2-13. NO-GO PROCESSING. No-go processing consists of the standby no-go mode and critical no-go processing.

a. The standby no-go mode processing subfunction provides the logic for maintaining the system in an operating condition during which a restart can be commanded except during overwrite in process. Further, system status is provided through the communications links and the IMU is maintained in a quiescent state.

b. The critical no-go processing subfunction provides the logic for performing and orderly shutdown during (1) overwrite-in-process, (2) when a fault is detected which could be detrimental to safety or equipment, (3) a restart occurs during overwrite in process. (See Figures 2-24, 2-25 and 2-26.)

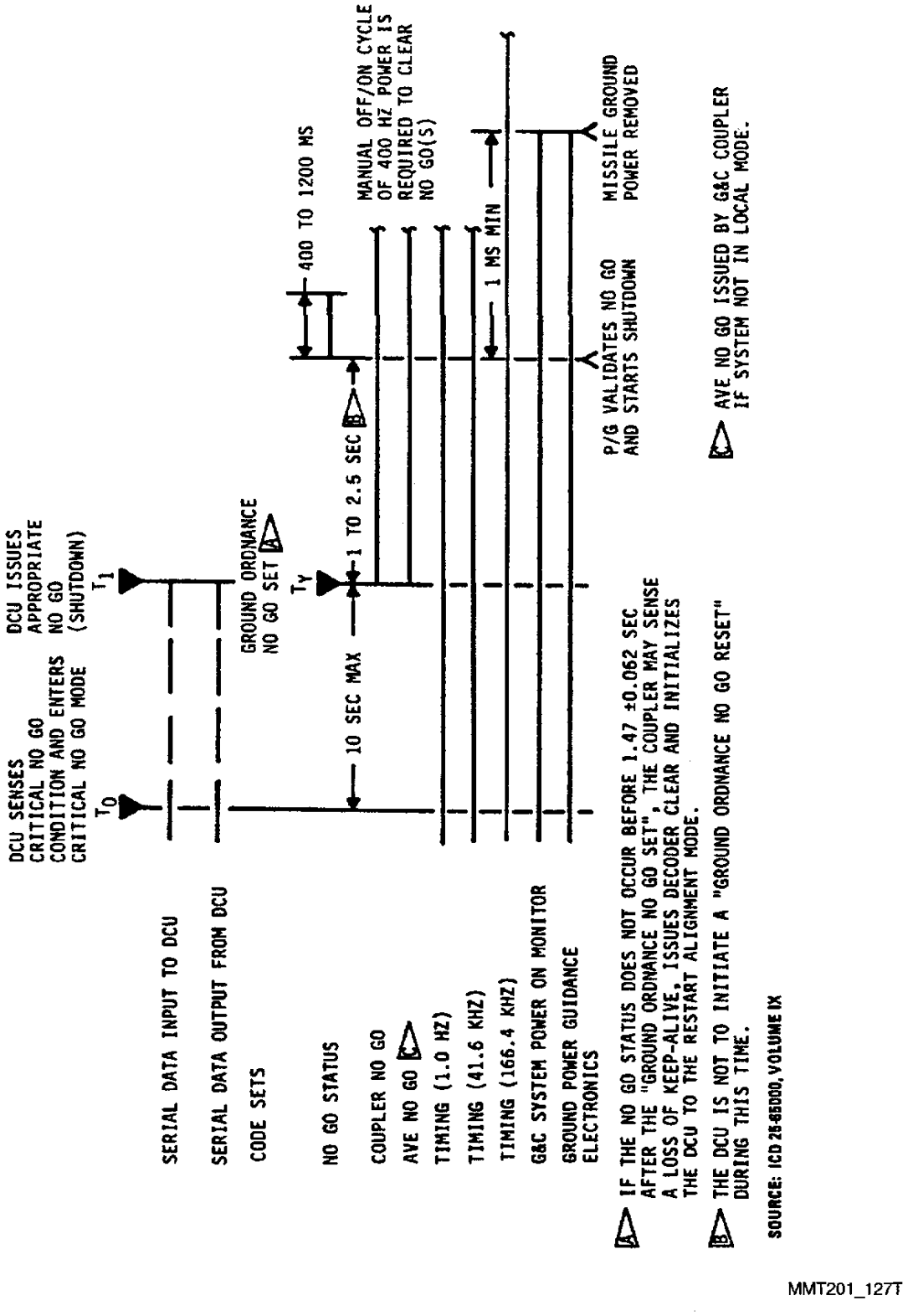
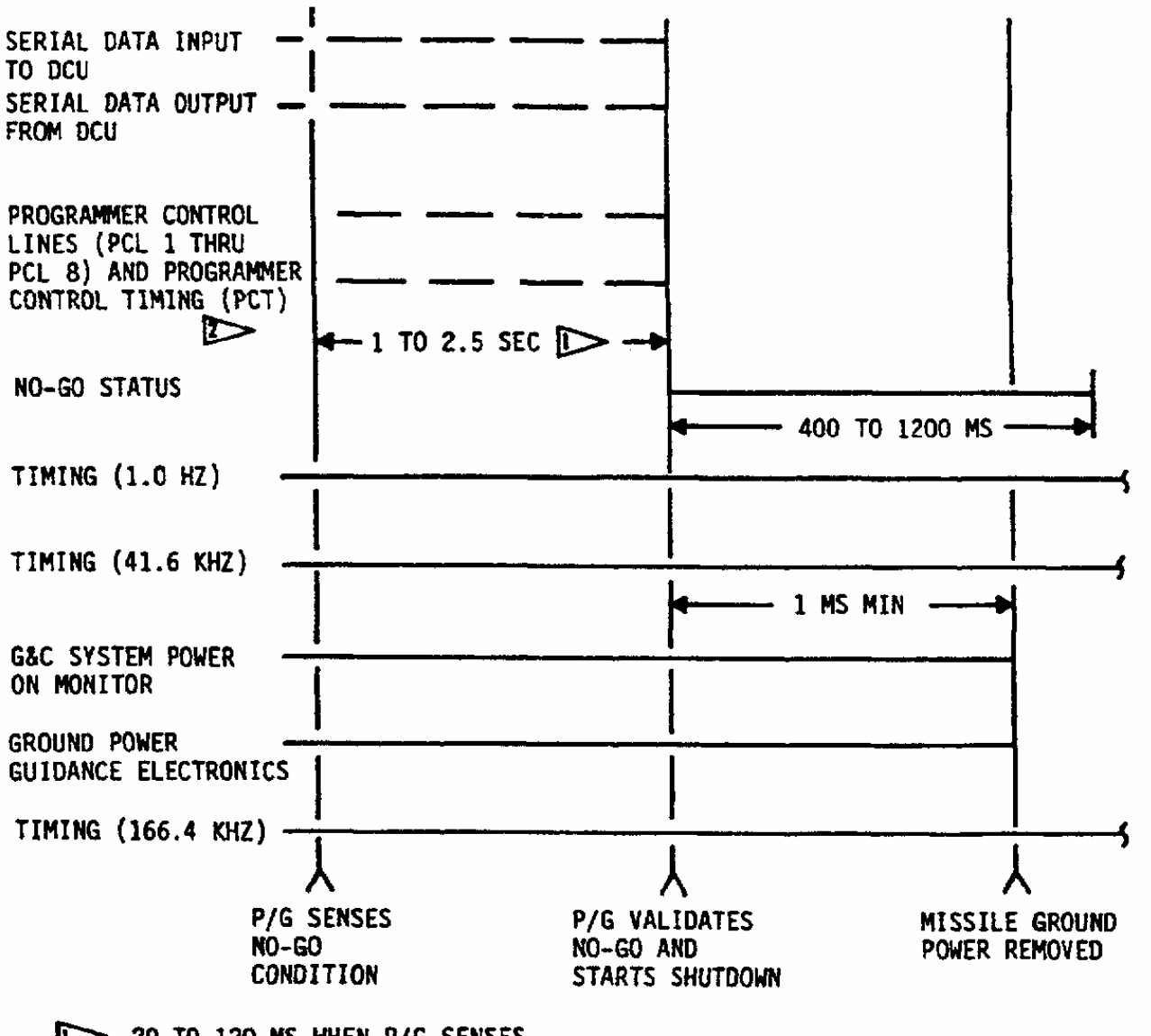


Figure 2-24. DCU Sensed Critical No-Go Shutdown Sequential Timing Diagram



1 20 TO 120 MS WHEN P/G SENSES LOSS OF 41.6 KHZ.

2 REFER TO ICD 25-65028 FOR EXPANSION OF PROGRAM CONTROL TIMING BETWEEN G&C COUPLER AND P/G.

SOURCE: ICD 25-65000, VOLUME IX

MMT201_128T

Figure 2-25. Programmer Sensed No-Go Shutdown Sequential Timing Diagram

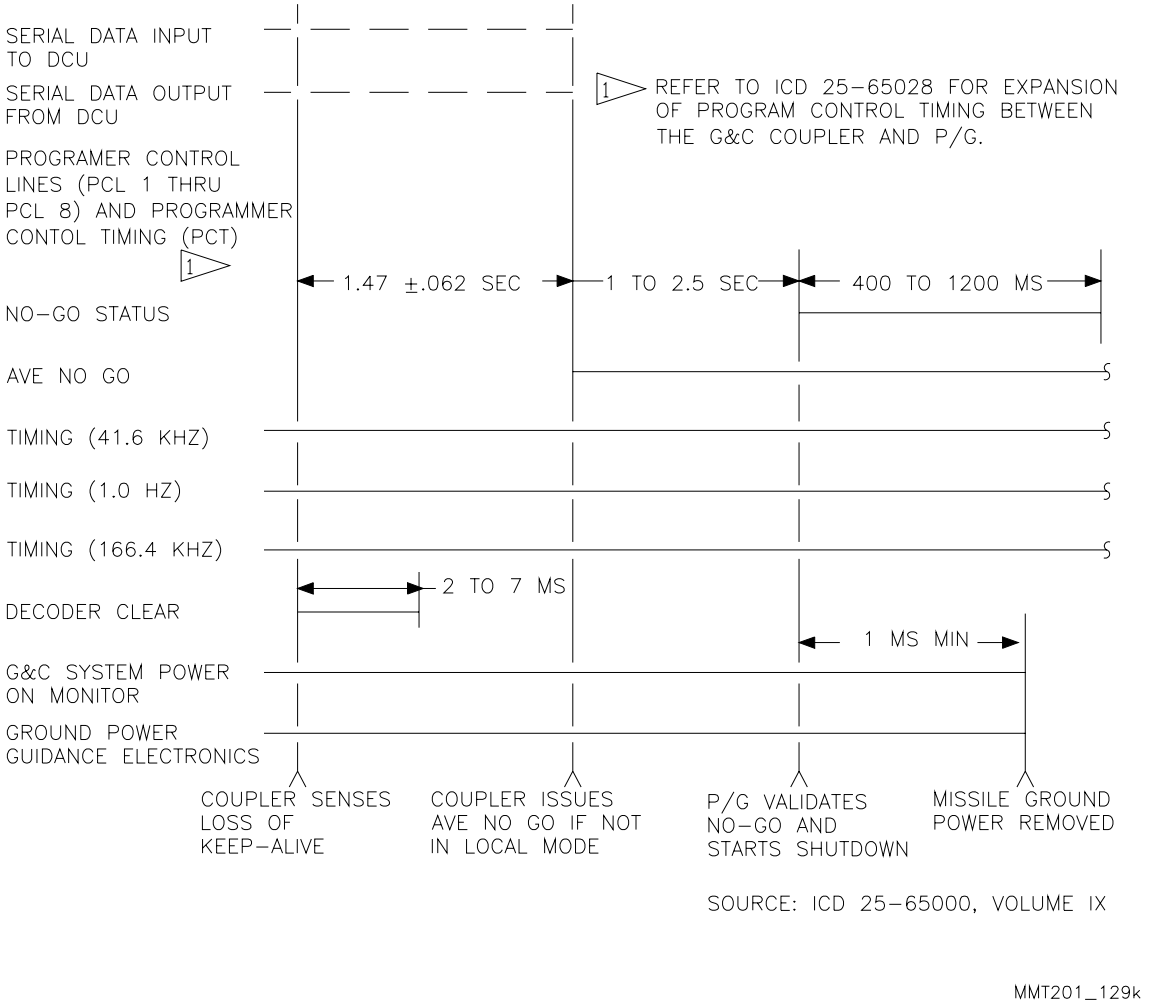


Figure 2-26. Loss of Keep-Alive Shutdown Sequential Timing Diagram

2-13.1. <u>Standby No-Go Initiating Conditions</u>. Initiating conditions for standby no-go processing are as follows:

a. Completion of a missile test which was entered from standby no-go and/or exit from missile test with any combination of items (1) through (13) occurring in the absence of circumvention reset or any combination of items (4) through (11) occurring in the absence of F/C power failure.

(1) Specific nuclear event detector failures (not all NED failures cause entry to standby no-go.)

(2) Ground ordnance test failure.

(3) Specific computer failures. (Not all computer failures cause entry to standby no-go).

(4) R/S discrete failure.

(5) Downstage discrete failure.

(6) PSRE discrete failure.

(7) Control and discrete unit failure.

(8) Downstage control failure.

(9) Stage II roll control failure.

(10) Stage III roll control failure.

(11) PSRE control failure.

(12) CSD(G) failure.

(13) SCS armed (except during SCS test).

b. Failure of the keep alive, AVE no-go, critical status override circuitry or coupler no-go in the guidance-control coupler during sensitive command network test.

c. Multiplexer test failure.

d. Two consecutive indications that the CSD(M) if off home or two consecutive indications that the CSD(M) computer home monitor is false.

e. CSD(M) armed during enable test or an enable test failure when the CSD(M) control failure MOSR bit had been previously set.

f. Platform failures.

(1) Excessive time for platform stabilization (slew and leveling).

(2) Excessive time for coarse zeta alignment.

(3) Excessive time for platform leveling following GCA case reversal.

(4) Platform loss-of-control check failure during platform slew.

(5) Platform loss-of-control check failure during the "stabilized" period.

(6) Three consecutive delta zeta check failures during coarse zeta alignment.

(7) LAI check fails or good IMU read/good IMU data failures after each of three consecutive PIGA data collection periods.

(8) Platform servo transient response test failure.

g. Gyrocompass failures:

(1) Gyrocompass scale factor check (initial/restart align) failure.

(2) Excessive time for GCA slew and stabilization.

(3) Filter failure counter run out during initial biasing.

(4) Two consecutive Ø2 check failures during initial biasing.

(5) Qi check failure during initial biasing.

h. Accelerometer failures: Absolute value of PIGA bias exceeds limit during PIGA calculations and checks.

i. G6B4 gyro bias check failure.

j. Two consecutive delta RL check failures in either IMU calibration segment 1 or 2.

k. Detection of a high level seismic or Nuclear Event Protection (NEP) occurrence prior to calculation of PIGA bias during initial alignment.

l. When Restart Alignment is initiated from SBNG with no Valid PIGA Biases, and a High Level Seismic or Nuclear Event Protection (NEP) occurrence is detected prior to establishing valid PIGA biases (E1 bias cycle), SBNG is reentered with Absolute PIGA Bias Failure MOSR set.

m. Character output code interface test failure.

n. Critical status override failure.

o. Acceptance of a local standby no-go command.

p. Acceptance of overwrite command during Strategic Alert when conditions to perform overwrite are satisfied.

q. PIGA leveling check failures: the total number of LAI check failures/velocity observable data rejections reaches 60.

r. MGSC/DCU communications failures (10 consecutive occurrences).

(1) MGSC mode error.

(2) Read/Write compare error.

s. CSD(M) Armed Prime Monitor failure during CSD(M) Code Change mode.

t. Executive processing failures:

(1) Illegal Address Fault.

(2) Illegal Instruction Fault.

(3) Task Overflow Failure.

(4) Miscellaneous Machine Error Interrupt Faults.

u. Inadvertent initiation of R/S fuzing.

v. Inadvertent RDA processing.

w. Inadvertent RDC termination.

x. Multiple null offset corrections required.

2-13.2. Standby No-Go Functions. When any of the conditions specified in paragraph 2-13.1 exist, the following conditions will take place:

a. Perform the following upon initial entry to standby no-go:

(1) Set SBNG in the system status.

(2) Enter Disenabled State and No Launch Mode.

(3) Reset Target Data Changed in the OSR.

(4) Allow completion of the bias cycle data calculations (period of time from data accumulation completion to IPDR calculations and checks completion). These calculations are not required to complete if SBNG is exited (to CNG or Command Restart).

(5) If SBNG was entered due to platform loss of control, Phi Cal Servo Test Failure or MGSC/DCU communications failures or SBNG was entered during PIGA Hot Start or during platform slew, items (a) and (c) below shall be performed. If SBNG was entered due to an accepted Overwrite command during strategic alert biasing, GSP/MGSC diagnostic processing and items (a) and (c) below shall

be performed. For all other entry conditions, items (b) and (c) below shall be performed.

(a) Set the Platform Mode Control word to Disable. Reset MGSC Servo Enable in the UIO Discrete Output Register.

(b) Set the Platform Mode Control word to stable and perform GSP/MGSC diagnostic processing.

(c) Set the GCA Mode Control word and PIGA Mode Control word to Disable. In addition, set the GCA Slew Controls word to Stable.

b. Perform the following continuously during standby no-go:

(1) Terminate the SBNG Mode and Start the CNG Mode upon occurrence of any of the conditions that causes critical no-go.

(2) Terminate SBNG mode upon acceptance of an MCC via remote communications or an IMU Calibration 1 Command via local communications and enter the Restart Alignment Initialization portion of initialization, if not in overwrite in process. Exit to Missile Test from SBNG mode if an MTC is accepted via local/remote communications, if not in overwrite in process.

(3) Perform Launch Facility (LF) memory overwrite upon acceptance of an OWC.

2-13.3. LF Memory Overwrite. The LF memory overwrite shall be performed as a result of a remote command from the Launch Control Center or a local command from the Controller Monitor (CMON) at the LF. LF Memory Overwrite shall be as follows:

a. Upon acceptance of an OWC via remote communications from the LCC or via local communications from the LF, the following shall be performed:

(1) Inhibit Local/Remote command acceptance except for Resync Reply (RSR), OWC, OWT, Airborne Launch Control Center (ALCC) Holdoff Command (AHC), IMU Performance Data Command (IPDC), local overwrite command, local advance command, an IMU Calibration 1 Command or MCC.

(2) Normal status monitoring and interrogation/response processing shall be maintained during OIP until CNG occurs.

(3) Acceptance of an MCC via remote communications or an IMU Calibration 1 Command via local communications shall result in entry to CNG.

(4) DCU write-protected memory shall be modified so that exit to CNG shall occur for subsequent Restarts/Startups without a complete tape fill.

(5) DCU write-protected memory shall be modified so that if Terminal Countdown is inadvertently entered. The SCS and CSD(G) will not become armed.

(6) Report Overwrite in Process (OIP) in the OSR until CNG occurs.

(7) If Remote Data Change (RDC) is in process, it shall be terminated and RDC Not in Process shall be reported in the OSR.

(8) The RDC Authorization Status shall be set to the unauthorized state and PLCA/PLCC Effectivity set to reflect not effective as reported in the Target Data Reply (TDR).

(9) Checksum shall be terminated, if in process. It shall then be restarted 1 ± 0.1 hours after acceptance of the OWC via remote or local communication. Checksum shall not be balanced during OIP.

b. After the conditions in step a. (4. through 9.) above have been established, this function shall perform LF Memory Overwrite as specified below:

(1) The required DCU memory overwriting during LF Memory Overwrite shall be accomplished by writing a predetermined overwrite pattern, one time, followed by its one's complement, one time.

(2) All secure code data, RDCT data set locations and variable memory locations that contain information derived from secure code or targeting data and memory locations that were temporarily used to store P-Plug words shall be overwritten. Note: TVR data shall be undefined during and after overwrite.

(3) Perform an accumulative sum of each 16-bit location each time it is overwritten.

(4) Enable Write shall be enabled only during that time data is being written into memory.

(5) Memory Overwrite shall be completed within 12 minutes. Overwrite shall provide a minimum time of 30 seconds in overwrite mode to allow the overwrite in process display indication during local operation.

(6) The OGP shall add a prestored constant to the accumulative sum such that if the overwrite was successful, the 24 least significant bits of the final sum number shall be equal to the Factory Penetration Code pattern (01234567_8).

(7) The Battery Flag discrete shall be reset by issuing the CPU Discrete Output bit 8 true.

c. Upon completion of the overwrite process in step b. above, the following shall be performed:

(1) Perform the following for remote operations:

(a) Without making a determination as to whether the overwrite was successful, the OGP shall transmit the Overwrite Sum computed in step b.6. above. The Overwrite Sum shall be reported in two Remote Verification Replies (RVRs) to two successive OSIs or OSI-Anti Jams (AJs) via remote communications in accordance with the OSI priority rules.

(b) When an OWT command is accepted via remote communications during OIP, a check shall be made to determine if the Overwrite Process was successful (step b.6. above). If the Overwrite Process was successful, the Factory Penetration Code shall be stored in the locations in DCU write-protected memory dedicated to penetration codes and then exit to CNG. If the Overwrite Process was unsuccessful, the OWT shall be ignored.

(2) For local operations, the Overwrite Sum shall be saved to allow readout of the Overwrite Sum.

2-13.4. Critical No-Go Initiating Conditions. Initiating conditions for critical no-go processing are as follows:

a. Detection of a second consecutive checksum failure.

b. Two consecutive indications that the ground ordnance power on monitor is true and cannot be reset except when commanded on.

c. Two consecutive indications that the any ground ordnance driver on monitor is true except when command on.

d. Downstage battery test failure during the flight program portion of terminal countdown.

e. An indication of an IMU power failure.

f. Terminal countdown not entered properly: Failure of the TCD validity test.

g. CSD(G) 19th bit monitor remains true after two reset attempts during the CSD(G) test.

h. Master reset occurrence during terminal countdown.

i. Acceptance of remote missile calibrate command or local IMU calibrate 1 command or remote overwrite terminate during overwrite in process.

j. Master reset occurrence during overwrite in process.

k. Initial alignment/startup without a complete tape fill following critical no-go shutdown during overwrite in process.

l. Executive processing faults:

(1) Illegal address fault during TCD or more than one within 200 msec or 5 occur within 15±1 minutes.

(2) Illegal instruction fault during TCD or more than one within 200 msec or 5 occur within 15±1 minutes.

(3) Five consecutive indications of missing computer IMU real time interrupt.

(4) Five consecutive indications of multiple computer IMU real time interrupt.

(5) Miscellaneous machine error fault occurrences during TCD more than once per 200 msec.

(6) Task over flow during TCD.

m. Weapon System Configuration Check failure in Initial Alignment initialization processing.

2-13.5. Critical No-Go. Upon occurrence of any of the conditions specified in 2-13.4, this function shall first execute steps a. through d., in any order as defined below, then the other steps shall be executed. If Critical Status Override Reset or SCS Safe Set are issued as defined in items d., f. and h. below, they shall be issued prior to issuing AVE No-Go, item g. below. Item e. shall be executed for all cases.

a. Mask all maskable interrupts and reset MGSC Servo Enable in the UIO Discrete Output Register.

b. Update the CNG Readout Word with the contents of the CNG Identifier. The CNG Identifier shall contain a unique bit pattern which identifies the cause of entry to CNG.

c. Issue the following character outputs prior to issuing the shutdown commands except for a CNG initiated due to a Weapon System Configuration Check failure:

(1) CSD(M) Reset Command Reset.

(2) Resets 9-9 through 9-15.

(3) Resets Codes 15-1 through 15-7.

(4) R/S Ground Power Reset.

(5) R/S Input Data Lines Reset.

d. If CNG is entered during SCNT, or Missile Test, the processing defined below shall be performed. In all cases, Keep Alive shall be issued at least once prior to the issuance of AVE No-Go Reset.

(1) If CNG is entered during SCNT, the items below shall be issued. In addition, items (a), (b) and (c) shall be done in that order and item (e) shall follow (d). Items (b) through (d) shall be issued at least once prior to power shutdown, while item (a) shall be issued only one time. SCS Safe Set shall be issued repeatedly until a power shutdown occurs.

(a) AVE No-Go Reset.

(b) Coupler No-Go Reset.

(c) Coupler Test Reset.

(d) SCS Arm Reset.

(e) SCS Safe Set.

(2) If CNG is entered during Missile Test, the items below shall be issued. In addition, items (b), (c) and (d) shall be done in that order and item (f) shall follow (e). Items (c) through (e) shall be issued at least once prior to power shutdown, while item (b) shall be issued only one time. SCS Safe Set and Critical Status Override Reset shall be issued repeatedly until a power shutdown occurs.

(a) Critical Status Override Reset.

(b) AVE No-Go Reset.

(c) Coupler No-Go Reset.

(d) Coupler Test Reset.

(e) SCS Arm Reset.

(f) SCS Safe Set.

(g) Auxiliary Status Enable Reset.

e. Issue Keep Alive at least twice every 1.4 seconds until a power shutdown occurs.

f. Issue Critical Status Override Reset when the CNG Mode was initiated for any one of the conditions specified below. Critical Status Override Reset shall be issued repeatedly until a power shutdown occurs.

(1) Battery Test Failure during the Flight Program portion of terminal countdown.

(2) Terminal countdown not entered properly (failure of the TCD Validity Test).

(3) Master Reset occurrence during terminal countdown.

g. Issue AVE No-Go Set when the CNG Mode was initiated for any one of the conditions specified below. AVE No-Go Set shall be issued repeatedly until a power shutdown occurs.

(1) Battery Test Failure during the Flight Program portion of terminal countdown.

(2) Terminal countdown not entered properly (failure of the TCD Validity Test).

(3) Detection of a second consecutive checksum failure.

(4) An indication of an IMU power failure.

(5) Acceptance of an MCC, IMU Calibration 1 Command or OWT during OIP.

(6) Master Reset occurrence during OIP.

(7) Initial Alignment/Startup without a complete tape fill following CNG shutdown during OIP.

(8) Master Reset occurrence during terminal countdown.

(9) Weapon system configuration check failure in Initial Alignment.

(10) Illegal address fault failure.

(11) Illegal instruction fault failure.

(12) Five consecutive indications of missing CIRTIs.

(13) Five consecutive indications of multiple CIRTIs.

(14) Miscellaneous Machine Error fault occurrences.

(15) Task overflow during TCD.

h. Issue SCS Arm Reset when CNG was initiated for the conditions specified in items 3 through 8 below and SCS Safe Set character output codes in that order when CNG was initiated for any one of the conditions specified below. SCS Safe Set shall be issued repeatedly until a power shutdown occurs.

(1) Battery Test Failure during the Flight Program portion of terminal countdown.

(2) Terminal countdown not entered properly (failure of the TCD Validity Test).

(3) Master Reset occurrence during terminal countdown.

(4) Illegal address fault failure during TCD.

(5) Illegal instruction fault failure during TCD.

(6) Five consecutive indications of missing CIRTIs during TCD.

(7) Five consecutive indications of multiple CIRTIs during TCD.

(8) Miscellaneous Machine Error fault occurrences during TCD.

(9) Task overflow during TCD.

i. Issue Ground Ordnance No-Go Set character output codes when CNG is initiated for any one of the conditions specified below. Ground Ordnance No-Go set shall be issued repeatedly until a power shutdown occurs.

(1) Two consecutive indications that the Ground Ordnance Power On Monitor is true and cannot be reset, except when commanded on.

(2) Two consecutive indications that the Any Ground Ordnance Driver On Monitor is true, except when commanded on.

(3) CSD(G) 19th Bit Monitor remains true after two reset attempts during CSD(G) test.

2-14. LOCAL COMMUNICATIONS. See section III. When the system is operating in the local communications mode, local communications perform the operations to detect Controller-Monitor (C-MON) keyboard inputs, process the received local command for acceptance, and initiate or execute the system response for the decoded command.

a. The decode keyboard input subfunction decodes the C-MON keyboard input, identifies the local command, performs local command acceptance checks, and determines the system response.

b. The data readout sequence subfunction provides the capability to read out any specified memory location. The specific data to be read out is identified by the data readout sequence subfunction.

c. The system status display subfunction provides system status and fault data change status information to the C-MON for display whenever local communications mode is not performing the data readout sequence.

2-15. REMOTE COMMUNICATIONS. See Section VI for details. When the system is operating in the remote communications mode, this function performs the operations to process cable and UHF radio messages, perform crypto sync operations, and execute remote data change operations.

a. The cable message subfunction accepts interrogations and commands issued by the LCFs, performs message acceptance checks and determines the system response. System response includes initiation of the following functions:

(1) Initialization

(2) Alignment

(3) Strategic alert

(4) Calibration

(5) Enable states

(6) Launch modes

(7) Missile test

(8) Sensitive command network test

(9) No-go processing

(10) Telemetry

b. Ultra high frequency radio. The UHF radio message processing is performed whenever the local or remote status indicator is in the remote state and the system is in the ALCC access allowed mode. The following ALCC designated messages are accepted:

(1) ENC

(2) PLCA 1 and PLCA 2

(3) PLCB

(4) ELC

(5) INC

The ENC, PLCA 1, PLCA 2, and PLCB have a radio/cable identifier. The ENC, PLCA 1, PLCA 2, and PLCB require two successive identical 48 bit messages for acceptance. In addition, this function shall not be performed whenever CMSC, missile test, or terminal, countdown is in process. There is no cable/ ALCC identification for ELC/INC. ELC/INC transmitted by the ALCC shall be processed as if LCF originated.

c. The crypto sync subfunction provides the counters, timers, and associated logic required for maintenance of crypto sync, clear text allowed, and ALCC access allowed modes. In addition, this function determines entrance and exit of the crypto sync, clear text allowed, and ALCC access allowed modes.

d. The remote data change subfunction provides for the transfer, storage, and verification of target and execution plan sets and program data ID.

2-16. STATUS MONITORING. This function performs selected monitoring of operational ground equipment, aerospace vehicle equipment, and real property installed equipment and is continuous during all operational modes except initialization missile test and terminal countdown unless otherwise specified. System status information is continuously updated and formatted for transmission. In addition, certain status information is used for internal control, i.e., initiation of control functions without external stimuli.

2-16.1. Processing. Status monitoring is performed during all modes of operation except during initialization, missile test and terminal countdown (which will be detected) unless otherwise specified. Status monitoring is interrupted upon entry into missile test or terminal countdown and shall resume upon exit from missile test. All standby no-go decisions utilizing OGE multiplexer status data shall be based on two consecutive samples 4 msec to 5 seconds apart. However, the results of the first sample shall not be used if a circumvention reset event has occurred since the last time that status was sampled. Ground ordnance power on failure and any ground ordnance driver on failure shall require two consecutive indications to cause entry to critical no-go. A circumvention reset shall cause the first sample of the critical status override failure, CO code interface test failure, multiplexer test failure, ground ordnance power on failure and any ground ordnance driver on failure to be rejected if it occurred since the last time that status was sampled. An indication of IMU power failure and 2nd consecutive checksum failure shall cause immediate processing to enter critical no-go.

2-16.2. Status. Data is assembled from status information and is made available to local and remote communications for processing. See section VI for further details on OSR, MOSR, TVR, IPDR, and TDR information processing.

2-16.3. Aerospace Vehicle Equipment Self Monitoring. AVE shall be monitored during all modes except missile test and terminal countdown unless otherwise specified.

a. The Stage III LITVC pressure monitor, platform pressure monitor, and AC instrument on shall be monitored at least once every 5 seconds. If either is false, the Stage III LITVC pressure failure or platform pressure failure shall be set in MOSR respectively. If AC instrumentation is false with the good IMU read indicator true, an IMU power failure has occurred. Within 10 seconds of detection of an IMU power failure, status monitoring shall set the

critical no-go identifier to indicate the IMU power failure and initiate critical no-go.

b. At least once every 5 seconds the multiplexer test pattern of a multiplexer status set shall be tested by issuing the multiplexer test set character output code, by sampling the status set for the predetermined pattern, and by issuing the multiplexer test reset character output code. At least two complementary sets except A and S shall be tested. Unless a Circumvention Reset Event has occurred, failure to detect the correct pattern after the second attempt shall result in setting the G&C coupler control monitor failure and entry into standby no-go.

c. Status Monitoring shall perform the arithmetic checksum operation as follows:

(1) The arithmetic sum of the write-protected memory except the secure code data (including penetration code) shall be compared with the predetermined sum at least once every hour when the checksum is not inhibited. However, checksum shall not be performed during RDC operations, secure code checksum operations or for 10 ± 0.1 minutes after a secure code checksum failure (item 2. below) or for 1.0 ± 0.1 hour after acceptance of an OWC. When the comparison agrees, the check is successful and the checksum failure shall be reset in MOSR. Failure shall result in setting CHKSUMFAIL in MOSR and in a restart of the check after the MOSR has been transmitted, but within 10.0 ± 0.1 minutes of the initial checksum failure. A second consecutive failure shall result in setting the critical no-go Identifier indicating checksum failure and the critical no-go shall be entered.

(2) The arithmetic sum of the secure code data (including penetration codes) shall be compared with the predetermined sum one time within 500 msec after acceptance of an AHC or SCNT unless an OWC has been accepted. If the checksum fails, CHKSUMFAIL shall be set in MOSR and the check shall be restarted within 500 msec after the MOSR has been transmitted, or within 10.0 ± 0.1 minutes of the initial checksum failure whichever occurs first. A second consecutive failure shall result in setting a checksum failure and critical no-go shall be entered. If an OWC is accepted, the checksum of secure data (initial and repeated performance) shall be terminated.

d. Status monitoring shall calculate TAU, the Ratio of Computer Time (PRCTME) to the nominal value of the External Precision Time (T_NOM), detect, and report Precision Time failures (PREC_F) by performing the following functions at least once every 0.98 seconds, except for 3.0 ±1.0 seconds after Missile Test and following a power on system startup. Initialize TAU to one following the occurrence of Initial Alignment.

(1) Calculate the difference between expected computer clock and actual computer clock increments accumulated between the 0.98461538 second precision time pulses (PRECTIMINP) from the ground equipment as follows.

T_N = PRCTME - PRCTMEP (see Note)

PRCTMEP = PRCTME

DELTAT_N = T_NOM - T_N

Note: PRCTMEP shall be initialized to zero at power on. The delta (T_N) calculation shall take into account the data wrap in PRCTME.

If IDELTAT_NI exceeds specified limits, the calculation of CPRM_N and updating of TAU shall be bypassed. If TAU updating is bypassed more than 10 consecutive times the Precision Time Failure shall be set for one MOSR.

(2) A value of CPRM_N shall be calculated as:

CPRM_N = CPRM_NLSS1 + BETA (CPRM_NLSS1 + DELTAT_N)

where

CPRM_NLSS1 shall be set to 0 following Initial/Restart Alignment entry

(3) If ICPRM_NI exceeds specified limits, the Precision Time Failure shall be set for one MOSR.

(4) TAU and CPRM_NLSS1 shall be calculated as follows:

$$TAU = \frac{CPRM\_N + CPRM\_NLSS1}{2 * T\_NOM} + 1$$

CPRM_NLSS1 = CPRM_N

e. The status of the Enable Write circuitry shall be monitored at least once every 5 seconds, except when Enable Write is set true during data storage of the Remote Data Change operation of Remote Communications, the DCU Self-Test portion of Missile Test, or the Overwrite in Process sequence of No-Go processing. Determination of the Enable Write capability shall include an actual attempt to store data in write-protected memory. The resulting fault interrupt due to attempting to store in write-protected memory

shall be masked or ignored. Memory integrity shall be maintained. Failure shall cause status monitoring to set G&C Coupler Control Monitor Failure in the MOSR and issuing the Enable Write Reset character output code.

f. The status of the CSD(M) shall be monitored at least once every 5 seconds during the Disenabled State and the indicated status shall be set within 10 seconds. The CSD(M) Computer Home Monitor and the CSD(M) Home monitor, shall be utilized for this check.

(1) If two consecutive checks show CSD(M) Computer Home Monitor false with CSD(M) Home indicating home, the CSD(M) Control Failure shall be set in MOSR and the Standby no-go Mode shall be entered. The second consecutive check shall be performed no sooner than 5.3 seconds after initiation of CSD(M) reset following a CSD(M) penetration.

(2) If CSD(M) Computer Home Monitor indicates false and CSD(M) Home Monitor indicates off-home, the CSD(M) shall be reset by issuing CSD(M) Reset Command Set, delaying 0.5 to 5.0 seconds, and then issuing CSD(M) Reset Command Reset. If the next check after CSD(M) reset indicates the CSD(M) is off-home, CSD(M) Control Failure shall be set in MOSR and Standby no-go Mode shall be entered.

(3) If CSD(M) Home Monitor indicates that the CSD(M) is home, the launch times shall be set to the maximum unexpired value, LCMVV shall be set to zero and the System Status shall be set to Disenabled State and No Launch Mode.

g. The following PSRE status shall be monitored at least once every 5 seconds and the status item set within 10 seconds of collecting sixteen consecutive false samples shall be collected prior to using the false state of this monitor.

Status item	**Criticality**
(1) PSRE pressure switch monitor false	Alarm - Set MOSR

h. The R/S Ground Power On monitor shall be sampled at least once every 5 seconds, except during fuzing. When a true state is detected on the monitor, the Programmer Group Failure shall be set in MOSR within 10 seconds. In addition, the Reset R/S Ground Power On Command shall be issued. T/S Ground Power shall not be monitored for at least 100 μsec after issuing Ground Power Start.

Status item	Criticality
(1) Programmer Group Failure (R/S) ground power on true when not in fuzing operation)	Alarm - Set MOSR

i. Status monitoring shall reset the Calibration Inhibited MOSR within 5 seconds whenever either of the following conditions is satisfied.

(1) The twelfth bias cycle has been completed after either of the following:

(a) A platform slew during a Return to Target sequence.

(b) Entry to Strategic Alert Biasing from Strategic Alert PIGA Leveling.

(2) Retarget Alignment is performed with a platform repositioning operation.

(3) Entry to Strategic Alert PIGA leveling.

2-16.4. Safety Control Switch Armed Monitor. The SCS armed status input shall be checked at least once every 5 seconds, except during SCNT. If SCS armed is true, the SCS armed indicator shall be set true, the SCS armed bit shall be set in the MOSR and the SCS arm reset and SCS safe set character output codes shall be issued, and after a minimum delay of 500 msec the SCS safe reset character output codes shall be issued. The SCS armed indicator shall remain true as long as the SCS armed status input is true.

2-16.5. Ground Ordnance Monitor. The Any Ground Ordnance Driver On and the Ground Ordnance Power On monitors shall be monitored at least once every 5 seconds. If ground ordnance power on is true when not commanded on and cannot be reset with the issuance of Ground Ordnance Interlock Clear Set, Ground Ordnance Interlock Clear Reset, character output codes or any Ground Ordnance Driver On is true when not commanded on for two consecutive samples, the critical no-go identifier shall be set to indicate the specific failure and the critical no-go shall be entered.

2-16.6. Critical Status Override. Critical status override shall be checked at least once every 5 seconds during normal monitoring. If critical status override is true and cannot be reset with issuance of Critical Status Override Reset character output for two consecutive samples, Standby no-go shall be entered, G&C Coupler Control Monitor Failure shall be set in the MOSR and Commanded Restart shall be inhibited.

2-16.7. Digital Computer Unit Monitoring. The DCU shall issue keep alive code to the operational ground equipment. The signal shall be issued at a rate of at least twice every 1.40 seconds except during the keep alive test portion of SCNT. The proper operation of

the DCU CPU shall be checked at least once every hour by performing the DCU CPU Self Test except for the issuance of the DCU Self Test character output display or entering Stop Mode. Failure of the check shall result in setting the Computer Failure in MOSR, and entry to the standby no-go mode.

2-16.8. Local/Remote Status. At least once every 5 seconds the local status indicator G4, shall be monitored and the appropriate status shall be stored as local or remote status for access by other functions as required.

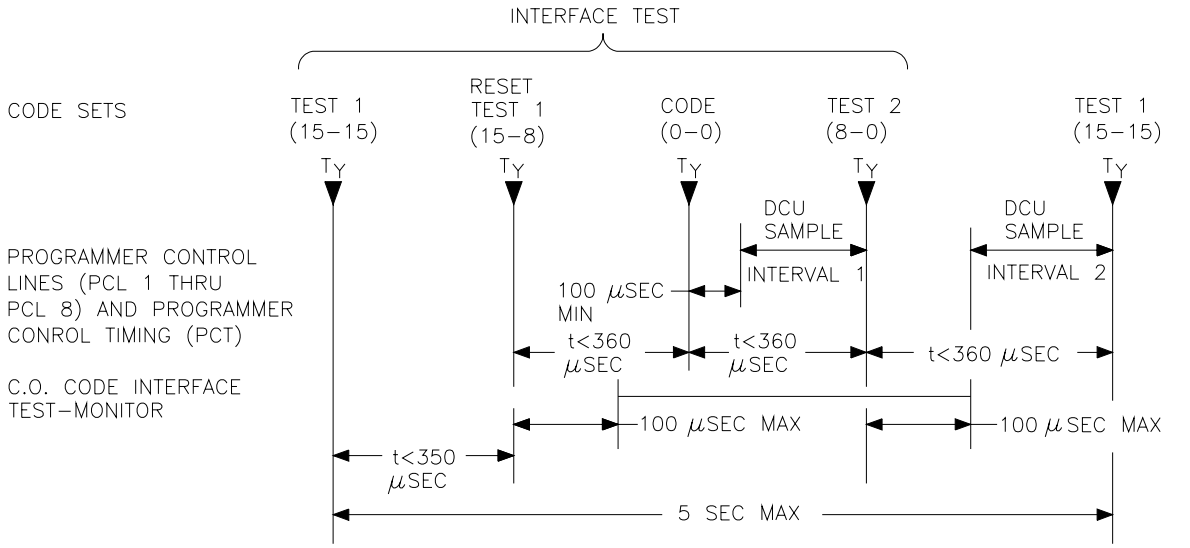
2-16.9. Character Output Code Interface Test. This test shall be performed at least once every five seconds. The Ground Ordnance Interlock Clear (Test 1), Reset Codes 15-9 through 15-15 and Select Status Set A character output codes shall be issued in that order. After a delay of at least 100 µsec, the CO Code Interface Test shall be sampled for true. The CO code Interface Test Reset (Test 2) character output code shall then be issued. After a delay of at least 100 µsec, the CO Code Interface Test shall be sampled for false. If the correct state of the CO Code Interface Test is not found for either of the circumstances noted above (true, then false) a failure has occurred. A delay of at least 360 µsec shall be allowed between issuance of each character output. Two consecutive failures of this test shall result in setting G&C Coupler Control Monitor Failure and Programmer Group Failure in MOSR within 10 seconds and entry into standby no-go within 5 seconds. See Figure 2-27.

2-16.10. Command Signal Decoder (G) Home Monitor. CSD(G) home monitor shall be monitored every 2 to 5 seconds. If a false state is detected, CSD(G) shall be reset by issuing CSD(G) reset command set character output code and after a delay of 96 to 400 msec, by issuing CSD(G) reset command reset character output code.

2-16.11. Gyro and Gyro Compass Data. The YZ Gyro J term and gyro compass average delta P_n and average delta P_n^2 terms shall be generated.

2-16.12. Gyro Speed Control Monitor. Status monitoring shall select XY and YZ DC Speed Controls (21 and 22) in ADC Spare Channel Select respectively to sample the XY and YZ Gyro Speed Control parameters [GSPD_BUF] at least once every five seconds during Strategic Alert Biasing. If XY Gyro speed Control voltage is not within the limits, $70 \leq$ GSPD_BUF(2) ≤ 96 counts, for three consecutive samples or YZ Gyro Speed Control voltage is not within the limits, $70 \leq$ GSPD_BUF(1) ≤ 96 counts, for three consecutive samples, the Gyro Speed Control Failure MOSR shall be set. If both XY and YZ Gyro Speed Control voltages are within the specified limits for three consecutive samples, Gyro Speed Control Failure shall be reset in MOSR.

2-16.13. MGC SRAM Battery Check. The status of the computer memory backup battery and control circuitry shall be checked once every 60.0 ± 1.0 minutes by sampling the computer memory backup battery voltage input and by checking the state of the Battery Flag discrete as follows:



NOTE: 1. THE INTERFACE TEST WILL NOT BE PERFORMED DURING A MISSILE TEST OR TCD.

2. FAILURE OF THE C.O. CODE INTERFACE TEST–MONITOR TO BE DETECTED TRUE DURING THE DCU SAMPLE INTERVAL 1 OR FAILURE OF THE DCU TO DETECT A FALSE STATE DURING THE DCU SAMPLE INTERVAL 2 SHALL RESULT IN A TEST FAILURE. TWO CONSECUTIVE TEST FAILURES SHALL RESULT IN A DCU STANDBY NO–GO.

SOURCE: ICD 25–65000, VOLUME IX

MMT201_130k

Figure 2-27. Interface Test Sequential Timing Diagram

a. Select Backup Battery Voltage Monitor by setting ADC Cycle Select in Flight Control Select/Event Markers to Stage 1.

b. Delay at least 2 msec and obtain the memory backup battery voltage reading by sampling Stage Auxiliary Monitor 1.

c. Calibrate the memory backup battery voltage reading.

d. Obtain the state of Battery Flag discrete by sampling MIA Error/Status register.

e. If the backup battery voltage is less than 5.2 volts, or the battery flag discrete is true (1-set), the Computer Battery Failure/Off MOSR bit shall be set as an alarm. Otherwise, the MOSR shall be reset.

2-17. CIRCUMVENTION RESET. Remote Communications performs the operations necessary to detect the occurrence of a Circumvention Reset (C/R) and NEP events and perform the processing to recover from their effects. A C/R is defined to have occurred when the circumvention reset indicator is detected true. A NEP event is defined to have taken place when an NEP interrupt occurs. Circumvention reset detection and recovery is required for all modes of program operation which are divided into the communications mode, missile test mode and terminal countdown mode.

a. The communications mode subfunction detects C/R and NEP events during all modes of operation except missile test and terminal countdown. In addition, this function performs the operations necessary to recover from the effects of C/R and NEP events and protect the system from a hostile environment. When an NEP interrupt occurs, a circumvention reset is also defined to have occurred.

b. The missile test mode subfunction detects C/R events which have occurred during missile test and performs the operations necessary to recover from the effects of C/R and protect the system from a hostile environment.

c. The terminal countdown mode subfunction detects C/R events during terminal countdown and performs the operations necessary to recover from the effects of C/R where required and protect the system from a hostile environment where required.

2-18. MINUTEMAN POWER PROCESSOR. See Figure 2-28. The Minuteman Power Processor (MPP) is RPIE used to control commercial power, standby power, and ASU in the LF. The MPP at the LCF operates similar to the LF MPP.

2-18.1. Operating Modes. The MPP operates in the following modes:

2-18.1.1. Auto Mode. The auto mode is the principle operating mode for the MPP. The MPP auto mode monitors primary power to the site, controls the transfer to standby power (DEU) and the return to commercial power. See Auto Mode Sequence and Timing Diagram Figure 2-28.

2-18.1.2. Manual Mode. The manual mode allows the DEU to be started and run without being connected to the site. This function is utilized to verify the operational status of the DEU following maintenance.

2-18.1.3. Test Mode. When the test mode is selected via the front panel switch, the MPP will transfer to standby power as when a commercial power fault occurs. The site will remain on standby power for 30 minutes or until the auto mode is selected.

2-18.1.4. Periodic Exercise Mode. A 30-day hardware timer is provided in the MPP. It is reset whenever standby power is successfully connected to the site. If the 30-day timer

expires, the DEU is started and monitored for 60 minutes. If during the exercise period the monitored DEU output fails four times or any DEU discrete becomes active, the site will be returned to commercial power and the DEU will be locked out. A failure during any DEU test will be indicated by the standby power fail and DEU inhibit LED on the MPP front panel.

2-18.2. Function. The MPP will provide switching under the following conditions:

2-18.2.1. Commercial Power Failure Parameters. Commercial power is disconnected from the site whenever the following out-of-tolerance (fail) conditions are sensed.

a. Abnormal Phase Sequence. Phase sequence error which persists for a time period greater than 150 (±50) milliseconds.

b. High Voltage. Greater than 132 (±1) vac line-to-neutral for 1.9 (±20%) continuous seconds on any phase.

c. Low Voltage. Less than 108 (±1) vac line-to-neutral for 1.9 (±20%) continuous seconds on any phase.

d. Unbalanced Phase. Two consecutive determinations within a 1.9 (±20%) second period in which the difference between any phase and the average of the three phases exceeds 12 vac.

e. Frequency greater than 62 Hz or less than 58 Hz.

2-18.2.2. Commercial and Standby Power Reconnect Parameters. When commercial or standby power is sensed out of tolerance it will not be considered back in tolerance until within the following specified limits.

a. Phase Sequence. Return to A-B-C positive sequence.

b. High Voltage. Line-to-neutral voltage is less than 132 (±1.0) vac on all phases.

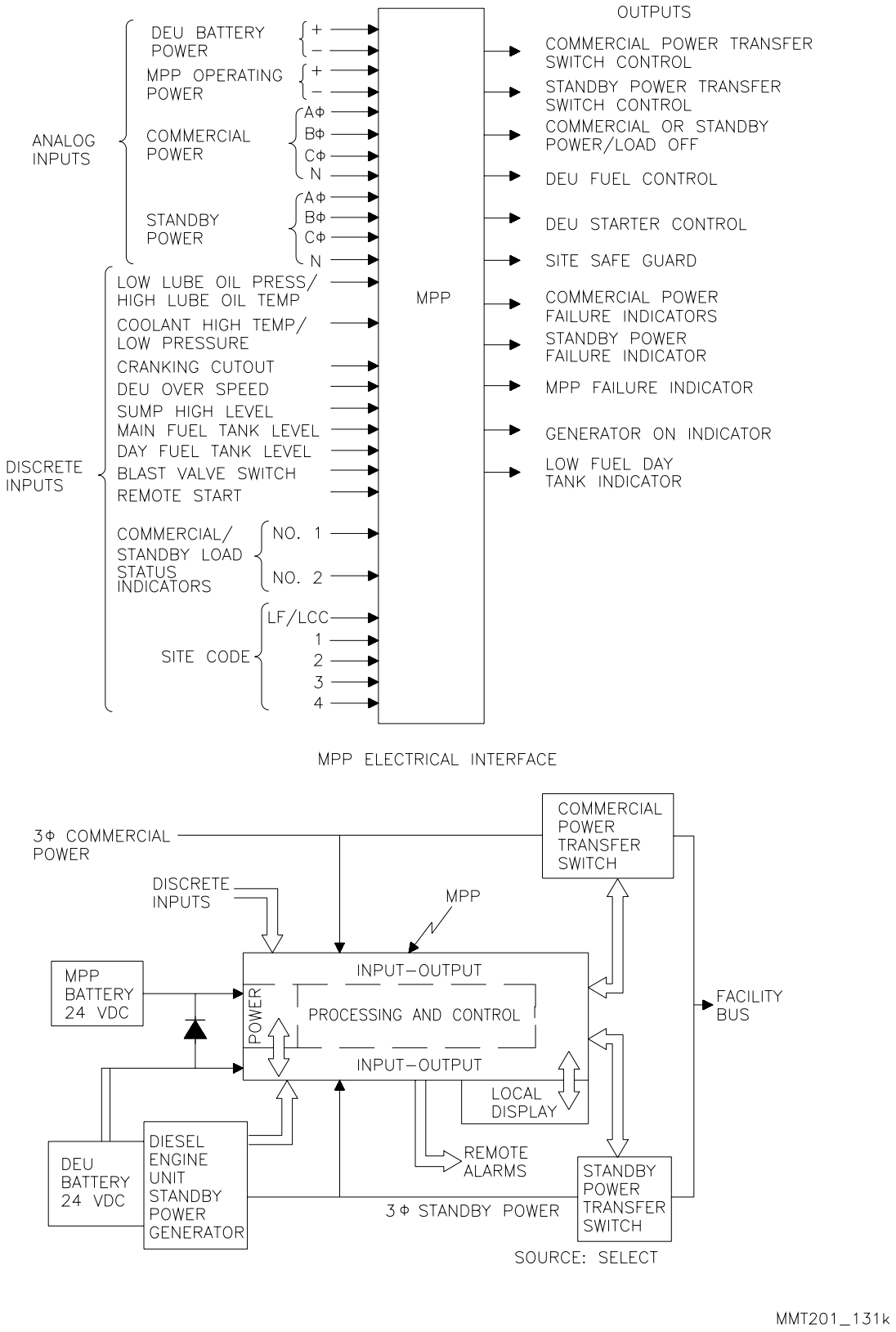


Figure 2-28. MPP Functional Block Diagram and Interface

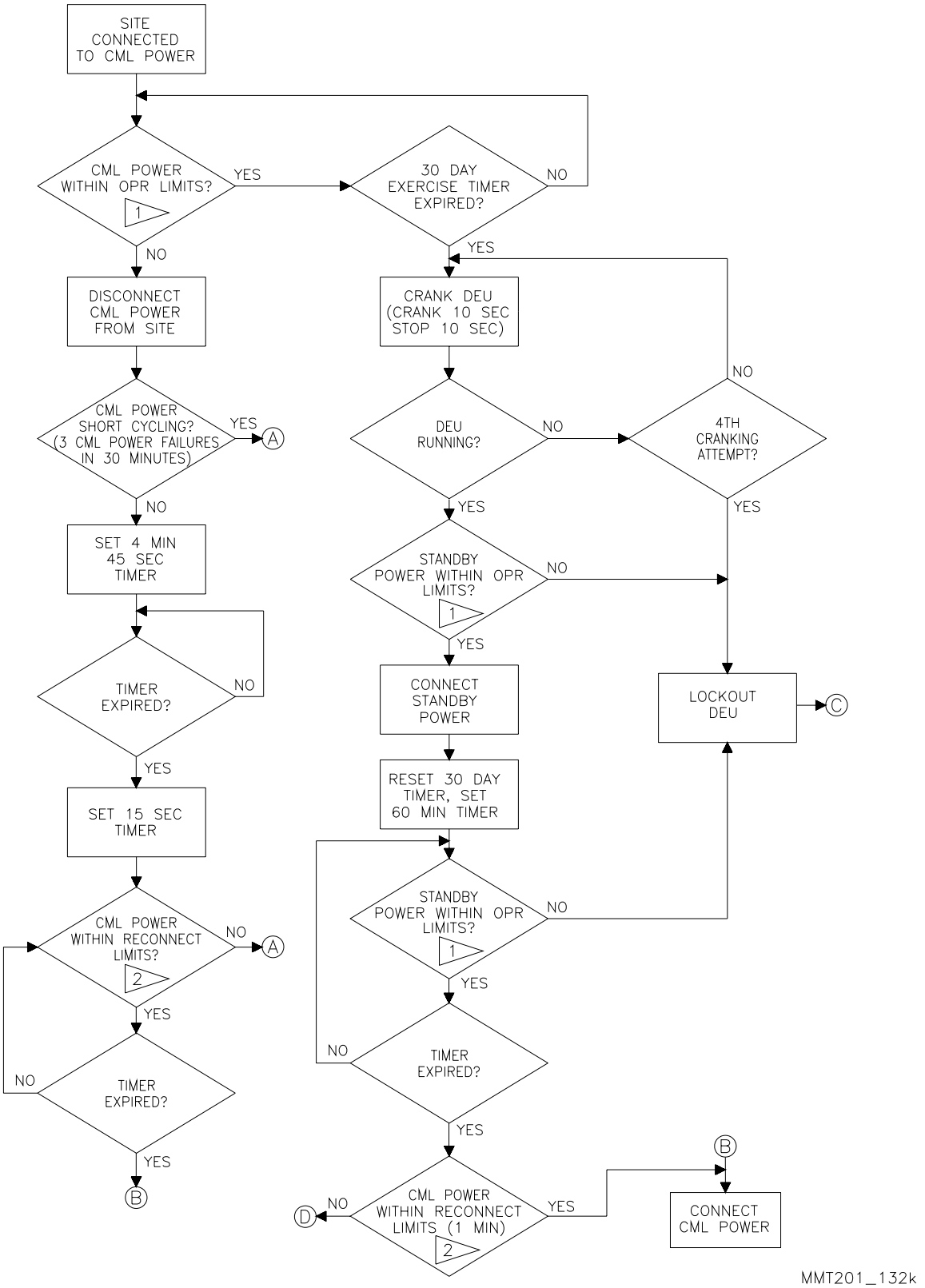


Figure 2-29. MMP Auto-Mode Sequence and Timing Diagram (Sheet 1 of 2)

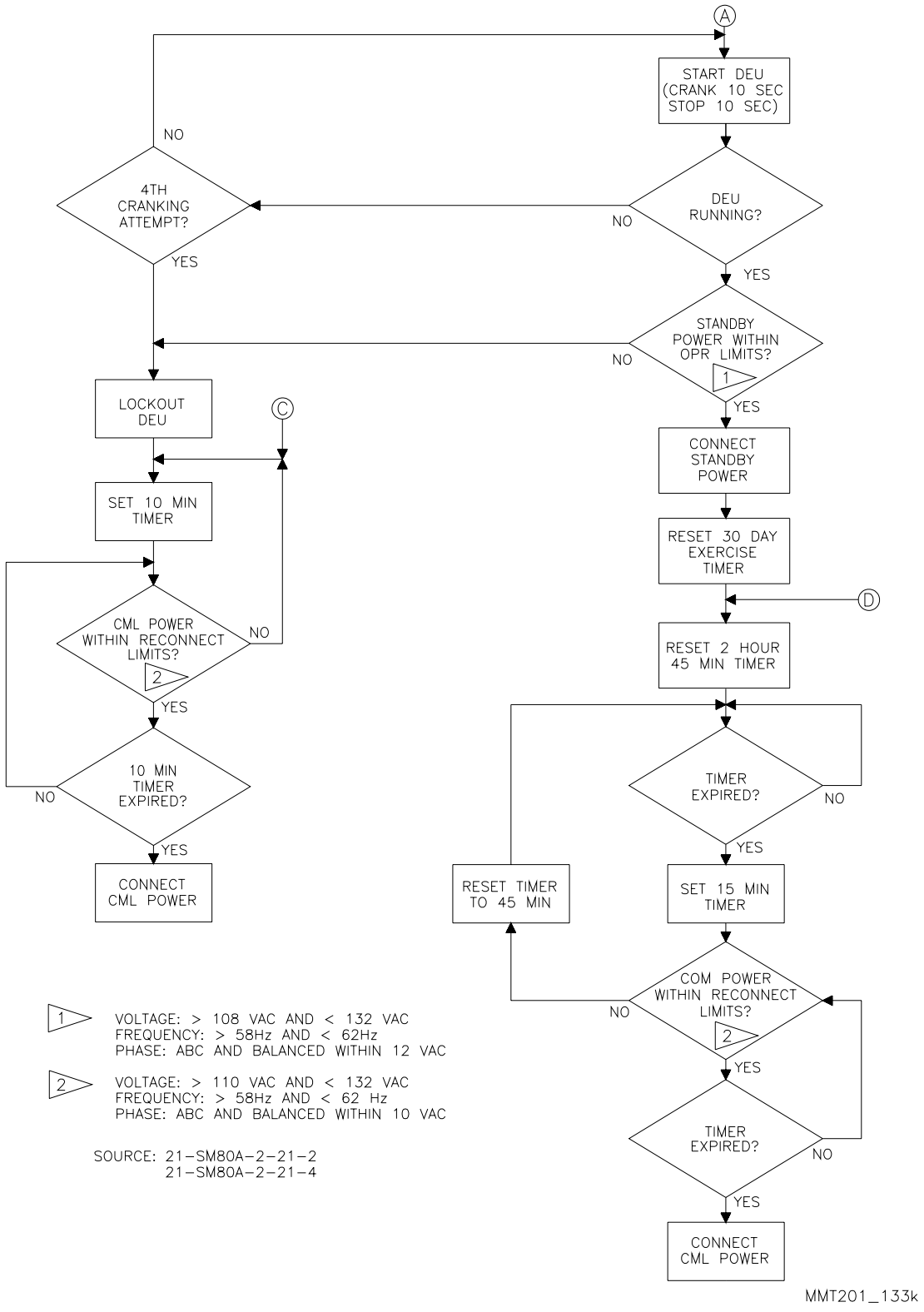


Figure 2-29. MMP Auto-Mode Sequence and Timing Diagram (Sheet 2 of 2)

c. Low Voltage. Line-to-neutral voltage is greater than 110 (±1.0) vac on all phases.

d. Unbalanced Phase. No phase voltage differs from the average of the three phase voltages by 10 or more vac.

e. Frequency less than 62 but greater than 58 Hz.

2-18.2.3. Fast Return to Commercial Power. If standby power fails (4 DEU start attempts), commercial power reconnect parameters will be monitored for 10 minutes. If the reconnect parameters were satisfied for the entire 10 minute period commercial will be reconnected. If the commercial power reconnect parameters were not satisfied, the 10 minute timer will be reset.

2-19. LAUNCHER SECURITY SYSTEM. The Improved Minuteman Physical Security System (IMPSS) provides security monitoring of inner zone (IZ) and outer zone (OZ) launch facility areas. The heart of the system is a computer processor which uses a Z8002 microprocessor. The processor, through signal conditioning circuitry, interfaces with a range gated pulsed Doppler radar system, **[1]** an OZ switch loop, six transducers, **[3] [5]** two transducers, **<** an IZ switch loop and launch facility equipment. A block diagram of the IMPSS system is shown in Figure 2-30. A security system cabling diagram is contained in Section IX. **[1]** The OZ system also monitors a continuity loop in the launcher support building. Detection of either an open or short to ground circuit in this loop causes an OZ alarm.

2-19.1. Outer Zone Function. The OZ system is a monostatic range gated pulsed Doppler radar system operating in the VHF/UHF band at a center frequency of about 300 MHz. The radar provides a single range gate and omnidirectional coverage of the surveillance area. The radar processor uses a Maximum Likelihood Estimation (MLE) algorithm to perform target detection and discrimination. Both target radar cross-section (RCS) and penetration distance are estimated by the processor for target detection assessment.

The system is made up of six major assemblies: antenna, transmitter, receiver, signal processor, interface and timing controller. The antenna assembly includes collinear transmit and receive dipole elements covered by a fiberglass radome. The transmitter and receiver assemblies are contained within the Receiver/Transmitter (R/T) Alarm Set drawer. The transmitter includes a crystal oscillator which is the reference for all RF and timing signals in the system (299.9875 MHz). The transmitter output is approximately 25 ns pulses of RF energy at a PRF of 100 KHz. Each pulse is also phase shifted at a 25 KHz rate in order to generate the 25 KHz intermediate frequency used by the receiver. Due to this phase shifting the transmitted center frequency is 300.0125 MHz.

The receiver is on (range gated) for approximately a 100 ns. The purpose of this is to limit the range of the system surveillance. Objects moving within the surveillance area create

a Doppler shift that is detected by the receiver and in turn processed for target discrimination.

Processing is accomplished by, the Z8002 microprocessor. The processor continuously estimates a targets incremental penetration distance and the target RCS. For a valid alarm, the target must penetrate the surveillance area more than a predetermined distance within a given time, and its RCS must also exceed a predetermined threshold.

The radar timing function controls pulse modulation timing, pulse width, range and A/D conversion. All timing is derived from and phase locked to the RF signal of the master oscillator (299.9875 MHz).

OZ system failure monitoring is accomplished via failsafe signal processing. Failsafe was implemented by monitoring the ambient reflections of the transmitted RF with no moving targets in the surveillance area. This ambient return is termed "DC clutter level". Two conditions are used to determine fault conditions. First, if the DC clutter level amplitude is below a predetermined factory threshold, the drawer will not initialize. Secondly, if the DC clutter level falls below the initialized adaptable failsafe threshold, the R/T Alarm Set will latch the OZ alarm (A9). The DC clutter level is sampled with the first SCNT after power turn-on with IZ switch loop secured. The failsafe threshold is determined from this measured value. If a one second average of the DC clutter level ever falls below the failsafe threshold, the latched OZ alarm is set. Upon receipt of a SCNT, the drawer will reset the alarm if the DC clutter level has returned to a value above the threshold.

In addition to OZ system failure monitoring, the security system monitors for attempts to defeat the system. Such attempts result in latched OZ alarms. The OZ Spoofing Alarm (A8) is latched if an outbound target is detected without an inbound detection. The OZ SAT/JAM Alarm (AB) is latched when the output from the receiver is above the maximum receiver power threshold.

2-19.2. Inner Zone Function. The IZ function processes the IZ transducer data and monitors the IZ continuity loop status discrete. The transducer data is monitored to detect values within a specified vibration signal envelope. Two types of latched alarms can be set due to transducer inputs. 1) IZ High Level (AO) indicates that the input from both transducers exceeds a threshold. 2) IZ Continuous Wave High Level Alarm (A2) indicates that at least one of the transducers has a continuous output which exceeds the threshold. The continuity loop status discrete is monitored for indications of an open or grounded continuity loop. Detection of either causes an IZ Continuity Loop Alarm (A3).

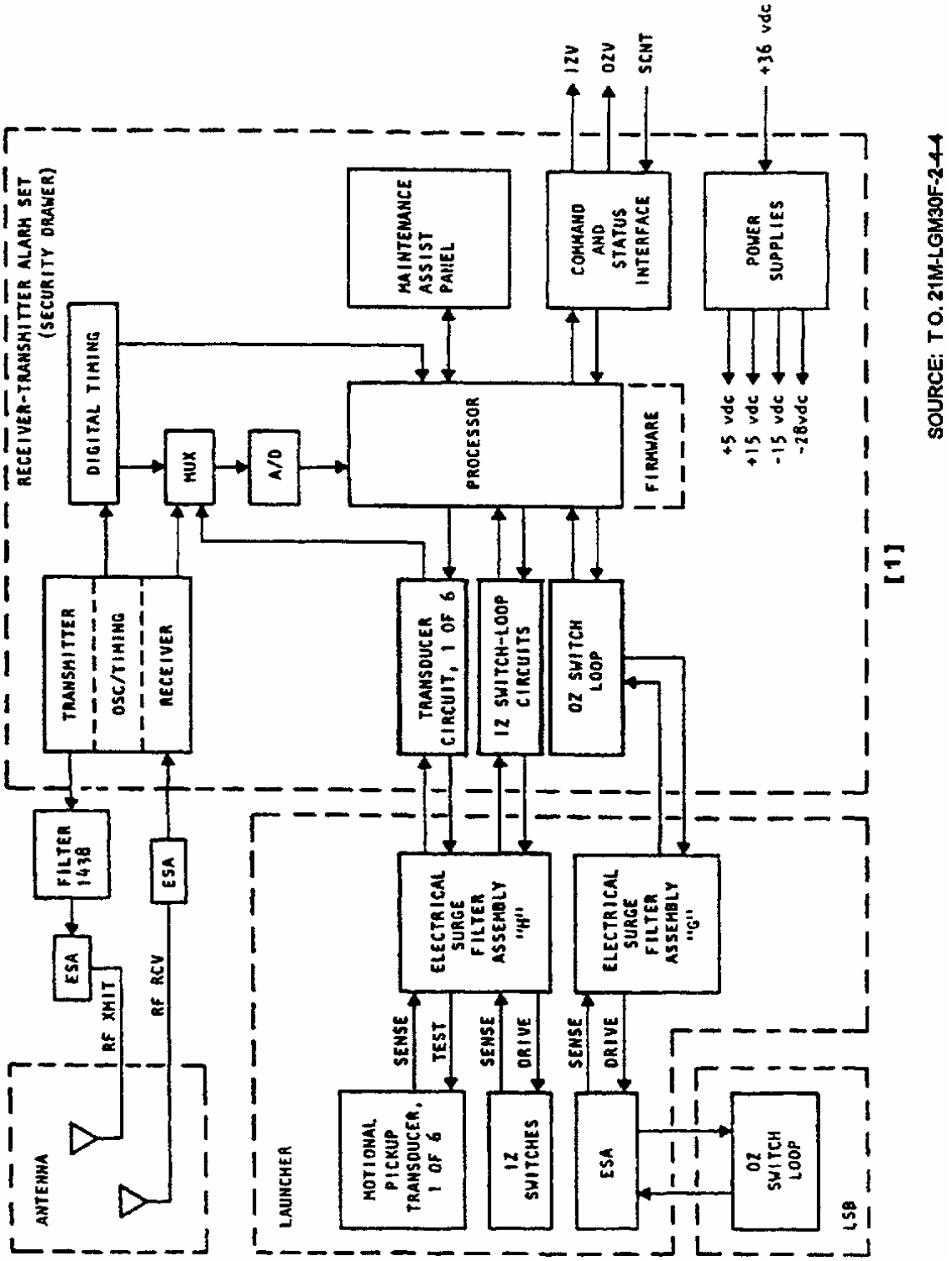


Figure 2-30. Security System Block Diagram (Sheet 1 of 2)

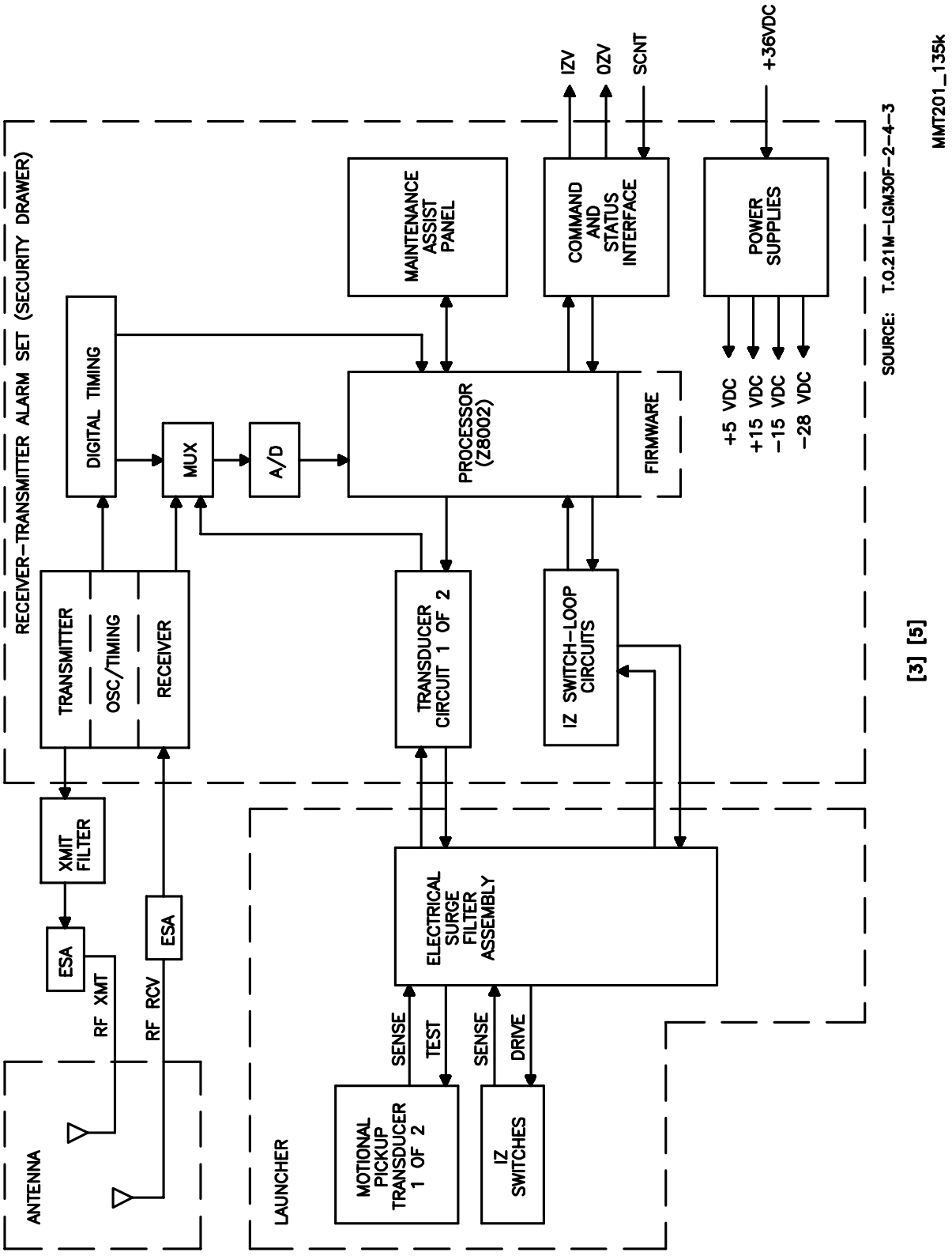


Figure 2-30. Security System Block Diagram (Sheet 2 of 2)

2-19.3. SCNT. Periodic checks of the security system operation may be made remotely from the Launch Control Facility. Upon receipt of a SCNT request, the processor concurrently sets the OZ and IZ violation signals. If the test passes, the OZ and IZ violation signals are reset along with the alarm buffers in approximately 7 to 11 seconds. If a fault is detected during the test sequence, the OZ and IZ violation signals are maintained until the conduct of a subsequent SCNT. If an OZ and/or IZ alarm and/or fault condition is detected during the test sequence, the applicable OZ and/or IZ alarm signals will be set for normal reporting periods. SCNT and periodic self tests perform the following functions:

a. RAM verification test

b. ROM verification test

c. Processor instruction test

d.* Keep-alive timer timeout test

e. IZ transducer test

f. IZ continuity loop test

g. OZ continuity loop test

h.* Reset buffers to zero

* Performed only during SCNT

2-19.4. OZ and IZ Alarm Reporting. The programmer group message processor drawer (Figure A 1201-A4) processes the OZ and IZ alarms from the R/T alarm set and reports alarm status via the OSR to the LCC. The R/T alarm set will report an outer or inner zone alarm to the message processor drawer for a minimum of 40 seconds for a detected violation. The message processor drawer will, in turn, report the alarm in the OSR for a minimum of 5.1 minutes. If a violation is being reported by the R/T alarm set at the end of the message processor 5.1 minute timer the alarm will continue to report in the OSR for an additional 5.1 minutes. The alarm indication will not clear from the OSR until the message processor 5.1 minute timer expires at a time when the R/T alarm set is not reporting a violation. During the course of a facility "back-out" operation where a team is departing an LF, a series of three SCN tests may be required to clear and validate the outer zone function of the security system. The first SCNT will clear any latched OZ or IZ alarm that is set, provided the source of the alarm is not still present. The second SCNT will extend by 5.1 minutes the alarm report in the OSR from the time that the SCNT is received by the message processor. Provided that no other violations are present at the end of the 5.1 minute timer, the system will be clear and no violations will be reported. The third SCNT will verify the operation of the security system as would a normal SCNT sent to a clear system. For this sequence of SCN tests to be effective a minimum of 5.1

minutes must have elapsed between each SCNT. If the SCN tests are sent in rapid succession the outer zone violation in the OSR may not clear following the last SCNT.

2-19.5. Maintenance Assist Function. The operator initiated maintenance assist requests are originated from the maintenance assist panel (MAP) controls on the R/T Alarm Set drawer. A maintenance assist function accepts and monitors the maintenance assist function code and the maintenance assist initiate request. The program decodes the requested data and initiates appropriate responses, including the conduct of manual processor and surveillance system self-tests and the retrieval of stored fault and alarm data to be displayed on the MAP. A table of function codes for manually initiated test and maintenance assist functions is shown in Table 2-17. Tables 2-18 through 2-20 define the various alarm, fault and abort displays.

The alarm and fault files may be printed out with any RS232 compatible printer via the J6 connector on the R/T Alarm Set drawer. The following sequence should be followed for printer use:

a. Connect printer to R/T drawer.

b. Connect printer to power.

c. Press test button on printer to test printer.

d. Enter "FA" (Print alarm files) on thumb wheels.

e. Record date and time of "FA" initiate.

f. Press "Initiate" button. "FO4" appears on display.

g. "FO8" appears on display when printing is complete.

h. Enter "FF" (Print fault files) on thumb wheels.

i. Press "Initiate" button. "FO4" appears on display.

j. "FO8" appears on display when printing is complete.

k. Enter "OO" (Exit printing mode) on thumb wheels.

l. Press "Initiate" button.

m. Display blinks Wing ID and then goes blank.

n. Disconnect printer from power and from R/T drawer.

NOTE: Alarm reporting is suspended during print mode.

Table 2-17. Maintenance Assist Panel Thumbwheel Function Codes

CODE	FUNCTIONS
00	BLANK MAP DISPLAY
01	DISPLAY ID OF FIRST NON-ZERO MA FILE FAULT BLOCK
02	DISPLAY OF NEXT ELEMENT IN MA FILE FAULT BLOCK
03	DISPLAY ID OF NEXT NON-ZERO MA FILE FAULT BLOCK
04	DISPLAY TOTAL NUMBER OF ALARMS RECORDED IN MA FILE
05	DISPLAY ID OF MOST RECENT NON-ZERO MA FILE ALARM BLOCK
06	DISPLAY NEXT ELEMENT IN MA FILE ALARM BLOCK
07	DISPLAY ID OF NEXT NON-ZERO MA FILE ALARM BLOCK
08	DISPLAY ID OF PREVIOUS NON-ZERO MA FILE ALARM BLOCK
10	DISPLAY CURRENT OZ/IZ ALARM STATUS
11	DISPLAY OZ/IZ VIOLATION STATUS
C0	**[1]** INITIATE MAP OZ CONTINUITY LOOP TEST **[3>**
C1	INITIATE **[1]** MAP TRANSDUCER 1 TEST**< [3] [5]** TRANSDUCER A TEST**<**
C2	INITIATE **[1]** MAP TRANSDUCER 2 TEST**< [3] [5]** TRANSDUCER B TEST**<**
C3	**[1]** INITIATE MAP TRANSDUCER 3 TEST
C4	**[1]** INITIATE MAP TRANSDUCER 4 TEST
C5	**[1]** INITIATE MAP TRANSDUCER 5 TEST
C6	**[1]** INITIATE MAP TRANSDUCER 6 TEST
C7	INITIATE MAP IZ CONTINUITY LOOP TEST **[3>**
C8	INITIATE MAP ROM TEST
C9	INITIATE MAP RAM TEST
CA	INITIATE MAP INSTRUCTION TEST
CB	INITIATE MAP SYSTEM TEST SEQUENCE **[1>**
DC	DISPLAY OZ CLUTTER VALUE **[2>**
DO	VERIFY CODE FOR MA FILE CLEAR REQUEST
EA	PRIMARY CODE FOR MA ALARM FILE CLEAR REQUEST
EF	PRIMARY CODE FOR MA FAULT FILE CLEAR REQUEST
FA	PRINT ALARM FILE
FF	PRINT FAULT FILE
F0	HALT PRINTING

[1> Does not include Watchdog timer test

[2> Available only when drawer is connected to test adapter at SMSB or depot

[3> C0 and C7 checks for voltage on continuity loop only when the drivers are turned off.

Source: S-133-01516

Table 2-18. Maintenance Alarm File

MAP DISPLAY	ALARM
[A] [0] [ ]	IZ HIGH LEVEL ALARM **[1>**
[A] [1] [ ]	IZ LOW LEVEL ALARM
[A] [2] [ ]	IZ CONTINUOUS WAVE HIGH LEVEL ALARM **[1>**
[A] [3] [ ]	IZ CONTINUITY LOOP ALARM
[A] [6] [ ]	OZ LOW BAND INTRUSION EGRESS ALARM (RF ALARM)
[A] [7] [ ]	OZ LOW BAND INTRUSION INGRESS ALARM (RF ALARM)
[A] [8] [ ]	OZ SPOOFING ALARM (RF ALARM) **[1> [2>**
[A] [9] [ ]	OZ FAILSAFE ALARM (RF ALARM) **[1>**
[A] [B] [ ]	OZ DATA SATURATION ALARM **[1>**
[A] [C] [ ]	**[1]** OZ CONTINUITY LOOP ALARM

[1> Latched Alarms

[2> A8 prints out as "OZ INT"

Source: **[3] [5]** T.O. 21M-LGM30F-2-4-3
[1] T.O. 21M-LGM30F-2-4-4

Table 2-19. Maintenance Fault File

MAP DISPLAY	FAULT
[F] [0] [ ]	R/T ALARM SET DRWER IZ CURRENT FAULT
[F] [1] [ ]	**[1]** IZ TRANSDUCER 1 FAULT **[3] [5]** IZ TRANSDUCER A FAULT **<**
[F] [2] [ ]	**[1]** IZ TRANSDUCER 2 FAULT **[3] [5]** IZ TRANSDUCER B FAULT **<**
[F] [3] [ ]	**[1]** TRANSDUCER 3 FAULT
[F] [4] [ ]	**[1]** TRANSDUCER 4 FAULT
[F] [5] [ ]	**[1]** TRANSDUCER 5 FAULT
[F] [6] [ ]	**[1]** TRANSDUCER 6 FAULT
[F] [7] [ ]	ROM TEST FAULT
[F] [8] [ ]	RAM TEST FAULT
[F] [9] [ ]	INSTRUCTION TEST FAULT
[F] [A] [ ]	CPCI PERFORMANCE FAULT
[F] [B] [ ]	KEEP-ALIVE TIMER TEST FAULT
[F] [C] [ ]	OZ FAIL SAFE FAULT (RF MODULE)
[F] [D] [ ]	OZ SYNCHRONIZATION FAULT (RF MODULE)
[F] [E] [ ]	**[1]** R/T ALARM SET DRAWER OZ CURRENT FAULT
[F] [F] [ ]	OZ INITIALIZATION FAULT (RF MODULE)

Source: **[3] [5]** T.O. 21M-LGM30F-2-4-3
[1] T.O. 21M-LGM30F-2-4-4

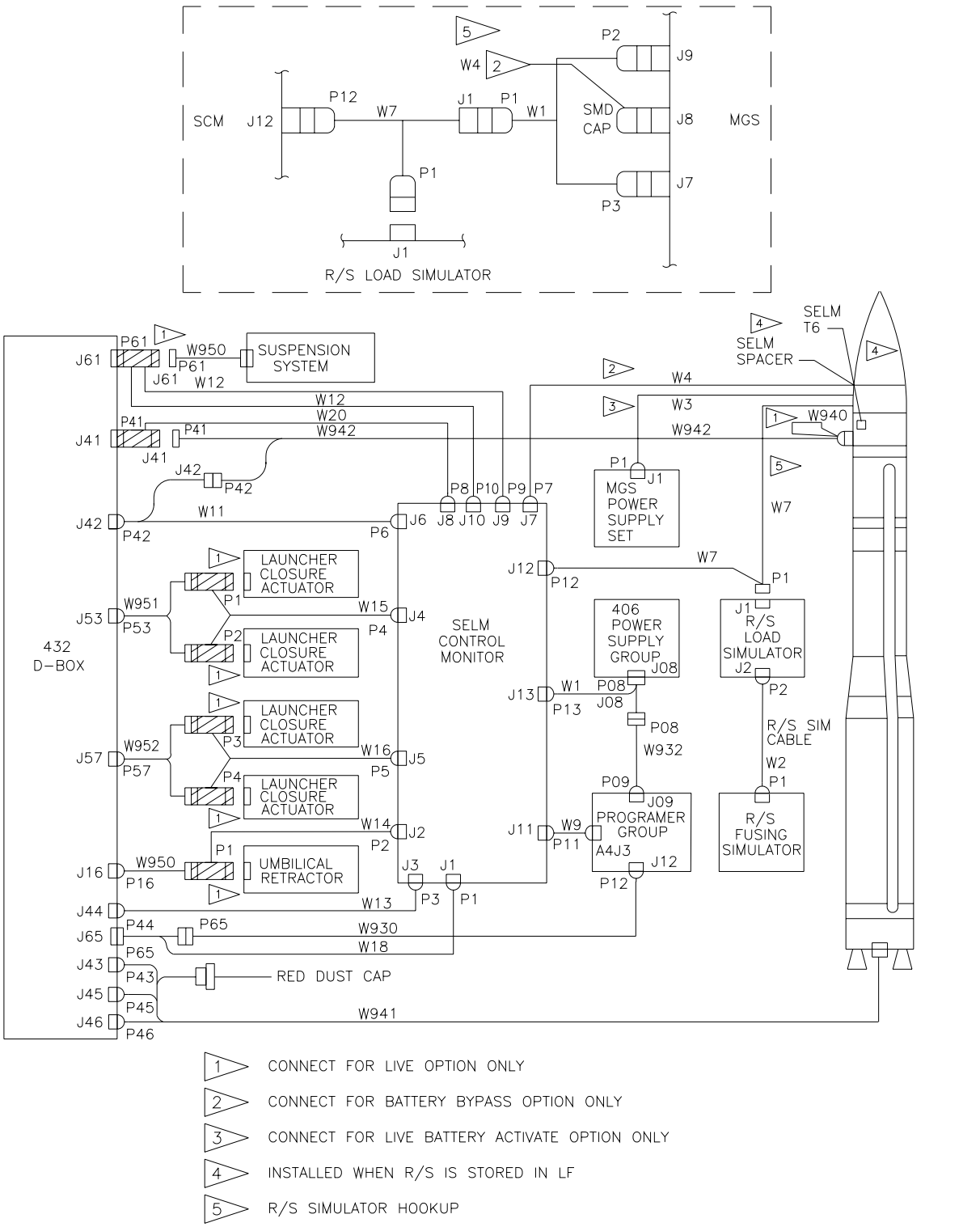
Table 2-20. Abort Displays

MAP DISPLAY	FAULT
[0] [0] [0]	PROCESSOR FAILURE
[0] [A] [0]	KEEP-ALIVE TIMEOUT SELF-TEST FAULT
	PROCESSOR INSTRUCTION FAULTS:
[0] [A] [1]	EXTENDED INSTRUCTION TRAP
[0] [A] [2]	PRIVILEGED INSTRUCTION TRAP
[0] [A] [3]	SEGMENT/ADDRESS TRAP
[0] [A] [4]	INVALID SELF-TEST INSTRUCTION
	PROGRAM PERFORMANCE FAULTS:
[0] [A] [5]	OZ TASK TIMEOUT
[0] [A] [6]	IZ TASK TIMEOUT
[0] [A] [7]	ALARM MANAGEMENT TIMEOUT
[0] [A] [8]	EXCESSIVE SLACK TIME
[0] [A] [9]	STACK BOUNDARY VIOLATION
[0] [A] [B]	SELF-TEST TASK TIMEOUT
[0] [A] [F]	ROM SELF-TEST FAULT

Source: **[3] [5]** T.O. 21M-LGM30F-2-4-3
[1] T.O. 21M-LGM30F-2-4-4

2-20. SELM TESTING. Simulated launches are conducted periodically at operational launch facilities to assess their capability to complete a successful launch. Special SELM equipment is installed to monitor the terminal countdown and provide ordnance isolation to safely conduct the test. The equipment installation is shown in Figure 2-31. The interlock circuit provided to ensure proper equipment installation is shown in Figure 2-32. The command codes, used to enter and extract information from the SELM test set, are given in Table 2-21. SELM TCD failure codes are given in Table 2-22. See the appropriate SELM T.O. for more detailed information.

With SELM equipment installed, and powered up, a remote missile test will cause the SELM Control Monitor to erroneously enter SELM Terminal Countdown (TCD). At the end of the SELM TCD, the SELM Control Monitor will remove power from the MGS, shutting down the LF.



SOURCE: T.O. 21M-LGM30G-1-17

MMT201_136K

Figure 2-31. SELM Test Set Hookup

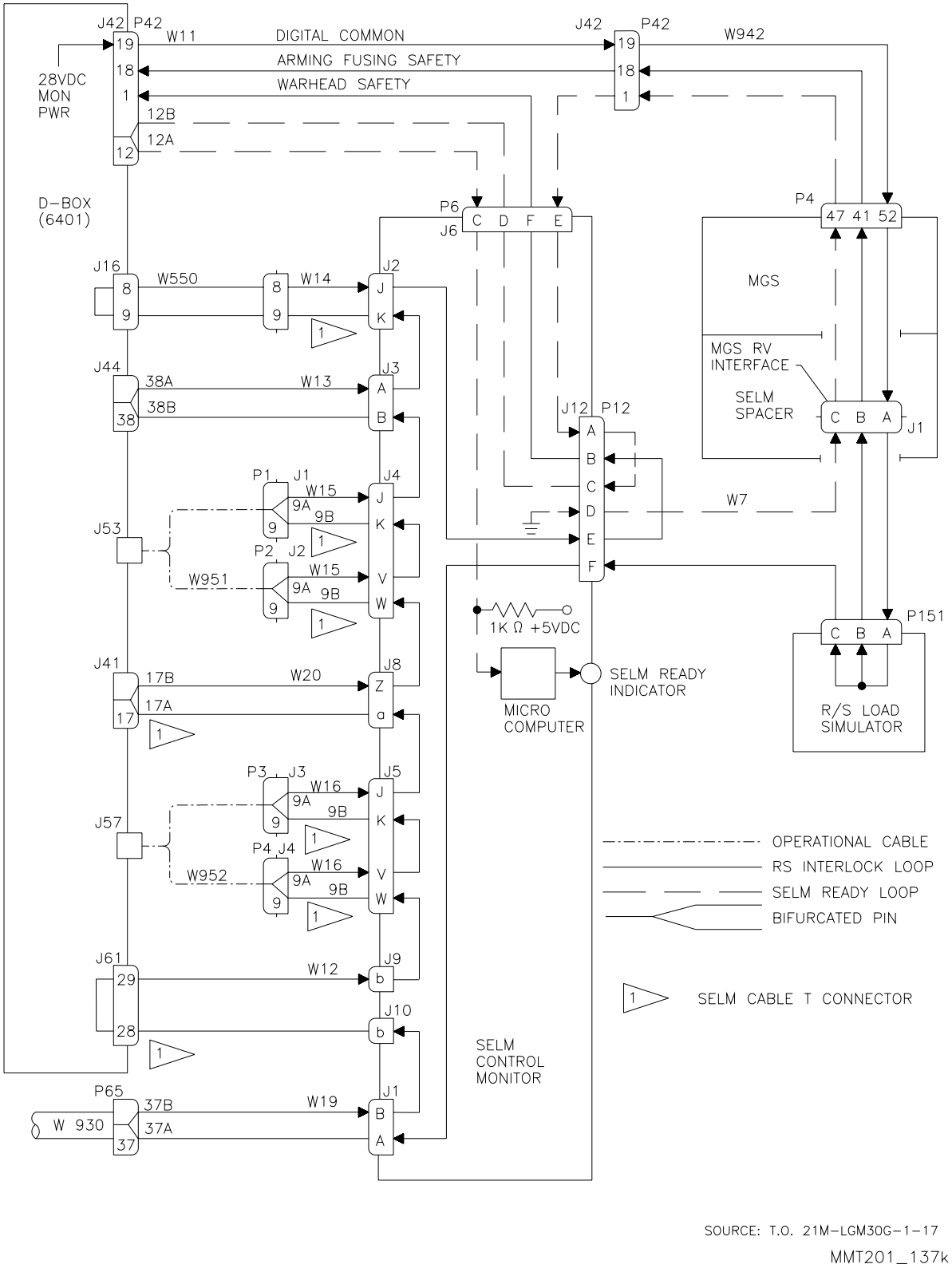


Figure 2-32. SELM Test Interlock Circuit

Table 2-21. SELM Command Codes

CODE	FUNCTION
000	Switch Test (Print Position of Ordnance Switches and Each Entry of Thumbwheel Data until "FFF" is entered)
001	Time Sync (Enter Time & Date)
002	Data Entry (Enter Site Data and Year)
003	Printer Test (Print Time, Site Data & Test Pattern)
004	Status Test (Set TCD Go Status & Clear Ready Status)
005	Status Reset (Clear TCD Go status and Set Ready Status)
006	SSMU Test (Write Site Data to SSMU and Verify Rest of SSMU is Blank)
007	SSMU Read (Transfer SSMU Data to TCD Buffer and Calculate/Print Checksum)
008	TCD Data Print (Print Detailed TCD Evaluation Data)
009	SSMU Erased Test (Check to see if Entire SSMU is Blank)

Table 2-22. SELM TCD Failure Codes

SCM PRINTOUT	DESCRIPTION	
	Failure	Surefire Level
001	BT3 - ACTIVATE BATTERY STAGE III	13.328v
002	MSS1A - ACTIVATE LATERAL RESTRAINT-1A	4.90v
003	MSS1B - ACTIVATE LATERAL RESTRAINT-1B	4.90v
004	MSS2A - ACTIVATE LATERAL RESTRAINT-2A	4.90v
005	MSS2B - ACTIVATE LATERAL RESTRAINT-2B	4.90v
006	MSS3A - ACTIVATE LATERAL RESTRAINT-3A	4.90v
007	MSS3B - ACTIVATE LATERAL RESTRAINT-3B	4.90v
008	MSS4A - ACTIVATE LATERAL RESTRAINT-4A	4.90v
009	MSS4B - ACTIVATE LATERAL RESTRAINT-4B	4.90v
010	MSS5A - ACTIVATE LATERAL RESTRAINT-5A	4.90v
011	MSS5B - ACTIVATE LATERAL RESTRAINT-5B	4.90v
012	MSS6A - ACTIVATE LATERAL RESTRAINT-6A	4.90v
013	MSS6B - ACTIVATE LATERAL RESTRAINT-6B	4.90v
014	LID3A - REMOVE LAUNCHER CLOSURE-3A	5.096v
015	LID3B - REMOVE LAUNCHER CLOSURE-3B	5.096v

Table 2-22. SELM TCD Failure Codes (Continued)

SCM PRINTOUT	DESCRIPTION	
	Failure	Surefire Level
016	LID4A - REMOVE LAUNCHER CLOSURE-4A (OR - Critical Leads Disconnect and both circuits of Release G&C Umbilical did not follow all eight signals of Remove Launcher Closure.)	5.096v
017	LID4B - REMOVE LAUNCHER CLOSURE-4B (OR - Both circuits of Retract G&C Umbilical did not follow Critical Leads Disconnect and both circuits of Release G&C Umbilical.)	5.096v
018	LID1A - REMOVE LAUNCHER CLOSURE-1A (OR - Both circuits of First Stage Ignition did not follow both circuits of Retract G&C Umbilical.)	5.096v
019	LID1B - REMOVE LAUNCHER CLOSURE-1B	5.096v
020	LID2A - REMOVE LAUNCHER CLOSURE-2A	5.096v
021	LID2B - REMOVE LAUNCHER CLOSURE-2B	5.096v
022	RTRA - RETRACT G&C UMBILICAL - A	5.096v
023	RTRB - RETRACT G&C UMBILICAL - B	5.096v
024	RLSA - RELEASE G&C UMBILICAL - A	5.096v
025	RLSB - RELEASE G&C UMBILICAL - B	5.096v
026	CLD - CRITICAL LEADS DISCONNECT	6.664v
027	BT1 - ACTIVATE BATTERY STAGE I	13.328v
028	IGNA - IGNITE FIRST STAGE - A	6.46v
029	IGNB - IGNITE FIRST STAGE - B	6.46v
030	ORD - ARM MISSILE ORDNANCE	0.0v
	NOTE: Failures 1 thru 30 indicate an ordnance signal pulse failed to exceed the applicable surefire voltage level for a minimum 20 ms pulse width.	
031 to 035	Not Used	
036	BATTERY ACTIVATE STAGE I, BATTERY ACTIVATE STAGE III and 12 CIRCUITS OF RELEASE LATERAL RESTRAINTS ORDNANCE did not follow FLIGHT CONTROL and NCU POWER ON.	
037	ARM MISSILE ORDNANCE DEVICES did not follow BATTERY ACTIVATE STAGE I, BATTERY ACTIVATE STAGE III, and 12 circuits of RELEASE LATERAL RESTRAINTS	
	Failure	

Table 2-22. SELM TCD Failure Codes (Continued)

SCM PRINTOUT	DESCRIPTION
038	ALL EIGHT SIGNALS OF REMOVE LAUNCHER CLOSURE ORDNANCE did not follow ARM MISSILE ORDNANCE DEVICES
039 to 047	Not Used
048	The REMOVE LAUNCHER CLOSURE signals did not precede FIRST STAGE IGNITION signals by 6 to 8 seconds
049	The ACTIVATE LATERAL RESTRAINTS signals did not precede FIRST STAGE IGNITION signals by 11 to 13 seconds
050	The FLIGHT CONTROL and NCU POWER ON signal was on less than 5.0 seconds long
051	The BATTERY ACTIVATE signals did not occur between 1.0 and 14.5 seconds after the start of FLIGHT CONTROL POWER ON signal
052	The ARM MISSILE ORDNANCE DEVICE signal did not start a minimum of 5.3 seconds after BATTERY ACTIVATE signals
053 to 098	Not Used
099	The time from TCD start to FIRST STAGE IGNITION was greater than 30.0 seconds

SOURCE: T.O. 21M-LGM30G-1-17

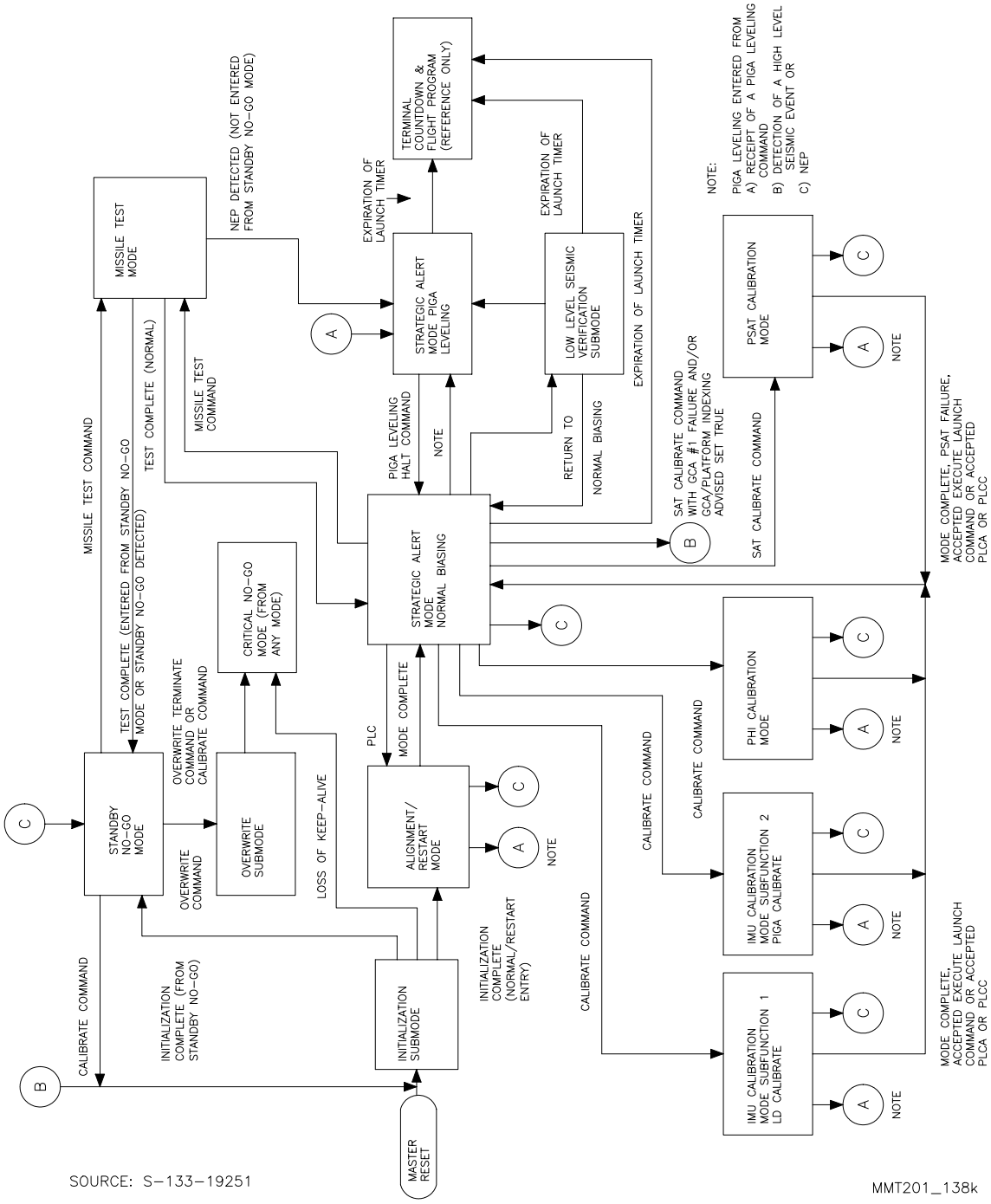


Figure 2-33. Missile Operational Modes and Submodes

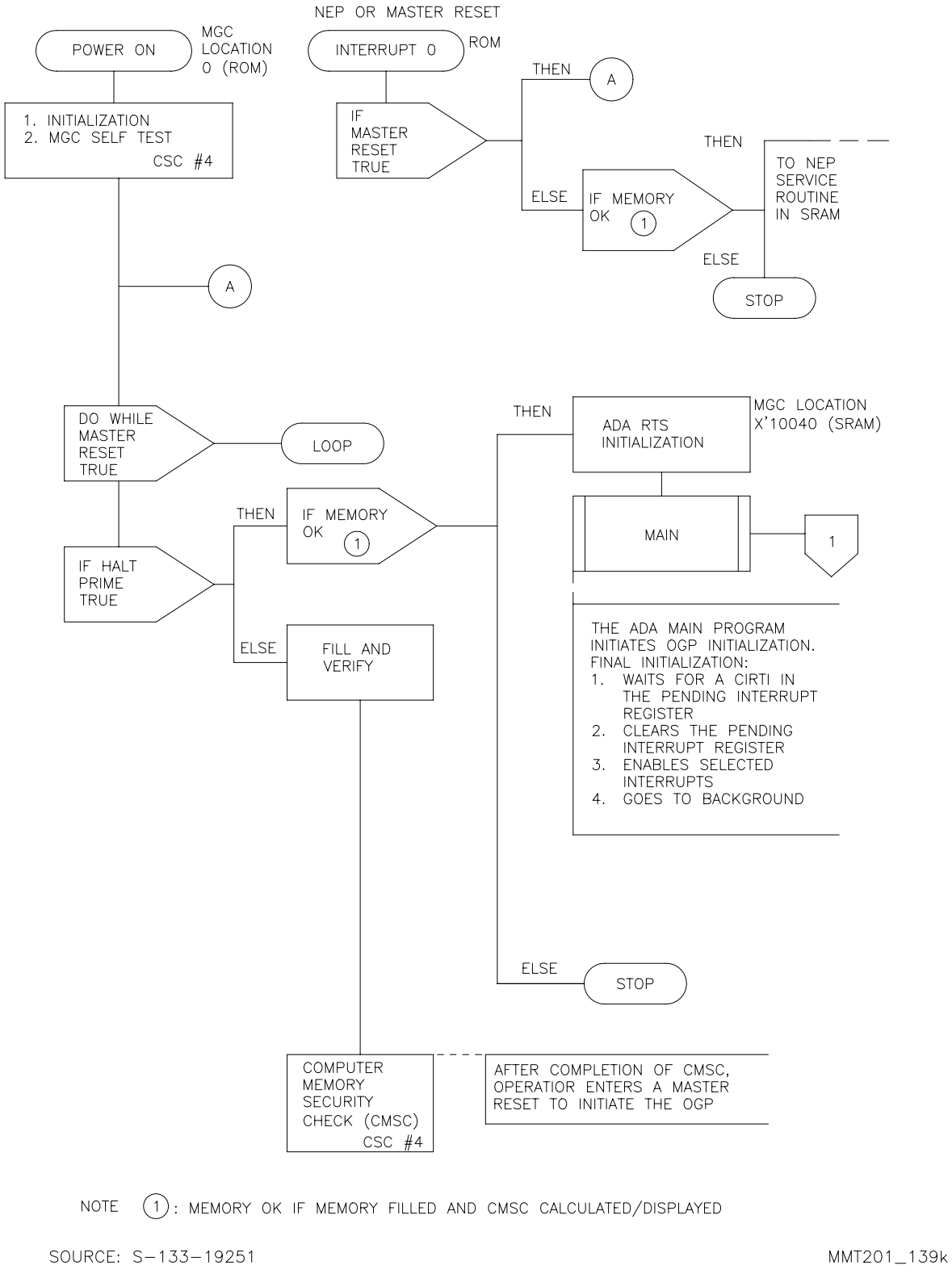


Figure 2-34. GRP OGP Task Level Overview (Sheet 1 of 2)

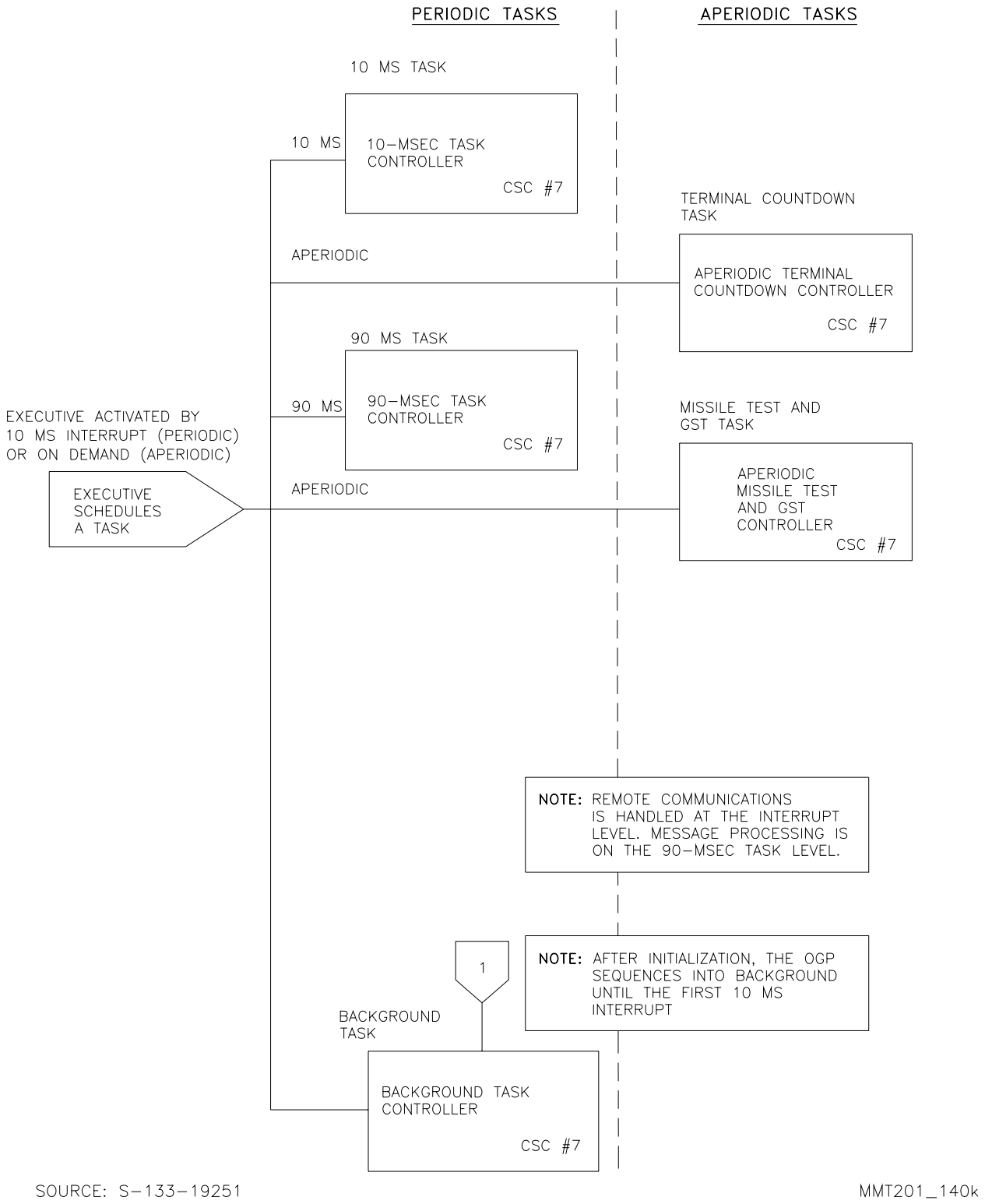
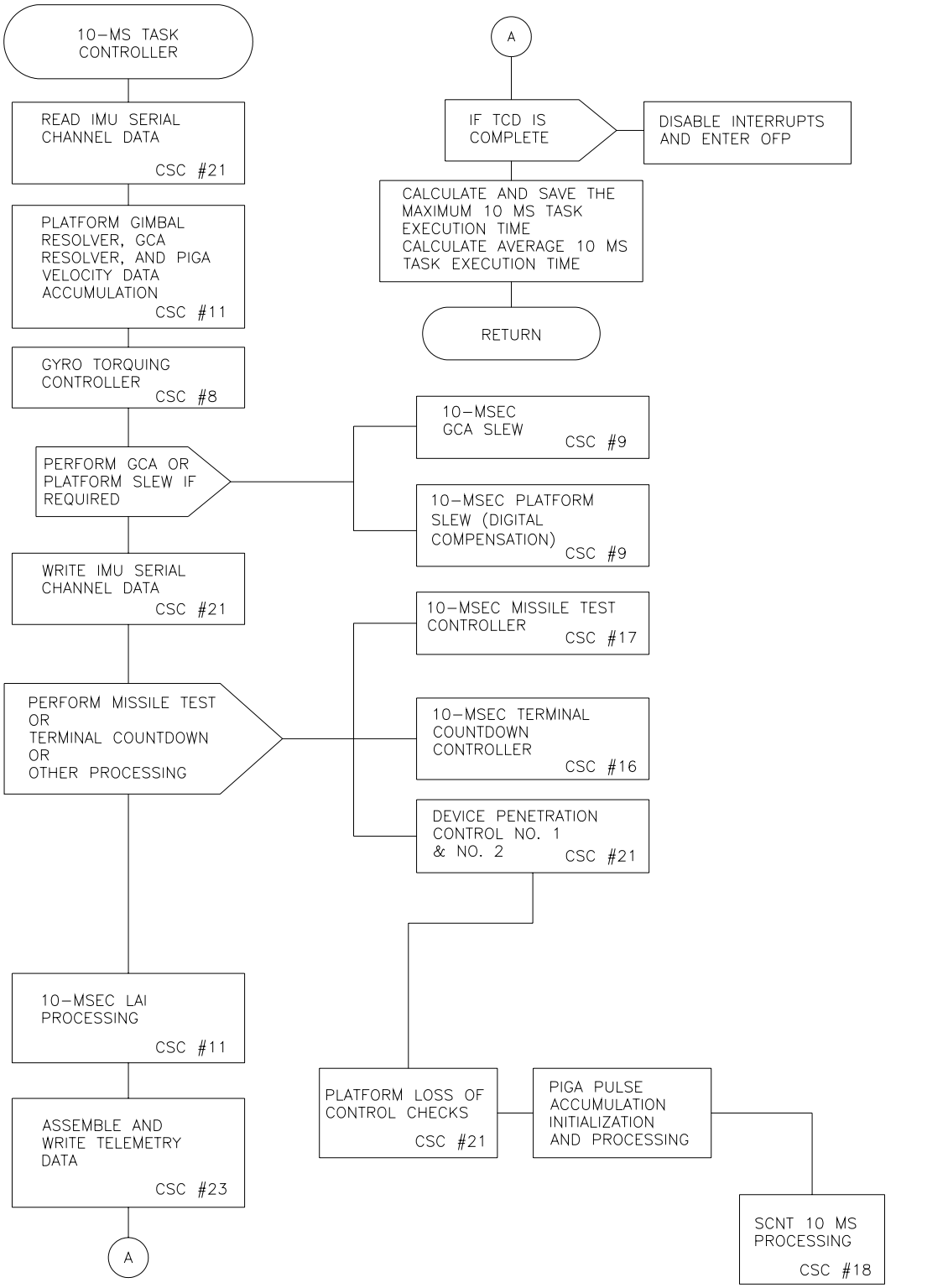


Figure 2-34. GRP OGP Task Level Overview (Sheets 2 of 2)



SOURCE: S–133–19251 MMT201_141k

Figure 2-35. 10-msec Task Controller (CSC #7)

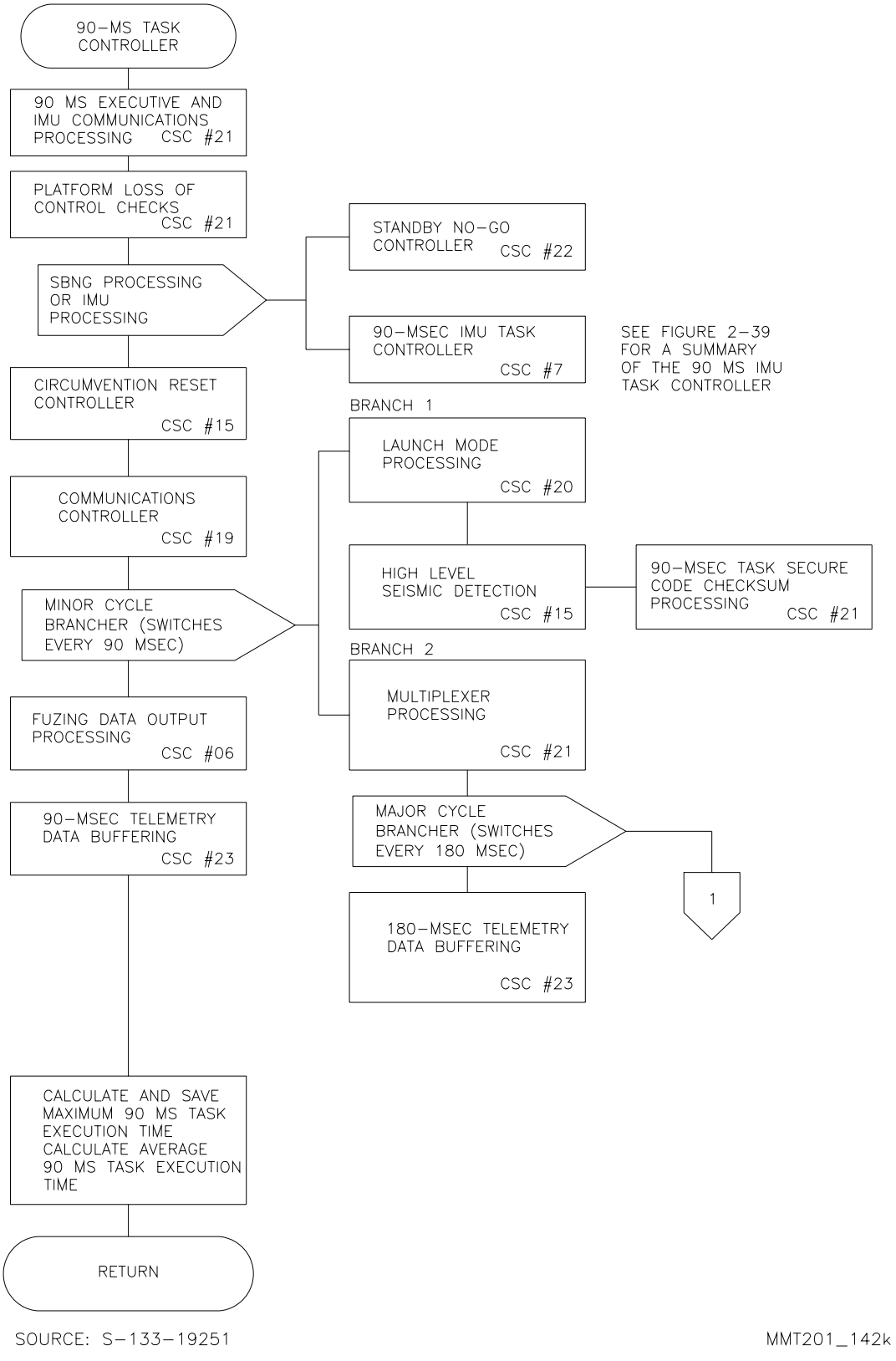


Figure 2-36. 90-msec Task Controller (CSC #7) (Sheets 1 of 3)