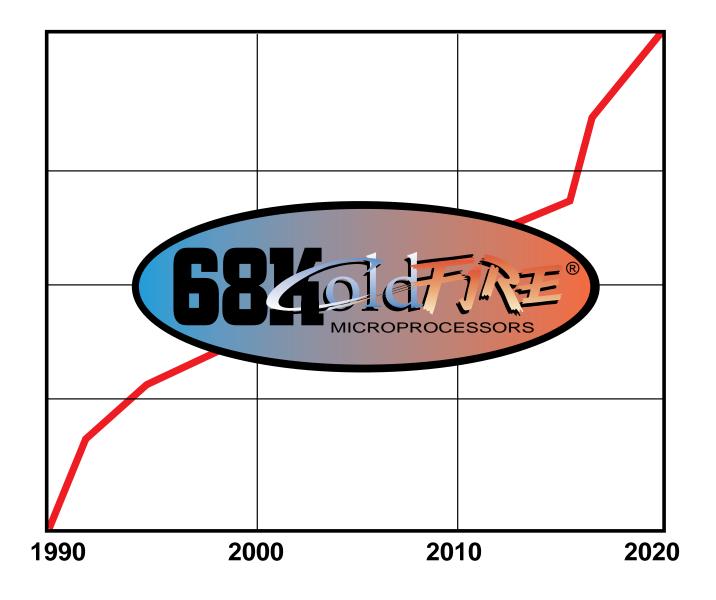
Motorola's ColdFire® Microprocessor Architecture: Setting the Standard for the Future





Motorola's 68K ColdFire® Microprocessor: Bringing the Future to the Legend

INTRODUCTION

In 1994, the innovative ColdFire® Microprocessor Family was added to Motorola's 68K Family tree. This new variable-length RISC 68K Family member delivers the necessary aggressive price/performance required by the cost-sensitive embedded market. In striving to meet the needs of the market with this innovative architecture, Motorola evaluated high-level source code from many 68K embedded systems customers. Among the positive results of this study were a reduced instruction set and addressing modes with which we created an efficient environment for processor operation. Like most RISC processors, the majority of ColdFire processor instructions can execute in a single cycle.

The variable-length RISC ColdFire architecture gives customers greater flexibility to lower memory and system costs. Because instructions can be 16-, 32- or 48-bits long, code is packed tighter in memory resulting in better code density than traditional 32- and 64-bit RISC machines. More efficient use of on-chip memory reduces bus bandwidth and the external memory required, which results in lower system cost.

Small and inexpensive, the static ColdFire core also lowers system cost because it is completely synthesizable and easily integrated with memories, system modules, and peripherals. Because of its portable nature, the ColdFire core is easily targeted to different process technologies, making it attractive as a standard offering in our semicustom FlexCore Library and as a product for third-party licensing. To date, Hewlett-Packard and Mitsubishi have licensed the ColdFire core technology. Motorola is currently developing additional strategic alliances.

With its architectural relationship to the 68K Family, customers using 68K products should consider a standard ColdFire product as their next solution. Because the ColdFire processor instruction set is a subset of the 68K Family instruction set, existing 68K customers should discover that designing with ColdFire microprocessors is a smooth transition. Current 68K tools developers should also find that the newest member of the 68K Family is easy to support. Moreover, the ColdFire architecture has a product performance roadmap that extends beyond the 68K Family to provide 300 MIPS in the year 2001, with highly integrated offerings that will include DRAM and FLASH in the near future. Thus, ColdFire processors will provide a performance path for every member of the 68K Family.

The ColdFire product portfolio offers a wide mix of performance, price, integration and debugging capabilities for embedded designers looking to upgrade their systems. The ColdFire product development tools offerings are unmatched—its integration possibilities are limited only by imagination, and its 18-year history of 68K legacy is something no other competitor can offer. With these features to work with, we see the ColdFire architecture as the leading 32-bit embedded architecture. You are invited to become a part of its success.

COLDFIRE PRODUCT PORTFOLIO

To date, six standard products are available in the ColdFire microprocessor family as shown in Figure 1. The MCF5102, called "The bridge chip to ColdFire processors," allows customers to execute both MC68EC040 code and ColdFire code, making a seamless transition from 68K to ColdFire products.

The MCF5202 was the first processor designed with the Version 2 ColdFire core. The MCF5202 contains a 2K unified, 4-way set associative cache and a multiplexed 32-bit bursting bus. Real-time trace and background debug are available in the unique Debug module integrated into the MCF5202 and all other ColdFire devices. The 16-bit multiplexed MCF5203 has the same design as the MCF5202 but is optimized for high performance on a 16-bit data bus at low system cost.

The MCF5204 integrates a Version 2 core with a 512-byte instruction cache, a 512-byte SRAM, a universal asynchronous/synchronous receiver-transmitter (UART), chip-selects, autovector generation, two general-purpose timers, a watchdog timer, and the debug module. System integration on the device supplies nonmultiplexed address and data lines that interface gluelessly to 8- and 16-bit SRAM, ROM, flash, and I/O devices.

The MCF5206 can be described as a superset of the MCF5204. This device contains a 512-byte instruction cache, a 512-byte SRAM, two independent UARTs, two timers, an I2C1 module, interfaces to various memories, and a DRAM controller. The DRAM controller provides a glueless 8-, 16-, and 32-bit interface to DRAM and supports both page-mode and extended-data-out (EDO) DRAMs. The debug module is also integrated onto this device. Due to their high levels of integration, both the MCF5204 and MCF5206 are popular follow-ons for customers using Motorola's integrated 68300 Family of products. In fact, the MCF5206 is often used as a direct replacement for the MC68306 device.

The MCF5267 is designed for multimedia applications. It contains the MCF5206 with an integrated MPEG 2 Transport Stream demultiplexor. In addition, an integrated dedicated processor supports graphics display. Besides a 32-bit bus interface, the MCF5267 supplies an audio and graphics interface for customers.

¹I²C is a proprietary Philips interface

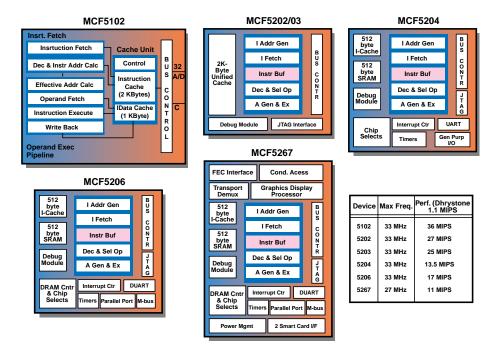


Figure 1. Standard ColdFire Product Portfolio

FLEXCORE COLDFIRE PRODUCT OFFERINGS

The ColdFire architecture is also available in Motorola's FlexCore library in the form of the ColdFire2 and ColdFire2M cores. The FlexCore Library contains a variety of Motorola microprocessor cores and peripherals that can be integrated with a customer's proprietary logic. This solution is ideal for designers of high-volume systems who want a proprietary solution that offers optimal integration in a cost-efficient manner. Both the ColdFire2 and ColdFire2M modules contain a Version 2 ColdFire core along with a misalignment module, debug module, and memory controllers to support from 0 to 32K bytes each of RAM, ROM, and instruction cache. The debug and misalignment modules are identical to those on ColdFire standard products. The ColdFire2M also includes a multiply-accumulate (MAC) module for DSP operations and fast multiples.

The MAC unit provides high-performance, digital signal processing capabilities for the ColdFire product family. Integrated as an execution unit in the processor's operand execution pipeline, the MAC unit implements a 3-stage arithmetic pipeline with a sustained instruction issue rate of 1 MAC per cycle for 16 x 16 operations. The MAC opcodes provide a full feature set of extensions to the standard ColdFire instruction set for signed and unsigned operands. The MAC unit is optimized for 16 x 16 multiples, while also supporting 32 x 32 operations. In addition to executing the MAC-specific instructions, this unit also performs all integer multiply opcodes providing higher performance for this class of operations.

FlexCore customers designing with the ColdFire2 and ColdFire2M will appreciate the unique hierarchical bus structure common to all ColdFire product family devices. The internal high-speed K-bus offers a one-cycle interface to important memories through its RAM, ROM, and instruction cache controllers that can each interface with 0 to 32K bytes of corresponding compiled memory. The M-bus is an internal two-cycle interface to the bus control signals of the embedded processor as well as to alternate masters that might be integrated on-chip. For customers designing with the ColdFire2 and ColdFire2M, cores must connect to the M-bus for their logic.

COMPREHENSIVE DEVELOPMENT TOOLS SUPPORT

In addition to its unique architectural design, a broad range of integrated third-party development tools support ColdFire processors. Many developers who provide 68K development tools have found it easy to support ColdFire products because the ColdFire instruction set architecture (ISA) is a subset of the 68K Family ISA. The Motorola Embedded Developer Program successfully establishes and maintains these developer relationships and helps to create interoperability among ColdFire micro-processor tools. This interoperability allows customers to choose compilers, debuggers, real-time operating systems (RTOS), and emulators that work seamlessly with each other. Figure 2 depicts the ColdFire Product Family's current integrated offerings.

Motorola has leveraged the Embedded Developer Program to work closely with developers and create a forum for new ideas. It's through this type of information exchange that Motorola conceived its unique on-chip debug module for the ColdFire product family. This module provides customers with immediate background debug (BDM) emulator support for new standard products and FlexCore ColdFire product designs. The debug module on each ColdFire microprocessor enables customers to reduce time to market. With the debug module and a source-level debugger or emulator, the product cycle time is reduced by offloading customers from having to develop a ROM monitor, allowing customers to control the target ColdFire microprocessor and platform in real-time, evaluate system peripherals, in-circuit programming of Flash, and accessing all system resources through intuitive graphical user interfaces (GUI). With the ability to perform real-time trace and debug in addition to background debug, this integrated debug module offers functionality on each of our ColdFire devices that is unparalleled by any other architecture. As the ColdFire product family grows, this comprehensive support will be carried into future devices and will remain a strong advantage over our competitor tool offerings.

The Integrated Tool Chain

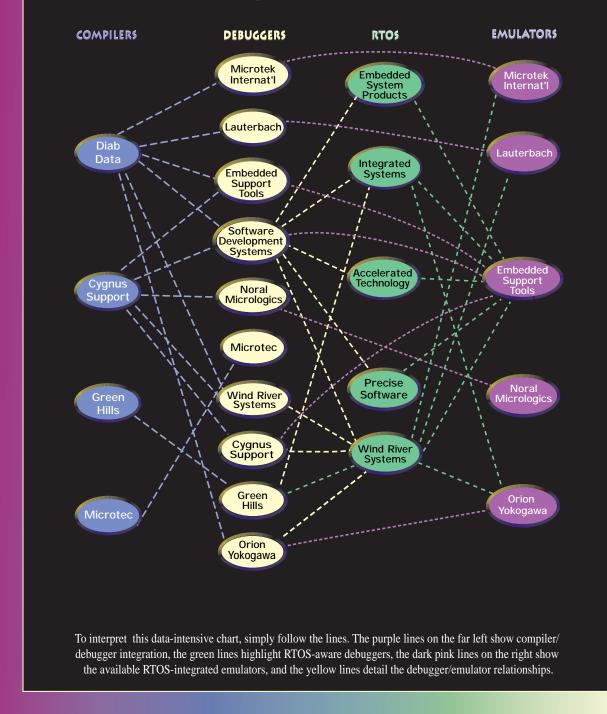


Figure 2. The ColdFire Product Family Integrated Tools Support: This diagram shows how compiler, debugger, RTOS, and emulator developers work together to create integrated tool offerings.

THE STRATEGY BEHIND COLDFIRE MICROPROCESSORS

Over the past three years, Motorola has been laying the foundation for the success of the ColdFire product family. We are moving forward to make the ColdFire architecture one of the most dominant architectures in the embedded market. We have already begun to realize the fruits of our labor with design wins in imaging, mass storage, and the general market. ColdFire microprocessors are designed into printers, copiers, set tops, communication equipment, and hard-disk drives. Motorola has launched an aggressive plan for the ColdFire architecture that achieves 300 MIPs in the year 2001. Through a strategic mission of quick-turn design, licensing and custom design, market focus and unmatched integrated development tools support, ColdFire microprocessors will be the leading 32-bit microprocessor in the embedded market.

QUICK-TURN DESIGN AND TEST METHODOLOGY

Leveraging the design methodology of the MC68060, Motorola's design team created a rapid design and test program for the ColdFire architecture that included synthesizable modules, fast prototyping, high-performance simulation, and thorough random instruction sequence (RIS) testing. This methodology enables quick turnaround of new standard products and an achievable goal of "bug-free" silicon at tape-out, which facilitates sample availability.

By making the ColdFire core and modules 100% synthesizable, retargeting the design to new process technologies is easy. This is especially valuable when the core is placed into the FlexCore library for customer-specific design.

Through constant simulation, synthesis, and physical builds, the design team can quickly create a working model. As changes are made, regular builds immediately catch any inconsistencies, which results in a more mature model at tape-out.

To verify a correct functional model, billions of RIS cycles are generated through software simulation on the processor model. This RIS testing includes random configurations of cache and chip-selects as well as emulator access through the debug port. Once the model has run without bugs for weeks, the device is taped out. When first silicon arrives, it too is tested against the same RIS cycles.

With all of these checks and balances in place, working first silicon schedules remain on target— means rapid time to market for ColdFire products.

FLEXCORE PROGRAM AND COLDFIRE PRODUCT LICENSING STRATEGY

The FlexCore program allows high-volume manufacturers to create their own integrated microprocessor containing a core processor and proprietary logic. A FlexCore integrated processor allows significant reductions in component count, power consumption, board space, and cost, resulting in higher system reliability and performance.

The ColdFire2 and ColdFire2M are already available for use in the FlexCore library by high-volume customers. We are committed to placing future ColdFire cores and modules in the standard cell library so that FlexCore customers are assured of a performance roadmap for their ColdFire product designs.

Because second-sourcing is always an important criteria for high-volume customers, Motorola has implemented a plan to license the ColdFire core to strategic partners. To date, this license has been extended to Hewlett Packard and Mitsubishi.

The ColdFire architecture features and 100%-synthesizable design make it easy to transfer the technology to other manufacturers. We will continue to develop such strate-gic licensing relationships with future ColdFire microprocessor generations.

The FlexCore program and ColdFire product licensing give Motorola the advantage for servicing our target vertical markets, such as imaging and storage, that require high-volume custom design.

MARKET-FOCUS STRATEGY

A portion of ColdFire product design wins will be in the imaging and storage markets, which includes laser printers, inkjet printers, digital copiers, scanners, multifunction peripherals, optical drives, digital video disk (DVD) storage, and hard disk drives. Because these markets are highly proprietary and cost-competitive, many of these customers will be serviced through the FlexCore Program. However, ColdFire processors in our standard product roadmap will serve as an entry point for these markets as well as other quickly growing markets such as settops, modems, ethernet controllers, global positioning systems (GPS), and data acquisition. As shown in Figure 3, ColdFire products will follow an aggressive roadmap that will offer 68K customers performance upgrades to 300 MIPS in the year 2001. Not only will ColdFire processors match competitive performance points, but aggressive pricing as well as peripheral and memory integration will continue to make the ColdFire product family attractive to distribution and small-volume customers.

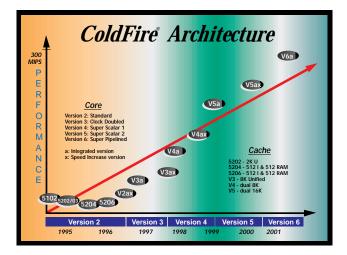


Figure 3. ColdFire Architecture Roadmap

INTEGRATED DEVELOPMENT TOOLS SUPPORT STRATEGY

Recognizing that the ColdFire product family development tools platform is currently a dominant advantage over our competitors, Motorola will continue to provide customers with a broad set of development tool solutions. To provide development tools with a quicker turnaround time and more interoperability among them, Motorola is working with third-party tool software developers to create an Embedded Application Binary Interface (EABI) standard that will define a software-support structure among ColdFire processor tool offerings. This provides tool interoperability and will increase customers' ability to plug and play with different compilers, compiler libraries, debuggers, and emulators without the worries of compatibility. The Motorola Embedded Developer Program will also continue to enhance the ColdFire microprocessor development tools portfolio by creating new relationships with third parties who are interested in supporting our devices. Our goal is to give customers a vast selection of development tool options.

CONCLUSION

ColdFire processors will be a driving force in 32-bit embedded design for Motorola. With its 68K heritage, aggressive pricing/performance points, highly integrated standard products, and comprehensive development tools support, Motorola's ColdFire architecture will drive the 68K Family into the future.

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