

# Development and Fabrication of IC Chips

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## 1.1 Introduction

At the end of the nineteenth century, the consumer products of that time included simple electrical circuits for lighting, heating, telephones, and telegraph. But the invention of radios and the need for electrical components that could rectify and amplify signals spurred the development of vacuum tubes. Vacuum tubes were found in products such as radios, televisions, communication equipment, and in early computers. Their use lasted until the late 1960s, when the development of semiconductor devices ushered in a new era in electronics. The semiconductor, containing an array of complex transistors and other components on a single IC chip, provided improved reliability and reduced power, size, and weight, and it made possible today's sophisticated electronic products.

This chapter, which is subdivided into five sections, presents a simplified approach to the understanding of the fundamentals of semiconductors, IC development, and IC chip fabrication. The topics cover

**1.2 Chapter 1**

- Atomic structure
- Vacuum tubes
- Semiconductor theory
- Fundamentals of integrated circuits
- IC chip fabrication

**1.2 Atomic Structure**

All matter, whether solid, liquid, or gas, is composed of one or more of the 109 presently recognized elements referenced in the periodic table (Fig. 1.1). Of these, 91 elements occur naturally, and the rest are either man-made or are by-products of other elements. An element is composed of molecules, which are divisible into even smaller particles called atoms. The atomic structure for each element is unique and defines the element's properties.

Materials can be categorized according to the way they conduct electricity when a voltage is applied across them. Insulators, as the name implies, do not conduct electricity, whereas conductors allow a large flow of current, depending on the voltage applied and the conductance properties of the material. Semiconductors have properties in between those of resistors and conductors, having limited current flow capabilities that depend on their atomic structure, the purity of the material, and temperature.

The structure of an atom, as was first proposed by Neils Bohr in 1913 and later supported by extensive experimental evidence, consists of negatively charged electrons rotating in somewhat defined orbits, or energy levels, about a highly dense nucleus consisting of protons and neutrons (Fig. 1.2). The protons are positively charged, and the neutrons have no charge, or are electrically neutral. Each atom has an equal number of (+) protons and (–) electrons, but the number of neutrons may vary.

Each element in the periodic table is assigned an atomic number, which is equal to the number of protons, and therefore electrons, contained in its atom. The atomic number is shown in the upper part of the box representing the element (Fig. 1.1).

The actual weight of an atom is extremely small, which makes it very difficult to work with. As a result, a weight scale was devised that assigns weights to atoms that show their weights relative to one another. The weights assigned are based on the densest part of the atom; namely, the sum of the number of protons and neutrons in the nucleus.

The positively charged protons exert an inward force on the negatively charged electrons, which is balanced by an outward centrifugal force created by the electrons spinning in their orbits around the nucleus. Thus, the two opposing forces provide a balanced structure for the atom.

The maximum number of electrons that a given orbit or shell can support is governed by the  $2n^2$  rule, where “n” is the shell number.<sup>6</sup> That is, shell #1 (closest to the nucleus) can hold a maximum of two electrons, shell #2 can have a maximum of 8 electrons, and so on. If the number of electrons for a given shell exceeds the maximum indicated by the  $2n^2$  rule, then the extra

1	IA	1	H	2	IIA	2	He
2		3	Li	4	Be	9	F
3		11	Na	12	Mg	17	Cl
4		19	K	20	Ca	35	Br
5		37	Rb	38	Sr	53	I
6		55	Cs	56	Ba	85	At
7		87	Fr	88	Ra	116	
		21	Sc	22	Ti	27	Co
		39	Y	40	Zr	45	Rh
		57	La	58	Ce	63	Eu
		89	Ac	90	Th	95	Am
		105	Db	106	Sg	111	112
		107	Bh	108	Hs	110	
		109	Mt	110		111	
		25	Mn	26	Fe	29	Cu
		43	Tc	44	Ru	47	Ag
		75	Re	76	Os	79	Au
		107	Bh	108	Hs	111	
		23	V	24	Cr	28	Ni
		41	Nb	42	Mo	46	Pd
		73	Ta	74	W	78	Pt
		105	Db	106	Sg	110	
		29	Cu	30	Zn	33	As
		47	Ag	48	Cd	51	Sb
		79	Au	80	Hg	83	Bi
		111		112		114	
		31	Ga	32	Ge	34	Se
		49	In	50	Sn	52	Te
		81	Tl	82	Pb	84	Po
		113		114		116	
		13	Al	14	Si	16	S
		31	Ga	32	Ge	34	Se
		49	In	50	Sn	52	Te
		81	Tl	82	Pb	84	Po
		113		114		116	
		5	B	6	C	7	N
		13	Al	14	Si	15	P
		31	Ga	32	Ge	33	As
		49	In	50	Sn	51	Sb
		81	Tl	82	Pb	83	Bi
		113		114		116	
		5	B	6	C	7	N
		13	Al	14	Si	15	P
		31	Ga	32	Ge	33	As
		49	In	50	Sn	51	Sb
		81	Tl	82	Pb	83	Bi
		113		114		116	
		58	Ce	59	Pr	60	Nd
		90	Th	91	Pa	92	U
		98	Dy	99	Ho	100	Er
		106	Lr	107	No	108	Lu
		64	Gd	65	Tb	66	Dy
		96	Cm	97	Bk	98	Cf
		104	105	106	107	108	109
		62	Sm	63	Eu	64	Gd
		94	Pu	95	Am	96	Cm
		102	Yb	103	Lu	104	105
		68	Er	69	Tm	70	Yb
		100	Fm	101	Md	102	No
		67	Ho	68	Er	69	Tm
		99	Es	100	Fm	101	Md
		107	Lu	108	No	109	Lr

Figure 1.1 Abbreviated periodic table of the elements.

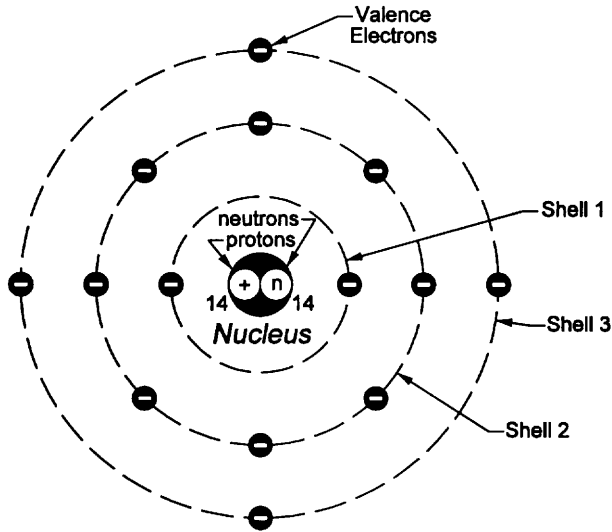


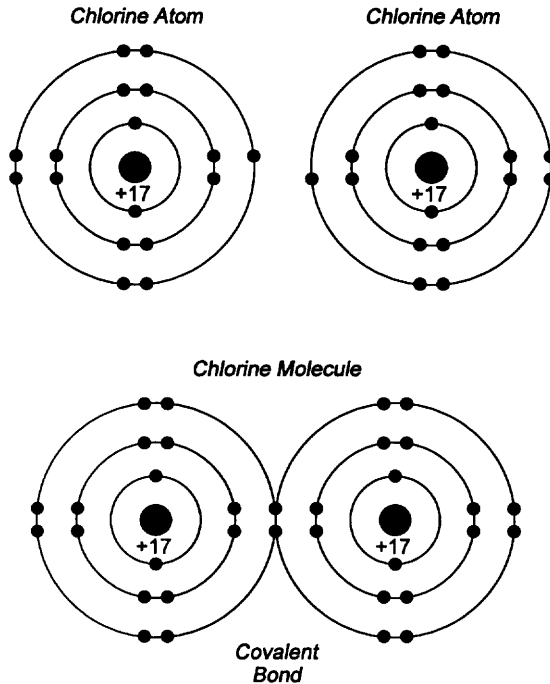
Figure 1.2 Bohr model of silicon atom.

electrons are being forced into the next higher shell. An atom is chemically stable if its outer shell is either completely filled with electrons, based on the  $2n^2$  rule, or has eight electrons in it. The electrons in the outer shell are called valence electrons and, if their number is less than eight, the atom will have a tendency to interact with other atoms either by losing, acquiring, or merging its electrons with other atoms.

In the periodic table (Fig. 1.1), elements with the same number of valence electrons have similar properties and are placed in the same group. For example, elements in Group I have atoms with one electron in their outer shell. Group II shows elements that have atoms with two electrons in their outer shell, and so on. Elements on the left side of the periodic table have a tendency to lose their valence electrons to other atoms, thus becoming electropositive. The elements on the right side of the periodic table show a tendency to acquire electrons from other atoms and become electronegative.

The type of interaction occurring between atoms, as they are brought together, depends largely on the properties of the atoms themselves. The interaction may form bonds that can be classified as ionic, covalent, molecular, hydrogen bonded, or metallic. Since this chapter is concerned with semiconductors, which tend to form covalent bonds with other elements and with themselves, the emphasis will be on covalent bonding.

Covalent bonds occur when two or more atoms jointly share each other's valence electrons. If the outer shell is partially filled with electrons, the atom will be attracted to other atoms also having a deficiency of electrons, so sharing each other's valence electrons will result in a more stable condition. As an example, two chlorine atoms will attract and share each other's single electron to form a stable covalent bond with eight electrons in each shell (Fig. 1.3).



**Figure 1.3** A chlorine molecule forms a covalent bond.

### 1.3 Vacuum Tubes

Modern electronics can trace its roots to the first electronic devices called vacuum tubes. Although, today, solid state devices have totally replaced the vacuum tube, the fundamental principle as to its usage remains relatively unchanged. For more than 40 years, until the late 1960s, the most important part in a consumer electronics product was the vacuum tube. It is with this historical perspective in mind that this section is presented so that readers will not lose sight of where it all started.

The vacuum tube got its start in 1883, when Edison was developing the incandescent lamp. To correct the premature burnout of the red-hot filament in light bulbs, Edison tried a number of experiments, one of which was to place a metal plate sealed inside a bulb and connect it to a battery and ammeter, as shown in Fig. 1.4. Edison observed that, when the filament was hot and the plate was positively (+) charged by the battery, the ammeter indicated a current flow through the vacuum, across the gap between the filament and the plate. When the charge on the plate was reversed to negative (–), the current flow stopped. As interesting as this phenomena was, it did not improve the life of Edison’s lamps and, as a result, he lost interest in this experiment and went on to other bulb modifications that proved more successful. For about 20 years, Edison’s vacuum tube experiment remained a scientific curiosity. In 1903, as radios were coming into use, J. A. Fleming, in England, found just

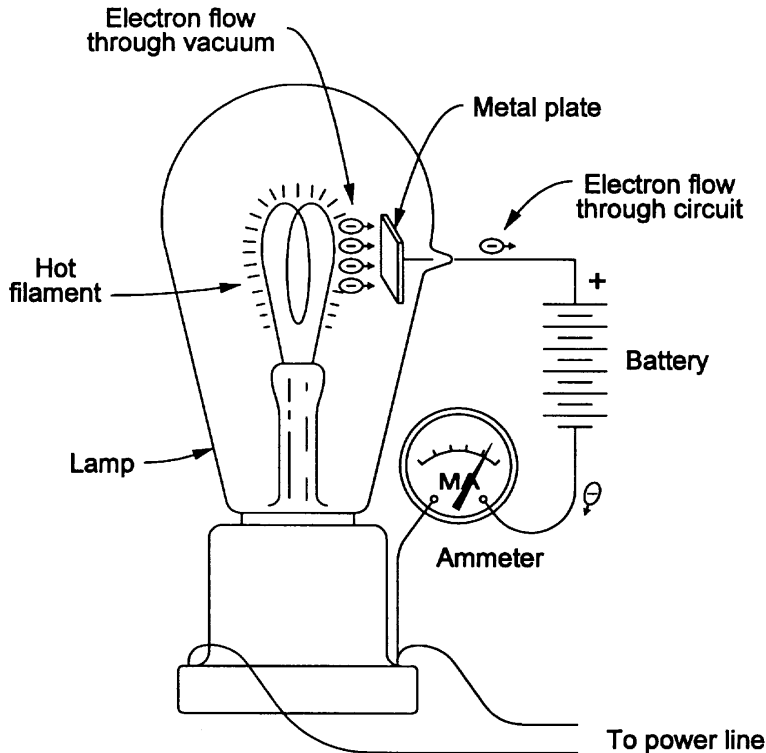


Figure 1.4 Edison's vacuum tube.

what he needed to rectify alternating radio signals into DC signals required to operate headphones. By hooking up Edison's vacuum tube to a receiving antenna, the tube worked like a diode. When the signal voltage increased in one direction, it made the plate positive (+), and the signal got through. When the signal voltage increased in the other direction of the AC cycle, applying a negative (−) charge to the plate, the signal stopped.

The vacuum tube, also called the electron tube, required a source of electrons to function. In Edison's original electron tube, the electron source, called the *cathode*, was the filament that, when heated red-hot, emitted electrons that flew off into the vacuum toward the positively charged plate, called the *anode*. The effect of heating the cathode to activate the electrons was called *thermionic*. Other electron tubes used high voltage to pull the electrons out of a cold cathode. Electronic emission also occurred by applying light energy to a photosensitive cathode. Tubes using this effect were called *photoelectronic* vacuum tubes. Although a variety of methods existed to remove electrons from the cathode, the thermionic vacuum tubes were the most widely used. The cathode was either heated by resistors within or used a separate source of power for heating. The vacuum tube consisted of a glass or metal enclosure with electrode leads brought out through the glass to metal pins molded into a plastic base (Fig. 1.5).

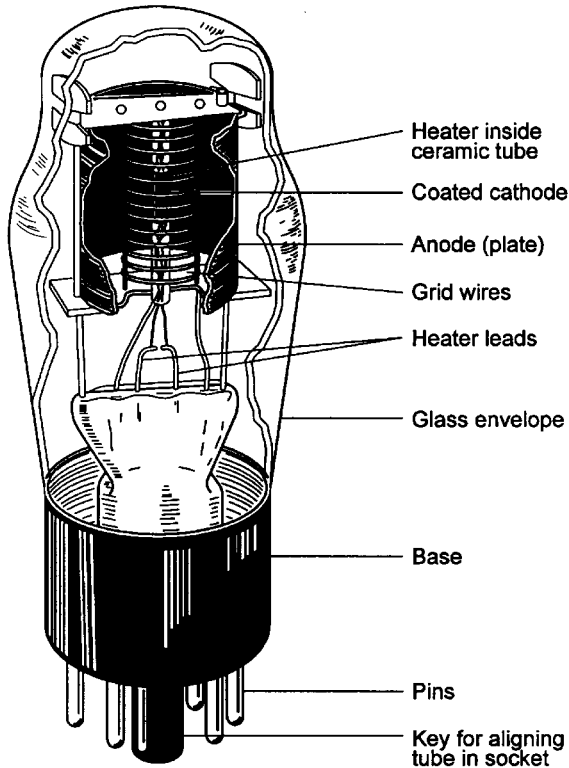


Figure 1.5 The construction of a triode vacuum tube.

When the electron tube contains two electrodes (anode and cathode), the circuit is called a *diode*. In 1906, Lee DeForest, an American inventor, introduced a grid (a fine wire mesh) in between the cathode and the anode. The addition of a third electrode expanded the application of electron tubes to other electronic functions. The grid provided a way of controlling the flow of electrons from the cathode to the plate (anode). Even though the grid had a weak positive or negative charge, its proximity to the cathode had a strong effect on the flow of electrons from cathode to plate. The open weave in the grid allowed most of the electrons to pass through and land on the stronger positively charged anode. When the grid was negatively charged, it repelled the electrons from the cathode, stopping the current flow (Fig. 1.6).

Thus, with the three electrodes (i.e., cathode, anode, and grid), it was possible to both rectify and amplify weak radio signals using one tube. The three-electrode vacuum tube was called a *triode*. Additional electrodes, such as a suppressor grid and screen grid, were also enclosed in electron tubes, making it possible to expand the functions of electron tubes.

Vacuum tubes, although widely used in the industry for a half a century, had a number of disadvantages, among them that they were bulky, generated a lot of heat, and were subject to frequent replacement because they would burn out. With the advent of solid state devices, which had none of the disad-

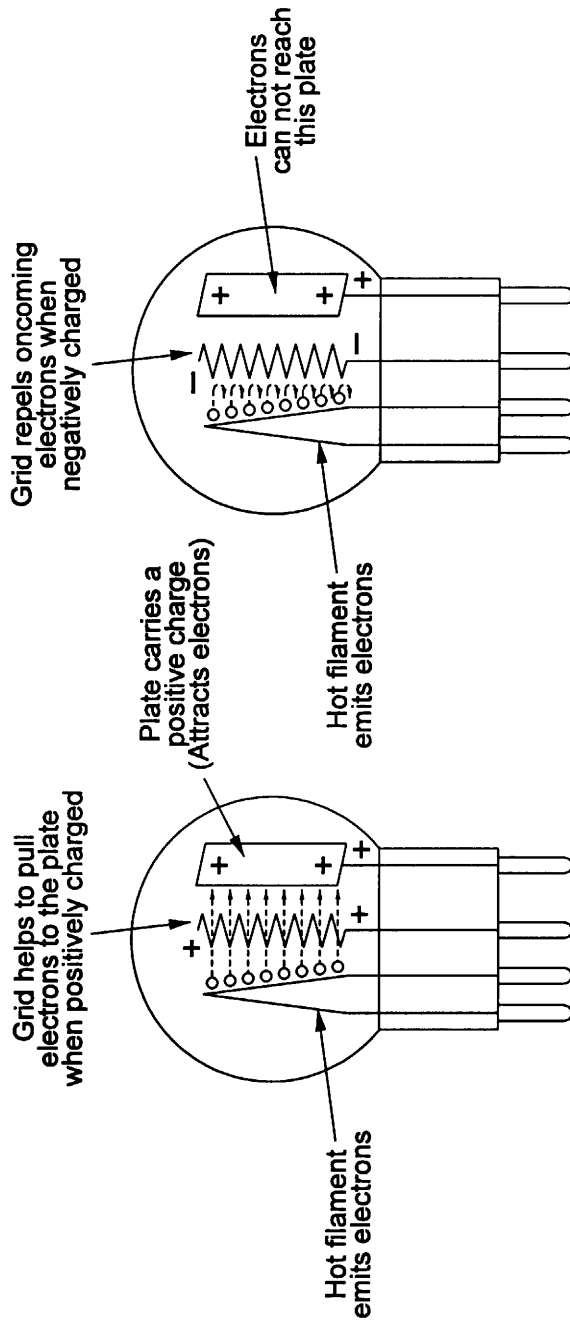


Figure 1.6 Grid controls the flow of electrons to the plate of a triode.



vantages of vacuum tubes, vacuum tubes started to fade from use in electronic products.

## 1.4 Semiconductor Theory

Semiconductor materials have physical characteristics that are totally different from those of metals. Whereas metals conduct electricity at all temperatures, semiconductors conduct well at some temperatures and poorly at others.

In the preceding section, it was shown that semiconductors are covalent solids. That is, the atoms form covalent bonds with themselves, the most important being silicon and germanium in Group IV of the periodic table (Fig. 1.1). Others may form semiconductor compounds where two or more elements form covalent bonds, such as gallium (Group III) and arsenic (Group V), which combine to form gallium arsenide.

Typical semiconductor materials used in the fabrication of IC chips are

- Elemental semiconductors
  - Silicon
  - Germanium
  - Selenium
- Semiconducting compounds
  - Gallium arsenide (GaAs)
  - Gallium arsenide–phosphide (GaAsP)
  - Indium phosphide (InP)

Germanium is an elemental semiconductor that was used to fabricate the first transistors and solid state devices. But, because it is difficult to process and inhibits device performance, it is rarely used now.

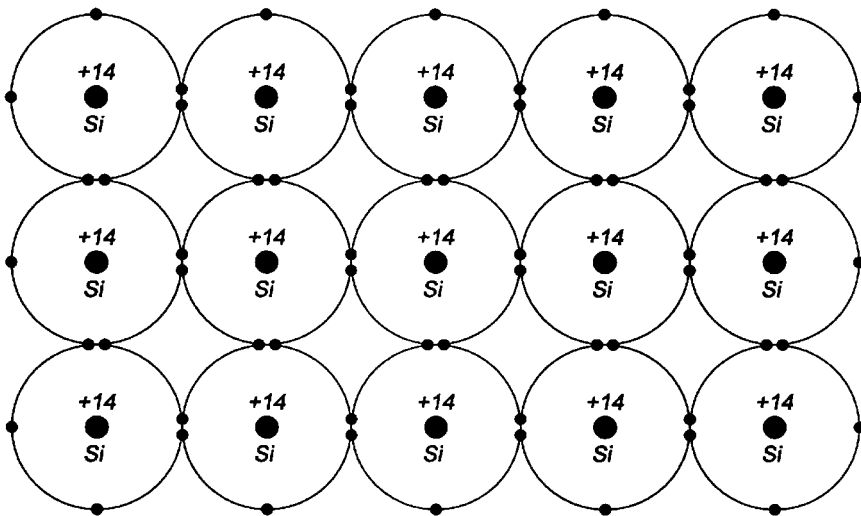
The other elemental semiconductor, silicon, is used in approximately 90 percent of the chips fabricated. Silicon's popularity can be attributed to its abundance in nature and retention of good electrical properties, even at high temperatures. In addition, its silicon dioxide ( $\text{SiO}_2$ ) has many properties ideally suited to IC manufacturing.

Gallium arsenide is classified as a semiconducting compound. Some of its properties, such as faster operating frequencies (two to three times faster than silicon), low heat dissipation, resistance to radiation, and minimal leakage between adjacent components, makes GaAs an important semiconductor for use in high-performance applications. Its drawbacks are the difficulty of growing the ingots and fabricating the ICs.

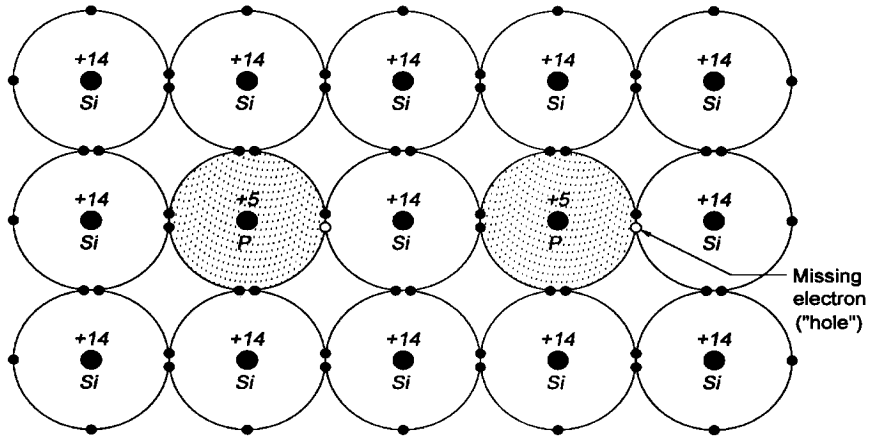
An elemental or compound semiconductor that was not contaminated by the introduction of impurities is called an *intrinsic semiconductor*. At an absolute zero temperature, intrinsic semiconductors form stable covalent bonds that have valence shells completely filled with electrons. These covalent bonds are very strong, so that each electron is held very strongly to the atoms sharing it. Thus, there are no free electrons available, and no electrical conduction is pos-

sible. As the temperature is raised to relatively high temperatures, the valence bonds sometimes break, and electrons are released. The free electrons behave in the same way as free electrons in a metal; therefore, electrical conduction is now possible when an electric field is applied.

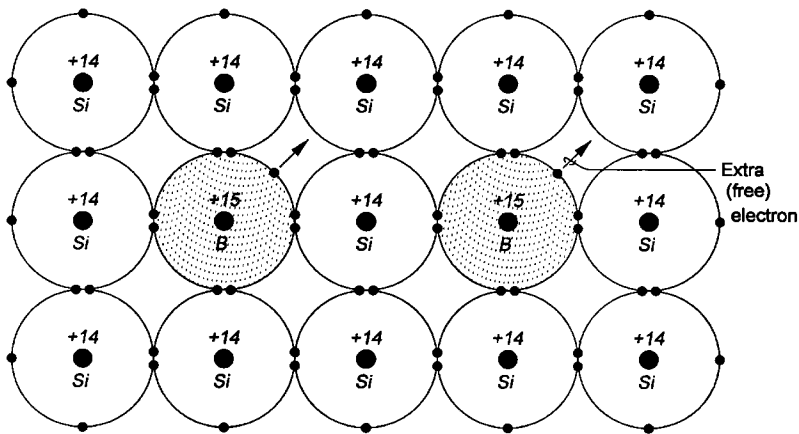
If an impurity, such as phosphorus or boron, is introduced into the crystal structure of an intrinsic semiconductor, its chemical state is altered to where the semiconductor will have an excess or deficiency of electrons, depending on the impurity type used. The process of adding a small quantity of impurities to an intrinsic semiconductor is called *doping*. As an example, consider an intrinsic silicon crystal structure with its covalent bonds, shown as a two-dimensional sketch in Fig. 1.7. Each atom is surrounded by four other atoms, with which it shares one pair of electrons, to form four covalent bonds. If the silicon crystal (Group IV) is doped with a controlled quantity of an impurity (dopant), such as phosphorus (Group V), the newly formed covalent bonds (Fig. 1.8) have an excess of electrons that are free to move from atom to atom when a voltage is applied across the semiconductor. The material thus altered is called an n-type (n for negative) semiconductor. Another semiconductor type, called p-type (p for positive), can be formed by doping the silicon crystal with a dopant from Group III, such as boron. The resultant combination (Fig. 1.9) has a deficiency of electrons and thus creates “holes,” or electron vacancies, in the positively charged atoms. A single semiconductor crystal structure can be selectively doped with two different kinds of impurities that will form adjacent p-type and n-type semiconductors (Fig. 1.10). The transition between the two types of semiconductors is the p-n junction and is where electrons and holes recombine. As the electrons enter the p-type region, filling the holes, the atoms become negatively charged while the atoms left behind, with fewer elec-



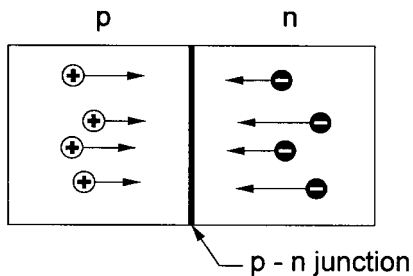
**Figure 1.7** Two-dimensional representation of an intrinsic silicon crystal (only valence electrons are shown).



**Figure 1.8** Two-dimensional representation of silicon crystal doped with phosphorus to create a p-type semiconductor (only valence electrons are shown).



**Figure 1.9** Two-dimensional representation of silicon crystal doped with boron to create an n-type semiconductor (only valence electrons are shown).



**Figure 1.10** P-type/n-type semiconductor junction. (After Tedeschi.<sup>1</sup>)

## 1.12 Chapter 1

trons, and new holes, become positively charged (Fig. 1.11). The process can be considered as a flow of holes or a current flow of positively charged vacancies, which is opposite to the electron flow. Since there is a depletion of electrons and holes in the contact region, the p-n junction is referred to as the *depletion region*. The double layer of charged atoms sets up an electric field across the contact that prevents further intermixing of electrons and holes in the region, creating a barrier.<sup>1</sup>

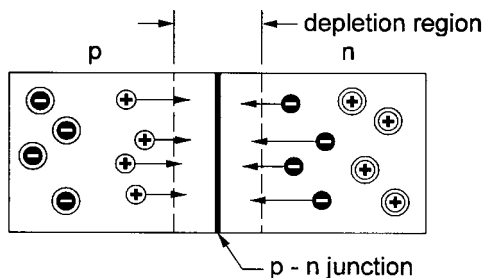
## 1.4.1 The diode

When an external battery is placed across the p-n junction, with the positive (+) terminal of the battery connected to the n-type side of the semiconductor and the negative (-) terminal connected to the p-type side, a so-called reverse bias condition is created across the junction. As the electrons are attracted to the positive terminal of the battery, and the holes are attracted to the negative side, the electrons and holes move away from the junction, thus increasing the depletion region and preventing current flow (Fig. 1.12).

If the battery terminals are reversed (Fig. 1.13), the electrons in the n-material and the holes in the p-material are repelled by their respective negative and positive potentials of the battery and move toward the junction. This reduces the barrier junction, allowing electrons and holes to cross the junction and continue to recombine. As the electrons and holes recombine, new electrons from the (-) terminal of the battery enter the n-region to replace the electrons that crossed into the p-region. Similarly, the electrons in the p-region are attracted by the (+) terminal, leaving new holes behind, which are filled by electrons coming from the n-region. The continuous recombining process creates a forward current flow across the p-n region, which is referred to as *forward biased*. Thus, a p-n junction acts as a diode (rectifier); i.e., when the junction is forward biased, it conducts current, and when the bias is reversed, the current stops.

## 1.4.2 The junction-type bipolar transistor

Combining two or more p-n junction arrangements (p-n-p, n-p-n, etc.) into one device resulted in the development of the transistor. The transistor is a device



**Figure 1.11** P-type/n-type semiconductor junction with depletion region. (After Tedeschi.<sup>1</sup>)

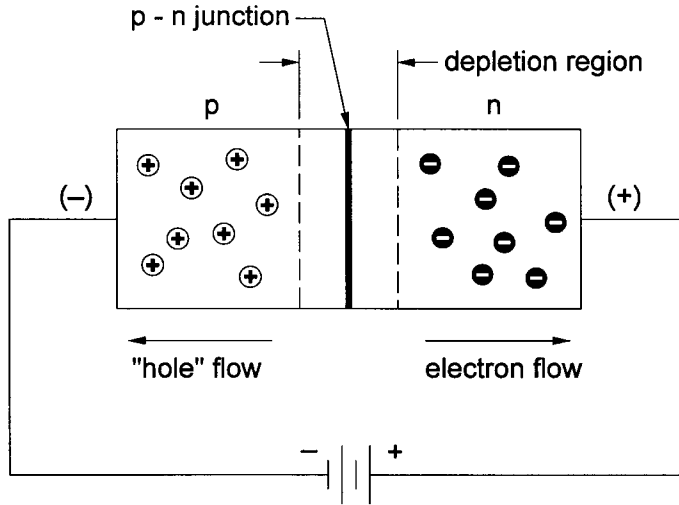


Figure 1.12 Reverse-biased p-n junction. (After Tedeschi.<sup>1</sup>)

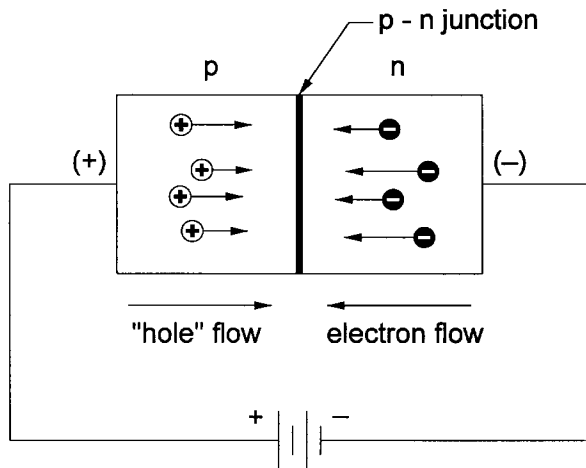
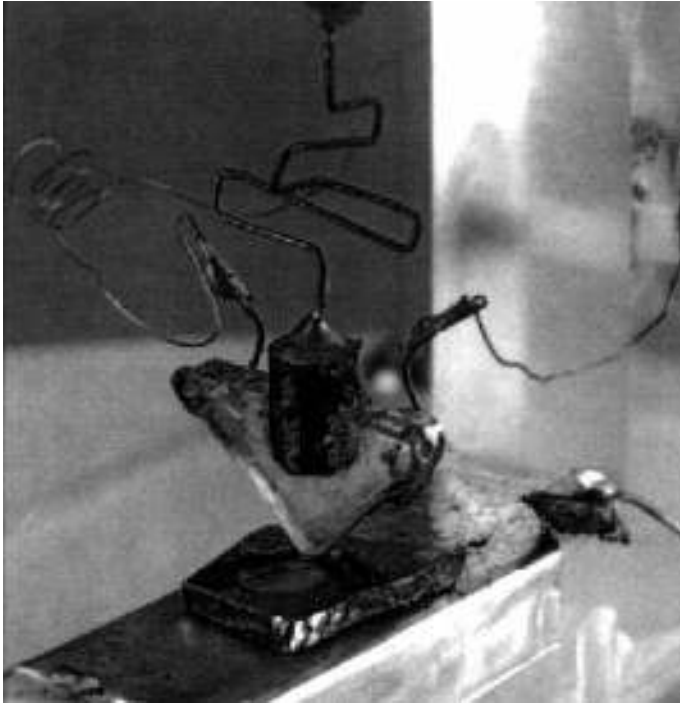


Figure 1.13 Forward-biased p-n junction. (After Tedeschi.<sup>1</sup>)

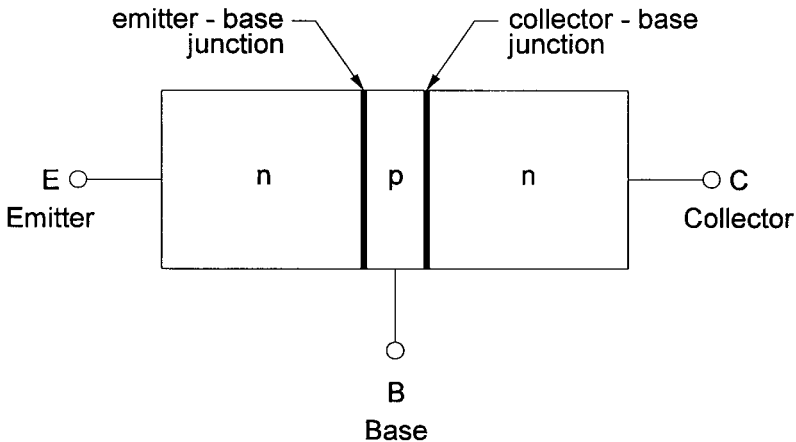
capable of amplifying a signal or switching a current *on* and *off* billions of times per second. Its development dawned a new age in electronics.

Since its inception in 1948 by W. Shockley, J. Bardeen, and W. Brattain of Bell Laboratories, the transistor has evolved into many forms. The original device (Fig. 1.14) used point contacts to penetrate the body of a germanium semiconductor. Subsequent transistors were of the junction (bipolar) type with germanium as the semiconductor. The semiconductor material was later replaced with silicon.

To illustrate how a bipolar transistor works, an n-p-n semiconductor configuration (Fig. 1.15) is used as an example. In this structure, a very thin, lightly



**Figure 1.14** The original point-contact transistor. (Courtesy of Bell Laboratories.)

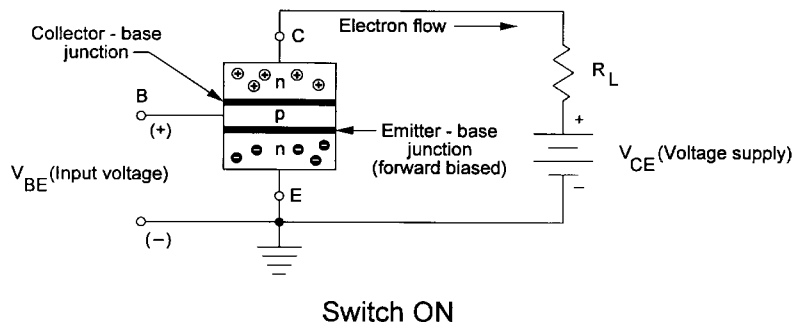
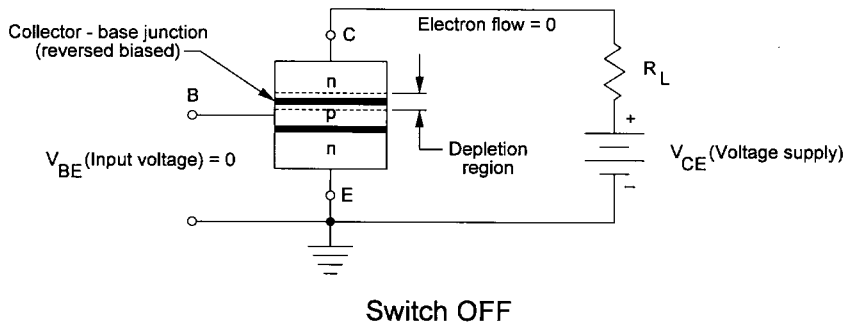


**Figure 1.15** Typical n-p-n transistor.

doped p-region, called the base (B), is sandwiched between two thicker outer n-regions, called the emitter (E) and collector (C). The emitter generates electrons, the collector absorbs the electrons, and an input signal applied at the base controls the electron flow from emitter to collector.

Figure 1.16 shows a typical circuit of a bipolar transistor functioning as a digital switch. A supply voltage  $V_{CE}$  is applied across the emitter and collector terminals, with the (+) positive terminal of the voltage source connected through a load resistor  $R_L$  to the collector terminal. Applying a positive voltage between the base and emitter terminals,  $V_{BE} > 0.5$  V, turns the transistor *on*. Since the emitter-base junction is forward biased, the electrons in the emitter region will cross the junction and enter the base region where a few of the electrons will recombine with holes in the lightly doped base. Because the base region is very thin, and the free electrons are close to the collector, the electrons are pulled across the collector-base junction by the positive potential of the collector and continue to flow through the external circuit. Decreasing the input voltage to zero no longer sustains a flow of electrons across the emitter-base junction and the transistor is turned *off*.

When the bipolar transistor is used as an amplifier, the strength of the emitter-to-collector current flow follows the variations in strength of the input voltage, but at a magnified level. That is, increasing the strength of the input voltage at the base causes proportionally more electrons to cross the emitter-base junction, thus increasing the current flow between the emitter and collector. Decreasing the input voltage causes the electrons to reduce their speed of



**Figure 1.16** Bipolar transistor functioning as a digital switch. (After Levine.<sup>2</sup>)

crossing the emitter-base junction, and the current flow decreases. Since the bipolar transistor can equally amplify both current and voltage, the transistor can also be considered a power amplifier.

The characteristic of the bipolar transistor is its high-frequency response capability, which equates with high switching speed. But to achieve high switching speeds, the transistor must operate at high emitter-to-collector current flow, causing increased power losses.<sup>2</sup>

### 1.4.3 The field-effect transistor (FET)

The FET transistor operates on a different principle from that of the bipolar transistor. The input voltage creates an electric field that changes the resistance of the output region, thus controlling the current flow. Its unique characteristic of having a very high input resistance will prevent a preceding device in the circuit from being loaded down, which could degrade its performance. The working principle of the FET transistor was known long before the bipolar transistor was developed, but, because of production difficulties, it was abandoned in favor of the bipolar transistor. The 1960s saw a revival of interest in FET transistors after the earlier production issues were resolved. The FET transistor has three semiconductor regions, similar to the bipolar transistor, but, because its principle of operation is different, the FET regions are called the *source*, the *drain*, and the *gate*. These regions are equivalent to the emitter, collector, and base of the bipolar transistor. If we again consider an n-p-n structure, the source and the drain regions are n-type semiconductors, and the gate region is a p-type material.

There are two types of FET transistors: the junction field-effect transistor (JFET) and the metal oxide semiconductor field-effect transistor (MOSFET).

### 1.4.4 The junction field-effect transistor (JFET)

In a junction field-effect transistor (JFET), the electrons do not cross the p-n junction but, rather, flow from the source to the drain along a so-called n-channel, which is formed between two p-type materials (Fig. 1.17). The n-channel is considered the output section of the transistor, and the gate-to-source p-n junction is the input section. In a typical JFET circuit (Fig. 1.18), where the transistor functions as a digital switch, the voltage supply  $V_{SD}$  is applied

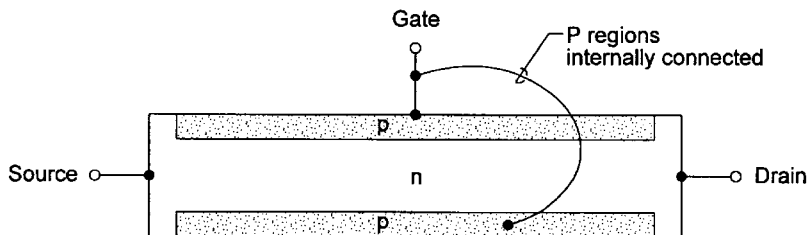
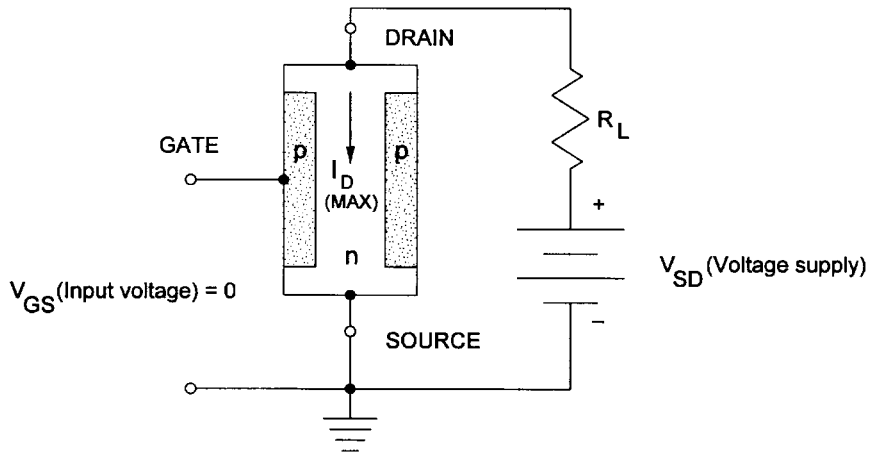


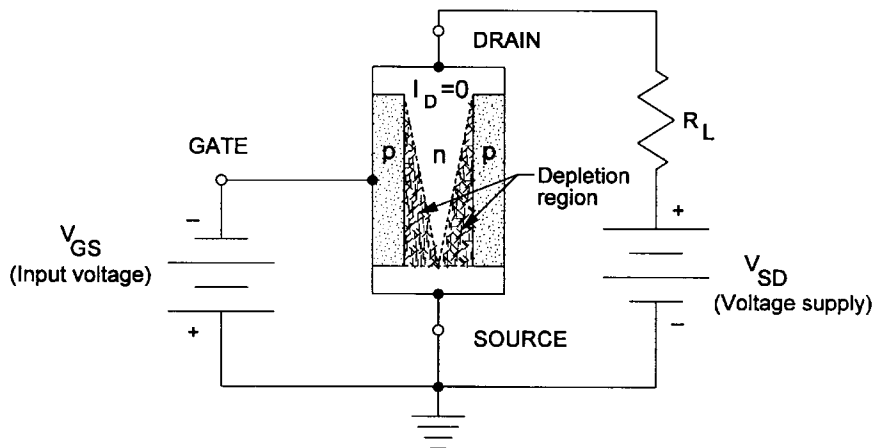
Figure 1.17 Junction field-effect transistor (JFET) construction. (After Levine.<sup>2</sup>)





**Figure 1.18** JFET functioning as an “on” switch, p-n junction forward biased. (After Levine.<sup>2</sup>)

across the (–) source and the (+) drain terminals, through a load resistor  $R_L$ . The input voltage  $V_{GS}$  is connected between the gate and source terminals with the negative polarity on the gate. With a reversed bias input voltage, the effect of the electric field creates depletion areas around the two p-n junctions, which are characteristically devoid of electrons. As the input voltage increases, the depletion areas penetrate deeper toward the center of the channel, restricting the electron flow between the source and the drain (Fig. 1.19). If the input voltage is large enough, the depletion areas will totally fill the n-channel, choking off the flow of electrons. Reducing the input voltage  $V_{GS}$  to zero, the depletion areas disappear, and the n-p channel is wide open, with



**Figure 1.19** JFET functioning as an “off” switch, p-n junction reverse biased. (After Levine.<sup>2</sup>)

very low resistance; thus, the electron flow rate will be at its maximum. When the JFET transistor is used as a linear amplifier, the input voltage variation will have an equivalent effect on the current flow in the n-channel and cause an output voltage gain across the source and drain terminals.<sup>2</sup>

#### 1.4.5 The metal-oxide semiconductor field-effect transistor (MOSFET)

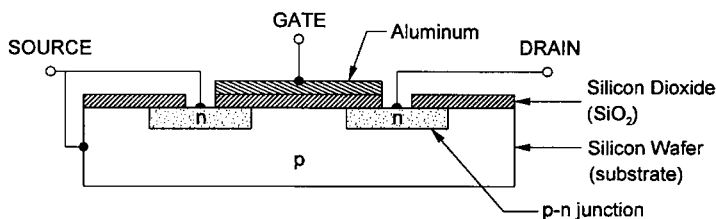
Another type of FET transistor is the metal-oxide semiconductor field-effect transistor (MOSFET). It operates on the same principle as the JFET transistor but uses the input voltage, applied across a built-in capacitor, to control the source-to-drain electron flow.

A MOSFET typically consists of a source and drain (n-type regions) embedded in a p-type material (Fig. 1.20). The gate terminal is connected to a metal (aluminum) layer that is separated from the p-type material by a silicon dioxide ( $\text{SiO}_2$ ) insulator. This combination of metal, silicon dioxide (insulation), and p-type semiconductor layers forms a decoupling capacitor. The gate region is located between the source and drain regions, with a fourth region located under the gate, called the *substrate*. The substrate is either internally connected to the source or is used as an external terminal.

The flow of electrons from the source to the drain is controlled by whether the gate has a positive or negative voltage. If the input voltage applied to the gate is positive, free electrons will be attracted from the n-regions and the p-region to the underside of the silicon dioxide layer, at the gate region. The abundance of electrons under the gate forms an n-channel between the two n-regions, thus providing a conductive path for the current to flow from the source to the drain (Fig. 1.21). In this case, the MOSFET is said to be *on*. If the input voltage at the gate is negative, the electrons in the p-region under the gate are repelled, and no n-channel is formed. Since the resistance in the p-region between the two n-regions is infinite, no current will flow, thus turning the MOSFET *off*. Although the MOSFET used in the above description was of an n-p-n type, a p-n-p type MOSFET can also be constructed, but its voltage polarities are reversed.<sup>2</sup>

#### 1.4.6 The CMOSFET transistor

When two MOSFET transistors, one an n-p-n type and the other a p-n-p type, are connected, the combination (Fig. 1.22) is called a complementary MOS-



**Figure 1.20** Typical construction of a MOSFET (metal-oxide semiconductor field-effect transistor). (After Levine.<sup>2</sup>)

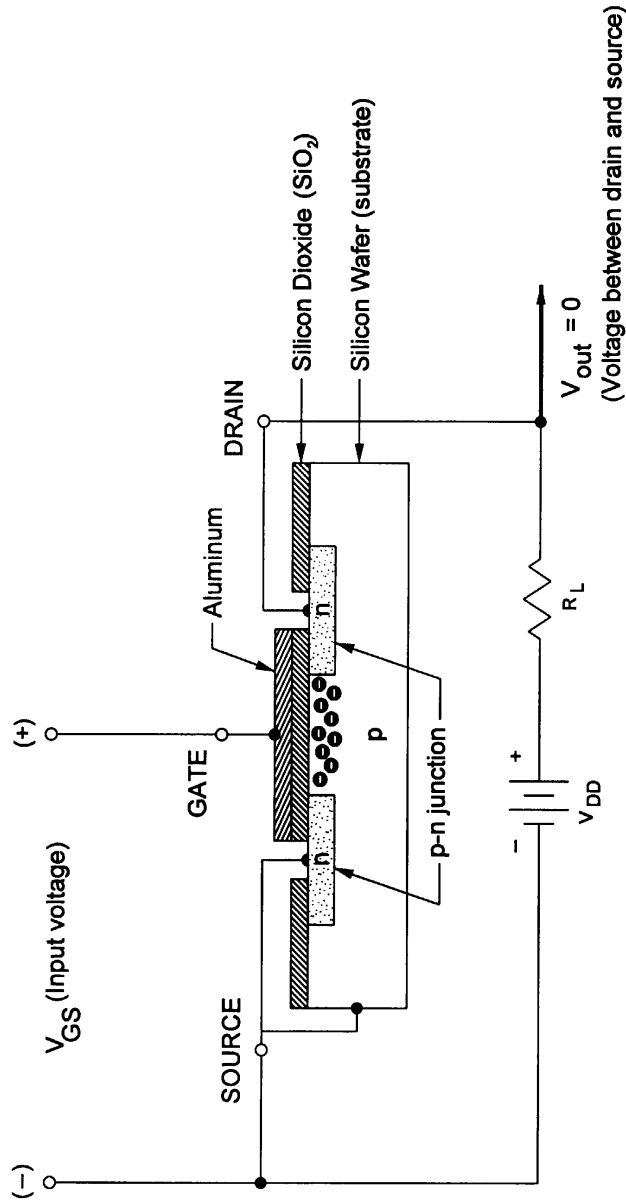


Figure 1.21 MOSFET functioning as an "on" switch. (After Levine.<sup>2</sup>)

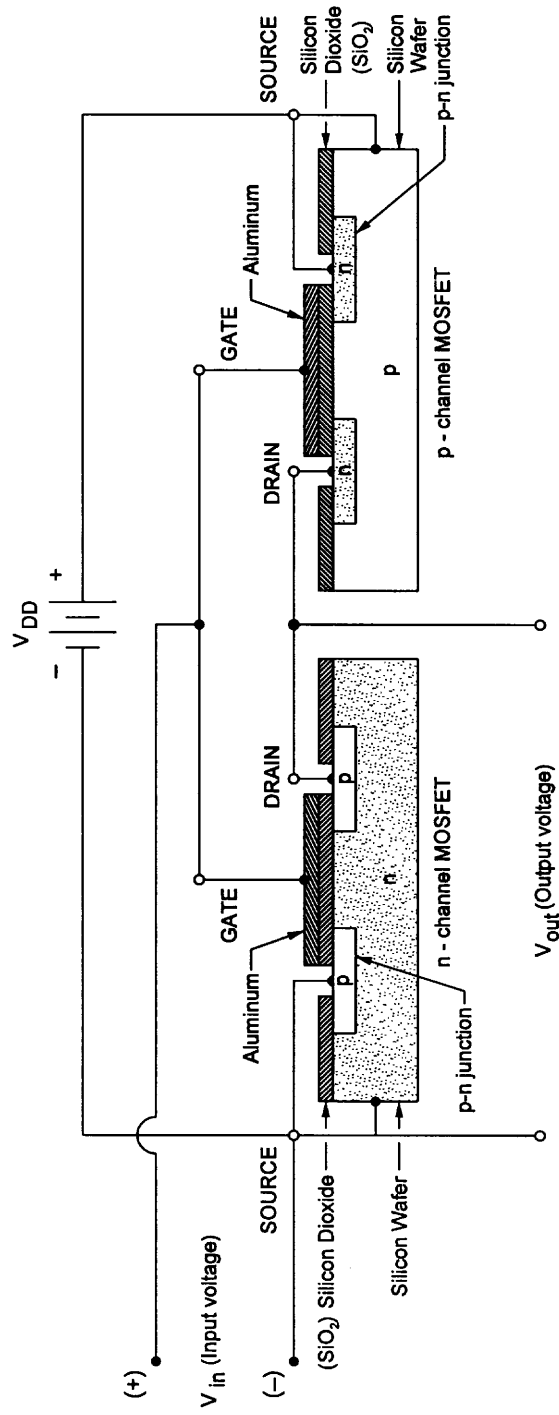
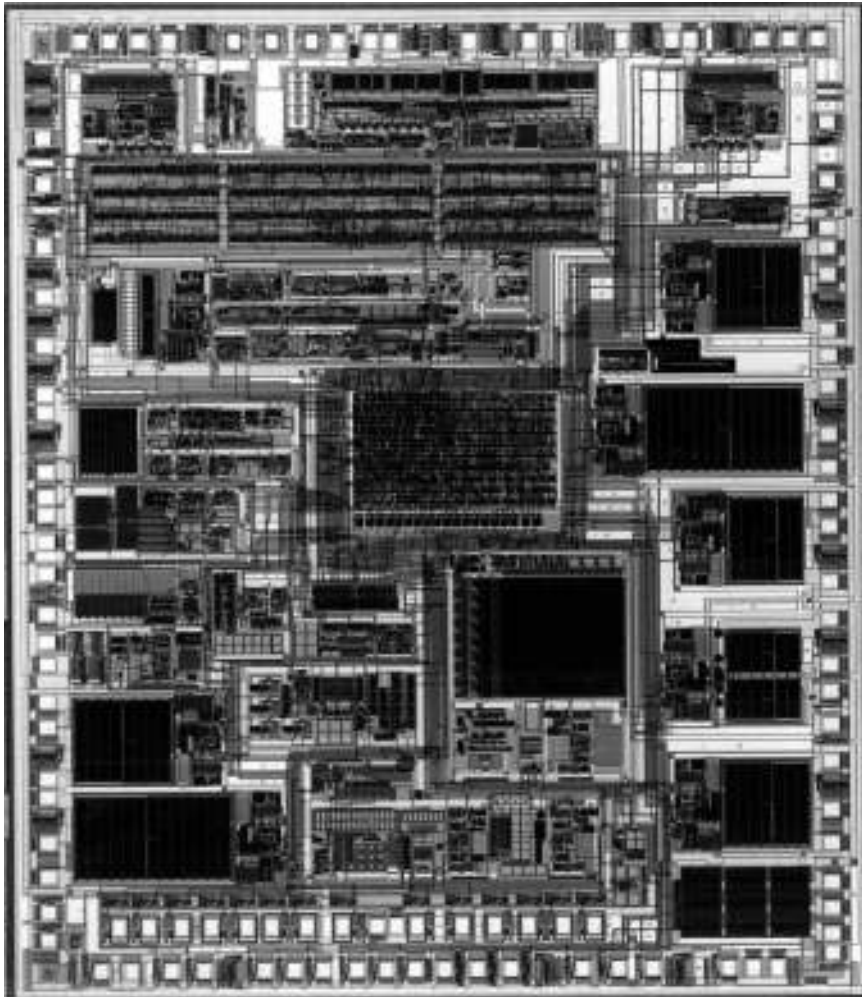


Figure 1.22 CMOSFET (n-p-n MOSFET connected to a p-n-p MOSFET to form a switch).

FET or CMOSFET. The advantages of a CMOSFET transistor are simplified circuitry (no load resistors required), very low power dissipation, and the capability to generate an output signal, which is the reverse of the input signal. For example, a positive input will have a zero output, or a zero input will create a positive output.

## 1.5 Fundamentals of Integrated Circuits

An integrated circuit (IC) chip is a collection of components connected to form a complete electronic circuit that is manufactured on a single piece of semiconductor material (Fig. 1.23). As described, the function of most solid state components is dependent on the properties of one or more p-n junctions



**Figure 1.23** Typical IC chip. (Courtesy of Agere Systems.)

## 1.22 Chapter 1

incorporated into their structures. Figure 1.24 illustrates the combination of various electrical components on an IC, showing their p-n junction structures.

Although the development of ICs was the result of contributions made by many people, Jack Kilby of Texas Instruments is credited with conceiving and constructing the first IC in 1958. In the Kilby IC, the various semiconductor components (transistors, diodes, resistors, capacitors, etc.) were interconnected with so-called “flying wires” (Fig. 1.25). In 1959, Robert Noyce of Fairchild was first to apply the idea of an IC in which the semiconductor

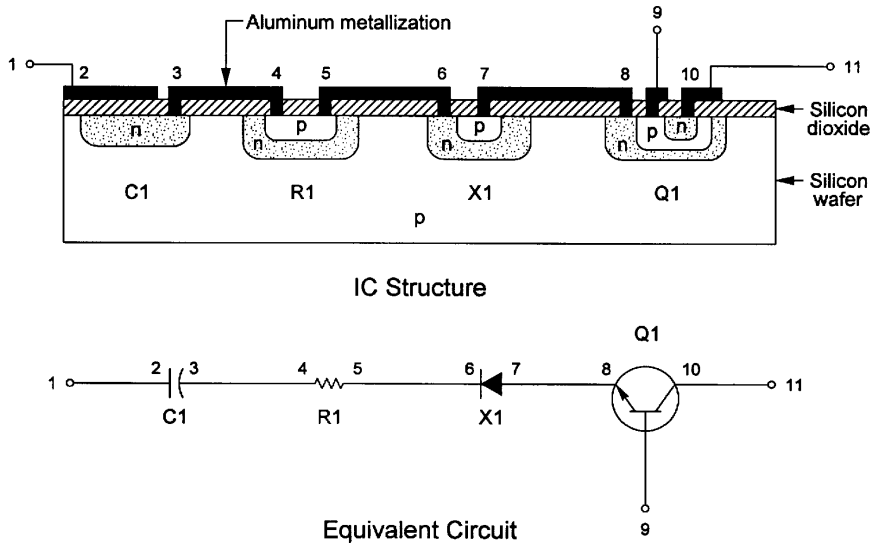


Figure 1.24 Typical silicon structure of electrical components.

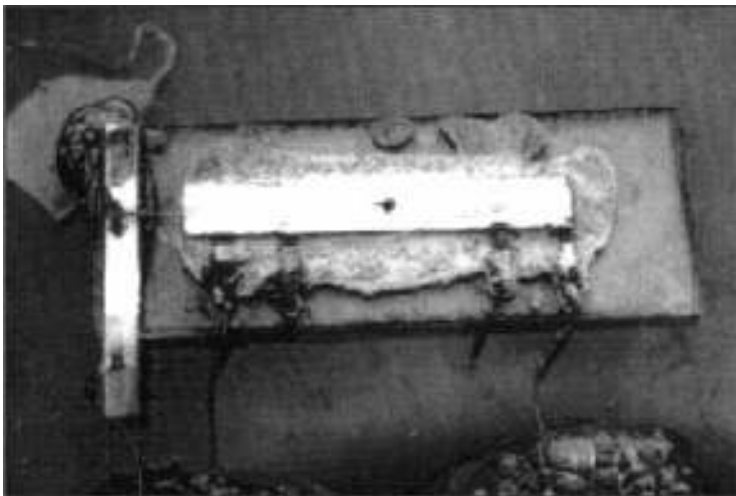


Figure 1.25 Jack Kilby's first integrated circuit.

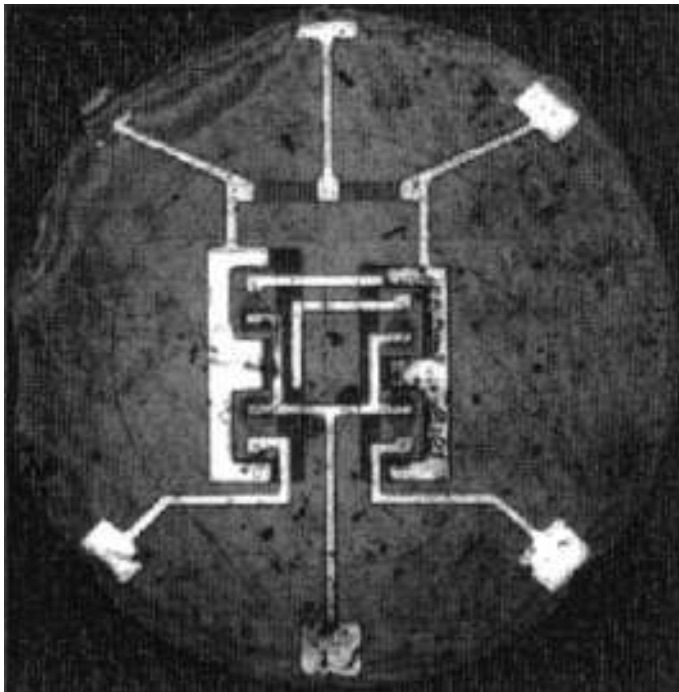
components are interconnected within the chip using a planar fabrication process, thus eliminating the flying wires<sup>4</sup> (Fig. 1.26).

Over the last four decades, the electronics industry has grown very rapidly, with increases of over an order of magnitude in sales of ICs. In the 1960s, bipolar transistors dominated the IC market but, by 1975, digital metal-oxide semiconductor (MOS) devices emerged as the predominant IC group. Because of MOS's advantage in device miniaturization, low power dissipation, and high yields, its dominance in market share has continued to this day.

IC complexity has also advanced from small-scale integration (SSI) in the 1960s, to medium-scale (MSI), to large-scale integration (LSI), and finally to very large-scale integration (VLSI), which characterizes devices containing  $10^5$  or more components per chip. This rate of growth<sup>3</sup> is exponential in nature (Fig. 1.27) and, at the current rate of growth, the complexity is expected to reach about  $5 \times 10^9$  devices per chip by the year 2005.

Continued reduction of the minimum IC feature dimensions<sup>3</sup> (Fig. 1.28) is a major factor in achieving the complexity levels mentioned. The feature size has recently been shrinking at an approximate annual rate of 11 percent. Thus, by the year 2006, it is expected to reach a minimum feature size of  $10^2$  nm (0.10  $\mu$ m).

Device miniaturization has further improved the circuit-level performance, one improvement being the reduction of power consumption at the per-gate level. Figure 1.29 illustrates the exponentially decreasing trend in the power



**Figure 1.26** Early Fairchild IC using planar fabrication process.

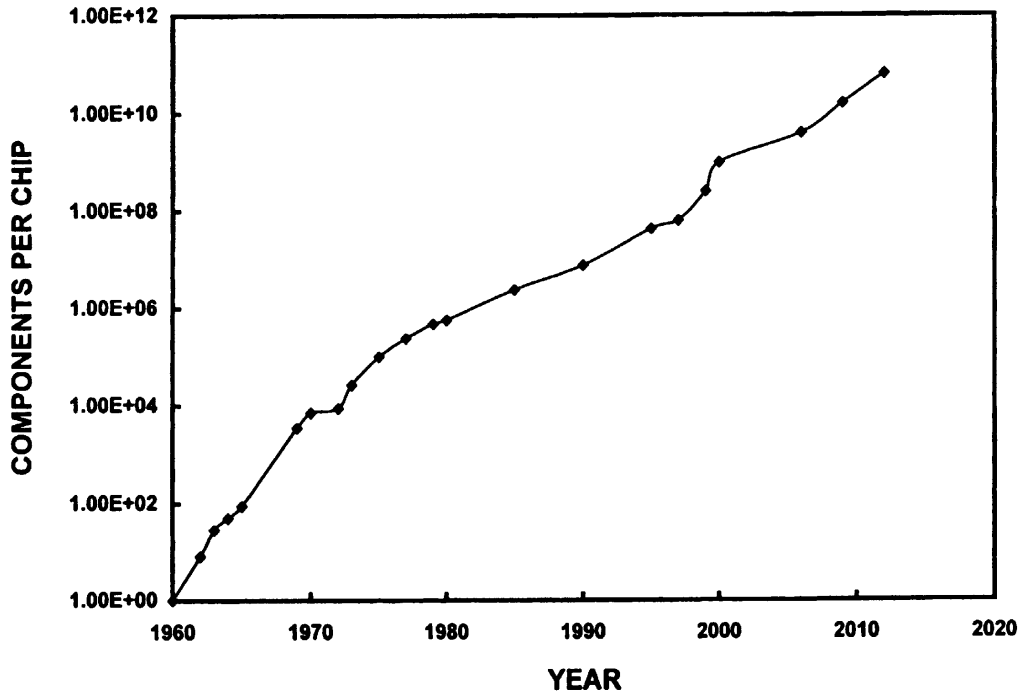


Figure 1.27 Exponential growth of components per IC ship for MOS memory. (After Harper.<sup>3</sup>)

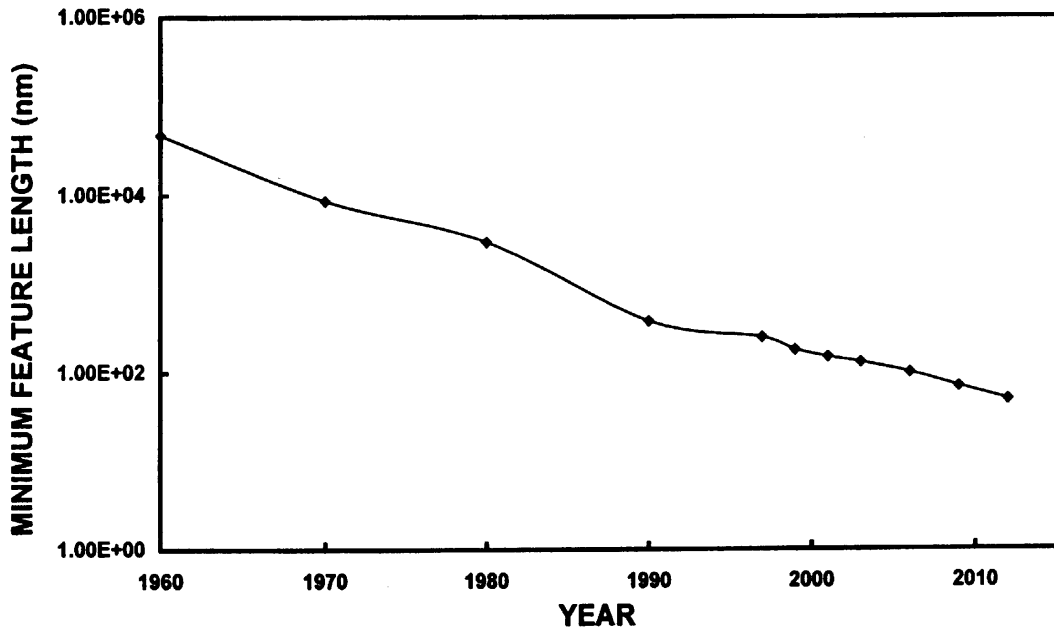


Figure 1.28 Exponential decrease of minimum device dimensions. (After Harper.<sup>3</sup>)



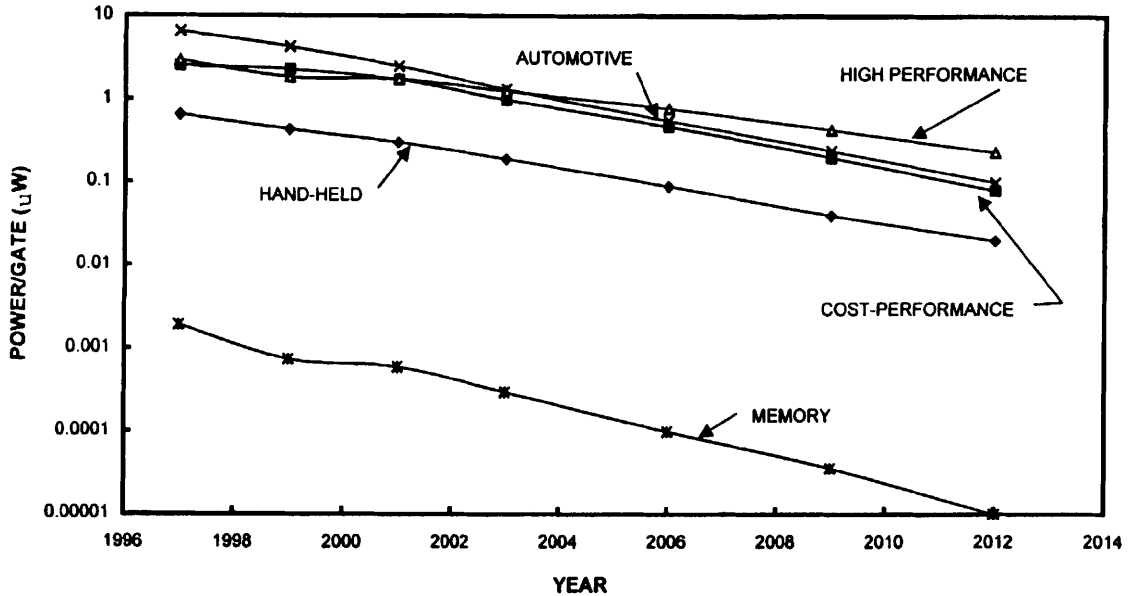


Figure 1.29 Trends in circuit power dissipation per gate. (After Harper.<sup>3</sup>)

per gate for five major IC application groups: automotive, high-performance, cost-performance, hand-held, and memory. Figure 1.30, on the other hand, shows that the power dissipation per chip actually increased over the same period of time for the high-performance and cost-performance groups, whereas, for the automotive, hand-held, and memory groups, the power dissipation remained relatively constant. This is explained by the fact that, while the power per gate scales linearly with feature size, the power dissipation per chip,  $P$ , is largely influenced by the inverse square of the feature-size, as shown below.

$$P = f(\text{Freq}, C, V^2, \text{Gate Count})$$

where  $\text{Freq}$  = clock frequency

$C$  = capacitance

$V$  = voltage

$\text{Gate Count}$  = chip area / (feature size)<sup>2</sup>

While the clock frequency and gate count have been increasing exponentially over the years (Figs. 1.27 and 1.31), the capacitance and voltage have been decreasing. Therefore, the increase in chip power dissipation is primarily due to the greater number of gates on a chip made possible by the decrease in the feature size.

Device miniaturization has resulted in significant improvements in on-chip switching speeds. Off-chip driver rise-time trends for ECL, CMOS, and GaAs are shown in Fig. 1.32. MOS circuits are known to be more sensitive to loading

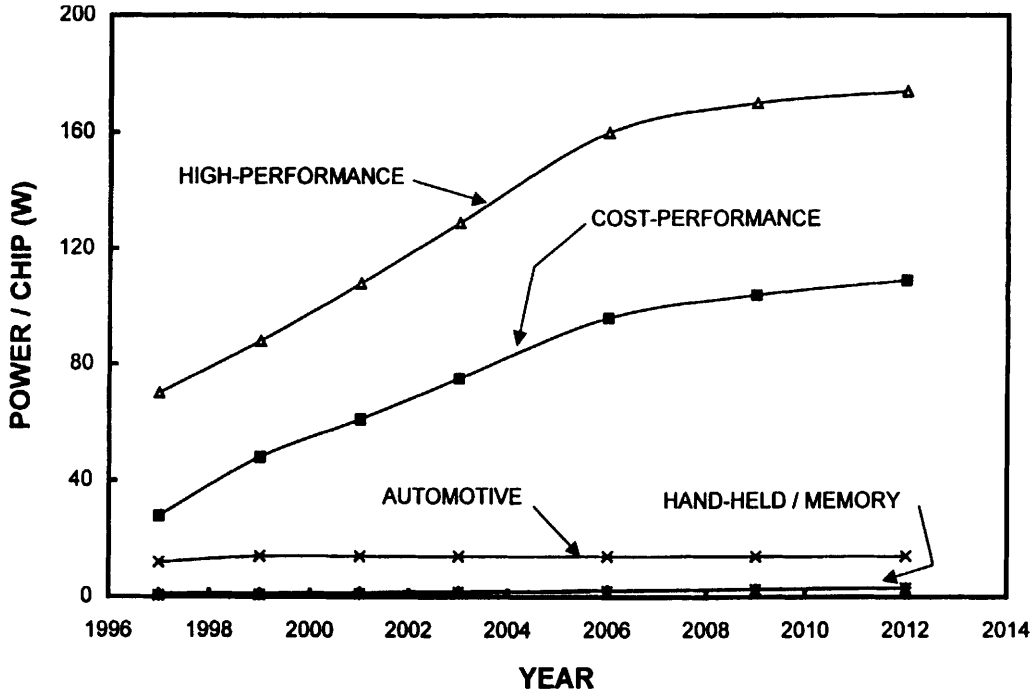


Figure 1.30 Trends in circuit power dissipation per chip. (After Harper.<sup>3</sup>)

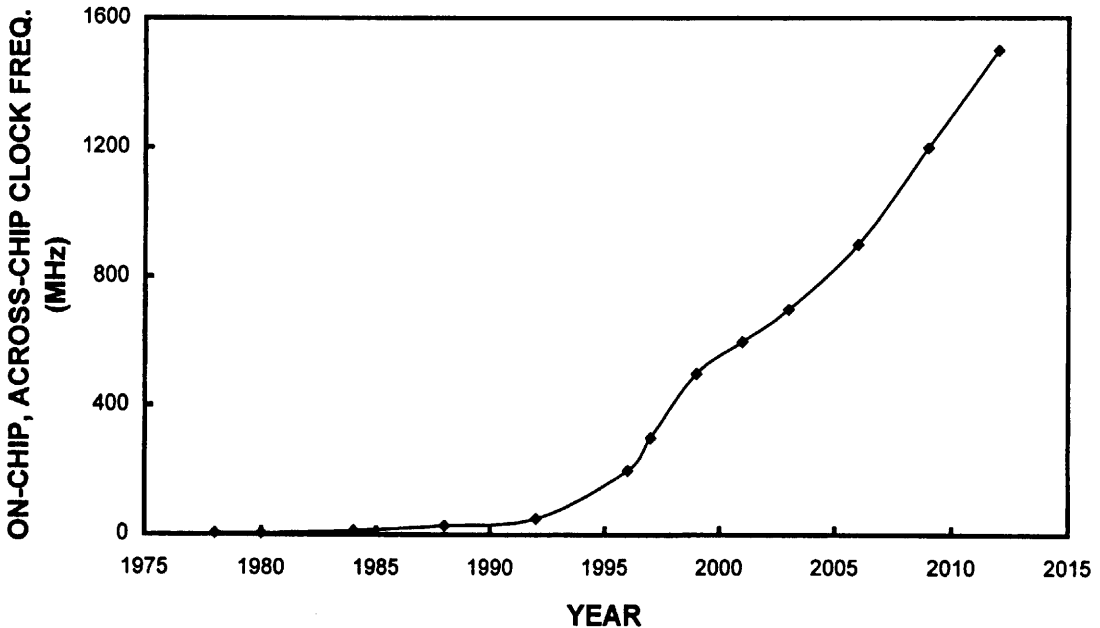


Figure 1.31 Frequency trends of high-performance ASIC chips. (After Harper.<sup>3</sup>)

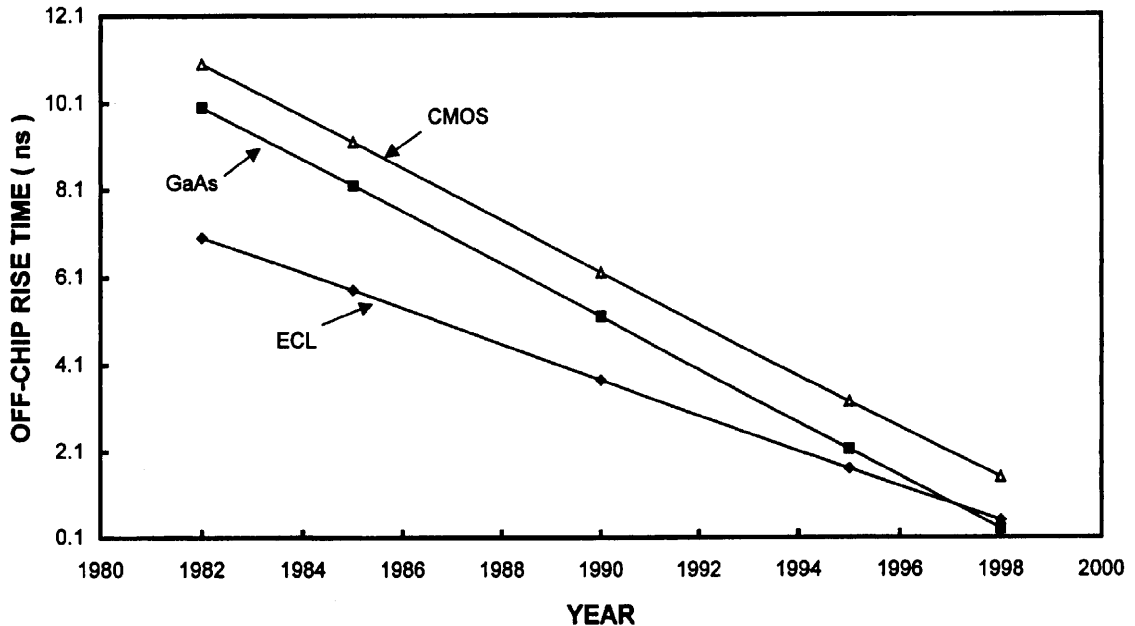


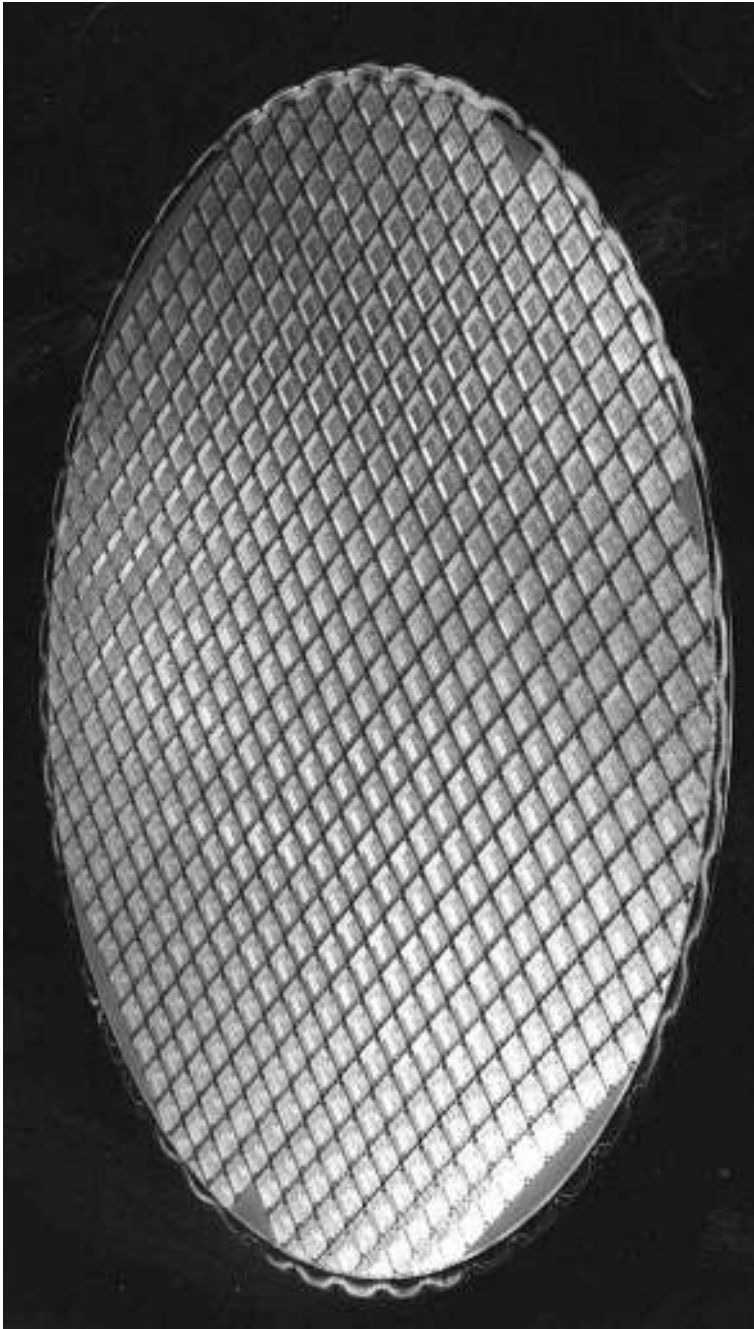
Figure 1.32 Off-chip rise times (typical loading). (After Harper.<sup>3</sup>)

conditions due to their relatively high output impedance. Hence, interconnect density is more important in MOS systems than for bipolar designs. As the applications for these devices tend toward the nanosecond and subnanosecond signal rise times, more attention will be directed to the electrical design consideration of packages and interconnections.

Reduced unit cost per function is a direct result of miniaturization. The cost per bit of memory chips was cut in half every two years for successive generations of DRAMs. By the year 2005, the cost per bit is projected to be between 0.1 and 0.2 microcents for a 1-Gb memory chip. Similar cost reductions are projected for logic ICs.

## 1.6 IC Chip Fabrication

This section describes wafer preparation and the processes involved in fabricating the solid state components (ICs). The IC chips, which are configured on the wafer in a step-and-repeat pattern, are formed in a batch process. The pitch of the chip array pattern is dependent on the IC chip size and the width of the “saw street” separating the chips from each other. The width of separation is equal to the thickness of the saw used in singulation. The economics of chip fabrication dictate that as many chips as possible be processed at the same time on a given wafer. Thus, reducing the size of the chips by decreasing their feature dimensions and using larger-diameter wafers are the most cost-effective ways of fabricating ICs. Figure 1.33 shows a typical wafer with chips covering the entire wafer surface.



**Figure 1.33** Typical wafer with an array of chips. (Courtesy of Agere Systems.)

Of all the semiconductor materials described in Sec. 1.4, silicon is used the most, because it is found in abundance in nature and its silicon dioxide ( $\text{SiO}_2$ ) has many properties ideal for IC fabrication. As a result, this section will use silicon as the exemplary material to describe IC fabrication.

IC fabrication comprises many physical and chemical process steps (Fig. 1.34) that involve state-of-the-art equipment in ultra-clean environments. The following are the step-by-step processes used to fabricate ICs.

### 1.6.1 Ingot growth and wafer preparation

Before starting on the fabrication of ICs, the silicon wafer, defined as the semiconductor substrate upon which ICs are formed, must be fabricated.

The first step in producing a silicon wafer is to refine raw silicon, which is obtained from either beach sand or quartz mined from agatized rock formations. The sand or quartz is heated along with reacting gases at approximately  $1700^\circ\text{C}$  to separate and remove the impurities. The remaining material is chemically purified silicon (nuggets), which has a polycrystalline structure that lacks uniformity in the orientation of its cells. The polycrystalline silicon cannot be used to fabricate wafers but has to be further processed to convert it into a monocrystalline structure containing a single-crystal silicon with uniform cell structures. The silicon nuggets are placed in a quartz crucible (Fig. 1.35) and heated to  $1415^\circ\text{C}$  (the melting point of silicon). From the molten silicon, a single-crystal ingot is grown and then sliced into wafers upon which ICs are fabricated.

There are several methods used to grow silicon ingot, but the Czochralski (CZ) method is the most popular. A single silicon crystal seed is placed at the end of a rotating shaft and lowered into the heated crucible until the seed touches the surface of the molten silicon (Fig. 1.35). By continually rotating the shaft and crucible in opposite directions and simultaneously pulling the seed away from the molten silicon, a silicon crystal is formed at the seed/melt interface with an identical crystal structure as the seed. The monocrystalline silicon ingot continues to be formed as the seed is slowly withdrawn from the crucible and the supply of molten silicon is replenished. To grow an n- or p-type crystal structure, small amounts of impurities (dopants) are introduced to the melt. For example, a phosphorus dopant, when mixed with the pure silicon melt, will produce an n-type crystal, whereas a boron dopant will produce a p-type.

The shape of the ingot consists of a thin circular neck formed at the seed end [approx. 0.12 in (3.0 mm) dia.], followed by the main cylindrical body, and ending with a blunt tail. The length and diameter of the ingot is dependent on the shaft rotation, withdrawal rate of the seed, and the purity and temperature of the silicon melt. Ingot sizes vary from 3 in (75 mm) to 12 in (300 mm) dia. and have a maximum length of approx. 79 in (2 m) (Fig. 1.36). The ingots are grown at a rate of about 2.5 to 3.0 in/hr (63.5 to 76.2 mm/hr).

The following are typical processing steps to prepare a silicon wafer for IC fabrication (Figs. 1.37 and 1.38):

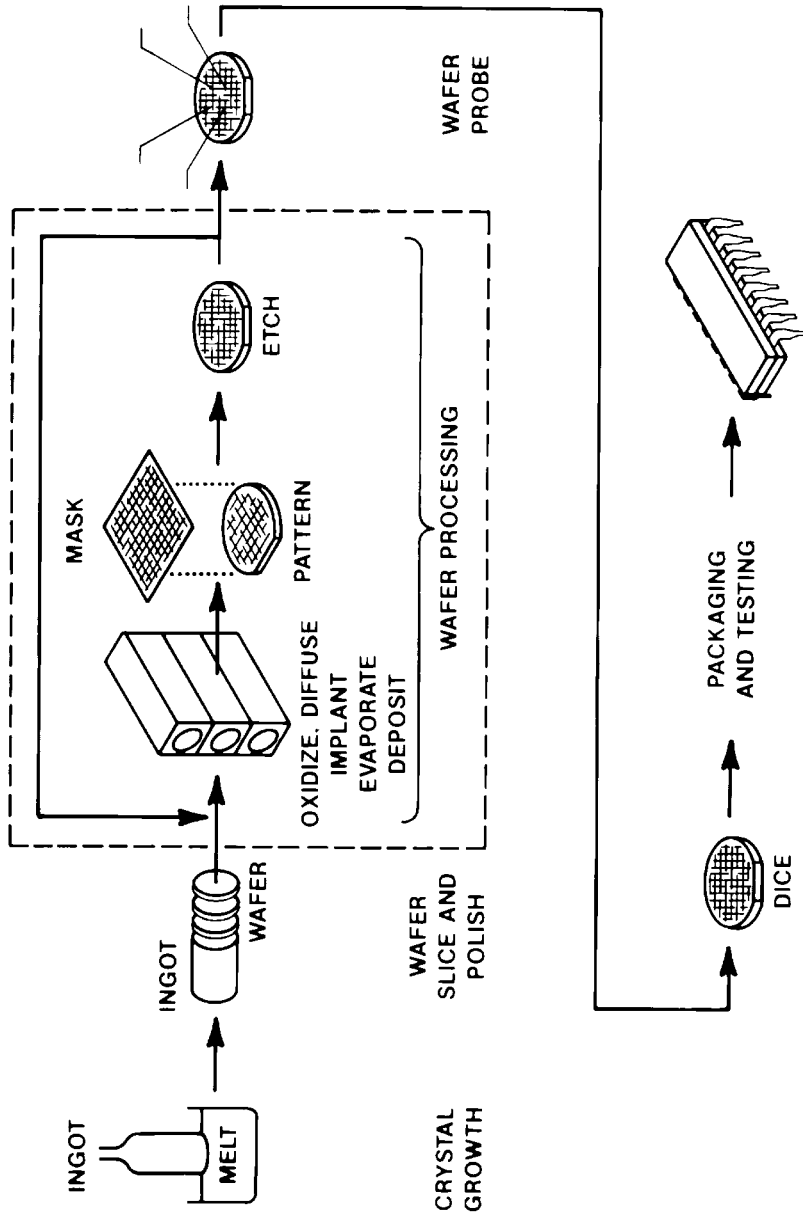
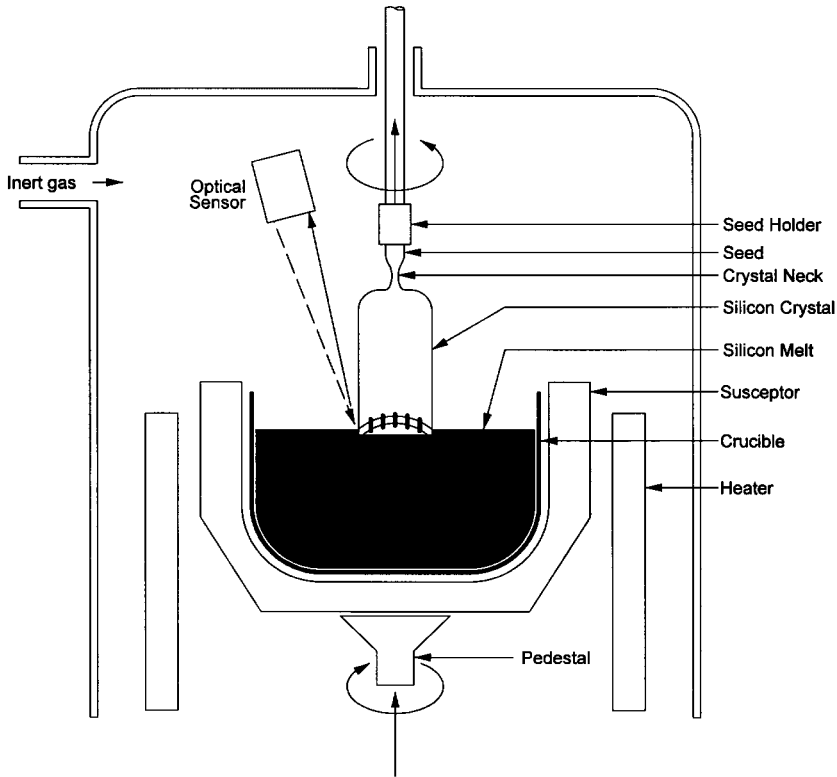


Figure 1.34 Typical IC fabrication processes.



**Figure 1.35** The Czochralski (CZ) method of growing a silicon ingot.

1. The ingot is cut to a uniform diameter and then checked for crystal orientation, conductivity type (n- or p-type), and resistivity (amount of dopant used).
2. A flat is ground along the axis to be used as reference for crystal orientation, wafer imaging alignment, and electrical probing of the wafer. Sometimes, a secondary, smaller flat is also ground, whose position with respect to the major flat signifies the orientation and type of conductivity (p- or n-type) the crystal has. Larger-diameter ingots may use a notch for this purpose.
3. The ingot is now ready to be sliced into thin disks, called wafers, which may vary in thickness from 0.020 in (0.50 mm) to 0.030 in (0.75 mm), depending on the wafer diameter. Wafers are sliced with either an inner diameter saw blade or a wire saw. The saw blade slicing technique consists of a 0.006-in (0.152-mm) thick stainless steel blade with an inside diameter cutting edge that is coated with diamonds. The cutting edge, being on the inner diameter of a large hole cut out of a thin circular blade, is fairly rigid. The slicing process is sequential; that is, one wafer is cut at a time, which takes approximately nine minutes.



**Figure 1.36** Typical silicon ingots. (Courtesy of Agere Systems.)

The wire saw, on the other hand, slices the wafers in a batch process, cutting all the wafers at once in a 16-in (410-mm) length of ingot. The process consists of a wire-winding mechanism, which positions the wires parallel to each other at a pitch equal to the wafer thickness to be cut. The wires are 0.007 in (0.170 mm) dia. and are made of stainless steel coated with brass. The slicing equipment includes a wire guiding unit and a tensioning and wire feed-rate mechanism. The wires continually travel in a closed loop by winding up on one spool and unwinding from another. A silicon carbide slurry, which acts as an abrasive, coats the wires prior to cutting through the silicon ingot. The wires travel about 10 m/s, and it takes approximately 5.5 hr to cut through all the wafers at once.

4. The wafers are laser marked for identification.
5. The sliced wafers are lapped, to remove any imperfections caused by sawing, and then deburred and polished on the top side, to a mirror-like finish. This provides a flat surface for subsequent IC fabrication processes.

### 1.6.2 Cleanliness

The processes explained so far involved preparation of the wafers for the next phase of IC fabrication, i.e., forming the circuitry. Before proceeding to describe new processes, we must first examine a critical aspect of IC fabrication that affects the yield at every step, namely the cleanliness of the environment where ICs are being produced. Contamination control in the fabrication area is of great concern, because lower yields, caused by unwanted particles, chemicals, or metallic ions in the atmosphere, increase IC costs.



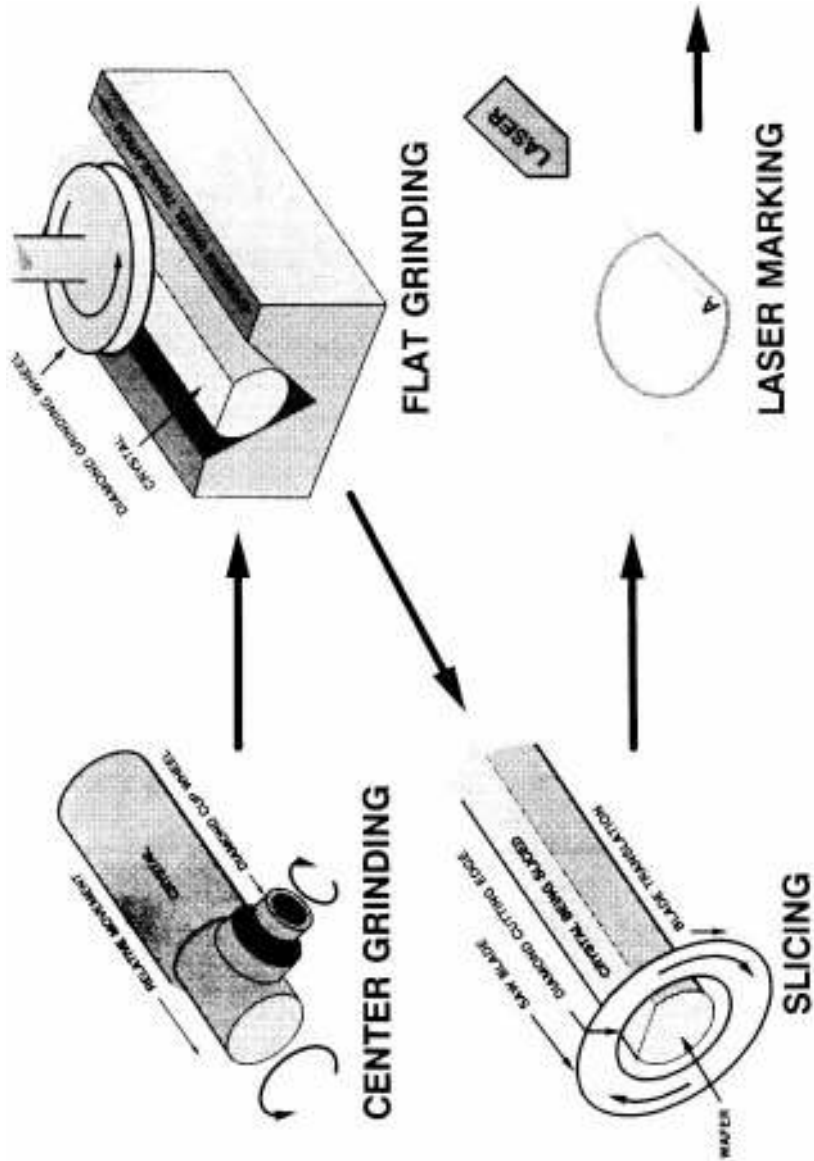


Figure 1.37 Cutting silicon ingot into wafers.

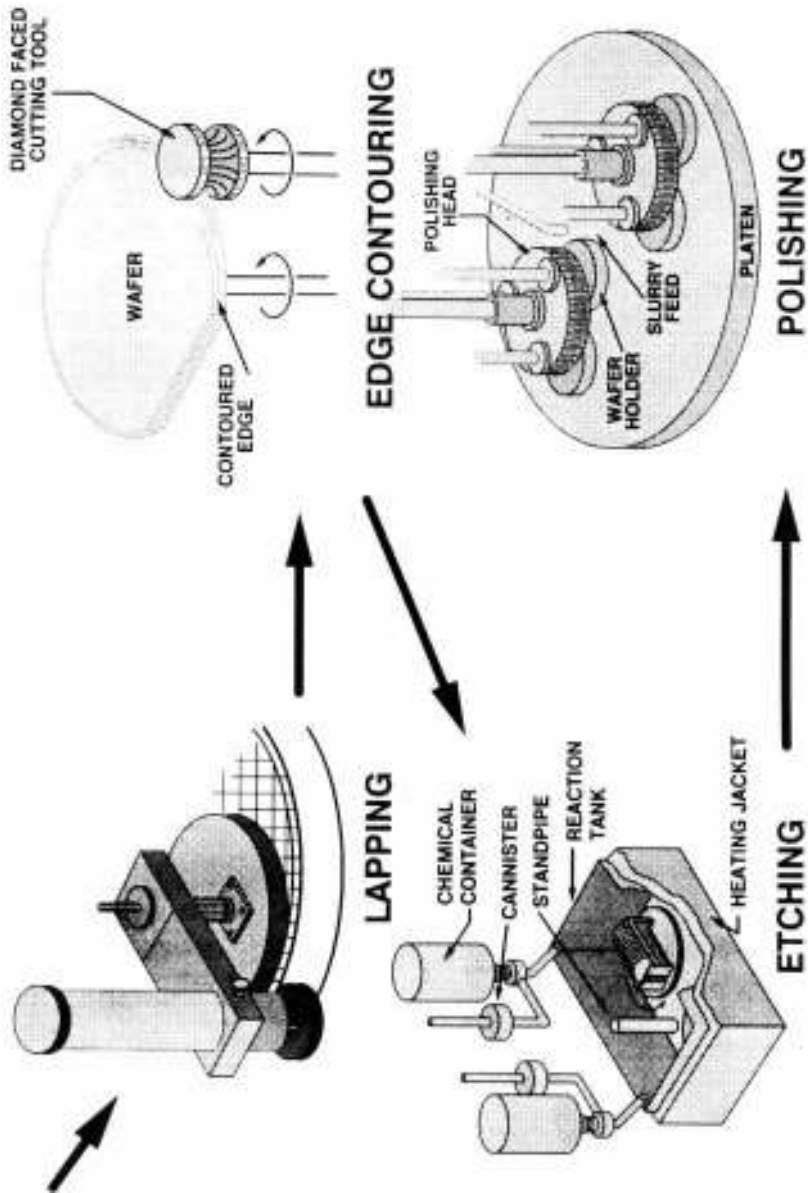


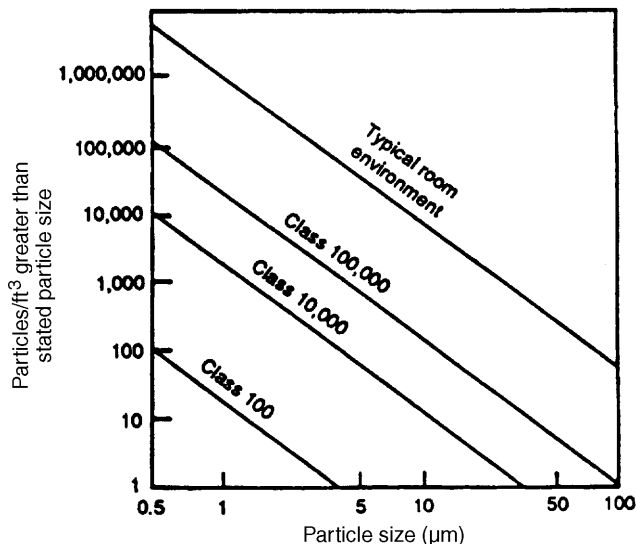
Figure 1.38 Wafer processing.

To control the environment, all IC fabrication processes are housed in clean rooms that are classified by how many particles, 0.5  $\mu\text{m}$  in diameter, are allowed in one cubic foot of air. In general, clean rooms range in classification from Class 1 to Class 100,000, with particle size distributions as shown in Figure 1.39. For example, a Class 1000 clean room can have 1000, 0.5- $\mu\text{m}$  size particles in one cubic foot. For IC fabrication, clean rooms range from Class 1 to Class 1,000, depending on the needs of the process.

### 1.6.3 IC fabrication

Having explained the importance of cleanliness on IC fabrication, let us resume with the processes involved in forming the circuitry in and on the wafers. The following ten basic IC fabrication processes are described:

- Oxidation
- Photolithography
- Diffusion
- Epitaxial deposition
- Metallization
- Passivation
- Backside grinding
- Backside metallization
- Electrical probing
- Die separation



**Figure 1.39** Particle size distribution in typical clean room atmosphere and in three classes of clean environments. (After Harper.<sup>3</sup>)

**1.6.3.1 Oxidation.** Oxidation is the process of forming a silicon dioxide ( $\text{SiO}_2$ ) layer on the surface of the silicon wafer. The silicon dioxide is an effective dielectric that is used to construct IC components, such as capacitors and MOS transistors. Because it acts as a barrier to doping and can easily be removed with a chemical solvent, the silicon dioxide is also an ideal template when used in the doping process. Silicon dioxide is formed by heating the wafer in an atmosphere of pure oxygen at a temperature between 900 and 1200°C, depending on the oxidation rate required. The oxidation can be speeded up if water vapor is introduced into the oxygen. The silicon dioxide growth on the silicon wafer, as the oxygen in contact with the wafer surface diffuses through the oxide layer to combine with the silicon atoms. As the oxide layer grows, it takes longer for the oxygen to reach the silicon, and the rate of growth slows. The growth of a 0.20-  $\mu\text{m}$  thick layer of silicon dioxide, at 1200°C and in dry oxygen, takes approximately 6 min, whereas, to double the oxide layer thickness to 0.40  $\mu\text{m}$  takes 220 min or 36 times as long.

The parameters that affect the silicon dioxide growth rate are

- Use of dry oxygen or in combination with a water vapor
- Ambient pressure within the furnace
- Temperature in the furnace
- Crystal orientation
- Time

The silicon dioxide layers vary in thickness from 0.015 to 0.05  $\mu\text{m}$  for MOS gate dielectrics or 0.2 to 0.5  $\mu\text{m}$  thick when used for masking oxides or surface passivation.

**1.6.3.2 Photolithography.** Photolithography is a patterning process whereby the elements representing the IC circuit are transferred onto the wafer by photomasking and etching. Photolithography has similarities to photographic processes. The images of the various semiconductor element layers are formed on reticles or photomasks made of glass, which are then transferred to a photoresist material on the surface of the silicon wafer. The resist may be of a type that changes its structure and properties to either UV light or laser. If it is a negative-acting photoresist, the areas that are exposed to UV light polymerize (harden) and thus are insoluble during development, whereas the unexposed areas are washed away. This results in a negative image of the photomask being formed in the photoresist. An alternative to the negative image forming photoresist is a positive-reacting photoresist, where the material behaves in the opposite way. Areas exposed to UV light become unpolymerized, or soluble when immersed in chemical solvents.

Until the advent of VLSI circuits in the mid 1980s, the negative-reacting photoresist, because of its superior developing characteristics, was the resist most commonly used in the industry. However, due to its poor resolution capability, the negative photoresist could no longer provide the requirements de-

manded by the high-density features of VLSI circuits. As a result, the semiconductor industry has transitioned to the positive-reacting photoresist because of its superior resolution capability. The transition was difficult, because not only was the photomask or reticle changed to a positive image, but the industry had to overcome the resist's lower adhesion capability and reduced solubility differences between polymerized and unpolymerized areas. Photomasking is used for patterning both the silicon dioxide and the metallization layers.

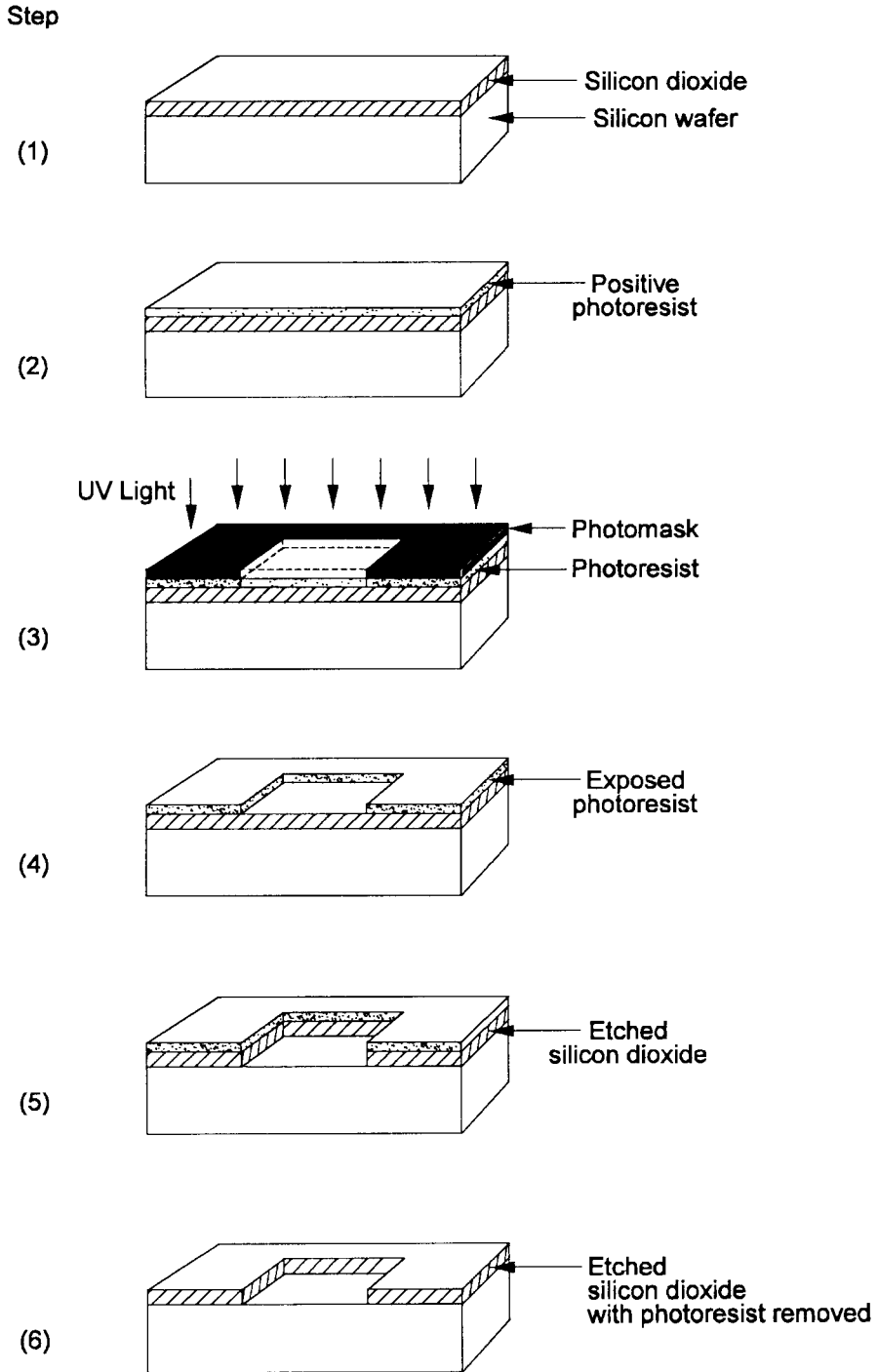
The increasing need for ICs to be smaller and operate at higher speeds has forced the industry to develop ICs with ever smaller features (see Sec. 1.5 for feature size trends). As feature sizes decrease, the patterning technology has to advance to where the requirements of high resolution, tight pattern registration (alignment), and highly accurate dimensional control are met. Photomasking is the most critical element of the IC fabrication process in that alignment of the different photomask overlays and mask contamination have an overwhelming effect on fabrication yield. The following photomasking methods are used for patterning:

- Optical exposure
  - Contact printing
  - Proximity printing
  - Scanning projection printing
  - Direct wafer stepping
- Non-optical exposure
  - Electron beam
  - X-ray lithography

The characteristics of each patterning method are described in Table 1.1.

A typical photolithography process for patterning the silicon dioxide layer consists of the following steps (Fig. 1.40):

1. The silicon wafer undergoes an oxidation process (Sec. 1.6.3.1) where a silicon dioxide ( $\text{SiO}_2$ ) layer is grown over its entire surface.
2. A drop of positive photoresist is applied to the  $\text{SiO}_2$ , and the wafer is spin coated uniformly across the surface.
3. If contact printing is used, a photomask, containing transparent and opaque areas that define the pattern to be created, is placed directly over the photoresist. In areas where the photoresist is exposed to UV light, projected through the mask, it becomes unpolymerized (does not harden), and where the UV light is blocked, the material polymerizes (hardens).
4. The photomask is removed, and the resist is developed to dissolve the unpolymerized areas, exposing the silicon oxide below.
5. The wafer is then wet or dry etched to remove the exposed oxide, resulting in a pattern identical to the photomask. Wet etching typically consists of



**Figure 1.40** Typical photolithographic process for selective removal of silicon dioxide.

**TABLE 1.1 Characteristics of Patterning Methods**

Patterning methods	Description	Advantages	Disadvantages
Contact printing	Mask is placed directly on resist with UV light shining through the mask onto the wafer.	Good resolution High throughput	Causes defects such as scratching of mask and resist Adherence of dirt to the mask may block the light
Proximity printing	Small separation between mask and resist with UV light shining through the mask onto the wafer.	Less damage to mask and resist High throughput	Poor resolution due to some light scattering Not used for VLSI photomasking
Scanning projection printing	The UV light source is a slit projected through the mask. By use of optics, the pattern image of one slit width at a time is projected onto the wafer, exposing the resist	Good resolution High throughput	Alignment problems Possible image distortion from dust and glass damage
Direct wafer stepping	Based on refractive optics, the image of one or several chip sites is projected onto the wafer exposing the resist. The process is step repeated until the whole wafer is patterned.	Good resolution with fewer defects Better alignment Less vulnerable to dust and dirt Most used for VLSI fabrication Medium throughput	Tight maintenance requirement of humidity and temperature control
Electron beam	An electron beam produces a small diameter spot that is directed in an x-y direction, onto the wafer. The electron beam is capable of being turned ON and OFF to expose the resist as needed to form the pattern.	No mask is used Excellent resolution	High cost Low throughput
X-ray lithography	The process resembles the UV light system of the proximity printing method, but high energy X-rays are used instead.	Produces smaller pattern than light sources Excellent resolution	Requires masks made from gold or other refractory materials capable of blocking X-rays Low throughput

immersing the wafer in a diluted solution of hydrofluoric acid for a specified time that will result in complete etching. The wafers are then rinsed and dried. Wet etching is primarily used for wafers with IC feature sizes greater than 3  $\mu\text{m}$ . For high-density etching, the dry etching technique is used, because it's more precise. Dry etching can be accomplished by three different etching techniques: plasma, ion beam milling, and a reactive ion etch. All three techniques use gases as the etching medium.

6. The remaining photoresist is removed with a chemical solvent.

This process is repeated a number of times to create the desired semiconductor elements on the wafer surface.

**1.6.3.3 Diffusion.** As was discussed in Sec. 1.4, when forming solid state components, silicon is not used in its natural or intrinsic state but is converted to either an n-type or p-type semiconductor. The n- or p-type materials, by themselves, are of little value unless they are joined to form a p-n junction. Diffusion or doping is the process of implanting impure atoms in a single crystal of pure silicon so as to convert it into n-type or p-type material. Depending on the dopant element used, antimony, arsenic, and phosphorus will produce an n-type material, whereas boron will produce a p-type structure. The basic dopant elements are available either in solid, liquid, or gaseous states as shown in Table 1.2. Type of dopant, dopant concentration, time of exposure, and temperature affect the diffusion process.

**1.6.3.4 Epitaxial Deposition.** This is a process whereby a thin layer of silicon (approximately 25  $\mu\text{m}$  thick) is deposited upon the surface of an existing silicon wafer and doped using the same dopant types and delivery systems used in the diffusion process. Thus, this is another technique for fabricating p-n junctions. Although there are several deposition methods available, chemical

**TABLE 1.2 Common Dopant Sources (after Zant<sup>6</sup>)**

Type	Element	Compound name	State
n-type	Antimony	Antimony trioxide	Solid
		Arsenic	Solid
	Phosphorus	Arsine	Gas
		Phosphorus oxychloride	Liquid
		Phosphorus pentoxide	Solid
		Phosphine	Gas
p-type	Boron	Boron tribromide	Liquid
		Boron trioxide	Solid
		Diborane	Gas
		Boron trichloride	Gas
		Boron nitride	Solid



vapor deposition (CVD) is the most commonly used technique. The basic CVD process consists of the following:

1. Silicon wafers are placed in a reaction chamber with an inert gas and heated to a temperature that depends on the reaction and parameters of the deposition method used and layer thickness required.
2. Reactant gases are introduced into the reaction chamber at a specified flow rate, where they come in contact with the wafer surface.
3. As the reactants are absorbed by the silicon wafer, the chemical reaction forms the deposition layer. The surface reaction rate is dependent on the temperature; increasing the temperature increases the reaction rate.
4. To dope the deposition layer, dopant gases are introduced into the reaction chamber where they combine with the deposited layer to form an n- or p-type material.
5. The gaseous by-products are flushed from the reaction chamber.
6. The wafers are removed from the chamber, and the deposited layer is checked for thickness, coverage, purity, cleanliness, and n- or p-type composition.

Variations in the CVD techniques, involving changes in vapor pressure and temperature in the chamber, have resulted in process enhancements. There are three different CVD techniques used in the industry:

- Atmospheric pressure CVD (APCVD)
- Low-pressure CVD (LPCVD)
- Plasma-enhanced CVD (PECVD)

The characteristics of the above techniques are shown in Table 1.3.

**TABLE 1.3 CVD Techniques (after Wolfe<sup>5</sup>)**

Process	Advantages	Disadvantages	Application	Temp. range
APCVD	Low chemical reaction temperature Simple horizontal tube furnace Fast deposition	Poor coverage Particle contamination	Low temperature oxides, both doped and undoped	300–500°C
LPCVD	Good coverage and uniformity Vertical loading of wafers for increased productivity	High temperature Low deposition rate	High temperature oxides, both doped and undoped	580–900°C
PECVD	Lower chemical reaction temperature Good composition, coverage and throughput	High equipment cost Particulate contamination	Low temperature insulators over metals or passivation	200–500 °C

**1.6.3.5 Metallization.** The deposition of a conductive material, to form the interconnection leads between the circuit component parts and the bonding pads on the surface of the chip, is referred to as the *metallization* process. As chip density increases, interconnection can no longer be accomplished on a single level of metal but requires multilevel metallization with contact holes or vias interconnecting the various levels.

Materials such as aluminum, aluminum alloys, platinum, titanium, tungsten, molybdenum, and gold are used for the various metallization processes. Of these, aluminum is the most commonly used metallization material, because it adheres well to both silicon and silicon dioxide (low contact resistance), it can be easily vacuum deposited (it has a low boiling point), it has a relatively high conductivity, and it patterns easily with photoresist processes. In addition to pure aluminum, alloys of aluminum are also used for different performance related reasons; i.e., small amounts of Cu are added to the aluminum to reduce the potential for electromigration effects. Electromigration may occur during circuit operation, when high currents are carried by the long aluminum conductors, inducing mass transport of metal between the conductors. Sometimes small amounts of silicon or titanium are added to the aluminum to reduce the formation of metal “spikes,” that occur over contact holes.

The aluminum metallization process consists of depositing aluminum on the wafer surface and again using the photoresist process to etch away the unwanted metallization. One of the techniques used to apply the aluminum is the vacuum deposition process wherein the aluminum is evaporated in a high-vacuum system and redeposited over the wafer surface. This process has the disadvantage of nonuniform metal coverage. Sputtering is another method for depositing aluminum metallization. Because it offers better control of the metallization quality than the vacuum deposition method, it's currently being used in the majority of IC metallization processes. Sputtering is a physical (nonchemical) method of deposition, which is performed by ionizing inert gas (Argon) particles in an electric field and then directing them toward an aluminum target. There, the energy of the incoming particles dislodge or “sputters off” atoms of the aluminum target, which are then deposited onto the wafer.

One of the problems encountered when pure aluminum is in contact with silicon, while being heated, is the formation of an eutectic aluminum-silicon alloy. The alloy formation penetrates into the wafer, where it can reach shallow junctions, causing leakages or shorting. To alleviate this problem, a metal barrier such as titanium tungsten (TiW) or titanium nitrate (TiN) is placed between the aluminum and the silicon. Adding silicon (1 to 1.5 percent by weight) to the aluminum is another way of preventing the formation of aluminum-silicon alloy, although this is less effective. Some alloying with the silicon wafer still occurs, but to a lesser extent.

The electrical performance of any given type of metallization is dependent on its resistivity, contact resistance, and the length and thickness of the conductor. To improve electrical performance in MOS circuits, the resistivity and contact resistance of the conductors are reduced through the use of barriers made of refractory metals such as titanium, tungsten, platinum, and molybde-

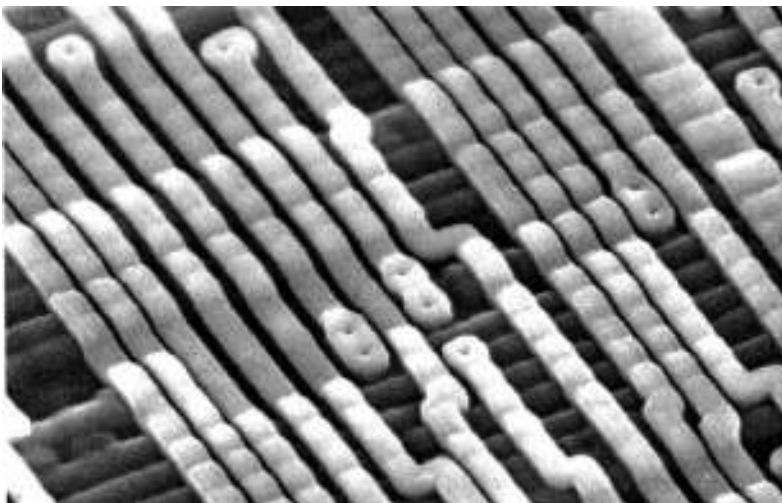
num, in combination with silicon, to form silicides of  $\text{TiSi}_2$ ,  $\text{WSi}_2$ ,  $\text{PtSi}_2$ , and  $\text{MoSi}_2$ , respectively. The silicides can also be used as conductors or via plugs.

As more and more chips are required to operate at higher frequencies, the current aluminum metallization can no longer meet the lower resistances needed to prevent data processing delays. As a result, copper has started to replace aluminum because of its lower resistance and reduced electromigration problems.

**1.6.3.6 Passivation.** The passivation layer is deposited at the end of the chip metallization process and is used to protect the aluminum interconnecting circuitry from moisture and contamination. An insulating or passivation layer of silicon dioxide or silicon nitride is vapor deposited over the chip circuitry (Fig. 1.41), with bond pads remaining exposed for wire bonding or flip-chip interconnection.

**1.6.3.7 Backside grinding.** At the end of the IC fabrication process, after the passivation layer is applied, wafers are sometimes thinned to fit the overall package height requirements. The thinning process consists of back grinding the wafer, similar to the procedure used in lapping the wafer, to remove any imperfections caused by sawing (Fig. 1.38)

**1.6.3.8 Backside metallization.** In cases in which the chip is to be eutectically bonded to a ceramic package, or where the back of the chip has to make electrical contact with the die attach area, it is necessary for the chip to have a gold film backing. The gold film is deposited by vacuum evaporation or sputtering and is done after backgrinding.



**Figure 1.41** IC circuitry covered by a passivation layer. (Courtesy of Agere Systems.)

**1.6.3.9 Electrical probing.** The last step in wafer processing is to test the die. A test probe makes contact with the bonding pads on the surface of the wafer, and the chips are electrically tested against predetermined specifications. Chips thought to be faulty are inked, or an electronic map is developed indicating the bad chips.

**1.6.3.10 Die separation.** After the chips have been electrically tested, the chips are separated by two different methods:

1. *For chips thinner than 0.010 in (0.25 mm):* The chips are separated by first scribing shallow, fine, diamond-cut lines between the chips and then mounting the wafer onto a release tape affixed to a steel ring. Pressure from a roller is then exerted on the wafer, breaking it up into individual chips. The individual chips that tested good are removed by pushing the chip up (with a pin) from the underside of the tape and then picking them up with a vacuum tool called the *collet*. The chips are placed in a tray or are automatically transferred to the die attach process for IC packaging. This type of separation method may cause rough and cracked edges on the chip.
2. *For chips greater than 0.010 in (0.25 mm) thick:* As above, the wafer is mounted onto a release tape affixed to a steel ring and then cut between the chips, through the silicon thickness, using a diamond-impregnated round saw. The method for removing the good chips from the tape is similar to that for thinner chips. Unlike the break-up method, this separation process leaves smooth edges on the chip.

#### 1.6.3.11 Typical construction of a p-n-p bipolar transistor (Fig. 1.42)

1. A silicon dioxide ( $\text{SiO}_2$ ) layer is grown on a p-doped silicon wafer (Sec. 1.6.3.1).
2. A positive photoresist layer is applied to the  $\text{SiO}_2$  (Sec. 1.6.3.2).
3. A photomask is created with opaque and clear areas, patterning the clear areas in locations where windows in the  $\text{SiO}_2$  are to be formed. The photomask image is transferred onto the positive photoresist, which becomes polymerized in the areas where it is not exposed to the UV light (opaque areas in the photomask).
4. The resist is developed, and the unpolymerized areas dissolve, forming a window that exposes the  $\text{SiO}_2$ .
5. The silicon dioxide is etched away in the photoresist windows, exposing the silicon wafer.
6. The photoresist is removed.
7. Using phosphorus as the dopant, an n-type region in the p-type silicon base is created by diffusion (Sec. 1.6.3.3).

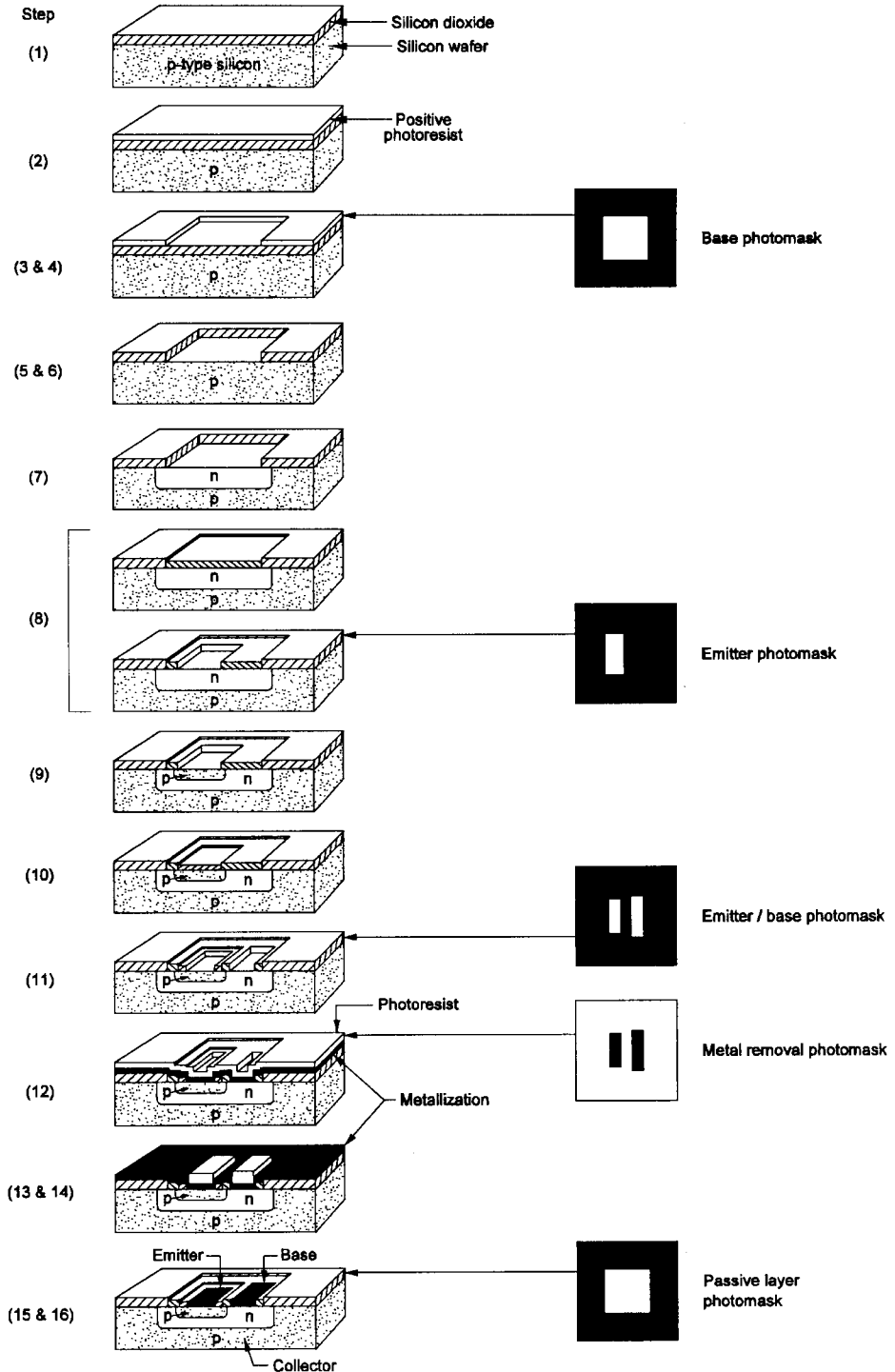


Figure 1.42 Typical process sequence in the fabrication of a silicon planar bipolar transistor.

8. A new layer of silicon dioxide is grown on the surface of the n-region, and steps (2) through (6) are repeated to create a new window in the  $\text{SiO}_2$ .
9. A second diffusion creates the p-type region in the n-type base by using boron as the dopant.
10. Silicon dioxide ( $\text{SiO}_2$ ) is again grown over the exposed silicon wafer, and the photoresist is applied over the  $\text{SiO}_2$ .
11. The photomask, containing the two clearances for the emitter and base, is placed over the positive photoresist, and steps (2) through (6) are repeated.
12. The structure is now ready for metallization. An aluminum film is deposited over the entire surface, followed by a coating of positive photoresist.
13. The photomask, with the emitter and base areas opaque, is placed over the photoresist and exposed to UV light.
14. The photoresist is developed, leaving the resist over the emitter and base areas.
15. The exposed metallization is etched away, followed by the removal of the resist over the emitter and base areas.
16. A passivation layer of silicon nitride is applied to the circuitry, leaving the bond pads exposed.
17. The silicon planar bipolar transistor is now complete.

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# Plastics, Elastomers, and Composites

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## 2.1 Introduction

Prior to 1930, most household goods and industrial components were made of metals, wood, glass, paper, leather, or vulcanized rubber. Since then, plastics have made significant advances in the markets of all these materials as well as creating new markets of their own. The widespread use of plastics has been brought about because of their unique combination of properties such as strength, light weight, low cost, and ease of processing and fabrication. Plastics are not the panacea of industry's material problems, but they offer such a unique combination of properties that they have become one of the important classes of materials and have found widespread use in the electrical and electronics industries.

Plastics play a key role in these industries and function in a variety of ways. The most common application of polymers in electrical and electronic devices is for insulation, which prevents the loss of the signal currents and confines them to the desired paths. Insulation systems exist in a variety of forms (liquids, solids, and gases), and the type of material used determines the life span of the device. Plastic materials also perform structural roles, support the circuit physically, and provide environmental protection from such elements as moisture, heat, and radiation to sensitive electronic devices. Continuing improvements in the properties of plastics over the years have made them even more important to the electrical industry by extending their useful range.

It is the purpose of this chapter to present to the reader an overview of the nature of plastic materials. This overview will include topics related to plastic fundamentals, thermoplastics, thermosets, elastomers, and applications in

## 2.2 Chapter 2

electrical and electronic systems. The overview pertains only to plastics that are of significant importance in the electronics industry.

## 2.2 Fundamentals

### 2.2.1 Polymer definition

Polymers are macromolecules, that is, large molecules formed by the linking together of large numbers of small molecules called *monomers*. The process involved in the joining of these monomers is called *polymerization*. Plastics are a group of synthetic polymers made up of chains of atoms or molecules. The long molecular chains contain various combinations of oxygen, hydrogen, nitrogen, carbon, silicon, chlorine, fluorine, and sulfur. As more repeating units are added, molecular weight of the plastic increases and can reach into the millions but, typically, most polymers used for practical applications fall into the molecular weight range of 5000 to 200,000.

### 2.2.2 Types of polymers

There are several different ways to classify polymers. They can be differentiated by the way in which their monomers are joined together, that is, addition or condensation polymerization. In addition polymerization, the molecular chains are formed by the successive addition of one monomer to another. Typical addition polymers are polyolefins, polystyrenes, acrylics, vinyls, and fluoroplastics. Condensation polymers are prepared by the reaction of two different molecules, each having two reactive end groups. Molecular weight is built up by the linking together of these end groups and elimination of a small molecule (such as water). The small molecule must be removed from the reaction medium to attain a high molecular weight. Examples of condensation polymers include polyamides, polyesters, polyurethanes, and polyimides.

All polymers can be classified in this manner, but they can also be further subdivided to define their structural and compositional characteristics more accurately. They can be linear, branched, crystalline, amorphous, or liquid crystalline copolymers, elastomers, and alloys. All of these, except elastomers, can be divided into two major groups—thermoplastics and thermosets. Both types of plastics are fluid enough to be formed and molded at some stage in their conversion to the finished product. Thermoplastics solidify by cooling and can be remelted. Thermoset resins undergo cross-linking to form a three-dimensional network, and, unlike thermoplastics, they cannot be remelted and reshaped.

With few exceptions, to meet processing and performance requirements, polymers are mixed with other materials to yield a compounded polymer, which may be in the form of pellets, granules, powder, or liquid. A monomer may be polymerized with one or more different monomers in a process called *copolymerization*. These polymers are called *copolymers* or *terpolymers*, depending on whether two or three comonomers are used during the copolymerization. Another technique used to vary the properties of polymers is to blend

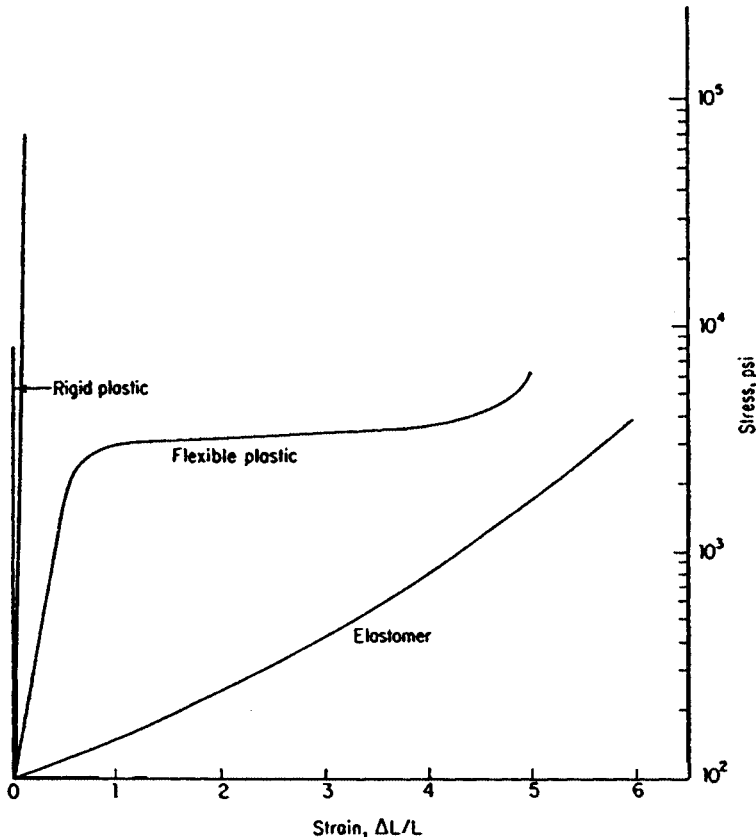


one polymer with another mechanically to form an alloy. The properties of these alloys generally fall between those of the starting polymers.

Elastomers differ significantly from plastics. While they are also polymers, elastomers easily undergo very large reversible elongations at relatively low stresses. For this to happen, the polymer must be completely amorphous with a low glass transition temperature and low secondary forces so as to obtain high mobility of the polymer chains. Some degree of cross-linking is needed so that the deformation is rapidly reversible. Figure 2.1 illustrates the differences between rigid and flexible plastics, and elastomers by way of a stress-strain plot.

### 2.2.3 Structure and properties

In addition to the broad categories of thermoplastics and thermosets, polymeric materials can be classified in terms of their structure: linear, branched, cross-linked, amorphous, crystalline, and liquid crystalline. As mentioned, a polymer molecule consists of monomer molecules that have been linked to-



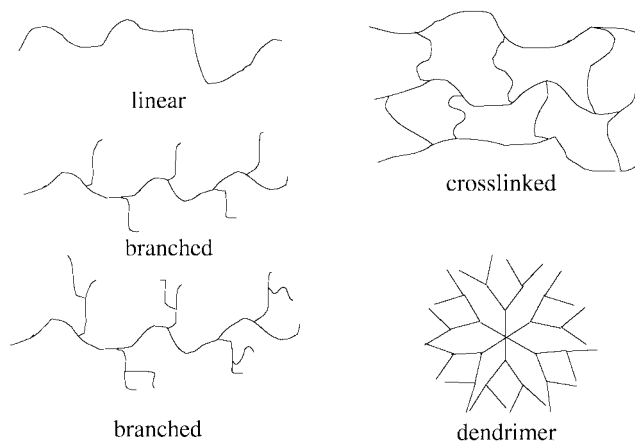
**Figure 2.1** Stress-strain plots for typical flexible and rigid plastics and elastomers. (From Odian,<sup>1</sup> reprinted with permission.)

gether in one continuous length. Such a polymer is termed a *linear polymer*. Branched polymers are those in which there are side branches of linked monomer molecules protruding from various points along the main polymer chain. By carefully controlling the reaction conditions to prevent cyclization, it is possible to prepare hyperbranched polymer and *dendrimers*.<sup>2</sup> Hyperbranched polymers have an irregular structure and reactive sites throughout the structure. Dendrimers are more regular structures, having a core and layers of branched repeat units radiating from the core. By derivatizing, the outer layer materials having unique properties are accessible. Cross-linked polymers are those in which adjacent molecules are linked together, resulting in a complex interconnected network. Figure 2.2 is a schematic illustration of these structures.

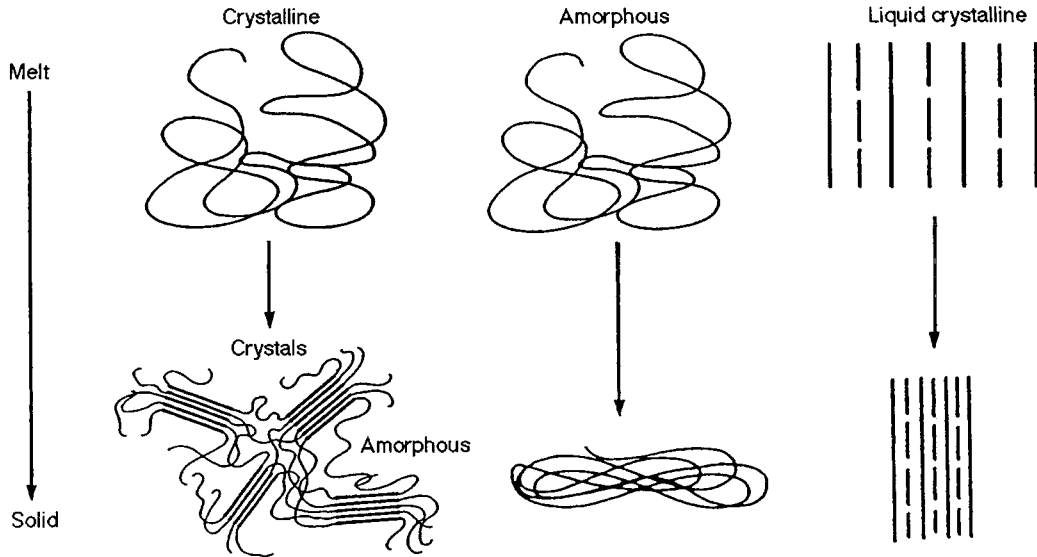
In some thermoplastics, the chemical structure is such that the polymer chains will fold on themselves and pack together in an organized manner (Fig. 2.3). The resulting organized regions show the behavior characteristics of crystals. Plastics that have these regions are called *crystalline*. Plastics without these regions are called *amorphous*. All of the crystalline plastics have amorphous regions between and connecting the crystalline regions. For this reason, the crystalline plastics are often referred to as *semicrystalline* in the literature.

Liquid crystalline polymers are best thought of as being a separate and unique class of plastics. The molecules are stiff, rod-like structures that are organized in large parallel arrays or domains in both the melted and the solid states. These large, ordered domains provide liquid crystalline polymers with unique characteristics as compared to those of the crystalline and amorphous polymers.

Many of the mechanical and physical property differences between plastics can be attributed to their structures. As a generalization, the ordering of crystalline and liquid crystalline thermoplastics makes them stiffer, stronger, and less impact resistant than their amorphous counterparts. Moreover, crystal-



**Figure 2.2** Structures of polymer molecules.



**Figure 2.3** Two-dimensional representation of crystalline, amorphous, and liquid crystalline structures. (From Hoechst Celanese,<sup>3</sup> reprinted with permission.)

line and liquid crystalline materials have a higher resistance to creep, heat, and chemicals. Crystalline materials are typically more difficult to process, because they have higher melt temperatures and tend to shrink and warp more than amorphous polymers. Amorphous polymers soften gradually and continuously as heat is applied, and in the molding process they do not flow as easily as do melted crystalline polymers. Liquid crystalline polymers have the high melt temperature of crystalline plastic but soften gradually and continuously like amorphous polymers. They have the lowest viscosity, warpage, and shrinkage of the thermoplastics.

One of the most important characteristics of a polymer is its molecular weight, because the properties of a polymer are a consequence of its high molecular weight. Strength does not usually develop in polymers until a minimum molecular weight (5,000 to 10,000) is attained. Above this value, there is a rapid increase in mechanical properties, then a leveling off as the molecular weight increases further. In most instances, there is some molecular weight range for which a given polymer property will be optimal for a particular application. Polymers are not all homogeneous but are composed of molecules of different sizes. To characterize the size of a polymer completely, one should know both its molecular weight and its molecular weight distribution. Both of these properties affect processing and strength significantly.

#### 2.2.4 Synthesis

There are four basic methods of producing a polymer. Many factors influence the choice of a particular method. In many instances, the nature of the reaction chemistry dictates the specific method to be used. In other instances, the

characteristics of resultant polymer (low or semiviscous liquid, friable or rigid solid) may limit one's choice. The interested reader is referred to any basic organic polymer chemistry text for more detailed descriptions.

**2.2.4.1 Bulk polymerization.** From the point of view of equipment, complexity, and economics, the simplest method is mass or bulk polymerization. This procedure merely allows the monomer to react at a predetermined reaction temperature, with or without catalysts, to form the polymer. Theoretically, the monomer can be a gas, liquid, or solid, but in practice almost all mass polymerizations take place in a liquid phase. Gaseous-phase bulk polymerization takes place under pressure, often requiring specific catalysts for conversion.

The polymer may be either soluble or insoluble in the monomer. If the former, then the mass viscosity continually increases until the final degree of polymerization is obtained. In the latter, the polymer will precipitate from the remaining unreacted monomer and can be separated subsequently.

A serious drawback to bulk polymerization is control of the heat of reaction. The generated exothermic heat tends to stay within the mass and is not easily withdrawn. Stirring the mass helps, but as the viscosity continues to increase, stirring becomes more difficult, with a less efficient heat-dissipation mechanism. This lack of control causes difficulty in the control of the molecular weight and the molecular weight distribution (MWD) of the final polymer. The method does, however, lend itself for use in small casting or batch production.

In summary, mass or bulk polymerization uses simple equipment, is highly exothermic with difficult heat control, and yields a polymer with a broad MWD.

**2.2.4.2 Solution polymerization.** Heat removal can be simplified if the polymerization is carried out in a suitable solvent, because the solution of solvent, monomer, and polymer is less viscous than molten polymer. This technique is called *solution* polymerization. If a solvent can be found in which the monomer is soluble but the polymer is insoluble, the resultant polymer precipitation facilitates the separation steps.

In summary, one can control heat more readily in solution polymerization, although higher-molecular-weight polymers are difficult to produce. A solution of the polymer itself may be marketable, but the purification of solid polymer may involve complex procedures.

**2.2.4.3 Emulsion polymerization.** If the monomer can be polymerized in a water emulsion, then we can retain the low viscosity needed for good heat control without the hazards associated with the handling of solvents. Such a procedure is called *emulsion polymerization*.

Reaction rates and molecular weights are usually higher with this method than with mass or solution polymerization. The MWD is often quite narrow, water is cheaper and less hazardous than solvent, and recovery steps are not

as complex. However, ingredients must be added to aid emulsification (emulsifying and stabilizing agents). This added contamination and the requirement of a drying step for the polymer constitute significant disadvantages to the process.

**2.2.4.4 Suspension polymerization.** Finally, there is suspension polymerization, in which the monomer and globules of the forming polymer are maintained in suspension by agitation without the use of an emulsifying agent. The polymer beads are formed by coalescence, and their size is regulated by suspension stabilizers and the amount and intensity of agitation. The final beads must be screened out of the liquid phase, washed, and dried before they can be used, although suspensions can be, and are, marketable. Control of exothermic heat is good, and high-molecular-weight polymers with relatively narrow MWDs are possible.

## 2.2.5 Terminology

To acquaint those unfamiliar with the language of polymers, Tables 2.1 and 2.2 present terms associated with polymers and their use in the electronics industry.

**TABLE 2.1 Definition of Terms for Plastic Materials**

Accelerator	A chemical used to speed up a reaction or cure. For example, cobalt naphthenate is used to accelerate the reaction of certain polyester resins. The term <i>accelerator</i> is sometimes used interchangeably with the term <i>promoter</i> . An accelerator is often used along with a catalyst, hardener, or curing agent.
Adhesive	Broadly, any substance used in promoting and maintaining a bond between two materials.
Aging	The change in properties of a material with time under specific conditions.
Arc resistance	The time required for an arc to establish a conductive path in a material.
B stage	An intermediate stage in the curing of a thermosetting resin. In this state, a resin can be heated and caused to flow, thereby allowing final curing in the desired shape. The term <i>A stage</i> is used to describe an earlier stage in the curing resin. Most molding materials are in the B stage when supplied for compression or transfer molding.
Blowing agent	Chemicals that can be added to plastics and that generate inert gases upon heating. This blowing or expansion causes the plastic to expand, thus forming a foam. Also known as <i>foaming agent</i> .
Bond strength	The amount of adhesion between bonded surfaces.
Capacitance	That property of a system of conductors and dielectrics that permits the storage of electricity when potential difference exists between the conductors. Its value is expressed as the ratio of the quantity of electricity to a potential difference. A capacitance value is always positive.
Cast	To embed a component or assembly in a liquid resin, using molds that separate from the part for reuse after the resin is cured. See <i>Embed, Pot</i> .

## 2.8 Chapter 2

TABLE 2.1 Definition of Terms for Plastic Materials (*Continued*)

Catalyst	A chemical that causes or speeds up the cure of a resin but that does not become a chemical part of the final product. Catalysts are normally added in small quantities. The peroxides used with polyester resins are typical catalysts.
Coat	To cover with a finishing, protecting, or enclosing layer of any compound (such as varnish).
Coefficient of expansion	The fractional change in the dimension of a material for a unit change in temperature.
Cold flow (creep)	The continuing dimensional change that follows initial instantaneous deformation in a nonrigid material under static load.
Compound	Some combination of elements in a stable molecular arrangement.
Contact bonding	A type of adhesive (particularly non vulcanizing natural rubber adhesives) that bonds to itself on contact although solvent evaporation has left it dry to the touch.
Cross-linking	The forming of chemical links between reactive atoms in the molecular chain of a plastic. It is this cross-linking in thermosetting resins that makes them infusible.
Crystalline melting point	The temperature at which the crystalline structure in a material is broken down.
Cure	To change the physical properties of a material (usually from a liquid to a solid) by chemical reaction, by the action of heat and catalysts, alone or in combination, with or without pressure.
Curing agent	See <i>Hardener</i> .
Curing temperature	The temperature at which a material is subjected to curing.
Curing time	In the molding of thermosetting plastics, the time it takes for the material to be properly cured.
Dielectric constant (permittivity or specific inductive capacity)	The property of a dielectric that determines the electrostatic energy stored per unit volume for unit potential gradient.
Dielectric loss	The time rate at which electric energy is transformed into heat in a dielectric when it is subjected to a changing electric field.
Dielectric loss angle (dielectric phase difference)	The difference between $90^\circ$ and the dielectric phase angle.
Dielectric loss factor (dielectric loss index)	The product of the dielectric constant and the tangent of the dielectric loss angle for a material.
Dielectric phase angle	The angular difference in phase between the sinusoidal alternating potential difference applied to a dielectric and the component of the resulting alternating current having the same period as the potential difference.
Dielectric power factor	The cosine of the dielectric phase angle (or sine of the dielectric loss angle).
Dielectric strength	The voltage that an insulating material can withstand before breakdown occurs, usually expressed as a voltage gradient (such as volts per mil).

TABLE 2.1 Definition of Terms for Plastic Materials (Continued)

Dissipation factor (loss tangent, $\tan \delta$ , approximate power factor)	The tangent of the loss angle of the insulating material.
Elastomer	A material that, at room temperature, stretches under low stress to at least twice its length and snaps back to its original length on the release of stress. See <i>Rubber</i> .
Electric strength (dielectric strength or disruptive gradient)	The maximum potential gradient that a material can withstand without rupture. The value obtained for the electric strength will depend on the thickness of the material and the method and conditions of test.
Embed	To completely encase a component or assembly in some material—a plastic for current purposes. See <i>Cast, Pot</i> .
Encapsulate	To coat a component or assembly in a conformal or thixotropic coating by dipping, brushing, or spraying.
Exotherm	The characteristic curve of a resin during its cure, which shows heat of reaction (temperature) vs. time. Peak exotherm is the maximum temperature on this curve.
Exothermic	A chemical reaction in which heat is given off.
Filler	A material, usually inert, that is added to plastics to reduce cost or modify physical properties.
Film adhesive	A thin layer of dried adhesive. Also describes a class of adhesives provided in dry-film form with or without reinforcing fabric, which are cured by heat and pressure.
Flexibilizer	A material that is added to rigid plastics to make them resilient or flexible. Flexibilizers can be either inert or a reactive part of the chemical reaction. Also called a <i>plasticizer</i> in some cases.
Flexural modulus	The ratio, within the elastic limit, of stress to corresponding strain.
Flexural strength	The strength of a material in bending, expressed as the tensile stress of the outermost fibers of a bent test sample at the instant of failure.
Fluorocarbon	An organic compound having fluorine atoms in its chemical structure. This property usually lends stability to plastics. Teflon <sup>®</sup> is a fluorocarbon.
Gel	The soft, rubbery mass that is formed as a thermosetting resin goes from a fluid to an infusible solid. This is an intermediate state in a curing reaction, and a stage in which the resin is mechanically very weak. <i>Gel point</i> is defined as the point at which gelation begins.
Glass transition point	The temperature at which a material loses its glass-like properties and becomes a semiliquid.
Hardener	A chemical added to a thermosetting resin for the purpose of causing curing or hardening. Amines and acid anhydrides are hardeners for epoxy resins. Such hardeners are a part of the chemical reaction and a part of the chemical composition of the cured resin. The terms <i>hardener</i> and <i>curing agent</i> are used interchangeably. Note that these can differ from catalysts, promoters, and accelerators.
Heat-distortion point	The temperature at which a standard test bar (ASTM D-648) deflects 0.010 in under a stated load of either 66 or 264 lb/in <sup>2</sup> .

TABLE 2.1 Definition of Terms for Plastic Materials (*Continued*)

Heat sealing	A method of joining plastic films by simultaneous application of heat and pressure to areas in contact. Heat may be supplied conductively or dielectrically.
Hot-melt adhesive	A thermoplastic adhesive compound, usually solid at room temperature, that is heated to a fluid state for application.
Hydrocarbon	An organic compound having hydrogen atoms in its chemical structure. Most organic compounds are hydrocarbons. Aliphatic hydrocarbons are straight-chained hydrocarbons, and aromatic hydrocarbons are ringed structures based on the benzene ring. Methyl alcohol and trichloroethylene are aliphatic; benzene, xylene, and toluene are aromatic.
Hydrolysis	The chemical decomposition of a substance involving the addition of water.
Hygroscopic	Tending to absorb moisture.
Impregnate	To force resin into every interstice of a part. Cloths are impregnated for laminating, and tightly wound coils are impregnated in liquid resin using air pressure or vacuum as the impregnating force.
Inhibitor	A chemical added to resin to slow down the curing reaction. Inhibitors are normally added to prolong the storage life of thermosetting resins.
Insulation resistance	The ratio of applied voltage to total current between two electrodes in contact with a specific insulator.
Modulus of elasticity	The ratio of stress to strain in a material that is elastically deformed.
Moisture resistance	The ability of a material to resist absorbing moisture, either from the air or when immersed in water.
Mold	To form a plastic part by compression transfer injection molding or some other pressure process.
NEMA standards	Property values adopted as standard by the National Electrical Manufacturers Association.
Organic	Composed of matter originating in plant or animal life, or composed of chemicals of hydrocarbon origin, either natural or synthetic. Used in referring to chemical structures based on the carbon atom.
Permittivity	Preferred unit of dielectric constant.
pH	A measure of the acid or alkaline condition of a solution. A pH of 7 is neutral (distilled water), pH values below 7 are increasingly acid as pH values go toward 0, and pH values above 7 are increasingly alkaline as pH values go toward the maximum value of 14.
Plastic	An organic resin or polymer.
Plasticizer	A material added to resins to make them softer and more flexible when cured.
Polymer	A high-molecular-weight compound (usually organic) made up of repeated small chemical units. Polymers can be thermosetting or thermoplastic.
Polymerize	To unite chemically two or more monomers or polymers of the same kind to form a molecule with higher molecular weight.
Pot	To embed a component or assembly in a liquid resin, using a shell, can, or case, which remains as an integral part of the product after the resin is cured. See <i>Embed, Cast</i> .



TABLE 2.1 Definition of Terms for Plastic Materials (Continued)

Pot life	The time during which a liquid resin remains workable as a liquid after catalysts, curing agents, promoters have been added; roughly equivalent to gel time. Sometimes also called <i>working life</i> .
Power factor	The cosine of the angle between the voltage applied and the resulting current.
Promoter	A chemical, itself a feeble catalyst, that greatly increases the activity of a given catalyst.
Resin	A high-molecular-weight organic material with no sharp melting point. For current purposes, the terms <i>resin</i> , <i>polymer</i> , and <i>plastic</i> can be used interchangeably.
Resistivity	The ability of a material to resist passage of electric current either through its bulk or on a surface. The unit of volume resistivity is the ohm-centimeter ( $\Omega$ -cm), and the unit of surface resistivity is the ohm.
Rockwell hardness number	A number derived from the net increase in depth of impression as the load on a penetrator is increased from a fixed minimum load to a higher load and then returned to minimum load. Penetrators include steel balls of several specified diameters and a diamond cone.
Rubber	An elastomer capable of rapid elastic recovery.
Shore hardness	A procedure for determining the indentation hardness of a material by means of a durometer. Shore designation is given to tests made with a specified durometer.
Solvent	A liquid substance that dissolves other substances.
Storage life	The period of time during which a liquid resin or adhesive can be stored and remain suitable for use. Also called <i>shelf life</i> .
Strain	The deformation resulting from a stress, measured by the ratio of the change to the total value of the dimension in which the change occurred.
Stress	The force producing or tending to produce deformation in a body, measured by the force applied per unit area.
Surface resistivity	The resistance of a material between two opposite sides of a unit square of its surface. Surface resistivity may vary widely with the conditions of measurement.
Thermal conductivity	The ability of material to conduct heat; the physical constant for the quantity of heat that passes through a unit cube of a material in a unit of time when the difference in temperature of two faces is 1°C.
Thermoplastic	A classification of resin that can be readily softened and resoftened by repeated heating. Hardening is achieved by cooling.
Thermosetting	A classification of resin that cures by chemical reaction when heated and, when cured, cannot be resoftened by heating.
Thixotropic	Describing materials that are gel-like at rest but fluid when agitated.
Vicat softening temperature	A temperature at which a specified needle point will penetrate a material under specified test conditions.
Viscosity	A measure of the resistance of a fluid to flow (usually through a specific orifice).
Volume resistivity (specific insulation resistance)	The electrical resistance between opposite faces of a 1-cm cube of insulating material, commonly expressed in ohm-centimeters ( $\Omega$ -cm). The recommended test is ASTM D-257-54T.

## 2.12 Chapter 2

TABLE 2.1 Definition of Terms for Plastic Materials (Continued)

Vulcanization	A chemical reaction in which the physical properties of an elastomer are changed by causing it to react with sulfur or other cross-linking agents.
Water absorption	The ratio of the weight of water absorbed by a material to the weight of the dry material.
Wetting	The ability to adhere to a surface immediately on contact.
Working life	The period of time during which a liquid resin or adhesive, after mixing with a catalyst, solvent, or other compounding ingredients, remains usable. See <i>Pot life</i> .

TABLE 2.2 Significance of Important Electrical Insulation Properties

Property and definition	Significance of values
Dielectric strength	
All insulating materials fail at some level of applied voltage for a given set of operating conditions. The dielectric strength is the voltage that an insulating material can withstand before dielectric breakdown occurs. Dielectric strength is normally expressed in volt-age gradient terms, such as volts per mil. In testing for dielectric strength, two methods of applying the voltage (gradual or by steps) are used. Type of voltage, temperature, and any preconditioning of the test part must be noted. Also, the thickness of the piece tested must be recorded because the voltage per mil at which breakdown occurs varies with the thickness of the test piece. Normally, breakdown occurs at a much higher volt-per-mil value in very thin test pieces (a few mils thick) than in thicker sections (1/8 in thick, for example).	The higher the value, the better the insulator. The dielectric strength of a material (per mil of thickness) usually increases considerably with a decrease in insulation thickness. Materials suppliers can provide curves of dielectric strength versus thickness for their insulating materials.
Resistance and resistivity	
Resistance of insulating material, like that of a conductor, is the resistance offered by the conducting path to passage of electric current. Resistance is expressed in ohms. Insulating materials are very poor conductors, offering high resistance. For insulating materials, the term volume resistivity is more commonly applied. Volume resistivity is the electrical resistance between opposite faces of a unit cube for a given material and at a given temperature. The relationship between resistance and resistivity is expressed by the equation $p = RA/l$ , where $p$ = volume resistivity in ohm-centimeters, $A$ = area of the faces, and $l$ = distance between faces of the piece on which measurement is made. This is not resistance per unit volume, which would be ohms per cubic centimeter, although this term is sometimes used erroneously. Other terms are sometimes used to describe a specific application or condition. One such term is surface resistivity, which is the resistance between two opposite edges of a surface film 1 cm square. Since the length and width of the path are the same, the centimeter terms cancel. Thus units of surface resistivity are actually ohms. However, to avoid confusion with usual resistance values, surface resistivity is normally given in ohms per square. Another broadly used term is insulation resistance, which again is a measurement of ohmic resistance for a given condition, rather than a standardized resistivity test. For both surface resistivity and insulation resistance, standardized comparative tests are normally used. Such tests can provide data such as effects of humidity on a given insulating material configuration.	The higher the value, the better; that is, a good insulating material. The resistance value for a given material depends on a number of factors. It varies inversely with temperature, and is affected by humidity, moisture content of the test part, level of the applied voltage, and time during which the voltage is applied. When tests are made on a piece that has been subjected to moist or humid conditions, it is important that measurements be made at controlled time intervals during or after the test condition has been applied, since dry-out and resistance increase occur rapidly. Comparing or interpreting data is difficult unless the test period is controlled and defined.

TABLE 2.2 Significance of Important Electrical Insulation Properties (*Continued*)

Property and definition	Significance of values
Dielectric constant	
<p>The dielectric constant of an insulating material is the ratio of the capacitance of a capacitor containing that particular material to the capacitance of the same electrode system with air replacing the insulation as the dielectric medium. The dielectric constant is also sometimes defined as the property of an insulation which determines the electrostatic energy stored within the solid material. The dielectric constant of most commercial insulating materials varies from about 2 to 10, air having the value 1.</p>	<p>Low values are best for high-frequency or power applications, to minimize electric power losses. Higher values are best for capacitance applications. For most insulating materials, the dielectric constant increases with temperature, especially above a critical temperature region, which is unique for each material. Dielectric constant values are also affected (usually to a lesser degree) by frequency. This variation is also unique for each material.</p>
Power factor and dissipation factor	
<p>Power factor is the ratio of the power (watts) dissipated in an insulating material to the product of the effective voltage and current (volt-ampere) input and is a measure of the relative dielectric loss in the insulation when the system acts as a capacitor. The power factor is nondimensional and is a commonly used measure of insulation quality. It is of particular interest at high levels of frequency and power in such applications as microwave equipment, transformers, and other inductive devices. Low values are favorable, indicating a more efficient system, with lower losses.</p> <p>Dissipation factor is the tangent of the dielectric loss angle. Hence the term <math>\tan \delta</math> (tangent of the angle) is also sometimes used. For the low values ordinarily encountered in insulation, dissipation factor is practically the equivalent of power factor, and the terms are used interchangeably.</p>	<p>Low values are favorable, indicating a more efficient system, with lower losses.</p>
Arc resistance	
<p>Arc resistance is a measure of an electrical breakdown condition along an insulating surface, caused by the formation of a conductive path on the surface. It is a common ASTM measurement, especially used with plastic materials because of the variations among plastics in the extent to which a surface breakdown occurs. Arc resistance is measured as the time, in seconds, required for breakdown along the surface of the material being measured. Surface breakdown (arcing or electrical tracking along the surface) is also affected by surface cleanliness and dryness.</p>	<p>The higher the value, the better. Higher values indicate greater resistance to breakdown along the surface due to arcing or tracking conditions.</p>
Comparative tracking index	
<p>This is an Underwriters Laboratories test which is run similar to arc resistance except that an electrolyte solution (ammonium chloride) is put on the surface. The CTI is the value of the voltage required to cause a conductive path to form between electrodes.</p>	<p>The test is useful because it measures the arc resistance on a contaminated surface, which is often the case with actual electrical and electronics equipment.</p>

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### 2.3 Thermoplastics

Thermoplastic materials are polymers that can be repeatedly softened when heated and hardened when cooled. Because the high temperatures required for melting may cause degradation, there is a limit to the number of reheat cycles for some thermoplastics. Thermoplastics are fabricated into parts by blow molding, extrusion, foaming, injection and rotational molding, stamping, and vacuum forming. Detailed descriptions of all thermoplastics can be found elsewhere.<sup>5-7</sup> Tables 2.3 to 2.6 contain basic property and application information on thermoplastics used in electrical and electronic applications. Supplier information is given in Kaplan,<sup>5</sup> and a brief description of these materials follows.

**TABLE 2.3 General Characteristics of Thermoplastics**

Material	Characteristic properties	Processing*	Electrical/electronic applications
Acrylics	Crystal clarity, good surface hardness, weatherability, chemical and environmental resistance, mechanical stability	1, 2, 3, 4, 5, 6	Colored electronic display filters, conformal coatings
Fluoroplastics	Heat resistance, superior chemical resistance, low dielectric losses, zero water absorption, low friction coefficient	9, 10, 11, 12, 13 Some fluoroplastics can be molded by more conventional methods (2, 7)	Wire and cable insulation, electrical components
Ketone plastics	Heat resistance, chemical resistance, high strength, resistance to burning, thermal and oxidative stability, excellent electrical properties, low smoke emission	1, 2, 8, 13	Wire insulation, cable connectors
Liquid crystal polymers	High-temperature resistance, chemical resistance, high mechanical strength, low thermal expansion	1	Chip carriers, sockets, connectors, relay cases
Nylon	Mechanical strength, tough, abrasion and wear resistance, low friction coefficient	1, 2, 3, 4, 6, 8	Connectors, wire jackets, wire ties, coil bobbins
Polyamide-imide	High-temperature resistance, superior mechanical properties at elevated temperature, dimensional stability, creep and chemical resistance, radiation resistance	1, 2, 7, 9	Connectors, circuit boards, radomes, films, wire coating
Polyarylate	Ultraviolet stability, dimensional stability, heat resistance, stable electrical properties, flame-retardant, flame-retardant, high arc resistance	1, 2, 3, 4	Connectors, coil bobbins, switch and fuse covers, relay housings
Polycarbonate	Clarity, toughness, heat resistance, flame-retardant	1, 2, 3, 4	Connectors, terminal boards, bobbins
Polyesters (PBT, PCT, PET)	Good electrical properties, chemical resistance, high-temperature resistance, low moisture absorption	1, 2	Connectors, sockets, chip carriers, switches, coil bobbins, relays

TABLE 2.3 General Characteristics of Thermoplastics (Continued)

Material	Characteristic properties	Processing*	Electrical/electronic applications
Polyetherimide	Good high-temperature strength, dimensional stability, chemical resistance, long-term heat resistance, low smoke generation	1, 2, 3, 7	Connectors, low-loss radomes, printed circuit boards, chip carriers, sockets, bobbins, switches
Polyolefins	Range of strength and toughness, chemical resistance, low friction coefficient, processability, excellent electrical properties	1, 2, 3, 4, 7, 8	Wire and cable insulation
Polyimides	Superior high-temperature properties, radiation resistance, flame resistance, good electrical properties	1, 6, 7	Insulation for electric motors, magnet wire, flat cable, integrated-circuit applications
Polyphenylene oxide	Low moisture absorption, good electrical properties, chemical resistance	1, 2, 3, 4	Connectors, fuse blocks
Polyphenylene sulfide	Flame resistance, high-temperature resistance, dimensional stability, chemical resistance, good electrical properties	1	Connectors
Polyphthalamide	Good combination of mechanical, chemical, and electrical properties	1	Connectors, switches
Styrenes	Range of mechanical, chemical, electrical properties depending on type of styrene polymer, low dielectric losses	1, 2, 3, 4, 8	Housings
Polysulfones	High-temperature resistance, excellent electrical properties, radiation resistance	1, 2	Circuit boards, connectors, TV components
Vinyls	Range of properties depending on type	1, 2, 3, 4	Wire insulation, tubing, sleeving

* 1 Injection molding	6 Casting	11 Dispersion coating
2 Extrusion	7 Compression molding	12 Compression molding
3 Thermoforming	8 Rotational molding	13 Electrostatic coating
4 Blow molding	9 Powder metallurgy	
5 Machining	10 Sintering	

SOURCE: From Harper<sup>4</sup> and Kaplan.<sup>5</sup> Reprinted with permission.

TABLE 2.4 Typical Physical Properties of Thermoplastics

Resin material	Coefficient of thermal expansion, $10^{-5}$ in/in/°C	Thermal conductivity $10^{-4}$ cal-cm/sec-cm <sup>2</sup> °C	Water absorption 24 h, %	Flammability,* in/min	Specific gravity
ABS	6–13	4–9	0.2–0.5	1.0–2	1.01–1.07
Acrylic	–9	1.4	0.3	9–1.2	1.18–1.19

TABLE 2.4 Typical Physical Properties of Thermoplastics (Continued)

Resin material	Coefficient of thermal expansion, $10^{-5}$ in/in/°C	Thermal conductivity $10^{-4}$ cal-cm/sec-cm <sup>2</sup> °C	Water absorption 24 h, %	Flammability,* in/min	Specific gravity
Chlorotrifluoroethylene	3.6	4–6	Nil	Nil	2.8–2.2
Fluorinated ethylene propylene	8.3–10.5	5.9	<0.05	Nonflammable	2.16
Polytetrafluoroethylene	2–12	6	<0.01	Nonflammable	2.14–2.28
Nylon 6	1.1–8.0	5.9	1.5	Self-extinguishing	1.07–1.15
Polycarbonate	6.7–7	4.6	0.15	Self-extinguishing	1.2
Polyethylene, low density	10–20	8	<0.01	Slow burning	0.910–0.925
Polyethylene, medium density	10–20	8	<0.01	Slow burning	0.926–0.940
Polyphthalamide	0.8–3.3	1.7–2.6	0.1–0.8	Self-extinguishing	1.13–1.70
Polyamide-imide	3.0	6.2	0.33	Self-extinguishing	1.42
Polyarylate	2.7–4.0	—	0.1–0.2	Self-extinguishing	1.19–1.22
Polybutylene terephthalate	6.0–9.5	4.2–6.9	0.08	—	1.30–1.38
Polyethylene terephthalate	6.5	3.4	0.1–0.2	—	1.29–1.40
Polyethylene, high density	5–11	11–12	<0.01	Slow burning	0.941–0.965
Polyethylene, high molecular weight	7–11	8	<0.01	Slow burning	0.93–0.94
Polyethylene, UHMW	13–20	—	<0.01	Slow burning	0.94
Polyimide	4.5–5.6	2.3–2.6	0.24	—	
Polypropylene	3.8–9	2.8–4	<0.01	Slow burning to non burning	0.90–1.4
Polystyrene	5–8	3	0.01–0.03	0.5–2.5	1.04–1.05
Polyurethane	10–20	7.4	0.60–0.80	Slow to self-extinguishing	1.11–1.26
Polyvinyl chloride (flexible)	7–25	3–5	0.15–0.75	Self-extinguishing	1.15–1.80
Polyvinyl chloride, rigid	5–10	3–5	0.07–0.40	Self-extinguishing	1.33–1.58
Polyvinyl dichloride, rigid	7–8	3–4	0.07–0.11	Self-extinguishing	1.50–1.54
Styrene acrylonitrile (SAN)	7	3	0.15–0.25	0.4–0.25	1.07–1.08
Polyphenylene oxide	3.8–7.0	3.8	0.06–0.1	Self-extinguishing	1.04
Polysulfone	5.6	6.2	0.3	Self-extinguishing	1.24–1.25

TABLE 2.4 Typical Physical Properties of Thermoplastics (Continued)

Resin material	Coefficient of thermal expansion, $10^{-5}$ in/in/°C	Thermal conductivity $10^{-4}$ cal-cm/sec-cm <sup>2</sup> °C	Water absorption 24 h, %	Flammability,* in/min	Specific gravity
Polyarylsulfone	3.1–4.9	—	0.1	Self-extinguishing	1.37 <sup>c</sup>
Polyethersulfone	5.5	3.2–4.4	0.12–1.7	Self-extinguishing	1.37
Polyetheretherketone	4.0–4.7	—	0.1	Self-extinguishing	1.31
Polyetherketone	1.8	10.5	0.05	Self-extinguishing	1.30
Polycyclohexylene dimethyl terephthalate (PCT), 30% glass reinforced	2.0	6.9	0.05		
Polyetherimide	4.7–5.6	1.6	0.25	Self-extinguishing	1.27
Polyphenylene sulfide	2.7–4.9	2.0–6.9	0.05	Self-extinguishing	1.35

\*Samples 0.125 in thick.

SOURCE: From Harper<sup>4</sup> and Kaplan.<sup>5</sup> Reprinted with permission.

### 2.3.1 Acrylics

Acrylic resins comprise a range of polymers and copolymers that are derived from acrylic acid-esters and their derivatives. These polymers are made by free-radical polymerization, and modifications are effected by the incorporation of other monomers during polymerization or by blending other resins such as vinyls, butadiene, polyester, or other acrylics so as to alter specific properties of the resin. Acrylics are characterized by their exceptional transparency (92 percent light transmission), with haze measurements ranging from 1 to 3 percent. They exhibit good weatherability and are resistant to solutions of inorganic acids, alkalies, and aliphatic hydrocarbons. Acrylics are attacked by chlorinated, aromatic, ester, and ketone solvents. The maximum service temperature is about 90°C, but it can go as high as 155°C with the new acrylic-imide copolymers. The excellent arc and track resistance of the acrylics has made them a good choice in some high-voltage applications such as circuit breakers. Acrylics are among the few plastics that exhibit an essentially linear decrease in dielectric constant and dissipation factor with increasing frequency. The acrylics are produced in many forms, including film, rod, sheet, tube, powder, solutions, and reactive syrups. Acrylics can also be formed into thermosetting resins, which are discussed in the section dealing with thermosetting resins. Resin suppliers include DuPont, Dow Chemical, Exxon, GE, ICI Acrylics, Asahi, and BASF.

### 2.3.2 Fluoropolymers

These materials are a class of hydrocarbon polymers that has some or all of its hydrogens replaced by fluorine or chlorine. They are polytetrafluoroethylene

TABLE 2.5 Typical Physical and Mechanical Properties of Thermoplastics

Resin material	Impact strength, notched (Izod), ft- lb/in, 1/8-in bar	Tensile strength 10 <sup>2</sup> lb/in <sup>2</sup>	Tensile modulus 10 <sup>2</sup> lb/in <sup>2</sup>	Elongation, %	Flexural strength 10 <sup>2</sup> lb/in <sup>2</sup>	Compressive strength 10 <sup>2</sup> lb/in <sup>2</sup>	Compressive modulus 10 <sup>2</sup> lb/in <sup>2</sup>	Heat distortion temperature, at 264 lb/in <sup>2</sup> °F	Heat resistance, continuous, °F
ABS	1.5–12	2.5–5.8	120–420	20–100	5–13.5	5–11	120–200	180–245	160–235
Acrylic	0.3–0.4	8.7–11.0	350–450	3–6	2–7	11–19	350–430	167–198	130–195
Chlorotrifluoroethylene	2.5–5.0	6	150–300	80–250	7.4–11	4.6–7.4	180	160–170	390
Fluorinated ethylene propylene	No break	2–3.2	50	250–350	—	2.2	70	124	400
Polytetrafluoroethylene	No break	2–5	50–80	200–400	—	1.7	70–90	132	500
Nylon 6		0.9–4	9.5–12.4	100–380	25–300	5.8–15.7	13–16	347	150–175
Polycarbonate	12–16	8–9.5	345	110–120	13.5	10–12.5	350	265–290	250
Polyethylene, low density	No break	1–2.4	14–38	100–965	—	—	—	—	140–175
Polyethylene, medium density	No break	1.7–2.8	50–80	100–965	—	—	—	—	150–180
Polyethylene, high density	0.4–4.0	2.8–5	75–200	10–1200	1–4	2.7–3.6	50–110	110–125	180–225
Polyethylene, high molecular weight	4.5	2.3–5.4	136	170–800	3.5	2.4	110	120	180–225
Polyimide	1.5	5–14.0	300	8–10	19–28.8	30–40	—	680	500–600
Polyethylene	0.5–1.5	4.5–6.0	150–650	100–600	6.0	5–8	—	140–205	250
Polystyrene	0.40	5.2–7.5	400–500	1.5–2.5	10–15	11.5–16	300–560	160–215	150–190
Polyurethane	No break	4.5–8	1–3.7	60–120	0.1	>20	85	—	190
Polyvinyl chloride, flexible	Varied	1–4	—	200–450	—	—	—	—	150–175
Polyvinyl chloride, rigid	0.4–22	7.5	200–600	40–80	10–15	10–11	300–400	140–175	160–165



TABLE 2.5 Typical Physical and Mechanical Properties of Thermoplastics (Continued)

Resin material	Impact strength, notched (Izod), ft- lb/in, 1/8-in bar	Tensile strength 10 <sup>2</sup> lb/in <sup>2</sup>	Tensile modulus 10 <sup>2</sup> lb/in <sup>2</sup>	Elongation, %	Flexural strength 10 <sup>2</sup> lb/in <sup>2</sup>	Compressive strength 10 <sup>2</sup> lb/in <sup>2</sup>	Compressive modulus 10 <sup>2</sup> lb/in <sup>2</sup>	Heat distortion temperature, at 264 lb/in <sup>2</sup> °F	Heat resistance, continuous, °F
Polyvinyl dichloride, rigid	1.0–6.0	7.5–9.0	360–450	160–240	14.2–17	13–22	—	212–235	195–235
Styrene acrylonitrile (SAN)	0.4–0.6	10	475–560	2–3	11–19	15–17.5	650	200–218	170–210
Polyphenylene oxide	3–6	6.8–7.8	380	50	8.3–12.8	15	380	375	250
Polysulfone	0.6–1.0	10.2	360	50–100	15.4	15.4	370	345	300
Polyphthalamide	1.0	>1.5	—	—	23.3	—	—	248	300
Polamide-imide	2.7	22	650	7	27.4–34.9	32	—	532	430
Polybutylene terephthalate	0.7–1.0	8.2	280–430	50–300	12–16.7	8.6–14.5	—	122–185	270
Polyethylene terephthalate	0.25–0.7	7–10	400–600	30–300	14–18	11–15	—	70–100	—
Polyethylene, UHMW	No break	5.6–7.0	—	420–525	—	—	—	110–120	—
Polyarylsulfone	1.2	9.0	310–380	40–60	12.4–16.1	—	374	400	—
Polyethersulfone	1.4	9.8–13.8	350	6–80	17–18.7	11.8–15.6	—	395	350
Polyetherketone	1.6	13.5	520	50	24.5	20	—	323	—
Polyetheretherketone	2.0	10–15	—	30–150	16	18	—	—	—
Polyetherimide	1.1	14	430	60	22	20	420	390	330–350
Polyphenylene sulfide	<0.5	7–12	480	1–3	14–20	16	—	250	350–400
Polycyclohexylene di-methyl terephthalate (PCT), 30% glass reinforced	1.7	18–19	—	1.9	24–28	—	—	500	300

SOURCE: From Harper<sup>4</sup> and Kaplan.<sup>5</sup> Reprinted with permission.

TABLE 2.6 Typical Electrical Properties of Thermoplastics

Resin material	Volume resistivity $\Omega\text{-cm}$	Dielectric constant at 60 Hz	Dielectric strength, ST, 1/8-in thickness, V/mil	Dissipation or power factor at 60 Hz	Arc resistance, s
ABS	$10^{15}\text{--}10^{17}$	2.6–3.5	300–450	0.003–0.007	45–90
Acrylic	$>10^{14}$	3.3–3.9	400	0.04–0.05	No tracking
Chlorotrifluoroethylene	$10^{18}$	2.65	450	0.015	$>360$
Fluorinated ethylene propylene	$>10^{18}$	2.1	500	0.0002	$>165$
Polytetrafluoroethylene	$>10^{18}$	2.1	400	$<0.0001$	No tracking
Nylon 6	$10^{14}\text{--}10^{15}$	6.1	300–400	0.4–0.6	140
Polycarbonate	$6.1 \times 10^{15}$	2.97	410	0.0001–0.0005	10–120
Polyethylene, low density	$10^{15}\text{--}10^{18}$	2.98	450–1,000	0.006	Melts
Polyethylene, medium density	$10^{15}\text{--}10^{18}$	2.3	450–1,000	0.0001–0.0005	Melts
Polyethylene, high density	$6 \times 10^{15}\text{--}10^{18}$	2.3	450–1,000	0.002–0.0003	Melts
Polyethylene, high molecular weight	$>10^{16}$	2.3–2.6	500–710	0.0003	Melts
Polyimide	$10^{16}\text{--}10^{17}$	3.5	400	0.002–0.003	230
Polypropylene	$10^{15}\text{--}10^{17}$	2.1–2.7	450–650	0.005–0.0007	36–136
Polystyrene	$10^{17}\text{--}10^{21}$	2.5–2.65	500–700	0.0001–0.0005	60–100
Polyurethane	$2 \times 10^{11}$	6–8	850–1,100	0.276	—
Polyvinyl chloride, flexible	$10^{11}\text{--}10^{15}$	5–9	300–1,000	0.08–0.15	60–80
Polyvinyl chloride, rigid	$10^{12}\text{--}10^{16}$	3.4	425–1,040	0.01–0.02	—
Polyvinyl dichloride, rigid	$10^{15}$	3.08	1,200–1,550	0.018–0.0208	—
Styrene acrylonitrile (SAN)	$10^{15}$	2.8–3	400–500	0.006–0.008	100–500
Polyphenylene oxide	$10^{17}$	2.58	400–500	0.00035	75
Polysulfone	$5 \times 10^{16}$	2.82	425	0.008–0.0056	122
Polyarylate	$2 \times 10^{14}$	3.08	610	0.002	125
Polybutylene terephthalate (PBT)	$1.4 \times 10^{15}$	3.3	420	0.002	190
Polybutylene terephthalate (PBT)	$2 \times 10^{15}$	3.2	470–530	0.0018	68–136

TABLE 2.6 Typical Electrical Properties of Thermoplastics

Resin material	Volume resistivity $\Omega\text{-cm}$	Dielectric constant at 60 Hz	Dielectric strength, ST, 1/8-in thickness, V/mil	Dissipation or power factor at 60 Hz	Arc resistance, s
Polyethylene terephthalate (PET)	$1 \times 10^{15}$	3.8	650	0.0059	123
Polyphenylene sulfide, 40% glass	$10^{16}$	3.5–3.8	340–450	0.0012	34
Polyetherimide	$6.7\text{--}10^{17}$	3.15	750–831	0.0013	126
Polyetherketone	$10^{17}$	3.5	—	0.002	—

SOURCE: From Harper<sup>4</sup> and Kaplan.<sup>5</sup> Reprinted with permission.

(PTFE), fluorinated ethylene-propylene (FEP), perfluoroalkoxy (PFA), ethylene-tetrafluoroethylene (ETFE), polyvinylidene fluoride (PVDF), polychlorotrifluoroethylene (PCTFE), ethylene-chlorotrifluoroethylene (ECTFE), and polyvinyl fluoride (PVF). The fluoropolymers and copolymers are synthesized by free-radical polymerization techniques. The polymers are characterized by their unique combination of chemical, electrical, mechanical, and thermal properties. They do not support flame propagation, are unaffected by most chemicals, and have excellent arc resistance, low dielectric losses, and essentially zero water absorption. Their limitation is that these polymers are relatively soft, difficult to process, expensive, and subject to creep. Service temperatures for these materials range from 110 to 260°C, depending on the type of polymer. Some specific properties of these materials are given in Table 2.7. Fluoropolymers are used in electronic circuits as coatings, films, tubing, fibers, and tapes. Suppliers include Elf Atochem, DuPont, Dyneon, Creanova, Solvay, and Ausimont.

### 2.3.3 Ketone resins

These materials are partially crystalline polymers and are characterized by the presence of the phenyl ring and both ether (–O–) and ketone ( $R_2\text{C}=\text{O}$ ) groups in the polymer chain. There are several types of ketone polymers that are synthesized by condensation polymerization. The major ketone polymers are polyetherketone (PEK), polyetheretherketone (PEEK), and polyetherketoneetherketoneketone (PEKEKK). These polymers are characterized by their excellent elevated-temperature properties, with continuous service temperatures approaching 260°C. The polymers are tough and have high impact strength as well as good dielectric strength, volume, and surface resistivity. Only concentrated, anhydrous, or strong oxidizing acids have an effect on these polymers. Common organic solvents do not attack these polymers, and they are highly resistant to hot-water hydrolysis. Their main use is for wire and cable insulation and connectors. Suppliers include Solvay, Shell, and Victrex.

TABLE 2.7 Properties of Fluoropolymers

	PTFE	FEP	PFA	ETFE	PVDF	PCTFE	ECTFE	PVF
Percent fluorine	76.0	76.0	76.0	59.4	59.4	48.9	39.4	41.3
Melting point, °C	327	265	310	270	160	218	245	200
Upper use temperature, °C	260	200	260	180	150	204	170	110
Density, g/cm <sup>3</sup>	2.13	2.15	2.12	1.7	1.78	2.13	1.68	1.38
Oxygen index, %	>95	95	95	28–32	44	—	48–64	—
Arc resistance, seconds	>240	>300	≥300	72	60	2.4	18	—
Dielectric constant	2.1	2.1	2.1	2.6	9–10	2.5	2.5	9
Dissipation factor	0.0002	0.0002	0.0002	0.0008	0.02–0.02	0.02	0.003	0.002
Tensile strength, lb/in <sup>2</sup>	5000	3100	4300	7000	6200	6000	—	—
Specific gravity	2.2	2.17	2.17	1.7	1.78	2.2	1.68	—
Water absorption, % 24 h	0	0	0.03	0.03	0.06	0	—	—
Electrical strength, V/mil	480	600	500	400	280	600	—	—

SOURCE: From Harper.<sup>8</sup> Reprinted with permission.

### 2.3.4 Liquid crystal polymers

These polymers belong to a material class that exhibits a highly ordered structure in both melt and solid states. Because of the high degree of molecular ordering, liquid crystal polymers (LCPs) exhibit a high degree of anisotropy. If the liquid crystalline phase forms on melting the polymer, it is known as a *thermotropic* liquid crystal, and if it forms in solution as the result of solvent addition, it is known as *lyotropic*. Condensation polymerization has been used to prepare these polymers. A number of polymers exhibit liquid crystalline behavior, but the three commercially important polymers are Xydar (Solvay Advanced Polymers, LLC), Vectra (Ticona Corp.), and the Zenite series (E.I. DuPont de Nemours & Co). There is no one chemical structure that characterizes LCPs; however, all LCPs have these common characteristics: the molecular shape has a large aspect ratio (length or diameter to width or thickness), the molecule has a large polarizability along the rigid chain axis as compared to the transverse direction, and the molecule must have good molecular parallelism of the rigid units comprising its structure.<sup>8</sup> To meet these requirements, an LCP should possess a rigid molecular structure, as do all three of these materials.

The major properties that characterize LCPs are low melt viscosity; exceptional tensile, compressive, and modulus values; and outstanding chemical, radiation, and thermal stability. A general comparison of flexural moduli and mold shrinkage for LCPs and other polymers is given in Figs. 2.4 and 2.5, and

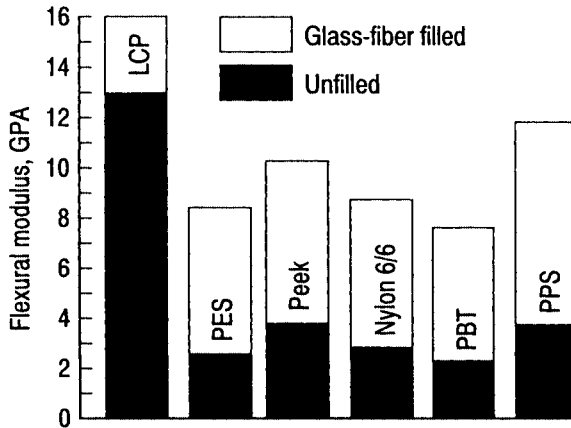


Figure 2.4 Comparison of flexural moduli of selected thermoplastics. (From Klein,<sup>10</sup> reprinted with permission.)

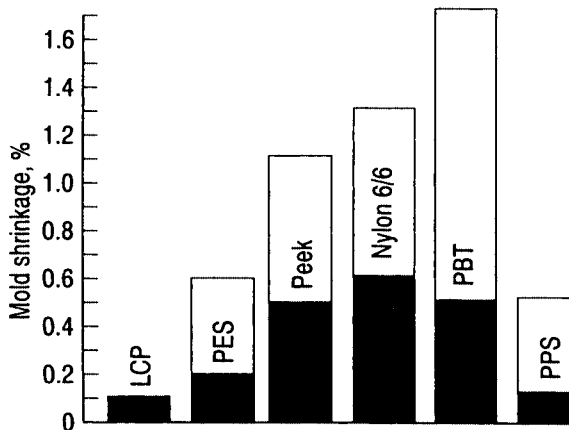


Figure 2.5 Comparison of mold shrinkage of selected thermoplastics. (From Klein,<sup>10</sup> reprinted with permission.)

Table 2.8 presents a comparison of specific properties of filled LCPs. The main uses for these polymers in the electronics industry are for the molding of high-precision complex parts, chip carriers, sockets, connectors, pin-grid arrays, bobbins, and relay cases.

### 2.3.5 Nylons

These materials, also known as polyamides, are characterized by having the amide group ( $-\text{CONH}-$ ) as an integral part of the polymer structure. While this chemical unit is present in all nylons, the multiplicity of monomers that can be used to prepare nylons has led to a wide variety of materials with different properties. Presently, there are 12 types of nylons available;<sup>11</sup> 10 are aliphatic, and 2 are aromatic. Nylons are synthesized by both condensation

**TABLE 2.8 Typical Properties of LCP Molding Compounds**

Grade	*Vectra A130	*Vectra B230	*Vectra A430	†Xydar G930	†Xydar MG350	‡Zenite 3130	‡Zenite 6140
Fillers	30% glass fiber	30% carbon fiber	50% glass/mineral, 5% graphite flake	30% glass fiber	50% mineral/glass	30% glass fiber	40% glass fiber
Tensile strength, 10 <sup>3</sup> lb/in <sup>2</sup>	27.7	29.1	23.3	19.6	13.1	20.3	19.2
@ temperature	1.9 @ 400°F	—	1.5 @ 400°F	2.8 @ 500°F	2.3 @ 500°F	—	—
Elongation, %	2.1	6.2	0.7	1.6	0.9	1.8	1.4
Flex modulus, 10 <sup>6</sup> lb/in <sup>2</sup>	2.2	3.7	1.0	2.26	2.33	1.7	2.2
@ temperature	0.85 @ 428°F	0.41 @ 428°F	—	0.46 @ 500°F	0.29 @ 500°F	—	—
Impact strength, notched, ft-lb/in	2.8	1.4	1.9	1.8	0.9	—	1.6
Coeff. thermal expansion, ppm/°F							
Flow direction	0.6	1.1	0.6	2.7	4	—	—
Transverse	26	2.1	45	43	33	—	—
Dielectric strength, V/mil	790¶	—	—	1,000§	970	—	—
Heat deflection temperature @ 264 lb/in <sup>2</sup> , °F	446	440	437	520	532	441	522
Dielectric constant @ 1 MHz	3.7	3.2	2.7	3.9	3.9	—	—
Dissipation factor @ 1 MHz	0.018	—	0.016	—	0.029	—	—
Resistivity, Ω-cm	10 <sup>15</sup>	10	10 <sup>15</sup>	—	—	—	—

\*Ticona

†Solvay Advanced Polymers

‡DuPont

¶At 1.50-mm thickness

§At 1.6-mm thickness

SOURCE: Supplier web sites

polymerization (types 6/6, 6/9, 6/10, 6/12) and addition polymerization (types 6, 11, 12). Most nylons are partially crystalline polymers. The nylons can be modified by the addition of additives or copolymerized with other monomers to produce a wide range of materials with different properties. In addition, some blending of nylon polymers can be done with acrylonitrile-butadiene-styrene and polyphenylene ether polymers. Transparent nylon is available, and, unlike the other grades of nylon polymers, it is amorphous. The nylons are strong, tough thermoplastics having good tensile, flexural, friction, and impact properties. Nylons can operate satisfactorily over the temperature range of 0 to 149°C. All nylons are hygroscopic, although the degree of water absorption decreases with increasing hydrocarbon chain length. This moisture absorption affects some physical properties. For example, it has a plasticizing effect on the polymer and increases flexural and impact strength while decreasing tensile strength. The electrical properties of nylons are quite sensitive to moisture and deteriorate with increasing water content. Nevertheless, these properties are quite adequate to allow the use of nylons in most 60-Hz power applications. Nylons have good chemical resistance to hydrocarbons and aromatic and aliphatic solvents and are attacked by strong acids, bases, and phenols. Elevated temperature and ultraviolet radiation exposure will degrade nylon depending on the duration and level of the exposure. The nylons can be processed by almost all of the common thermoplastic fabrication techniques. The reader is directed to the references for additional information and specific properties.<sup>4,6,10</sup> Applications for nylons include card guides, connectors, terminal blocks, antenna mounts, coil bobbins, and receptacle plugs. Resin suppliers include Honeywell, Quadrant, DuPont, Elf Atochem, and Bayer.

**2.3.5.1 High-temperature nylon.** In addition to the aforementioned nylons, there is another class of polyamides that is based on the presence of an aromatic ring in the chemical structure. Two materials compose this class: Nomex [(poly)1,3-phenylene isophthalamide] and Kevlar [(poly)1,4-phenylene terephthalamide] (both registered trademarks of E.I. duPont de Nemours & Co.).

Kevlar is spun into fiber and is mostly used in composite applications, while Nomex is processed into fiber, paper, sheet, and pressboard and is used extensively in the electrical industry as insulation for transformer coils and motor stators. Nomex is recognized by Underwriters Laboratories as a 220°C material. Table 2.9 gives some electrical properties of Nomex.

### 2.3.6 Polyamide-imides

These polymers are amorphous materials produced by the condensation polymerization of trimellitic anhydride and aromatic diamines. The characteristic chemical groups in the polymer chain are the amide linkage (–CONH–) and the imide linkage (–CONCO–). These polymers can be solution cast into film or converted into powders for further processing into various forms. The poly-

TABLE 2.9 Electrical Properties of Nomex\*

Nomex	Thickness, mil	Dielectric, strength, V/mil, ASTM D-149	Dielectric constant, at 60 Hz, ASTM D-150	Dissipation factor at 60 Hz, ASTM D-150	Volume resistivity, $\Omega$ -cm, ASTM D-257
410	3	540	1.6	0.005	$10^{16}$
411	5	230	1.2	0.003	—
414	3.4	530	1.7	0.005	$10^{16}$
418	3	730	2.9	0.006	$10^{16}$
419	7	325	2.0	—	—
992	125	380	1.7	0.020	$10^{17}$
993	120	540	2.6	0.015	$10^{17}$
994	250		3.5	0.010	$10^{16}$

\*Unless otherwise noted, the Nomex properties are typical values measured by air under “standard” conditions (in equilibrium at 23°C, 50% relative humidity) and should not be used as specification limits. The dissipation factors of types 418, 419, 992, and 993 and all of the volume resistivities are measured under dry conditions. Nomex is a registered trademark of E.I. duPont de Nemours & Co. for its aramid products.

SOURCE: From duPont Co.<sup>12</sup> Reprinted with permission.

mers possess outstanding high-temperature (260°C) and radiation stability (109 rads) as well as excellent mechanical properties, low dielectric losses, and good wear resistance. The polymers are useful over a wide temperature range (–195 to +260°C) and are inherently fire-resistant (oxygen index of 43 and UL-94 rating of V-0). Their chemical resistance is excellent, but they are attacked by hot caustics and acid as well as steam. Applications for molded parts include electronic connectors and jet engine component generator parts. The solution form of the polymer is used for wire enamels and a variety of electronics applications. Suppliers include Quadrant and Solvay.

### 2.3.7 Polyimides

These materials are derived from the solution condensation polymerization of aromatic dianhydrides and diamines and are characterized by the presence of only the imide linkage (–CONCO–). The polyimides are characterized by high glass transition temperatures, excellent radiation resistance, toughness, good electrical properties, and good flame resistance. The properties of polyimides can be modified by adjusting both the type and the ratio of the monomers. Fillers have also been added to polyimides to alter their properties. These modifications have produced a variety of polyimide materials. The polyimides can be processed in solution or powder form and can be converted into films, molding powders, tapes, and varnishes. Polyimides can be compression and injection molded, but considerable expertise is required because of the high glass tran-



sition temperatures and melt viscosities of these polymers. Kapton<sup>®</sup> is perhaps the most widely known of the polyimide family, but other types include Vespel<sup>®</sup> and Pyralin<sup>®</sup> (DuPont), and Pyre ML<sup>®</sup> (Industrial Summit Technologies). Although there are differences in the properties of the various polyimides, the properties of the polyimide family are illustrated with those of Kapton film. Tables 2.10 and 2.11 show these properties. Further details are available in Ghosh and Mittal.<sup>14</sup>

**TABLE 2.10 Physical and Electrical Properties of Kapton 100 HN Film**

Physical properties	Typical values at		Test method
	23°C (73°F)	200°C (392°F)	
Ultimate tensile strength, MPa (psi)	231 (33,500)	139 (20,000)	ASTM D-882-91, Method A*
Yield point at 3%, MPa (psi)	69 (10,000)	41 (6,000)	ASTM D-882-91
Stress to produce 5% elongation, MPa (psi)	90 (13,000)	61 (9,000)	ASTM D-882-91
Ultimate elongation, %	72	83	ASTM D-882-91
Tensile modulus, GPa (psi)	2.5 (370,000)	2.0 (290,000)	ASTM D-882-91
Impact strength, N-cm (ft-lb)	78 (0.58)		DuPont pneumatic impact test
Folding endurance (MIT) cycles	285,000		ASTM D-2176-89
Tear strength—propagating (Elmendorf), N (lbf)	0.07 (0.02)		ASTM D-1922-89
Tear strength—initial (Graves), N (lbf)	7.2 (1.6)		ASTM D-1004-90
Density, g/cc	1.42		ASTM D-1505-90
Coefficient of friction—kinetic (film-to-film)	0.48		ASTM D-1894-90
Coefficient of friction—static (film-to-film)	0.63		ASTM D-1894-90
Refractive index (sodium D line)	1.70		ASTM D-542-90
Poisson's ratio	0.34		Avg. 3 samples Elongated at 5%, 7%, 10%
Low temperature flex life	Pass		IPC TM650, Method 2.6.18
Dielectric strength at 60 Hz, V/mil	7,700		ASTM D-149-91
Dielectric constant at 1 kHz	3.4		ASTM D-150-92
Dissipation factor	0.0018		ASTM D-150-92
Volume resistivity, Ω-cm	1.5 × 10 <sup>17</sup>		ASTM D-257-91

\*Specimen size: 25 × 150 mm; jaw separation: 100 mm; jaw speed 50 mm/min; "ultimate" refers to the tensile strength and elongation measured at break.

SOURCE: DuPont,<sup>12</sup> reprinted with permission.

TABLE 2.11 Thermal Properties of Kapton 100HN Film

Thermal properties	Typical values	Test condition	Test method
Melting point	None	None	ASTM E-794-85 (1989)
Coefficient of thermal expansion	20 ppm/°C (11 ppm/°F)	-14 to +38°C	ASTM D-696-91
Thermal conductivity (W/m-K)	0.12	296 K	ASTM F-433-77 (1987)
(cal/cm-s-°C)	$2.87 \times 10^{-4}$	23°C	
Specific heat (J/g-K)	1.09		Differential Scanning
(cal/g-°C)	0.261		Calorimetry
Flammability	94 V-0		UL-94 (2-8-85)
Shrinkage (%)	0.17	30 min @ 150°C	IPC TM 650, Method 2.2.4A
	1.25	120 min @ 400°C	ASTM D-5214-91
Heat sealability	Not heat sealable		
Limiting oxygen index, %	37		ASTM D-2863-87
Solder float	Pass		IPC-TM-650, Method 2.4.13A
Smoke generation	DM<1	NIST smoke chamber	NFPA-258
Glass transition temperature	A second-order transition occurs in Kapton between 360°C (680°F) and 410°C (770°F) and is assumed to be the glass transition temperature. Different measurement techniques produce different results within the above temperature range.		

SOURCE: DuPont<sup>12</sup> Reprinted with permission.

### 2.3.8 Polyetherimide

Although this material belongs to the polyimide family of resins and has properties similar to those of the all-aromatic polyimides, it has lower thermal stability. (It is UL-rated for 170°C continuous use, compared to 220°C for Kapton polyimide.) It is an amorphous polyimide having aromatic imide and ether repeating units in its molecular chain. It processes much better on conventional thermoplastic equipment compared to the completely aromatic polyimides and is easily molded into complex shapes. It has a UL-94 V-0 flame resistance rating and an oxygen index of 47. Chemical resistance is good against hydrocarbons, and it resists mild acid and base for short exposure times. It has excellent ultraviolet and gamma radiation resistance (94 percent retention of tensile strength after exposure to 400 Mrads of cobalt irradiation). The polymer retains 85 percent of its tensile strength after 104 h in boiling water. Electrical properties show very good stability under various

conditions of temperature, humidity, and frequency. Its low dissipation factor makes it transparent to microwaves. Applications include low-loss radomes, printed-wiring boards, IC chip carriers, bobbins, and infrared switches. Selected properties of Ultem<sup>®</sup>, a representative polyetherimide from GE Plastics, are listed in Table 2.12.

**TABLE 2.12 Properties of Ultem<sup>®</sup> Polyetherimide**

Property	Ultem 1000 unfilled	Ultem 2300 30% glass	Method
Tensile strength (psi @ 0.2 in/min)	16,000	24,500	ASTM D-638
Tensile modulus (psi @ 0.2 in/min)	520,000	1,350,000	ASTM D-638
Flexural modulus (psi)	510,000	1,300,000	ASTM D-790
Izod impact, notched (ft-lb/in @ 73°F)	1.0	1.6	ASTM D-256
Coefficient of thermal expansion			ASTM E-831
Flow (ppm/°F @ 0–300°F)	31	11	
Cross-flow (ppm/°F @ 0–300°F)	30	—	
Thermal conductivity (W/m-C)	0.22	—	ASTM C-177
Volume resistivity (Ω-cm)	$1 \times 10^{17}$	$3 \times 10^{16}$	ASTM D-257
Dielectric strength (V/mil in air; 0.062 in)	831	630	ASTM D-149
Dielectric constant (1 kHz)	3.15	3.70	ASTM D-150
Dissipation factor (1 kHz)	0.0015	0.0015	ASTM D-150

SOURCE: GE Plastics web site, [www.geplastics.com](http://www.geplastics.com)

### 2.3.9 Polyarylate and polyesters

The thermoplastic polyesters include polyarylate (PA), polybutylene terephthalate (PBT), polyethylene terephthalate (PET), and polycyclohexylene dimethylene terephthalate (PCT). These linear polyesters range from amorphous to crystalline materials and have the characteristic ester functional group (–COOR–) present along the polymer chain. Except for the polyarylates, the other polyesters are made by a transesterification of the appropriate alcohol and ester monomers. Polyarylate is prepared from the reaction of bisphenol A and a mixture of isophthalic and terephthalic acids. Because of the variety of alcohols, acids, and esters that are available for reaction, polyesters with a broad range of properties can be synthesized. Suppliers include Eastman, Honeywell, Bayer, DuPont, Dow Chemical, GE, Ticona, and Creanova.

*Polyarylate* (PA) resins are aromatic, linear, amorphous polyesters with excellent toughness, ultraviolet resistance, flex strength, dimensional stability,

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flame retardance, and electrical properties. Electrical properties are fairly constant over a broad temperature range. These polymers are susceptible to stress cracking when exposed to ketone, aromatic hydrocarbon, ester, and chlorinated solvents. If polyarylates are alloyed with other polymers, the stress crack resistance is improved. Polyarylates are processed by most conventional melt processes such as injection extrusion, flow molding, and thermoforming. Electrical applications include connectors, relay housings, coil bobbins, and switch and fuse covers.

*Polybutylene terephthalate* (PBT) is a linear, semicrystalline, aliphatic polyester, although it does have some aromatic character. It has excellent chemical and temperature resistance and good electrical properties that are unaffected by humidity. PBT is unaffected by water, weak acids and bases, and common organic solvents at room temperature. It cannot be solvent bonded because of its solvent resistance. PBT resins are processed mostly by injection molding.

*Polyethylene terephthalate* (PET) is also a linear, semicrystalline, aliphatic polyester that is produced as a standard-grade and an engineering-grade material. The latter grade has superior properties (strength, stiffness, dimensional stability, chemical and heat resistance, and electrical properties) and is therefore preferred for electrical applications. The material is processed by injection molding and is used for lamp sockets, coil forms (audio/video transformers), connectors, and terminal blocks.

*Polycyclohexylene dimethylene terephthalate* (PCT) is a linear high-temperature semicrystalline material. Its high heat resistance distinguishes it from PET and PBT. PCT has a melting point of 290°C, as compared to 224°C for PBT and 250°C for PET. This high-temperature resistance makes PCT useful for surface-mount electronic components. The material has an excellent balance of physical, chemical, electrical, mechanical, and thermal properties. Injection molding is the preferred processing method. Applications include sockets, chip carriers, pin grid arrays, coil bobbins, and surface-mount components.

**2.3.10 Polycarbonates**

Polycarbonate is a linear, amorphous material synthesized by interfacial polymerization. The characteristic properties of this polymer are excellent transparency, toughness, and high-temperature properties (up to 140°C). The polymer is essentially self-extinguishing. The electrical properties are good with a stable dielectric constant over a wide temperature and frequency range. The ultraviolet and chemical resistance of polycarbonate is limited. The polymers are attacked by alkali, amines, ketones, esters, and aromatic hydrocarbons. Stressed polycarbonate parts are sensitive to many solvents and will crack on exposure. Polycarbonate is processed by most conventional thermoplastic processing methods. Applications include connectors, circuit breaker boxes, and bobbins. Suppliers include Bayer, Dow Chemical, and GE.

**2.3.11 Polyolefins**

This class of materials includes the polymers and copolymers of polyethylene and polypropylenes. The grades include a range of densities (0.83 g/cm<sup>3</sup> for

polymethylpentene to  $0.96 \text{ g/cm}^3$  for the high-density polymers) and a range of molecular weights, including ultrahigh molecular weight. These polymers are characterized by the  $-(\text{CH}_2- \text{ or } -\text{CHR})-$  repeat unit, where R represents hydrogen or an alkyl radical. There are a multitude of materials available, but they all have a low dielectric constant, low dissipation factor, low water absorption, low coefficient of friction, and excellent chemical resistance (resistant to acids, alkalis, and most solvents). Special grades of polyolefins, such as the higher-molecular-weight material, exhibit increased toughness, abrasion resistance, and freedom from environmental stress cracking. Wire and cable insulation are the main uses for these materials in the electrical industry. Suppliers include Eastman, Quadrant, Honeywell, Elf Atochem, DuPont, Dow Chemical, Nova Chemical, and Equistar. Further information is available in Vasile.<sup>15</sup>

### 2.3.12 Polyphenylene oxide

Polyphenylene oxide (PPO) is a linear amorphous polymer made by a procedure called *oxidative coupling*. The glass transition temperature of pure PPO is  $210^\circ\text{C}$ . This polymer is not used in its neat form but rather is blended with polystyrene to produce the commercial materials Noryl<sup>®</sup> and Prevex<sup>®</sup> (both General Electric Co.). This modification reduces the glass transition temperature of the blend. The PPO alloys have good resistance to acids and alkalis but are attacked by some aromatic and chlorinated solvents. A number of grades are available, all of which can be easily processed on conventional thermoplastic molding equipment. Applications include computers, connectors, fuse blocks, relays, and bus bar insulation.

### 2.3.13 Polyphenylene sulfide

Polyphenylene sulfide (PPS) is a semicrystalline material that is inherently flame retardant. Two forms of PPS are available, a linear and a branched polymer. The former has better strength and melt viscosity properties. PPS is inert to all solvents except hot nitric acid. It is processed like most thermoplastics and can be injection and compression molded. Cross-linkable grades are available with exceptional heat resistance. The PPS polymers are rated UL-94 V-0. The polymers have stable electrical properties over broad temperature, frequency, and humidity ranges. Both volume and insulation resistance are excellent in wet and dry environments, and the arc resistance is good. The primary uses of PPS resins are in electric connectors, coil forms, bobbins, yokes, and terminal boards. Suppliers include Chevron Phillips, GE, Ticona, and Toyobo.

### 2.3.14 Styrenics

The styrene polymers include acrylonitrile-butadiene-styrene (ABS), acrylic-styreneacrylonitrile (ASA), polystyrene (PS), styrene-acrylonitrile (SAN), styrene-butadiene (SB), and styrene-maleic anhydride (SMA). The properties of these polymers are dependent on the ratio of the monomeric components,

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which leads to a broad range of material properties. These polymers are generally not used in electrical applications except as electronic housings. Polystyrene has very low dielectric losses ( $\epsilon' = 2.45$ ,  $\tan \delta = 0.001$ ), and its chief use in electronics is in striplines. The styrenics are amenable to all forms of thermoplastic processing. Suppliers include Chevron-Phillips, Elf Atochem, Bayer, Dow Chemical, GE, and Creanova.

**2.3.15 Polysulfones**

Polysulfones are amorphous polymers of high-temperature resistance. These materials contain the arylsulfone group as part of their chemical structure. There are three important sulfone polymers, all of which have excellent electrical properties: polysulfone, polyarylsulfone, and polyethersulfone. These materials are resistant to acid and alkaline hydrolysis but can exhibit stress crazing when exposed to certain chemicals (esters, ketones, and some hydrocarbons). All the polymers have excellent creep and radiation resistance. Processing is carried out on standard thermoplastic equipment. Applications include printed-wiring board substrates, television components, coil bobbins, connectors, and switch housings. Suppliers include Solvay and BASF.

**2.3.16 Vinyls**

The vinyl polymers include polyvinylchloride (PVC), polyvinylidene chloride (PVDC), and chlorinated polyvinylchloride (CPVC). The vinyl resins contain the structural unit  $-(\text{CH}_2-\text{CHCl})-$  in the polymer chain, although the PVDC and CPVC contain extra chlorine atoms. All the resins show good chemical and flame resistance, with PVC being the weakest member of the family with regard to these properties. PVC is the most versatile of the plastics because of its wide blending capability. CPVC has excellent chemical resistance, rigidity, strength, and weatherability. PVDC has low permeability to gases and liquids, good barrier properties, and also good chemical resistance. All the vinyl resins are processed on conventional thermoplastic equipment. Electrical applications include wire insulation, cable jackets, sleeving, and tubing. Suppliers include BASF, Creanova, Dow Chemical, Eastman Chemical, Elf Atochem, Geon, and Solvay.

**2.3.17 Thermoplastic alloys and blends**

The ability of polymers to be mixed together to form a new polymer mixture with greatly expanded properties has given rise to this new group of materials. Alloys are synergistic polymer combinations with real property advantages derived from a high level of thermodynamic compatibility between the components. Alloys exhibit strong intermolecular forces and form single-phase systems with one glass transition temperature.<sup>5</sup> Noryl, an alloy of polystyrene and PPO, is a typical example. Blends do not have the exacting thermodynamic capabilities that alloys have, and they exhibit discrete phases and multiple glass transition temperatures. In general, the properties of a blend reflect the weighted average of the properties of the components of the blend.

Alloys and blends are processed on all conventional thermoplastic equipment. A list of common alloys and blends is given in Table 2.13 along with supplier names and important properties. More detailed information on alloys and blends can be obtained in Utracki.<sup>16</sup>

**TABLE 2.13 Common Alloys and Blends**

Alloy or blend	Trade name	Supplier	Key properties
PPO/PS	Noryl Luranyl Vestoran Xyron	GE Plastics BASF Creanova Asahi Chemicals	Heat resistance, toughness, good moisture resistance, low cost, injection molding, blow molding, calendaring, extrusion
Nylon/ABS	Stapron Triax Ultramid	DSM Bayer ASF	Heat and chemical resistance, wear and abrasion resistance, low-temperature impact strength, injection molding, extrusion, thermoforming
Nylon/elastomers	Capron Durethan Fiberfil Minlon Technyl Ultramid Vydyne Zytel	Honeywell Bayer DMS DuPont Rhodia BASF Dow Chemical	Improved toughness, fatigue resistance, chemical and heat resistance, extrusion, injection molding, compression molding, transfer molding, blow molding
PPO/Nylon	Noryl GTX Xyron	GE Plastics Asahi Chemicals	High-temperature resistance, chemical resistance, low moisture absorption, dimensional stability, high temperature creep resistance, extrusion, thermoforming, injection molding
ABS/PC	Bayblend Cycology Iupilon Lexan	Bayer GE Plastics Mitsubishi Engineering Plastics	Heat resistance, processability, low-temperature impact, high stiffness and strength, injection molding, extrusion, thermoforming
PPO/PBT	Gemax	GE Plastics	High-temperature resistance, solvent resistance, dimensional stability, processability
Polyester/elastomer	Celanex Rynite Makroblend Ultradur	Ticona DuPont Bayer BASF	Stiffness, toughness, high-temperature and solvent resistance, injection molding, extrusion, compression molding
PC/PBT, PET	Makroblend Xenoy	Bayer GE Plastics	High impact strength and modulus of wide temperature range, chemical resistance, injection molding, extrusion
ASA/PC	Geloy	GE Plastics	Impact resistance, thermal stability, weather resistance, extrusion, injection molding
PET/PBT	Celanex Valox	Ticona GE Plastics	Heat resistance, fast molding, low cost

TABLE 2.13 Common Alloys and Blends (Continued)

Alloy or blend	Trade name	Supplier	Key properties
Acetate/ elastomer	Celcon Delrin Thermocomp Ultraform	Ticona DuPont LNP Engineering Plastics BASF	Stiffness, toughness, fatigue, wear, extrusion, injection molding, compression molding, transfer molding
SMA/ABS	Cadon Luran Magnum Terluran	Bayer BASF Dow Chemical	Heat resistance, impact, low cost, plating, extrusion, thermoforming, injection molding
Polysulfone/ ABS	Mindel	Solvay Advanced Polymers	Processability, low cost, heat resistance, plating, extrusion, injection molding
PEEK/PES	Victrex	Victrex	High heat distortion temperature, processability, low cost, impact resistance, injection molding, extrusion, compression molding
PC/TPU	Texin	Bayer	Stiffness, wear, low-temperature impact, extrusion, injection molding
Nylon/PE	Selar	DuPont	Heat/chemical resistance, barrier properties, wear resistance, extrusion, injection molding, compression molding

## 2.4 Thermosets

Unlike thermoplastics, thermoset materials are polymers that form three-dimensional cross-linked networks of polymer chains that cannot be softened or reheated for additional use. In general, these materials can provide higher temperature capability than the thermoplastic materials. Thermoset materials, before being cured, are fabricated by casting, compression molding, filament winding, laminating, pultrusion, or injection and transfer molding. Most thermoset materials, before they are cross-linked, are considerably more fluid than thermoplastics during processing. A thermoset material must contain a functionality greater than 2 to facilitate cross-linking; that is, the polymer chain must have enough reactive sites to form a three-dimensional network. Difunctional materials form linear or branched uncross-linked polymers but can be cross-linked through the addition of either a catalyst or a curing agent. These ingredients promote the formation of active sites for further reaction. The curing or cross-linking reaction is an exothermic reaction, and consideration must be given to control the temperature rise to prevent a runaway reaction. Thermoset materials usually shrink when they are cross-linked, but the shrinkage can be controlled with additives such as fillers and reinforcing fibers or fabrics. The conversion of these materials to the thermoset state can be accomplished at room or elevated temperature, the latter giving a faster and more complete cure of the resin. The reader is referred to other texts for more detailed descriptions of all thermosetting plastics.<sup>5-7,17</sup> Properties of thermosets for electronics applications are given in Table 2.14.



TABLE 2.14 Properties of Thermosetting Plastics

	Epoxy			Phenolics			Alkyds						Bismaleimides	Cyanate esters	Benzocyclobutene
	DAP (GDI-30)	Glass-filled	Mineral-filled	General-purpose	Glass-filled	Mineral-filled	MAG	MAI-60	Polyester GPO-3	Polyimide	Polyurethane	Mineral-filled silicone			
Dielectric constant, D-150															
60Hz	4.2	5.0	4.0	12.0	50.0	6.0	6.3	5.6	4.5	3.5	6	3.6	—	—	—
10 <sup>6</sup> Hz	3.5	4.6	5.0	6.0	6.0	10.0	4.7	4.6	—	3.4	3	3.7	3.5	2.66–3.10	2.65–2.70
Dissipation factor, D-150															
60Hz	0.004	0.01	0.01	0.3	0.3	0.07	0.04	0.10	0.05	0.0025	0.1	0.005	—	—	—
10Hz	0.01	0.01	0.01	0.7	0.8	0.10	0.02	0.02	—	0.01	0.04	0.003	0.007	0.01–0.005	–0.002
Dielectric strength, D-149; V/mil															
400	360	400	400	350	400	400	400	375	300	6500	500	425	480–508		
Volume resistivity, D-257; Ω-cm															
10 <sup>13</sup>	3.8 × 10 <sup>15</sup>	9 × 10 <sup>15</sup>	10 <sup>13</sup>	10 <sup>13</sup>	10 <sup>14</sup>	10 <sup>14</sup>	10 <sup>13</sup>	—	10 <sup>18</sup>	10 <sup>14</sup>	10 <sup>15</sup>	—	10 <sup>16</sup>	9 × 10 <sup>19</sup>	
Arc resistance, D-495; seconds															
140	140	180	50	70	180	>180	180	>180	230	120	240	—	Excellent		—
Specific gravity, D-792															
1.7	1.8	2.1	1.45	1.95	1.83	2.24	2.07	1.95	1.4	1.1	2.05	1.30	1.10–1.43		
Water absorption, D-570; % 24 h															
<0.2	0.2	0.04	0.7	0.5	0.5	0.08	0.07	0.5	2.9	0.2	0.15	4.0–4.4*	0.6–2.5*		—
Heat deflection temperature, D-648; at 264 lb/in <sup>2</sup> , °F															
500	400	250	340	400	500	350	>400	—	680	190	>500	520	480		—
Tensile strength (Izod), D-256; ft-lb/in															
10,000	30,000	15,000	10,000	7000	11,000	3000	6000	9000	17,000	1000	6500	12,000	13,000		—
Impact strength (Izod), D-256; ft-lb/in															
5.0	10	0.4	3.5	15.0	0.3	9.5	8.0	1.5	25	0.5	0.3–0.5	0.7–0.9		—	
Coefficient of thermal expansion, D-696; 10 <sup>-5</sup> /°F															
2.6	1.7	2.2	2.5	—	0.88	3	2	2	2.8	25	2.8	40 ppm/°C	50 ppm/°C		42–70 ppm/°C
Thermal conductivity, C-177; Btu-in(h-ft <sup>2</sup> -°F)															
—	6	—	0.3	0.34	0.2	7.2	3.6	4	6.8	0.1	3.1	—	—		—

\*500-h water boil.

SOURCE: From Harper.<sup>8</sup> Reprinted with permission.

**2.36 Chapter 2****2.4.1 Allyl resins**

The allyl resins are thermosetting polyester materials that retain their desirable physical and electrical properties on prolonged exposure to severe environmental conditions such as high temperature and humidity. These resins have good chemical resistance and can withstand between  $10^4$  and  $10^{12}$  rads of gamma radiation.<sup>17</sup> These polymers have the allyl radical  $\text{CH}_2\text{--CH=CH}_2$  as part of their chemical structure. The principal allyl resins are based on diallyl phthalate (DAP) and isophthalate (DAIP) monomers and prepolymers. There are other resins that are used alone or in combination with DAP and DAIP. They are diethylene glycol bis(allyl carbonate), allyl methacrylate, diallyl fumarate and maleate, as well as triallyl cyanurate. The allyl resins are converted to thermoset materials by heat and by the addition of free-radical sources such as benzoyl peroxide and t-butyl perbenzoate to the resin formulation. Curing of these resins is slow below  $150^\circ\text{C}$ . These resins are used as cross-linking agents in other polyester systems and as molding compounds, preimpregnated glass cloth, sealants, insulating coatings, and decorative laminates. Most critical electronics applications requiring high reliability under adverse conditions use allyl resins, such as connectors in communications, computers, and aerospace systems; insulator switches; chip carriers; and circuit boards. The allyl resins have a low loss factor, high volume and surface resistivity, and high arc resistance. Those properties are retained under high-humidity conditions. The allyl resins can be compression, transfer, and injection molded, and they can also be used in prepregging operations. In general, DAP compounds are designed for continuous operation at about  $176^\circ\text{C}$ , whereas DAIP can operate at about  $232^\circ\text{C}$ . Suppliers include Cosmic Plastics and Rogers.

**2.4.2 Bismaleimides**

Within the polyimide family of resins, there is a class of thermosetting polymers that have a preimidized structure and form a three-dimensional network via addition polymerization without the evolution of volatile material. These materials are classified as bismaleimides (BMIs), and the monomers and prepolymers are prepared by the reaction of maleic anhydride and diamines. The material is very reactive and can be homopolymerized or copolymerized to produce a wide variety of thermosetting resins. The polymers are characterized as having the processing ease of epoxy resins but superior elevated-temperature performance properties. Epoxies operate in the  $150^\circ\text{C}$  temperature range, and the BMIs operate in the range of  $200$  to  $232^\circ\text{C}$ . Compression, transfer, and injection molding; filament winding; and prepregging are the normal processing methods for bismaleimides. Bismaleimides are sold as powders or as solutions in polar solvents. These materials are primarily used in printed-wiring board substrates.

**2.4.3 Epoxy resins**

Epoxy resins are characterized by the presence of the epoxy (oxirane) ring. Most commercial epoxy resins are derived from bisphenol A and epichlorohy-

drin, but there are many other types based on the epoxidation of multifunctional molecules that give rise to epoxy resins with a broad range of properties. Epoxy resins can be liquids or solids. Curing of these resins is accomplished by reaction through the epoxide and hydroxyl functional groups. Curing agent type and amount, and temperature determine the condition of cure and the final properties of the resin. Typical curing agents include the aliphatic amines and amides for ambient-temperature cure, and the anhydrides, organic acids, aromatic amines, and various phenolic condensation products for elevated-temperature cure. Most common epoxy resins are solventless (100 percent solids). However, higher-molecular-weight and multifunctional epoxies are solid and are usually processed in solution form. The curing reaction is exothermic, which may be necessary to control in large-batch operations. The cured resins have an excellent combination of physical, chemical, mechanical, and electrical properties and are used extensively in many electrical and nonelectrical applications. Epoxies can be compression and transfer molded and filament wound. They are used in casting, prepregging, and laminating operations. Epoxies can be formulated to produce conformal coatings, adhesives, and varnishes and are used in the electrical industry as bobbins, connectors, and chip carriers, and as the matrix resin in printed-wiring-board substrates. Suppliers include Dow Chemical, Vantico, and Resolution Performance Products.

#### 2.4.4 Phenolic resins

Phenolic resins are the reaction product of phenol and formaldehyde. Two kinds of phenolics are produced: the resols (alkaline condensation products) and the novolacs (acid condensation products). The basic difference between a resol and a novolac is the presence of one or more free methylol groups on the resol. The resins are heat cured to form a dense cross-linked network, which gives the phenolic resins their high heat resistance and dimensional stability. Phenolic resins have poor arc resistance. They are available in solution form or as powders and can be converted to molding compounds, varnishes, and laminates. They are processed by injection, compression, and transfer molding. Phenolics are used as chip carriers, connectors, and bobbins, and as matrix resins for printed-wiring board substrates. Suppliers include Durez, Plenco, and Rogers.

#### 2.4.5 Polyesters

Polyester resins are versatile materials and are available as low-viscosity liquids up to thick pastes. Included within the polyester family are alkyd resins, unsaturated resins, vinyl esters, and the allyl resins discussed in Sec. 2.4.1. The characteristic functional group present in these resins is the ester group ( $-\text{COOR}-$ ), but the composition of these polyester resins can be varied tremendously to produce resins having widely different properties. Table 2.15 lists the various components available for preparing polyester resins. Cross-linking of these materials is accomplished by the addition of polyfunctional acids or alcohols, unsaturated monomers, and a peroxide catalyst. Curing is done from

TABLE 2.15 Unsaturated Polyester Components

Components	Ingredients	Characteristics
Unsaturated anhydrides and dibasic acids	Maleic anhydride	Lowest cost, moderately high heat-deflection temperature (HDT)
	Fumaric acid	Highest reactivity (cross-linking), higher HDT, more rigidity
Saturated anhydrides and dibasic acid	Phthalic (orthophthalic) and anhydride	Lowest cost, moderately high HDT, provides stiffness, high flexible and tensile strength
	Isophthalic acid	Higher tensile and flexible strength, better chemical and water resistance
	Adipic acid, azelaic acid sebacic acid	Flexibility (toughness, resilience, impact strength); adipic acid is lowest in cost of flexibilizing acids
	Chlorendic anhydride	Flame retardance
	Nadic methyl anhydride	Very high HDT
	Tetrachlorophthalic	Flame retardance
Glycols	Propylene glycol	Lowest cost, good water resistance and flexibility, compatibility with styrene
	Dipropylene glycol	Flexibility and toughness
	Ethylene glycol	High heat resistance, tensile strength, low cost
	Diethylene glycol	Greater toughness, impact strength, and flexibility
	Bisphenol-A adduct	Corrosion resistance, high HDT, high flexible and tensile strength
	Hydrogenated bisphenol-A adduct	Corrosion resistance, high HDT, high flexible and tensile strength
Monomers	Styrene	Lowest cost, high reactivity, fairly good HDT, high flexible strength
	Diallyl phthalate	High heat resistance, long shelf life, low volatility
	Methyl methacrylate	Light stability, good weatherability, fairly high HDT
	Vinyl toluene	Low volatility, more flexibility, high reactivity
	Triallyl cyanurate	Very high HDT, high reactivity, high flexible and tensile strength
	Methyl acrylate	Light stability, good weatherability, moderate strength

SOURCE: From Schwartz and Goodman.<sup>7</sup> Reprinted with permission.

room temperature to about 160°C. Fillers, pigments, and fibers can be mixed with the resins. Characteristic properties include ease of processing, low cost, good electrical properties, and high arc resistance. Applications include bob-bins, terminal boards, connectors, and housings. Polyester resins can be compression or transfer molded, laminated, pultruded, and filament wound. Suppliers include Bayer, Creanova, DSM, DuPont, Eastman Chemical, GE Plastics, Honeywell, and Ticona.

#### 2.4.6 Polyurethanes

These polymers are derived from the reaction of polyfunctional isocyanates and polyhydroxy (polyether and polyester polyols) compounds that yield linear or branched polymers. The basic chemical unit of polyurethanes is the urethane ( $-RNHCOOR-$ ). These resins are produced as castable liquids (prepolymers) and are cross-linked by adjusting the stoichiometry and functionality of the isocyanate or polyol. Catalysts are added to enhance the rate of reaction. A variety of other ingredients (active hydrogen compounds) can be added to produce polyurethanes with different properties, ranging from elastomeric to rigid polymers. The polyether urethanes are more hydrolytically stable than the polyester urethanes, but the latter give better strength and abrasion resistance. Polyurethanes have poor solvent resistance. They are sensitive to chlorinated and aromatic solvents as well as to acids and bases. Urethanes are used as conformal coatings to encapsulate sensitive electronic components. They are processed by reaction injection molding (RIM), compression molding, and casting. Suppliers include Bayer, BASF, and Dow Chemical.

#### 2.4.7 Silicones

Silicones are polymers that consist of alternating silicon and oxygen atoms along the backbone of the polymer chain. The backbone is modified by attaching organic side groups to the silicon atom; in so doing, this imparts the unique properties found in these polymers. The silicones can be produced in the form of liquids, greases, elastomers, and hard resins. The organic group attached to the silicon atom can be aliphatic, aromatic, or vinyl, which affects the properties of the final silicone polymer. The silicone fluids are low-molecular-weight polymers in which the organic group on the silicone is methyl or phenyl, or a mixture of both. The silicone resins are branched polymers that cure to a solid while the elastomers are linear oils or higher-molecular-weight silicones that are reinforced with a filler and then vulcanized (cross-linked). The elastomers come in three forms: heat-cured rubber, two-component liquid injection molding compounds, and room-temperature vulcanizing (RTV) products. The conversion of silicones to cross-linked elastomers can be accomplished by free-radical condensation, addition, and ultraviolet radiation curing techniques. The silicones are characterized by their useful properties over a broad temperature range ( $-65$  to  $248^\circ\text{C}$ ). They exhibit excellent weatherability; arc and track resistance; and impact, abrasion, and chemical resistance. Silicones can also be copolymerized with other polymers to produce

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materials with a variety of interesting properties, such as silicone-polyimide, silicone-EPDM, and silicone-polycarbonate. Electronics applications include wire enamels, laminates, sleeving and heat-shrinkable tubing, potting for electronic components, conformal coatings, and varnishes. Properties of various silicone polymers are listed in Tables 2.16 through 2.19. Suppliers include Dow-Corning and GE Silicones.

**TABLE 2.16 Approximate Physical Properties at 25°C of Methylpolysiloxane Fluids (Rhodorsil Oil 47V)**

Viscosity, cSt	VTC*	Specific gravity	Flash point, °C	Freezing point, °C	Surface tension, dynes/cm	Vapor <sup>†</sup> pressure, mm Hg	VCE, <sup>‡</sup> cm <sup>3</sup> /cm <sup>3</sup> ·°C	Dielectric constant <sup>¶</sup>	Dielectric strength, kV/mm
5	0.55	0.910	136	-65	19.7	—	$1.05 \times 10^{-3}$	2.59	—
10	0.57	0.930	162	-65	20.1	—	$1.08 \times 10^{-3}$	2.63	13
20	0.59	0.950	230	-60	20.6	$1 \times 10^{-2}$	$1.07 \times 10^{-3}$	2.68	—
50	0.59	0.959	280	-55	20.7	$1 \times 10^{-2}$	$1.05 \times 10^{-3}$	2.8	15
100	0.60	0.965	>300	-55	20.9	$1 \times 10^{-2}$	$0.05 \times 10^{-3}$	2.8	16
300	0.62	0.970	>300	-50	21.1	$1 \times 10^{-2}$	$0.95 \times 10^{-3}$	2.8	16
500	0.62	0.970	>300	-50	21.1	$1 \times 10^{-2}$	$0.95 \times 10^{-3}$	2.8	16
1000	0.62	0.970	>300	-50	21.1	$1 \times 10^{-2}$	$0.95 \times 10^{-3}$	2.8	16
5000 to 2,500,000	0.62	0.973	>300	45	21.1	$1 \times 10^{-2}$	$0.95 \times 10^{-3}$	2.8	18

\*Viscosity/temperature coefficient =  $1 - (\text{viscosity at } 99^\circ\text{C}/\text{viscosity at } 38^\circ\text{C})$ .

<sup>†</sup>At 200°C.

<sup>‡</sup>Volume coefficient of expansion between 25 and 100°C.

<sup>¶</sup>Between 0.5 and 100 kHz.

SOURCE: From Goodman.<sup>17</sup> Reprinted with permission.

**TABLE 2.17 Typical Properties of Condensation Cure Methylphenyl RTV Silicone Rubber Products Cured at Room Temperature**

Viscosity, cSt	Specific gravity	Hardness, Shore A	Tensile strength, lb/in <sup>2</sup>	Useful temperature range, °F	Dielectric strength, V/mil	Dielectric constant at 1 kHz	Dissipation factor at 1 kHz
16,000	1.21	42	380	-175 to +400	520	3.6	0.005
30,000	1.35	55	690	-175 to +500	540	3.9	0.02
700,000	1.35	48	440	-175 to +500	470	3.9	0.02

SOURCE: From Goodman.<sup>17</sup> Reprinted with permission from *General Electric Silicones*.

**TABLE 2.18 Typical Properties of Addition Cure Clear RTV Silicone Rubber Products**

Viscosity, cSt	Specific gravity	Hardness, Shore A	Tensile strength, lb/in <sup>2</sup>	Useful temperature range, °F	Dielectric strength, V/mil	Dielectric constant at 1 kHz	Dissipation factor at 1 kHz
4,000	1.02	44	920	-75 to +400	520	2.7	0.0006
5,200	1.04	45	920	-175 to +400	530	2.69	0.0004

SOURCE: From Goodman.<sup>17</sup> Reprinted with permission from *General Electric Silicones*.

**TABLE 2.19 Estimated Useful Life of Silicone Rubber at Elevated Temperatures**

Service temperature, °F	Useful life*
250	10–20 years
300	5–10 years
400	2–5 years
500	3 months
600	2 weeks

\*Retention of 50 percent elongation.

SOURCE: From Goodman.<sup>17</sup> Reprinted with permission from *General Electric Silicones*.

#### 2.4.8 Cross-linked thermoplastics

Overall property enhancement is the underlying principle for the commercial development of cross-linked thermoplastics. This enhancement manifests itself in improved resistance to thermal degradation of physical properties, stress cracking, creep, and other environmental effects. Thermoplastics are cross-linked by radiation and chemical techniques. The techniques, which include X-rays, gamma rays, high-energy electrons, and organic peroxides, under controlled conditions, can be used to produce beneficial changes in the properties of irradiated polymers. Typical polymers capable of being cross-linked include the polyolefins, fluoroplastics, vinyls, neoprene, and silicone. Electrical applications include shrink-fit tubing, underground cable insulation, and microwave insulation. Table 2.20 lists cross-linked thermoplastic products and their applications.

#### 2.4.9 Cyanate ester resins

Cyanate ester resins are bisphenol derivatives containing the cyanate  $-O-C\equiv N$  functional group. These monomers and polymers cyclotrimerize on heating to form a cross-linked network of oxygen-linked triazine rings via addition polymerization. The cyanate ester resins range from liquids to solids and are characterized by superior dielectric properties, adhesion, low mois-

**TABLE 2.20 Heat-Shrinkable Insulation and Encapsulation Tubings**

	Product	Description	Typical Applications
Flexible polyolefins	RNF-100 type 1	General-purpose, flame-retarded, flexible polyolefin	Insulation of wire bundles; cable and wire identification; terminal and component insulation, protection, and identification
	RNF-100 type 2	General-purpose, flexible, transparent polyolefin	Transparent coverings for components such as resistors, capacitors, and cables where markings must be protected and remain legible
	RT-876	Highly flame-retarded, very flexible polyolefin with low shrink temperature	Coverings for cables and components where excellent flexibility and outstanding flame retardance are needed
	RT-102	Highly flexible, flame-retarded, polyolefin with very low shrink temperature	Flexible material for general-purpose protection and insulation; especially effective for low-temperature use
	RVW-1	Highly flame-retarded, flexible polyolefin	Lightweight harness insulation, terminal insulation, wire strain relief and general-purpose component packaging and insulation where a UL recognized product with a VW-1 (FR-1) rating is needed
Semirigid polyolefins	CRN type 1	General-purpose, flame-retarded, semirigid polyolefin	Insulation and strain relief of soldered or crimped terminations; protection of delicate components; cable and component identification
	RT-3	Semirigid, flame-retarded, opaque polyolefin	Particularly suited for automated application systems to insulate and strain relieve crimped or soldered terminals; furnished in cut pieces
Dual-wall polyolefins	SCL	Melttable inner walls, selectively cross-linked semirigid polyolefin	Encapsulation of components, splices, terminations, requiring moisture resistance, mechanical protection and shrink ratios as high as 6:1.
	TAT	Flexible, dual-wall adhesive tubing	Insulates and seals electrical splices, bimetallic joints, and components from moisture and corrosion



	ATUM	Semiflexible, high expansion, heavy dual-wall, adhesive tubing	Environmental protection for a wide variety of electrical components, including wire splices and harness breakouts
Fluoroplastics	Kynar*	High-temperature, flame-resistant, clear, semirigid fluoroplastic	Transparent insulation, mechanical protection of wires, solder joints, terminals, connections, and component covering
	Conovolex	Convolute, flexible, irradiated polyvinylidene fluoride	Mechanical protection of cable harnesses; excellent flexibility and chemical resistance; good high-temperature performance
	RT-218	Semirigid, white, high-temperature, low-outgassing fluoroplastic tubing	Insulation of splices and terminations in aircraft and mass transit markets; cable and wire identification
Vinyl	PVC	Flexible, flame-resistance, polyvinyl chloride	Insulation and covering of cables, components, terminals, handles
Elastomers	NT (neoprene)	Heavy-duty, flexible, abrasion-resistant, flame-retarded elastomer	Insulation and abrasion protection of wire bundles and cable harnesses
	SFR (silicone)	Highly flexible, flame-retarded, heat or cold shock-resistant	Cable and harness protection requiring maximum flexibility and resistance to extreme temperatures; ablative protection for cables in rocket blast
	Viton† (fluoroelastomer)	Flexible, flame-retarded, heat and chemical resistant fluoroelastomer	Insulation and protection of cables exposed to high temperature and/or solvents such as jet fuel
Caps	PD	Semirigid polyolefin, meltable inner wall	Encapsulation of stub splices, especially fractional-horsepower motor windings

\*Registered trademark of Atofina Chemicals, Inc.

†Registered trademark of E.I. duPont de Nemours & Co.

SOURCE: From Goodman.<sup>17</sup> Reprinted with permission from RayChem Corp.

ture absorption, flame resistance, high-temperature capability, and excellent dimensional stability. Glass transition temperatures range from 250 to 290°C. Several grades are available and can be formulated to produce laminating varnishes for impregnating inorganic and organic reinforcements. The formulations can be homopolymers, blends with other cyanate esters or with bismaleimides, and epoxy resins. Some properties of the neat resins are shown in Figs. 2.6 through 2.9<sup>18</sup> and of E-glass laminates in Tables 2.21 and 2.22.<sup>18</sup> Cyanate ester resins can be processed by melt polymerization, prepregging, and lamination operations. Applications in the electrical industry include printed-wiring-board substrates and radome structures. Cyanate ester resins can be toughened with thermoplastics such as polyethersulfone, polyetherimide, polyarylates, polyimides, and methylethylketonesoluble copolyesters and elastomers. Suppliers include Vantico.

**TABLE 2.21 Comparison of AroCy B-40S Laminate Properties with 60 Percent Epoxy Modification and FR-4 Reference\***

Laminate property	100% cyanate <sup>‡</sup>	60% epoxy <sup>†</sup> 40% cyanate <sup>‡</sup>	100% Epoxy <sup>†</sup>
Press cure, h/°C	1/177	1/177	1/177
Post cure, h/°C	3/225	—	—
T <sub>g</sub> (T <sub>MAS</sub> ), °C	225	183	130
CTE (Z), ppm/°C	44	55	60
Steam/solder, min	120	120	45
Flammability, UL-94	Burns	V-0	V-0
Peel strength, lb/in			
25°C	12.3	11.4	12.0
200°C	9.4	8.5	4.2
D <sub>k</sub> , 1 MHz	4.05	4.2	4.8
D <sub>k</sub> , 1 MHz	0.003	0.008	0.020

\*Laminates are 8-ply, style 7628 E-glass reinforced; 55 ± 2% resin by volume.

<sup>†</sup>Brominated hard epoxy, WPE 500, 27% Br.

<sup>‡</sup>AroCy B-40S.

SOURCE: From Shimp.<sup>18</sup> Reprinted with permission.

#### 2.4.10 Benzocyclobutenes

Benzocyclobutenes (BCBs) are thermally polymerized (addition polymerization) to produce a cross-linked resin without the evolution of volatiles. BCB is

**TABLE 2.22 Comparison of E-glass Laminate Properties for Several Resin Systems at Equal Resin Volume Content\***

Resin	D <sub>k</sub> , 1 MHz, vol. %			DMA T <sub>g</sub> , °C	TGA Onset, °C	Flammability rating, UL-94	Peel strength, lb/in		
	70	55	D <sub>f</sub> (10 <sup>-3</sup> )				258C	2008C	Pressure cooker, min.
Cyanate ester									
ArOCy F-40S	3.5	3.9	2	290	400	V-0	11	9	120
ArOCy M-40S	3.6	4.0	2	290	415	VI	12	10	120
XU 71787	3.6	4.0	3	255	426	†	8	6	120
ArOCy B-40S	3.7	4.1	3	290	405	†	12	10	120
Polyimide									
BMI-MDA	4.1	4.5	9	312	400	VI	9	6	120
Epoxy FR-4	4.5	4.9	20	145	300	V-0	12	4	45

\*Except for D<sub>k</sub> measurements on 70 vol % resin laminates, tests were performed on 55 vol %, 0.060-in, 8-ply laminates prepared with 7628 E-glass and postcured 4 h at 225–235°C.

†Burn times exceed self-extinguishing classifications.

SOURCE: From Shimp.<sup>18</sup> Reprinted with permission.

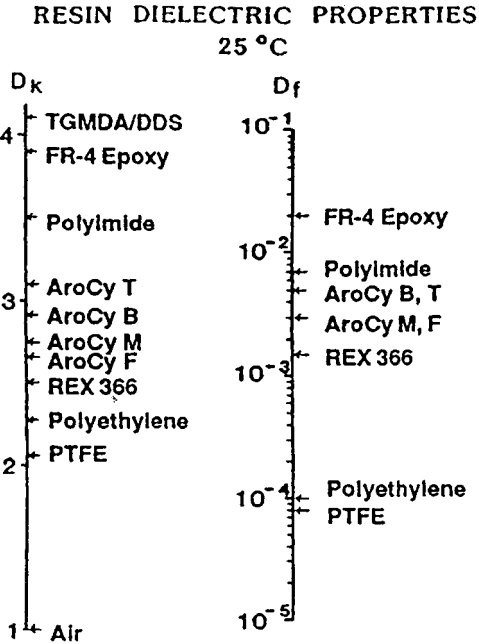


Figure 2.6 Comparison of dielectric constant and dissipation factor values measured at 25°C and 1 MHz for representative thermoset and thermoplastic polymers. (From Shimp,<sup>18</sup> reprinted with permission.)

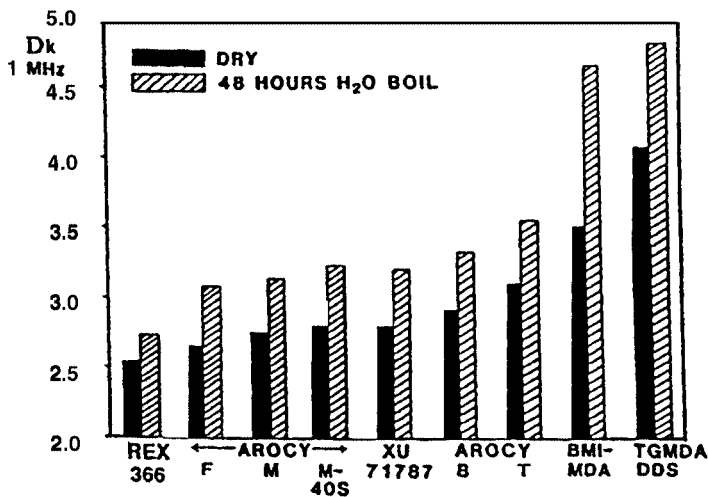
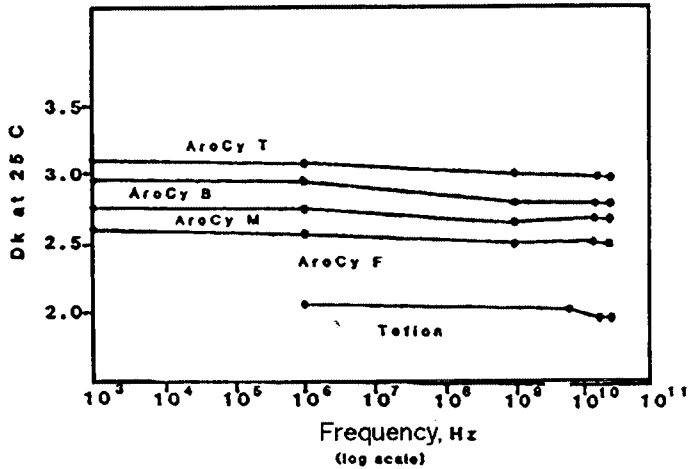
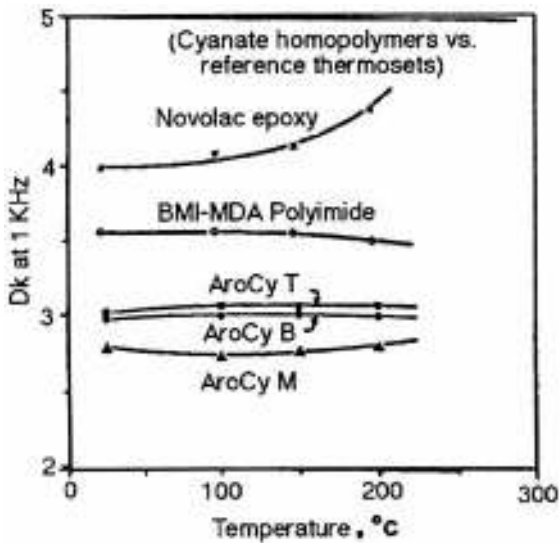


Figure 2.7 Effect of moisture conditioning on dielectric constant of several thermoset resins. (From Shimp,<sup>18</sup> reprinted with permission.)



**Figure 2.8** Flat dielectric constant response of cyanate ester homopolymers to increasing test frequency. (From Shimp,<sup>18</sup> reprinted with permission.)



**Figure 2.9** Flat dielectric constant response of cyanate ester homopolymers over 25 to 200°C temperature range. Epoxy novolac is reference resin. (From Shimp,<sup>18</sup> reprinted with permission.)

supplied as a prepolymer partially polymerized in hydrocarbon solvents such as toluene or mesitylene (20 to 70 percent solids). BCB resins have low dielectric constant, low water absorption, good thermal stability, high adhesion, and good planarization and chemical resistance. Properties of several BCB resins are listed in Table 2.23.<sup>19</sup> Suppliers include Dow Chemical.

TABLE 2.23 Typical Properties of BCB-Based Resins

Property	
Glass transition temperature (°C)	>350
Tensile modulus (GPa)	2.9
Tensile strength (MPa)	87
Coefficient of thermal expansion, 25 to 175°C, (ppm/°C)	40–60
Dielectric constant	2.5 (1 GHz)
Dissipation factor	0.0008 (1 MHz); 0.002 (10 GHz)

SOURCE: So et al.<sup>19</sup>

## 2.5 Elastomers

Elastomers are considered apart from other polymeric materials because of their special properties.<sup>8,20</sup> The distinguishing characteristics of elastomers are their ability of sustain large deformations (5 to 10 times the unstretched dimensions) and their capacity to spontaneously recover nearly all of that deformation without rupturing. The unique structural feature of all rubber-like substances is the presence of long polymer chains interwoven and joined together through cross-linkages. Generally, elastomers are not as widely used as plastics for electronics applications, and only a brief review of elastomer types, properties, and their applications will be presented here. A compilation of electrical property information on thermoplastics, thermosets, and elastomers is given in Ku.<sup>21</sup> For a detailed listing of the properties, the reader is referred to Kaplan<sup>5</sup> and Ohm.<sup>22</sup>

### 2.5.1 Properties

Elastomers are almost always used in the compounded state. The neat material is blended with a variety of additives to cure and enhance the properties of the elastomer.

**2.5.1.1 Aging.** Elastomers are affected by the environment more than other polymers. Thermal aging of the elastomer increases stiffness and hardness and decreases elongation. Radiation has a similar effect. Elastomers are sensitive to oxidation and in particular to the effects of ozone. Ultraviolet radiation acts similarly to ionizing radiation, so some elastomers do not weather well. Environmental effects are especially noted on highly stressed parts, and some elastomers are particularly affected by hydrolysis.

**2.5.1.2 Creep.** Creep with regard to elastomers refers to a change in strain when stress is held constant. Special terms are used for elastomers. Compres-

sion set (ASTM D-395)<sup>23</sup> is creep that occurs when the elastomer has been held at either constant strain or constant stress in compression. Constant strain is most common and is recorded as a percentage of permanent creep divided by original strain. Strain of 25 percent is common. Permanent set is deformation remaining after a stress is released.

**2.5.1.3 Hardness.** The hardness of elastomers is a measure of the resistance to deformation measured by pressing an instrument into the elastomer surface. Special instruments have been developed, the most common being the Shore durometer. Figure 2.10 shows the hardness of elastomers and plastics.

**2.5.1.4 Hysteresis.** Hysteresis is energy loss per loading cycle. This mechanical loss of energy is converted into heat in elastomers and is caused by internal friction of the molecular chains moving against each other. The effect causes a heat buildup in the elastomer, increasing its temperature, changing its properties, and aging it. A similar electrical effect can occur at high frequencies when the dissipation factor of the elastomer is high.

**2.5.1.5 Low-temperature properties.** As temperatures are decreased, elastomers tend to become stiffer and harder. Each material exhibits a stiffening range and a brittle point at the glass transition temperature. These effects are usually time-dependent.

**2.5.1.6 Tear resistance.** This is a measure of the stress needed to continue rupturing a sheet elastomer after an initiating cut or notch. Elastomers vary widely in their ability to withstand tearing.

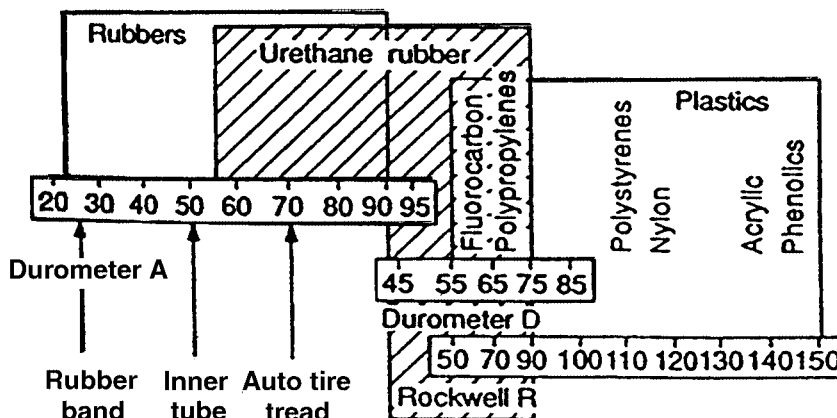


Figure 2.10 Hardness of rubber and plastics. (From Harper.<sup>8</sup>)

**2.5.1.7 Tensile strength, elongation, and modulus.** In tension, metals behave in accordance with Hooke's law, and in strain, they react linearly to the yield point. Polymers and plastics (unreinforced) deviate somewhat from linearity (logarithmically). Special tensile tests are used for elastomers per ASTM D-412.<sup>24</sup> Elastomers are not generally designed for tensile service, but many other physical properties of the elastomers correlate with tensile strength.

## 2.5.2 Types of elastomers

A large number of chemically different elastomers exist. ASTM D-1418<sup>25</sup> describes many of these. Tables 2.24 and 2.25 list elastomers and their properties.

*Natural rubber* (NR) is still used in many applications. It is not one uniform product but varies with the nature of the plant producing the sap, the weather, the locale, the care in producing the elastomer, and many other factors. A variant of NR, *guttapercha*, was used in most of the early electrical products, especially cable. It has excellent electrical properties (as shown in Table 2.25), low creep, and high tear strength. On aging it reverts to the gum.

*Isoprene rubber* (IR) is similar in chemistry to NR but it is produced synthetically. Polyisoprene constitutes 97 percent of its composition. It is more consistent and much easier to process than NR.

*Acrylic elastomer* (ABR) has a heat resistance that is almost as good as that of fluorinated compounds and silicones. It also ages well but is sensitive to water. Its chief use is in contact with oils.

*Butadiene elastomer* (BR) is used to copolymerize with SBR and NR in tire stocks.

*Epichlorohydrin elastomer* (CO, ECO) are flame-retardant because of the presence of chlorine. Their electrical properties are modest, but they age well and resist most chemicals. Dissipation factors are high.

*Carboxylic elastomer* (COX) has good low-temperature performance, excellent weather resistance, and extremely good wear resistance. Electrical properties are average.

*Neoprene* (CR) (chloroprene) was the first synthetic elastomer and is widely used in industry. It is nonflammable and resists ozone, weather, chemicals, and radiation. However, it is highly polar and has a high dissipation factor and dielectric constant.

*Chlorosulfonated polyethylene* (CSM) is similar to CR, with some improvement in electrical properties and better heat resistance. It is available in colors and often used in high-voltage applications.

*Ethylene-propylene terpolymer* (EPDM) is synthesized from ethylene, propylene, and a third monomer, a diene. The diene permits conventional sulfur vulcanization. The elastomer is exceptionally resistant to radiation and heat. The glass transition temperature is  $-60^{\circ}\text{C}$ , and electrical properties are good.

*Ethylene-propylene copolymer* (EPM), which was often used as a wire insulation, is being replaced by EPDM, because its processing qualities are somewhat inferior to those of EPDM.



TABLE 2.24 Chemical Description of Elastomers

ASTM D-1418	Chemical type	Properties
NR	Natural rubber polyisoprene	Excellent physical properties
IR	Polyisoprene synthetic	Same as NR, but more consistency and better water resistance
ABR	Arylate butadiene	Mechanical elastomer; excellent heat and ozone resistance
BR	Polybutadiene	Copolymerizes with NR and SBR; abrasion resistance
CO	Epichlorohydrin	Chemical resistance
COX	Butadiene-acrylonitrile	Used with NBR to improve low-temperature performance
CR	Chloroprene, neoprene	Withstands weathering, flame-retardant, chemical resistance
CSM	Chlorosulfonated polyethylene	Colors available, weathering and chemical resistance, poor electrical properties
EPDM	Ethylene-propylene terpolymer	Similar to EPM, good electrical properties, resists water and steam
EPM	Ethylene-propylene copolymer	Similar to EPDM, good heat resistance, wire insulation
FPM	Fluorinated copolymers	Outstanding heat and chemical resistance
IIR	Isobutyleneisoprene, butyl	Outstanding weather resistance, low physical properties, track resistance
NBR	Butadiene-acrylonitrile, nitrile, Buna N	General-purpose elastomer, poor electrical properties
PVC/NBR	Polyvinyl chloride and NBR	Colors available, weather, chemical, and ozone resistance
SBR	Styrene: butadiene, GRS, Buna S	General-purpose elastomer, good physical properties, poor oil and weather resistance
SI (FSI, PS1, VS1, PVS1)	Silicone copolymers	Outstanding at high and low temperatures, arc- and track-resistance, resist weather and ozone, excellent electrical properties, poor physical properties
T	Polysulfide	Excellent weather resistance and solvent resistance
U	Polyurethane	High physical and electrical properties

SOURCE: From Harper.<sup>8</sup> Reprinted with permission.

*Fluorinated elastomers* (FPM) include several types—fluorocarbons, fluoro-silicones, and fluoroalkoxy phosphazenes. The elastomers can be used to 315°C, do not burn, are unaffected by most chemicals, and have excellent electrical properties. In thermal stability and aging, only the silicones are better. Physical property qualities are high, but so is the cost.

TABLE 2.25 Electrical Properties of Elastomers

ASTM elastomer	Dielectric strength, V/mil	Dissipation factor $\tan \delta$	Dielectric constant	Volume resistivity, $\Omega$ -cm
COX	500	0.05	10	$10^{15}$
CR	700	0.03	8	$10^{11}$
CSM	700	0.07	8	$10^{14}$
EPDM	800	0.007	3.5	$10^{16}$
FPM	700	0.04	18	$10^{13}$
IIR	600	0.003	2.4	$10^{17}$
MR	800	0.0025	3	$10^{16}$
SBR	800	0.003	3.5	$10^{15}$
SI	700	0.001	3.6	$10^{15}$
T	700	0.005	9.5	$10^{12}$
U	500	0.03	5	$10^{12}$

SOURCE: From Harper.<sup>8</sup> Reprinted with permission.

*Butyl rubber* (IIR) is highly impermeable to water vapor. Its nonpolar nature gives it good electrical properties. Compounded with aluminum oxide trihydrate, it has exceptional arc and track resistance. Butyl has good aging characteristics and good flexibility at low temperatures.

*Nitrile rubber* (NBR) is resistant to most chemicals, but its polarity gives it poor electrical properties, so its major use is in mechanical applications.

*Polyvinyl chloride copolymers* (PVC/NBR) are similar to NBR. They can be colored and are used in wire and cable jackets.

*GRS* (SBR) stands for “government rubber, styrene,” a nomenclature derived during World War II when natural rubber was not available in the West. It is used in mechanical applications.

*Silicone elastomers* (SI), which are composed of silicon and oxygen atom backbones, have the highest temperature ability (315°C), a wide temperature range (–100 to 600°F), and excellent electrical properties. They do not burn and are arc resistant. Physical properties are modest.

*Polysulfides* (T) weather best of all and are highly chemical resistant. Dissipation factors are excellent (as low as 0.001); physical properties are modest.

*Polyurethanes* (U) are either ester- or ether-based. Ester-based elastomers are poor in water resistance. They are excellent in electrical applications, with outstanding physical properties. Abrasion resistance is particularly high. They become stiff at low temperatures. They can be compounded like regular elastomers, used as cast elastomers, or injection molded like thermoplastics.

### 2.5.3 Thermoplastic elastomers (TPEs)

These materials have the functional requirements of elastomers (extensibility and rapid retraction) and the processability of thermoplastics. The principal advantages of the TPEs as compared to vulcanized rubber are (1) reduction in compounding requirements, (2) easier and more efficient processing cycles, (3) scrap recycling, and (4) availability of thermoplastic processing methods. There are six generic classes of TPEs: styrenic block copolymers, polyolefin blends (TPO), elastomeric alloys, thermoplastic polyurethanes (TPU), thermoplastic copolyesters, and thermoplastic polyamides. TPEs are processed almost exclusively by extrusion and injection molding but can be blow molded, thermoformed, and heat welded. None of these methods is available to thermoset-type elastomers. Additional information can be obtained from Kaplan<sup>5</sup> and Bhowmick and Stephens.<sup>20</sup>

## 2.6 Applications

This section describes how polymers are processed and used in a variety of forms in electrical and electronic applications. The fundamental differences among the classes of polymers, namely, thermoplastics, thermosets, and elastomers, dictate the processing method to be used. Furthermore, within each class, the differences in the thermal and melt properties of the polymers also dictate what processing methods are best suited for a given material. This section is designed to acquaint the reader with some basic information about polymer processing. The reader is directed to the references for a more detailed description of each of the processing methods.<sup>4-6</sup> It is recommended that the plastics suppliers be used as a resource for guidance in both design and processing of polymers. The process sequence for all polymers involves heating the polymer to soften it, forcing the softened polymer into a mold or through a die to shape it, and then cooling or curing the molten polymer into its final shape. While polymers are not necessarily all solids (some are liquids), heating facilitates their processing.

### 2.6.1 Laminates

Most printed wiring boards (PWBs) are fabricated from reinforced thermosetting resins, although thermoplastics may be used in special applications. Laminates are prepared by impregnating a woven reinforcement material with a liquid resin, which is usually dissolved in a solvent. The impregnated fabric is heated to drive off the solvent and advance the cure of the resin slightly to the “B stage” so that the material is stiff at room temperature and easily handled. At this point, the composite material is referred to as a “prepreg.” A PWB is fabricated by stacking several layers of prepreg and laminating with heat and pressure to reflow the resin and bring about full cure. Before laminating, a prepreg may be bonded with copper on one or both sides so as to create a conductive layer or conductive traces in the finished PWB. Considerable effort is given to ensure good compatibility between the resin and reinforcement material to avoid delamination, microcracks, voids, and

other defects in the finish composite. Resin and reinforcement materials must be chosen carefully for each application. PWB materials are chosen for a given application based on requirements for thermal expansion, dielectric constant and loss, and thermal stability. Table 2.26 gives some key properties of various classes of PWB materials.

For selected applications, PWBs based on high-performance thermoplastics may be chosen. In particular, PWBs based on fluoropolymers and liquid crystal polymers are attractive for high-frequency applications because of their low dielectric constant and low loss, which are important in microwave applications. In many cases, these materials can be processed in the same manner as the thermosetting laminates, because they incorporate a fluoropolymer fabric reinforcement in a low-loss thermosetting material. In other cases, they are essentially filled thermoplastics, so they are processed like a thermoplastic by, for example, injection molding.

A processing method related to laminating is filament winding, used for preparing cylindrical or rounded shapes. Continuous filaments are wrapped around a mandrel then impregnated with a resin and cured. Removing them from the mandrel leaves the cured piece. Tubes and cylindrical vessels are fabricated using this technique.

## 2.6.2 Molding and extrusion

These processing methods are discussed together because, in many cases, the techniques are combined. In extrusion, powdered or pelletized material is fed into a machine that contains a screw in a heated barrel, which may melt, mix, and devolatilize the mixture while pushing it through a die. Extrusion may also be used to compound a formulation and pelletize it for subsequent molding or extrusion into its final shape. Details on molding and extrusion are available in other texts.<sup>27,28</sup>

Hollow parts can be fabricated by blow molding, rotational molding, or slush molding. In *blow molding*, an extruded thermoplastic tube is placed in a mold while still hot from the extruder and expanded into the mold with gas pressure. The mold is opened and the part ejected. *Slush molding* starts with a thermosetting molding powder, which is poured into a heated mold. Before the material is completely polymerized, the mold is opened and uncured material removed from the center of the piece. The part is then removed and taken to full cure in an oven. In *rotational molding*, the inside of the mold is coated by rotating it, and unreacted or excess material is removed after a sufficient thickness builds up on the inside surface of the mold.

Solid parts can be fabricated by compression molding, injection molding, and transfer molding. Many microelectronic packages are made by one of these molding processes. In *compression molding*, a thermoplastic or B-staged thermosetting powder is subjected to heat and pressure in a mold. The material flows, and heat cures the part, or the mold is cooled sufficiently that the part can be removed from the mold. A related process is *injection molding*, in which the raw material (either thermoplastic or thermoset powder) is heated to a softening point then forced into a mold, solidified rapidly, and then ejected

**TABLE 2.26 Properties of Selected PWB Laminate Materials**

Laminate	$T_g$ (°C)	CTE below $T_g$ (ppm/°C)		Water uptake MIL-P-13949F	Dielectric constant (@ 1MHz) z	Dissipation factor (@ 1MHz) z	Tensile strength (MPa) x, y	Modulus of elasticity (GPa) x, y	Thermal conductivity (W/m°C) z
		x, y	z						
E-glass/epoxy	120	12–16	60–80	10	4.7	0.021	276	17.4	0.35
E-glass/polyimide	220–300	11–14	60–80	25	4.5	0.018	345	19.6	0.35
E-glass/PTFE	75	24	261	—	2.3	0.006	68–103	1.0	0.26
Quartz/polyimide	260	6–12	34	25	3.6	0.010	—	27.6	0.13
Quartz/Quartrex	185	—	62	—	3.5	—	—	18.6	—
Kevlar-49/Quatrex	185	3–8	105	10	3.7	0.030	—	22–28	0.16
Kevlar-49/polyimide	180–200	3–8	83	25	3.6	0.008	—	20–27	0.12

SOURCE: Pecht, et al.<sup>26</sup>

from the mold. In the related process of *reaction injection molding*, liquid components of a thermosetting formulation are pumped through a mixing head into the mold and cured in the mold. *Transfer molding* is a similar process in which a thermosetting material is softened in a transfer chamber then forced into a mold, cured, and ejected. While in the transfer chamber or the mold, the chamber may be evacuated to reduce void content of the molded part.

### 2.6.3 Casting and potting

Low-volume production can be accomplished by casting liquid thermosets into a mold and curing. Many electrical assemblies include a potting step in which a thermoset material is cast around a component, connector pins, or printed wiring boards. Depending on the application, the potting resin may be intended to protect the components from environmental exposure, dirt, moisture, mechanical shock, or vibration. Casting resins include epoxies, polyesters, polyurethanes, silicones, bismaleimides, and cyanate esters. For electrical applications, these materials are typically formulated without solvents to prevent void formation during cure at elevated temperature. Low-viscosity components also help prevent void formation by minimizing trapped air during the casting or potting process. In choosing a casting or potting resin, there are several characteristics to consider in addition to the desired electrical or mechanical properties in the cured material. In particular, stress on the embedded components can be minimized by having a low shrinkage during cure and by having a coefficient of thermal expansion that matches that of the embedded components, and adhesion to the components should be good to minimized cracking and void formation. A general comparison of encapsulating resins is offered in Table 2.27

**TABLE 2.27 A Comparison of Encapsulating Resins**

Resin	Dielectric properties	Overall adhesion	Shrinkage	Maximum-use temp., °C	Coefficient of thermal expansion	Chemical resistance
Epoxy	Excellent	Excellent	Low	150	Moderate	Good
Bismaleimide	Excellent	Good	Moderate	180	Low	Good
Cyanate ester	Excellent	Excellent	Low	175	Low	Excellent
Polyester	Good	Fair	High	175	Moderate	Poor
Silicone	Excellent	Low	Low	200	High	Good
Silicon-carbon (SYCAR)	Excellent	Good	Low	160	Moderate	Excellent

### 2.6.4 Adhesives

Adhesives used in electrical and electronic applications often have special requirements related to electrical or thermomechanical properties. In some ap-

plications, dielectric constant and loss tangent may be important. Often, the adhesive is called on to accommodate the mismatch in thermal expansion between bonded pieces, such as semiconductor and a plastic or ceramic package or between a ceramic package and an organic PWB.

### 2.6.5 Organic coatings

Coatings are applied to a variety of substrates primarily to protect that substrate from deterioration due to the action of outside agents. They give the substrate an extra level of protection against chemical, radiation, thermal, and oxidative attack. A detailed list of all types of organic coatings can be found in Stevens.<sup>11</sup> Although most organic polymers can be used as coatings in one form or another, only polymers that can be converted into formulations for conformal applications are discussed in this section. Conformal coatings are generally liquid resin formulations used in the protection of assembled printed-wiring boards from a variety of environmental effects. These resins conform to the topography of the board and the components thereon and are cured to form a relatively thin (1 to 10 mil) protective coating. The main function of the coating is to provide a moisture barrier for circuit traces and components, but secondary benefits are provided as protection against dust, other contaminants, chemicals, and abrasion, and some degree of shock and vibration. No coating will totally resist the effects of environmental stresses, and so these coatings do have a finite time of protection and are designed to operate under the requirements of the system in which they are used. Humidity and process contaminants can lead to serious degradation of electrical components, causing lower insulation resistance between conductors, premature high-voltage breakdown, corrosion of conductors, and even short circuits. As a result, the chosen coating material must have an excellent combination of physical, chemical, and electrical properties in addition to ease of application.

**2.6.5.1 Conformal coating types.** A variety of conformal coating materials are available to meet specific application needs. MIL-I-46058 defines five classes of polymers for conformal coatings. They are acrylics, epoxies, polyurethanes, silicones, and paraxylylene polymers. While not defined in the MIL specifications, other polymer types that could be considered include the polyimides, diallyl phthalate resins, and the benzocyclobutenes. The properties of these materials are shown in Table 2.28. These coatings can be solvent based, water based, or solventless systems. They can be applied as liquids, solids (powder), or film (vapor deposition), and the coatings can be cured either thermally or with radiation. They can be applied by brushing, spraying, dipping, or flow coating. A relative coating selection chart is given in Table 2.29.

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TABLE 2.28 Typical Characteristics of Various Coating Materials

Properties	Acrylic	Urethane	Epoxy	Silicone	Polyimide	DAP
Volume resistivity (50% RH, 23°C), Ω-cm	10 <sup>15</sup>	11 × 10 <sup>14</sup>	10 <sup>12</sup> × 10 <sup>17</sup>	2 × 10 <sup>16</sup>	10 <sup>16</sup>	1.8 × 10 <sup>16</sup>
Dielectric constant						
60 Hz	3–4	5.4–7.6	3.5–5.0	2.7–3.1	3.4	3.6
1 kHz	2.5–3.5	5.5–7.6	3.5–4.5		3.4	3.6
1 MHz	2.5–3.5	4.2–5.1	3.3–4.0	2.6–2.7	3.4	3.4
Dissipation (power) factor						
60 Hz	0.02–0.04	0.015–0.048	0.002–0.010	0.007–0.001	—	0.010
1 kHz	0.02–0.04	0.04–0.060	0.002–0.02	—	0.002	0.009
1 MHz	2.5–3.5	0.05–0.07	0.030–0.050	0.001–0.002	0.005	0.011
Thermal conductivity, 10 <sup>-4</sup> cal/(s-cm <sup>3</sup> .°C)	3–6	1.7–7.4	4–5	3.5–7.5	—	4–5
Thermal expansion, 10 <sup>-3</sup> /°C	5–9	10–20	4.5–6.5	6–9	4.0–5.0	—
Resistance to heat, continuous, °F	250	250	250	400	500	350
Effect of weak acids	None	Slight to dissolve	None	Little or none	Resistant	None
Effect of weak alkalis	None	Slight to dissolve	None	Little or none	Slow attack	None
Effect of organic solvents	Attacked by ketones, aromatics, and chlorinated hydrocarbons	Resists most	Generally resistant	Attacked by some	Very resistant	Resistant

SOURCE: From Coombs.<sup>29</sup> Reprinted with permission.

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TABLE 2.29 Coating Selection Chart\*

	Acrylic	Urethane	Epoxy	Silicone	Polyimide	DAP
Application	A	B	C	C	C	C
Removal (chemically)	A	B	—	C	—	—
Removal (burn through)	A	B	C	—	—	—
Abrasion resistance	C	B	A	B	A	B
Mechanical strength	C	B	A	B	B	B
Temperature resistance	D	D	D	B	A	C
Humidity resistance	A	A	B	A	A	A
Humidity resistance (extended period)	B	A	C	B	A	A
Pot life	A	B	D	D	C	C
Optimum cure	A	B	B	C	C	C
Room-temperature curing	A	B	B	C	—	—
Elevated-temperature curing	A	B	B	C	C	C

\*Property ratings (A–D) are in descending order, A being optimum.

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# Ceramics and Glasses

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## 3.1 Introduction

Ceramics and glasses are among the enabling technologies in nearly all electronics markets. Electronic data transmission with low signal attenuation is quite common using low-permittivity ceramics or glass matrix media in digital or analog modes throughout the radio and microwave frequency ranges. High-quality glass fibers have enabled high-volume data transmission at optical frequencies over long distances with minimal distortion of the original signal. Today, most long-distance telecommunication occurs through optical fibers in which data is transmitted via light through a glass fiber rather than electrons through a metal wire.

High-permittivity, electrically insulating ceramics are the necessary ingredient for the largest market segment of energy-storing capacitors. High-permittivity ceramics, which undergo a lattice distortion with applied field or output an electrical signal when stressed, are under active element for sonar technology and sonic imaging in medical applications. The development of processing techniques to form optically transparent, high-permittivity ceramics whose index of refraction can be modified by an applied electric field allows the creation of devices that are capable of modulating optical signals.

Applications for ferrite ceramics have expanded with the rapid growth of the electronics industry, and they include inductors, transformers, permanent magnets, magneto-optical devices, electromechanical devices, and microwave electronics devices. Superconducting ceramics, which allow conduction at virtually zero resistance, provide the opportunity to eliminate energy dissipation in power lines and generation of large magnetic fields for unique medical applications and zero-friction magnetic levitation devices and transportation systems.

## 3.2 Chapter 3

## 3.2 Ceramic Interconnections for Microelectronics

Ceramic interconnect technology offers significant benefits in terms of design flexibility, density, and reliability. These advantages, inherent in the ceramic materials themselves, often make this material the preferred alternative for high-density, high-reliability applications. Ceramic packaging can be categorized as thin film, thick film, or multilayer.

Table 3.1a shows a comparison of various ceramic substrate materials. If one were to design the ultimate substrate material, a thermal expansion matched to that of the semiconductor chips (3.5 ppm/°C for Si, 7.5 ppm/°C for GaAs) would be desirable to improve reliability, particularly as chip sizes continue to grow. Low dielectric loss is desirable, because it has a direct impact on the transmission losses of the thin or thick film circuits. Typically, high ther-

**TABLE 3.1a Electrical and Thermal Properties of Various Electronic Materials**

	Electrical resistivity ( $\Omega$ -cm)	Thermal conductivity (W/m-K)
<i>Conductors</i>		
Copper	$1.7 \times 10^{-6}$	395
Gold	$2.3 \times 10^{-6}$	298
Molybdenum	$5.2 \times 10^{-6}$	138
Tungsten	$5.5 \times 10^{-6}$	174
Platinum	$10.5 \times 10^{-6}$	72
Palladium	$11 \times 10^{-6}$	72
<i>Semiconductors (pure)</i>		
Silicon	$>10^2$	118
Germanium	40	60
Silicon carbide (SiC)	10	270
<i>Insulators</i>		
Low-voltage porcelain	$10^{12} \times 10^{-14}$	2–4
SiO <sub>2</sub> glass	$>10^{14}$	2
Al <sub>2</sub> O <sub>3</sub>	$>10^{15}$	25
Soda-lime-silica glass	$10^5$	2–3
Aluminum nitride (AlN)	$>10^{15}$	230
Diamond	$>10^{15}$	2000

mal conductivity is desired, particularly in power devices, to conduct heat away from the chips. Thermal management is a key element in the mechanical design of today's advanced electronics. The trend to high circuit densities within ICs and packaging leads to higher heat densities. Component failure rates increase exponentially as temperature is increased. High mechanical strength is desirable for mechanical stability and reliability. Low-density materials are typically desired for lightweight systems. The desired dielectric constant may vary, depending on the application. A lower dielectric constant generally allows closer spacing of signal lines and higher transmission speeds. In some devices, such as resonators or filters, higher dielectric constants result in reduced feature dimensions.

The speed of data transmission in semiconductor devices has been the focal point of development; however, the levels of packaging materials through which the signals must eventually pass have not kept pace, and packaging has become one of the limiting factor in the transmission speed of microelectronic devices. The transmission time delay is related to the dielectric constant of the packaging material by

$$\tau_d = K^{1/2} l/c \quad (3.1)$$

where  $l$  = length of the circuit

$c$  = speed of light

$K$  = dielectric constant of the transmission media

Therefore, it is desirable to design in low-dielectric constant media, such as that of the silicates. For instance, silica with a relative permittivity of  $\approx 4$  would yield a transmission delay about twice that of pure vacuum ( $\epsilon_r = 1$ ), whereas alumina with a relative permittivity of  $\approx 10$  would yield about three times the delay.

### 3.2.1 Thin film

Thin film metallization on ceramic substrates was developed to take advantage of high circuit density and tight dimensional tolerances of deposited and etched metals and the high thermal conduction and mechanical stability of ceramic substrates. Typically, the substrate used is high-purity alumina (99.5 to 99.6 percent), polished to a fine surface finish and good flatness. However, thin film circuitry has been used on a wide variety of ceramics, including glasses, multilayer ceramics, and magnetic ceramics, as a method of forming surface features with tight dimensional control and fine line resolution ( $\approx 0.5$ - to 1-mil lines and spaces). Standard grain size for the 99.5 percent alumina is about 2 to 2.5  $\mu\text{m}$ , yielding a surface finish of  $<0.15 \mu\text{m}$  ( $<6 \mu\text{in}$ ). The more expensive 99.6 percent alumina substrates are used in applications for very fine line depositions, because they are generally more defect free and have a finer surface finish. Thin film metallization is applied to a suitable substrate by a variety of deposition methods such as evaporation, sputtering, plating, and chemical vapor deposition (CVD). The metallization is generally deposited

## 3.4 Chapter 3

over the entire substrate surface and then photoimaged and etched to produce the desired circuit pattern.

All of the desirable high-conductivity metallizations, Au, Cu, Ag, Al, can be deposited as thin films. Additionally, thin film resistors of materials such as tantalum nitride ( $\text{Ta}_2\text{N}$  or  $\text{Ta}_2\text{N}_3$ ) and nickel chrome (NiCr) are used. Materials such as silicon oxides or nitrides have been deposited to serve as passivation and capacitor dielectrics. The evaporation method is a vacuum deposition process whereby a source metal is heated to its vaporization temperature under high vacuum ( $10^{-5}$  to  $10^{-6}$  torr). Figure 3.1 shows the schematic for a typical vacuum evaporator. Sputtering involves bombardment of a metal target with an ion plasma. The metal target is used as the cathode, and the substrate to

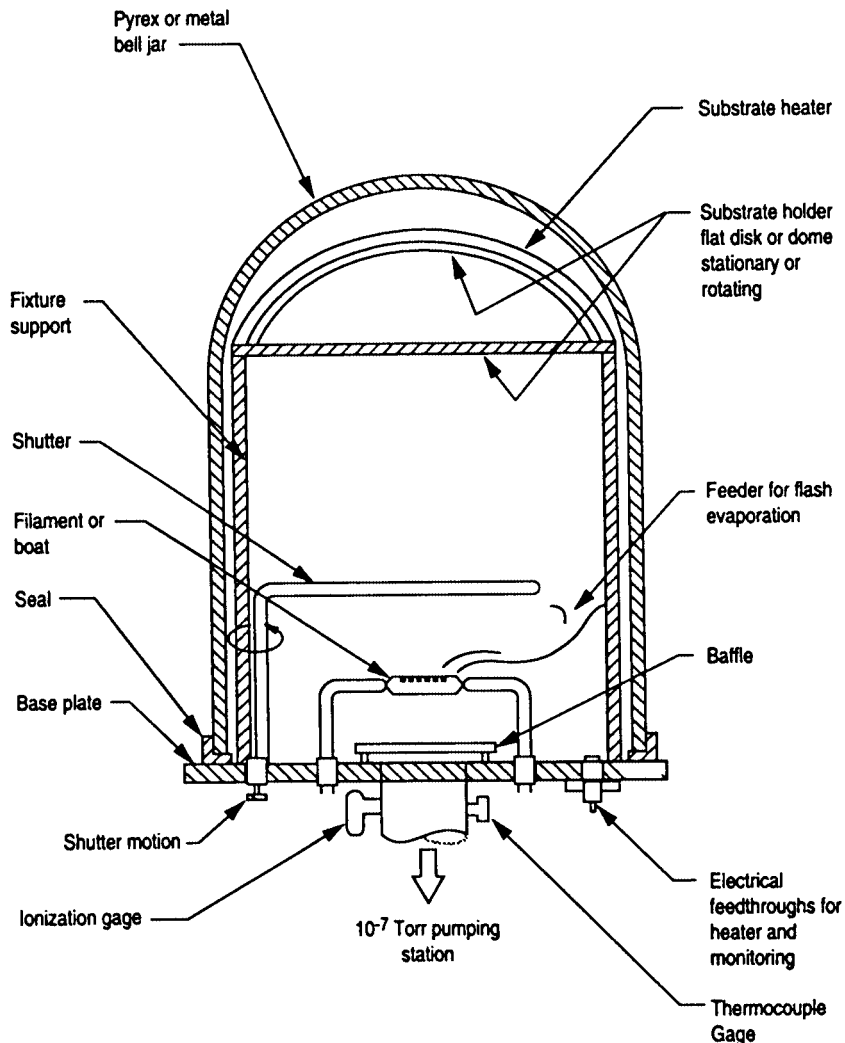


Figure 3.1 Schematic for vacuum evaporator.<sup>12</sup>

be plated is the anode. When a high electric field is applied between the electrodes in an evacuated chamber, argon purge gas is ionized. The  $\text{Ar}^+$  ion is then accelerated by the electric field into the metal cathode. The high-energy collisions sputter ions of the target metal, forming a plasma that then deposits on the substrates at the anode. Figure 3.2 shows a schematic of a sputtering system. Because the material is depositing at a high kinetic energy level, the sputtered film is typically better adhered and more dense than evaporated films.

The properties of deposited films are highly dependent on the processing conditions and substrate properties such as surface chemistry and finish. Typically, a thin adhesion layer, such as Cr, Ti, NiCr, or TaN, is first deposited onto the substrate. This is followed by the high-conductivity metallization layer. Sometimes it is necessary to apply a final barrier layer over the metallization to prevent oxidation.

### 3.2.2 Thick film

In its simplest form, thick film technology involves the deposition of metal circuitry on a dense ceramic substrate using screen-printing technology. The metallizations are formulated with glasses and oxides to aid in densification of the metal and adhesion to the substrate at relatively low temperatures (600 to 950°C). The ability to build up multiple layers of circuitry using insulating dielectric layers is a key advantage of this technology. Successive layers are

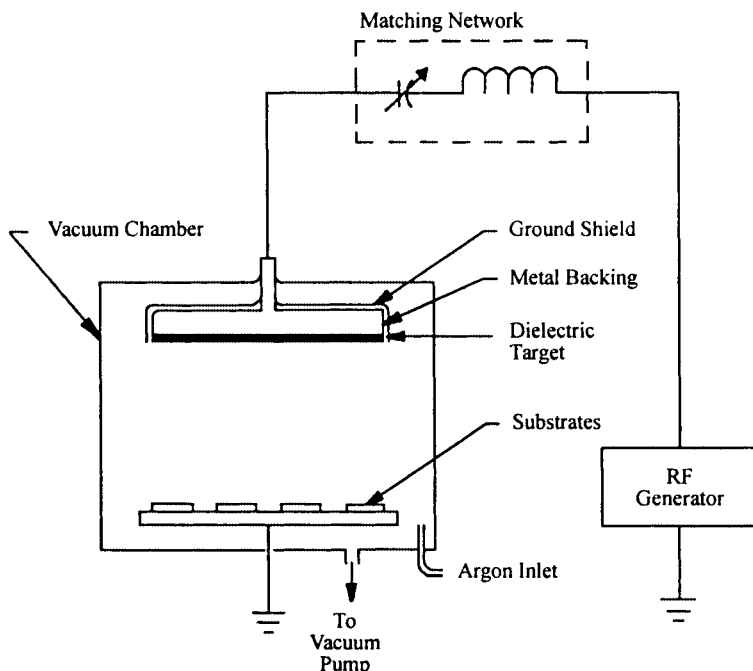


Figure 3.2 Schematic of RF sputtering unit.<sup>12</sup>

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printed, dried, and fired to build up a multilayer structure on a rigid ceramic or metal base. The substrate material is widely varying; thick film metallization is used in nearly all forms of electronic ceramics, including magnetic, electro-optic, and superconductor substrate ceramics. Thick film circuits are often used as hybrid packaging, that is, as a method to interconnect active ICs and passive components such as capacitors, resistors, and inductors. Special pastes for deposition of inductors, capacitors, and resistors have been developed, greatly expanding the capabilities of the technology. Thick film has been in use in various forms since the 1920s and is one of the longest-running commodity markets in the electronics industry.

The metal, dielectric, resistor, and ferrite pastes consist of the organic vehicle, the metal or oxide powders, and a glass frit. The organic vehicle consists of a solvent, dispersants, and a binder system. The binder system is used to hold the fine inorganic particles together and form a temporary bond with the underlying substrate prior to the firing process. The organic binder resin dissolved in solvents and easily decomposed in air or nitrogen atmosphere. The solvents and dispersants are used with the binder and inorganic particles to form a paste form which can be deposited onto substrates using a rubber squeegee. Glass frit and/or bismuth or copper oxides are added to promote adhesion to the substrate. Typically, the frit consists of high lead or bismuth glasses are added to conductor paste blends to aid in adhesion. Glasses are chosen with a melting point approximately 200°C lower than the firing temperature of the paste.

Figure 3.3 shows the basis of the thick film process, screen printing. In screen printing, a rubber squeegee is used to force a thick paste through a screen, imaged for the circuit features, onto the substrate material. Typically, stainless steel mesh screens are used. The mesh of the screen is filled with a UV light-curable emulsion. Normally, the emulsion is thicker than the metal mesh, is flush with the mesh on the squeegee surface, and extends beyond the

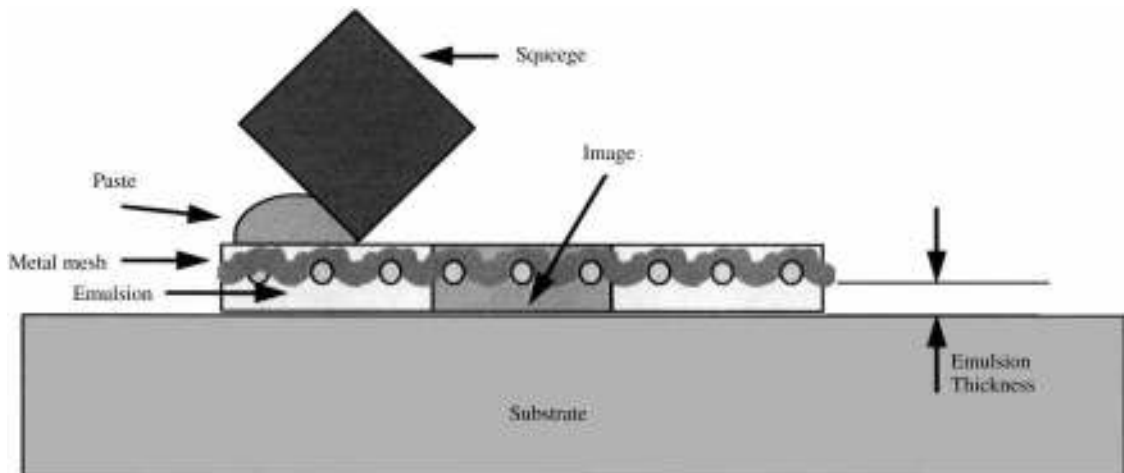


Figure 3.3 Contact printing schematic.



mesh on the substrate side of the screen. Emulsions typically extend beyond the thickness of the wires by several ten-thousandths of an inch. This additional emulsion is used to control print thickness and eliminate the mesh patterns from being transferred to the printed features. The circuit patterns to be printed are imaged into the screen emulsion using positive image artwork on Mylar film or glass plates. Those areas exposed to the UV light are cured. The uncured emulsion is water soluble and is washed away, leaving the open stainless steel mesh through which the thick film pastes will be deposited. Screen parameters such as mesh, emulsion thickness, wire diameter, and mesh angle determine the thickness and quality of the printed circuits. Screen meshes range from 200 to 400 mesh (wires per inch), but 325 mesh is most common. In general, finer wire diameters are desirable, but the fineness is limited by the tensile strength of stainless steel; 0.0006- to 0.002-in wires are used. Equipment parameters such as squeegee pressure, speed, and angle; snap-off; and down-stop also affect print quality. Also, material parameters such as paste rheology and control and substrate surface finish, porosity, and flatness affect print quality and variability.

Typically, two prints are used for each dielectric layer to avoid pinholes that would result in shorts between layers. The two dielectric layers are applied in print-dry-fire-print-dry-fire or print-dry-print-dry-fire fashion. As shown in Fig. 3.4, openings of  $\approx 10$  mils are designed into the dielectric layers to be filled with conductive pastes on subsequent processing. These metallized “vias” serve as the interconnect between the layers of circuitry. As increasing numbers of layers are applied, the substrate surface becomes less planar. Non-planar surfaces can result in difficulties in automated assembly of components to the package. This limits the number of circuit layers that can be applied using thick film technology to approximately seven or eight layers. The screen-printing operation limits the resolution of thick film circuitry to approximately 4-mil lines and spaces in volume production, and 6- and 8-mil lines are more common. Other technologies are being developed to expand the capabilities of thick film. Direct writing machines such as the Micropen can print circuitry through a dispensing nozzle. This system is capable of writing 3- to 4-mil lines with fine spaces (1 to 2 mil) over nonplanar surfaces and in cavities. Photoimageable and etchable thick film systems have been developed to improve the circuit resolution of thick film. DuPont’s Fodel and Hereaus’ KQ systems are examples. Some systems involve polymerization of the pastes by exposure to a UV light through a photonegative mask. The paste containing uncured polymer is washed away. This process of photo-imaging results in finer circuit features such as via diameters down to 100  $\mu\text{m}$ . This allows for more densely packed circuitry. Etchable thick film metallizations have also been developed. The substrate is covered with a thick film layer of fired gold rather than deposited metal as in thin film processes. This metal can then be processed through subsequent thin film photoresist and etching processes to form fine-resolution circuits that are compatible with subsequent thick film printing and firing processes.

One of the key advantages of thick film is the use of high-conductivity metallizations such as Au-, Ag-, and Cu-based systems, as shown in Table 3.1b.

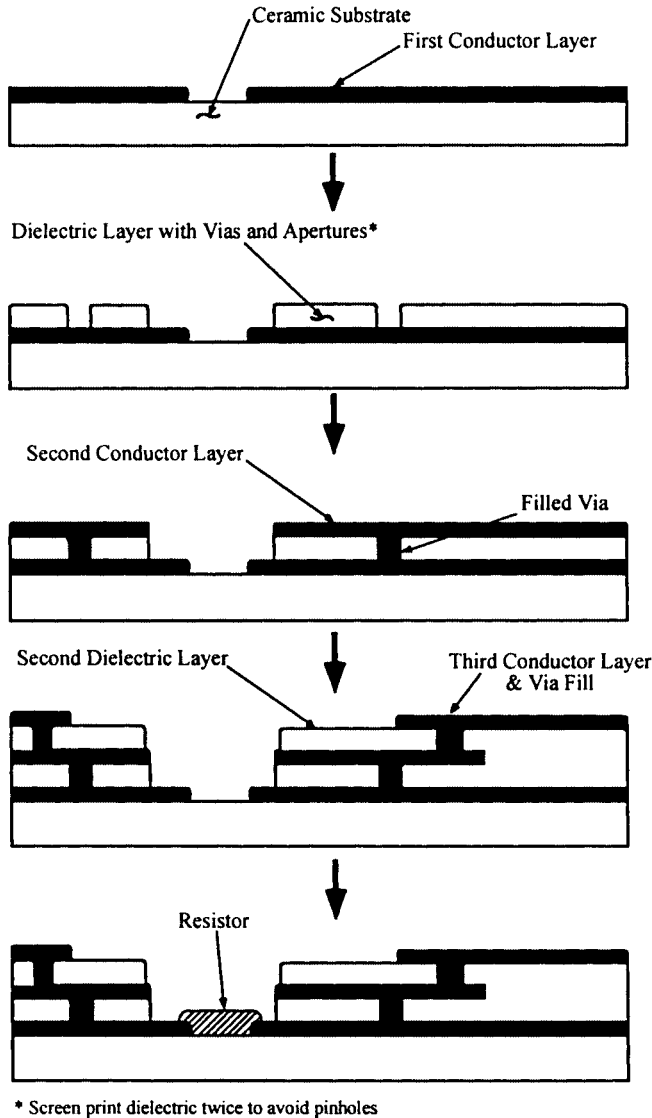


Figure 3.4 Thick film multilayer fabrication steps.<sup>12</sup>

The choice of metal systems is based on cost, package assembly, and performance requirements. Thick film may be Au and Al wire bondable, low-temperature solderable, or high-temperature brazable. Gold is often used for its noble metal properties; that is, its inertness to oxidation, migration, and chemical reaction. Gold circuits have excellent thermocompression bonding and high-temperature brazing (with Au-Sn, Au-Ge) properties but are not well suited for soldering because of poor leach resistance. Adding Pt and Pd to Au forms solid solutions that are more leach resistant but less conductive. The need for lower cost drove the development of Ag- and Cu-based conductors. Silver (1.5

TABLE 3.1b Properties of Dielectric Insulators

Material	Thermal expansion (ppm/°C)	Dielectric constant	Dielectric loss	Thermal conductivity (W/m-K)	Flexural strength (MPa)	Density (g/cc)
96%	7.4–8.2	9.5	0.0004	26	400	3.75
99.5% Al <sub>2</sub> O <sub>3</sub>	7.5–8.3	9.9	0.0002	35	552	3.90
Mullite	3.7–5.3	5.4–6.8	0.003	4–6.7	186	2.82–3.1
AlN	4.3–4.6	8.6–10.0	0.0002–0.001	140–220	207–345	3.25–3.30
BeO	7.5–8.8	6.5–6.7	0.0003	260	207	2.85
Steatite	4.2–7.2	5.7	0.00070.001	2.5	170–200	2.7
Fosterite	9.8–10.7	6.2	0.0002–0.0005	3.3–4.6	170–210	2.9–3.22
Spinel	7.0–8.8	6.6–8.3		7.6–15	200	3.6
Cordierite	1.4–2.5	4.5–5.7	0.004–0.008	2.5	120–245	2.0–2.53
Cristobalite	3.8	50.0				2.27–2.32
Porcelain	5.0	6.5		21–43	150–1200	3–3.18
SiC	3.1–4.7	40		36–270	230–860	3.2
a-quartz	11.2	3.8		2.0	180	2.2
BN	3.8	4.1		60 (cubic)– 1300 (hex)	110–150	2.2
Diamond	1.1	5.5		2000	1400	3.5
Lead-borosilicate glass	7.0	7.0	0.004	2.5	320	3.1
Borosilicate glass	3.1	4.1	0.0006	2.0	150	2.3
Fused quartz	0.5	3.8	0.0004	1.6	80	2.2

to 3 mΩ/□) and Cu (2 to 4 mΩ/□) have better conductivity than Au (3 to 5 mΩ/□) and are dramatically lower in cost, but they are prone to oxidation during firing. Silver also has problems with migration, especially in humid conditions. Alloying silver with palladium helps to reduce Ag migration. Copper has excellent stability and solderability but must be fired in an inert atmosphere to avoid oxidation. The metal powders are typically of spherical morphology. Flake-shaped particles are sometimes used for improving particle contact.

### 3.2.3 Multilayer packaging

The multilayer ceramic technology allows multiple circuitry's to be handled in a single, self-contained, hermetic package. Structures incorporating buried

components allow increased design flexibility by providing a mechanism for establishing both stripline and microstrip within the same medium. The ability to integrate digital, analog, RF, microwave, and buried passive components in this manner reduces assembly complexity and improves overall component and system reliability by reducing part count and interconnections.

The multilayer systems use low-dielectric-constant materials similar to traditional ceramic substrates for dielectric layers and an internal circuit metallization that is designed to be cofired with the ceramic dielectric. Cofiring of metallization with a ceramic dielectric required development of compatible systems that would have matching shrinkage onsets, shrinkage rates, and total volumetric shrinkage. Because the metal thermal expansions are considerably higher than that of the ceramic matrix, the metal must be compliant or have additives to make its thermal expansion more closely match that of the ceramic. Additionally, the thick film pastes must be formulated with solvents and binder systems that are compatible with that of the ceramic green tape. Additives to the metallization, in the form of glass frits or oxide bonding agents, are used to promote adhesion of the metal to the ceramic. Because these additives increase the resistivity of the metallization, the amount that can be employed is limited.

### 3.2.4 High-temperature cofired ceramics

The most common multilayer packaging technology to evolve uses alumina based material (90 to 94 percent) with silica and alkaline fluxes, such as MgO and CaO, added as sintering aids. The small amount of glass that forms is needed to improve the densification behavior of the dielectric and achieve better adhesion to the metallization. HTCC was first developed by IBM for use in mainframe computers. In the early 1980s, IBM developed a multilayer tape casting process for fabrication of a 33-layer cofired Mo metallization package housing 100 bipolar chips. The relatively high firing temperature of alumina-based ceramics,  $\approx 1600^\circ\text{C}$ , requires the use of more refractory metallizations for cofired internal circuitry. Because these metals possess high electrical resistivities (approximately four times that of gold), the electrical losses are higher than in other ceramic packaging technologies.

Figure 3.5 shows the fabrication process for HTCC packaging. The ceramic powders are dispersed in a solvent mixture with binder and plasticizers. The slurry is cast into thin tape form using a doctor blade process. The thin (0.5 to 10 mil) tape is heated during a continuous casting operation to dry off the solvents, leaving behind a thin flexible ceramic-organic composite. These flexible sheets enable low-cost assembly of very complex packages by forming the three-dimensional structure in the green state.

The thin sheets are cut to standard processing sizes. The circuit connections between layers (vias) are formed using programmable pneumatic punches or hard dies. These vias are filled with conductive metallization using stencils in a screen-printing process. The unique internal circuits are printed on the individual tape layers. Three-dimensional cavity patterns are formed by cutting the patterns in individual layers using punches, cutting dies, routing, and la-

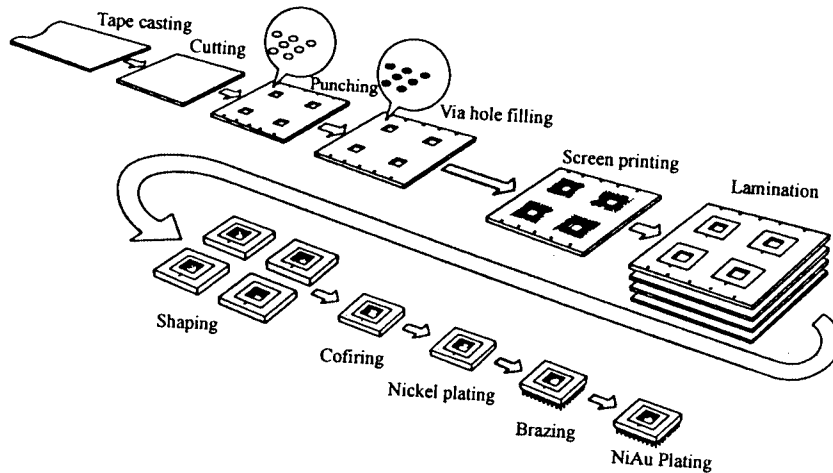


Figure 3.5 HTCC multilayer fabrication steps.<sup>11</sup>

ser cutting processes. The layers are stacked and registered relative to one another. The individual layers are laminated together using heated hydraulic presses. Typically, isostatic pressure is achieved on the three-dimensional structure with isostatic pressing or through the use of molds or conformal bladders or bags. Finally, the laminates are green cut to final or near-net expanded dimensions. The multilayer parts are then heated in a burnout and firing process to remove organics and densify the ceramic and metal materials.

The cofirable metal systems based on W, Mo, and Mn cannot be interconnected with traditional methods; that is, they are not wettable with solder systems or wire- or ribbon-bondable. Therefore, these packages require post-fire plating, electrolytic or electroless, with a Ni base layer, followed by a thin Au layer, to provide solder-wettable and wire-bondable terminations for interconnection. Electrolytic plating requires electrical connection to all pads requiring plating. The electroless systems plate all exposed metal surfaces.

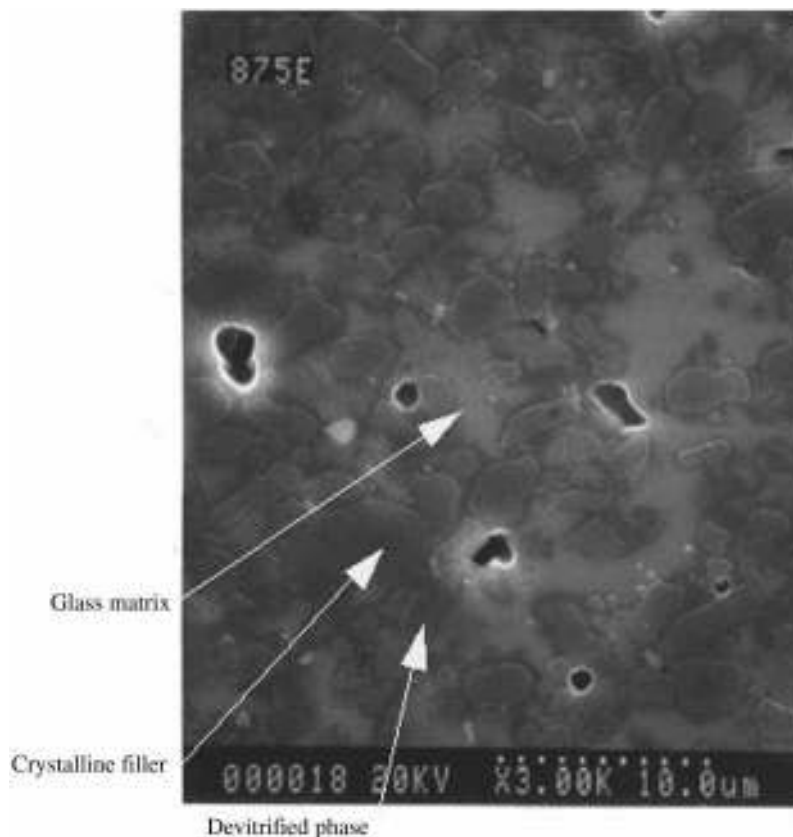
### 3.2.5 Low-temperature cofired ceramics

Low-temperature cofired ceramic (LTCC) technology is based on inorganic materials and used as the housing material containing layers of dense circuit paths and assembled electronic components. LTCC has widespread applications in military, aerospace, wireless telecommunications, optical data transmission, and automotive and medical devices and equipment. LTCC technology was first developed for military avionics applications in the 1980s. Westinghouse Electric Corporation and Hughes Aircraft were the two companies driving the use of the technology in advanced weapon systems.

Monolithic LTCC structures incorporating buried passive components (resistors, capacitors, and inductors) reduces assembly complexity and improves overall component and system reliability of microelectronic packages by reducing part count and interconnections. Additionally, the reduced weight of

LTCC packages and the low microwave-frequency-loss characteristics of the dielectrics and conductors make this packaging technology an ideal candidate for high-performance commercial and military electronic systems.

Low-temperature cofired ceramic material is a glass ceramic composite that provides highly integrated, high-performance electronic packaging. LTCC utilizes material technologies and manufacturing processes developed for two very mature systems: high-temperature cofired ceramic (HTCC) and multilayer thick film substrates. The LTCC material system consists of a low-firing-temperature ceramic with the multilayering capability of HTCC and the high-conductivity metals (gold, silver, and copper) used in the thick film process. This combination of material technologies allows for low-temperature (<1000°C) processing of three-dimensional packages and the use of conventional chip and wire technologies for the fabrication of various complex LTCC packages. Traditional LTCC materials are glass-based systems that undergo devitrification to a crystalline phase during the firing process or consist of a glass matrix with crystalline filler. Figure 3.6 shows the microstructure of an LTCC material with crystalline filler and partial devitrification.



**Figure 3.6** LTCC microstructure.

Because the glass phase of a material behaves as a supercooled liquid, it will densify at lower temperatures than the crystalline phase. The crystalline filler is added for thermal expansion match to the semiconductor chip, to control the densification behavior of the LTCC, and to achieve specific electrical performance. Figure 3.7 shows the effect of crystalline filler on TCE of a glass matrix LTCC. The crystalline phase is used for creating a thermal expansion match to other components. The key discriminating feature of LTCC is the low firing temperature, which enables the use of high conductivity metallizations in multilayer structures. This technology allows the high-density and high-resolution circuitry of HTCC in complex three-dimensional structures but uses the low firing temperature and, therefore, more highly conductive metallizations. The lower dielectric constants allow circuits with finer spacing without signal coupling.

Unlike the thick film process wherein successive lamination and firing steps cause bowing and line degradation at high layer counts, the single-step lamination and firing of LTCC produces a flat substrate with fine, high-quality line definition. In addition, the elimination of costly repeated firings greatly increases the number of conductive layers achievable. The ability to form complex three-dimensional structures with multilayer ceramic technologies offers a significant advantage in integrating multiple functions into a single cofired structure. That is, analog and digital signals from DC through microwave frequencies can be channeled through one package, achieving isolation of one section from another. Typically, ground via fences are used in the wall to divide various devices and achieve a high degree of electrical isolation.

Figure 3.8 depicts the core processing steps in the LTCC manufacturing process flow. The nine basic processes in the fabrication of an LTCC device are blanking, via formation, via filling, circuit printing, cavity formation, lay-up, lamination, firing, and post processing.

Blanking is the process by which sections of green tape of an appropriate size for processing are stripped from the Mylar carrier film and stabilized to remove residual stresses from the tape-casting process. Thermal and electri-

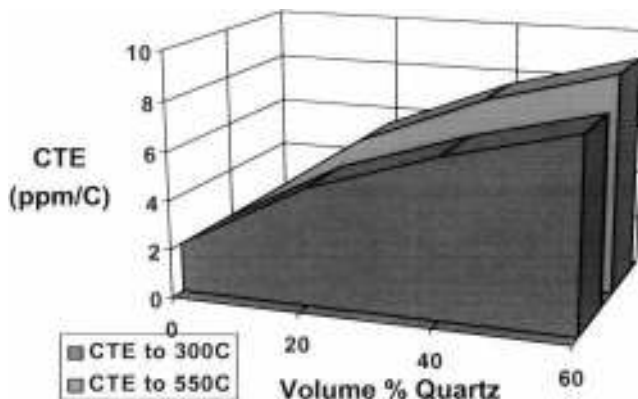
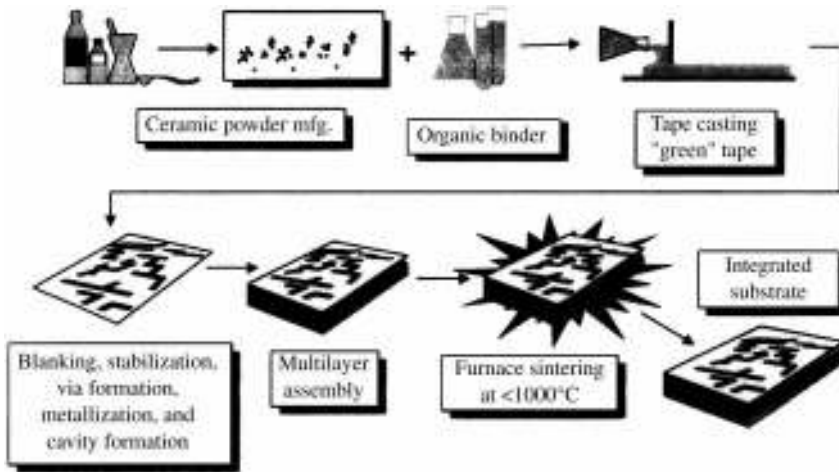


Figure 3.7 Effect of crystalline filler on thermal expansion of LTCC.



**Figure 3.8** LTCC multilayer fabrication steps.

cal vias for interconnection between layers of circuitry (diameters ranging from 0.002 to 0.020 in) are formed in the appropriate layers of unfired tape using pneumatic punching equipment with 10,000+ vias per layer. In high volumes, specialized “gang” punches or fixed die sets are used.

Vias are subsequently filled with a specially formulated conductive material applied through a stencil in a screen-printing process. The stencil is made from 0.002- to 0.003-in thick brass or stainless steel containing etched or punched vias of the same pattern as the tape. The stencil and punched tape typically are optically aligned before printing the conductive pastes into the vias. Quality factors are completeness of fill, without overfill, and accuracy of the fill material placement.

Conductor patterns are printed on the green tape using the process used for printing thick film conductors. In general, printing on green tape is of better quality and higher resolution than is possible on a thick film substrate for two reasons: the printing is always done on a flat surface without the warping and topography characteristics of multilayer thick film, and the paste is deposited on a porous surface, which inhibits the tendency of the paste to spread.

The three-dimensional cavity structure is formed by cutting the patterns in each layer of tape in the required location using die punching, mechanical machining, or a carbon dioxide laser cutting process.

The individual sheets of processed tape used in a substrate are collated and aligned using tooling holes aligned to the via and circuit pattern in each layer of tape. The multilayer stack is then laminated under elevated temperature (70 to 90°C) and pressure (2000 to 6000 psi) to bond the individual layers into one cohesive stack.

Laminated stacks are fired in belt or box furnaces to burn out organic binders and densify the ceramic and metallic constituents. Burnout and firing can be accomplished in one continuous operation so that the part does not experience thermal gradients from end to end as the temperature is changed. Fin-



ished parts may be metallized with either a screen-printed thick film or a sputtered and etched thin film conductor.

The current state of the LTCC technology allows high-density circuitry (as fine as 0.003-in lines and spaces) interconnected with conductive vias (as fine as 0.0035-in diameter). The wide range of available dielectric constants in LTCC increases design flexibility. Dielectric constants as low as 3.8 are particularly well suited for high-speed digital applications. Moderate dielectric constants ranging from 6 to 80 are well suited for higher-frequency applications. The availability of high dielectric constants (up to 5,000) allows integration of capacitor devices into the multilayer structure. Resistor pastes are available that can be printed on internal layers of circuitry and cofired into the structure. This integration of passive components reduces the number of surface mount components, reducing the number of solder and wirebond connections, thereby increasing reliability. The ability to form complex three-dimensional structures with multilevel cavities and the ability to form grounded “walls” of conductive vias enables considerable isolation potential. This isolation allows multiple signals to be handled in one cofired package, reducing the number of substrates required, reducing interconnections, and thereby improving reliability. The fact that there are fewer exterior walls or housings when multiple circuits are contained in the same package also contributes to a reduction in volume as compared to individually packaged modules. The reduced part count leads to reduced labor hours in package manufacturing and assembly and therefore reduces costs. The reduction in the number of interconnections realized by combining functions or passive components into one package dramatically improves the reliability of the system.

Interconnect technologies such as land grid arrays (LGAs) and ball grid arrays (BGAs) used on ceramic packaging typically require the soldering of the ceramic package to an organic PWB. The large coefficient of thermal expansion (CTE) mismatch between the ceramic (6 to 7 ppm/°C typical) and organic (12 to 16 ppm/°C typical) can result in significant strain at the interface. Kyocera’s HITCE system, formulated with high CTE glass and crystalline filler having a combined CTE of 11.5ppm/°C, is well suited for applications wherein the ceramic is to be attached to a PWB with a CTE in the 12 to 16ppm/°C range.

A comparison of the high-frequency electrical properties for several LTCC systems is shown in Figs. 3.9a and 3.9b. Table 3.2 provides a comparison of properties for various LTCC and HTCC systems.

### 3.3 Capacitors

Capacitors are essential components in most electronic circuits. Capacitors function to provide energy storage, current blocking, electrical noise filtering, high-frequency tuning, and other functions. Since the first demonstration of the energy-storage capability of a capacitor device in 1745 in Leiden, Netherlands (hence the “leyden” jar), in which a glass was used as the dielectric, capacitors have taken on a wide variety of designs. In the early 1900s, the first practical capacitor devices were fabricated from steatite porcelains, paper, and

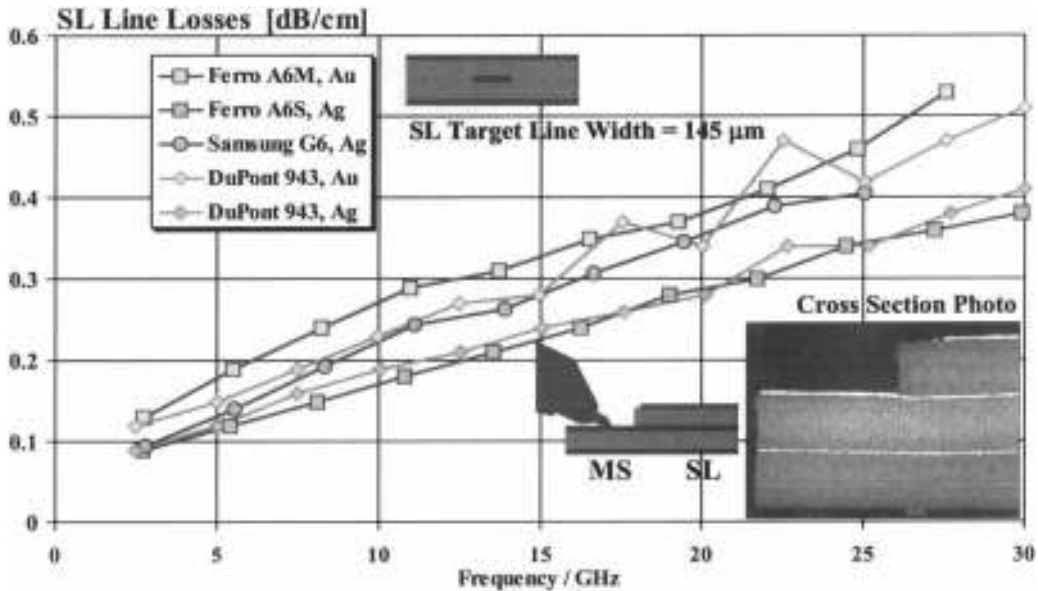


Figure 3.9a Measured line losses of buried striplines.<sup>15</sup>

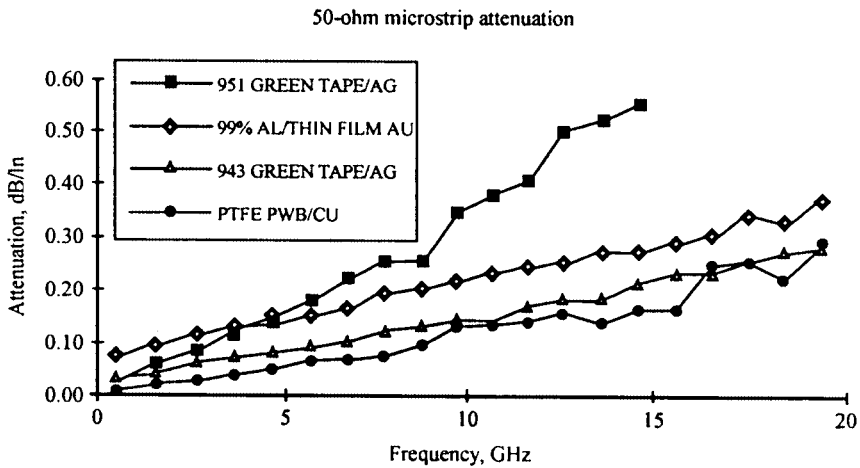


Figure 3.9b Attenuation vs. frequency for DuPont LTCC with silver conductor vs. thin film and PTFE printed wiring board.

mica. Lower-loss porcelains were developed in the 1920s, followed by higher-dielectric-constant  $\text{TiO}_2$ -based ceramics in the 1930s. In 1942, researchers at the American Lava Co. discovered the ferroelectric behavior of  $\text{BaTiO}_3$ .  $\text{BaTiO}_3$  has been modified over the years, forming solid solutions with other perovskites and doping with various ions.  $\text{BaTiO}_3$  remains the most widely used material in the ceramic capacitor industry today. Process refinements have

TABLE 3.2 Properties of Multilayer Ceramic Packaging

Material	Primary phase	Thermal expansion (ppm/°C)	Dielectric constant	Dielectric loss	Thermal conductivity (W/m-K)	Flexural strength (MPa)	Density (g/cc)
<i>HTCC</i>	Al <sub>2</sub> O <sub>3</sub>	7.1	9.5	0.0004	25	420	3.9
Kyocera	Al <sub>2</sub> O <sub>3</sub>	7.0	10	0.002	18	275	3.6
NTK	>92% Al <sub>2</sub> O <sub>3</sub>	6.8	9.4		17		
IBM	92% Al <sub>2</sub> O <sub>3</sub>	6.5	9.5		20	275	
NTK	Mullite	4	6.6		5		
Kyocera	Mullite	4.2	6.4	0.002	5	196	2.9
ALN	ALN	4.4	8.9	0.0004	175	320	3.3
NTK	AlN		8.9		170		
Kyocera	AlN	4.6	8.5	0.0004	150	343	3.4
Kyocera	SiC	3.7	45		270	441	
<i>LTCC</i>	Glass-matrix, crystallized	3–7	3.9–7.5	0.0002–0.003	2	180–210	2.25–3.0
NTK	Crystallized glass	3	4.9–5.6		3		
IBM	Cordierite	3	5.3–5.7		5		
IBM	Spodumene	2.8	5.65				
DuPont 951	Pb-BSG + CaZrO <sub>3</sub> + Al <sub>2</sub> O <sub>3</sub>	7	7.1	.007	3	206	
DuPont 943	Crystallized glass + Al <sub>2</sub> O <sub>3</sub>	5.3	7.5	0.001	3.0	230	3.2
Ferro A6	Crystallized Ca-BSG	3	5.9	.002	2		2.
Northrop	BSG + Quartz	6.8	3.9	.0008	2	100	2.3
Fujitsu	BSG + Al <sub>2</sub> O <sub>3</sub>	4	5.7		2.5	200	
NEC	Pb-BSG + Al <sub>2</sub> O <sub>3</sub>	7.9	7.8	0.003		343	
Kyocera	Glass-ceramic	7.9	7.9	0.003	2	196	2.8
Kyocera	Glass-ceramic	4.0	5.0	0.0029	2	186	2.5
Murata		8.0	6.1	0.0007	4.2	196	

contributed to dramatic improvements in capacitor performance through the years. The development of tape casting and cofired metallizations enabled the fabrication of multilayer capacitors (MLCs) with extremely high capacitance density. Chemical synthesis techniques have led to fine-particle dielectric powders that densify at lower temperatures and have better breakdown strengths.

The capacitance of a device is a measure of the charge stored per applied voltage and is measured in units of farads or  $\text{s}^2\text{coulomb}^2/\text{kgm}^2$ . In its simplest form, a capacitor consists of two parallel electrodes separated by a dielectric medium. The capacitance of such a device, in units of farads, is given by

$$C = A\epsilon_r\epsilon_o/t \quad (3.2)$$

where  $A$  = effective area of electrode plates

$\epsilon_o$  = permittivity of free space

$\epsilon_r$  = materials relative permittivity (dielectric constant)

$t$  = separation distance between electrodes

The intrinsic volumetric energy density ( $U$ ) of a parallel plate capacitor, in units of  $\text{J}/\text{cm}^3$ , is given by

$$U_{vol} = \int EdP = \frac{1}{2}\epsilon_r\epsilon_o E^2 \quad (3.3)$$

where  $P$  is the polarization resulting with an applied electric field  $E$ .

Substituting Eq. (3.2), the electrical energy stored, in units of joules (W-s), in a capacitor is given by

$$U_{device} = \frac{1}{2}CV^2 \quad (3.4)$$

where  $V$  is the applied voltage. These relationships show that the energy density could be maximized by increasing the permittivity, the applied electric field, or both.

While all capacitors are based on metal electrodes separated by a dielectric material, they come in many different forms. Table 3.3 gives a list of various capacitor materials and designs. The capacitance per unit volume of a device can be increased by increasing the area:thickness ratio or using higher-permittivity materials. The development of cofired multilayer process in the 1950s enabled fabrication of thin dielectric layers, mechanically stacked in series and electrically connected in parallel. High-permittivity materials will raise capacitance values but, in general, with higher permittivity comes higher loss.

Polymer film capacitors are fabricated by interleaved polymer sheets and aluminum electrodes. The dielectric thickness is typically several microns, so relatively high capacitive densities can be achieved. The use of thin layers of oil-impregnated polymer dielectrics with low permittivities ( $\epsilon_r = 3$  to 10) has enabled operation at fields up to 300 MV/m, yielding energy densities as high as  $3 \text{ J}/\text{cm}^3$ . Ceramic capacitors have significantly higher permittivities (up to

TABLE 3.3 Alternative Capacitor Materials and Designs

Type	Materials	Operating freq., Hz	Benefits
Polymer film	Polystyrene, polypropylene, polyester, poly-carbonate, PVD, PVDF, paper	0–10 <sup>10</sup>	High voltage, high energy density, self-healing
Electrolytic	Aluminum foil electrodes with electrolyte-impregnated paper dielectric	0–10 <sup>4</sup>	High capacitance
Tantalum	Porous Ta with MnO <sub>2</sub> or wet electrolyte	0–10 <sup>4</sup>	Stable
Mica	Mica plates clamped in multilayer stack	10 <sup>3</sup> –10 <sup>10</sup>	Low cost, one of the first capacitor materials
Ceramic	Ferroelectric perovskites	10 <sup>2</sup> –10 <sup>10</sup>	High capacitance
Multilayer ceramic	Tape-cast ferroelectric dielectrics cofired with internal electrodes	10 <sup>2</sup> –10 <sup>10</sup>	Embedded passives in hybrid circuits
Thick film	Usually BaTiO <sub>3</sub> -based paste with glass adhesion promoters fired onto substrate	10 <sup>2</sup> –10 <sup>10</sup>	Embedded passives in hybrid circuits
Thin film	Dielectrics such as SiO <sub>2</sub> or TiO <sub>2</sub> deposited on a substrate	10 <sup>2</sup> –10 <sup>10</sup>	Embedded passives in hybrid circuits

≈25,000), however, ceramic dielectrics have not realized their full potential because of a reduction in permittivity and resistivity at high fields and, therefore, low breakdown strengths. Recent improvements in ceramic processing and materials properties are rivaling the state-of-the-art polymer capacitors. Polymer film capacitors currently hold at least 25 percent of the market.

Electrolytic capacitors consist of aluminum foil electrodes separated by a thin sheet of porous paper and wound into a cylindrical shape. The paper is impregnated with an electrolyte solution. These capacitors are relative inexpensive to fabricate and allow very high capacitance values. The drawbacks to electrolytics are that they are polar and operate only at lower frequencies (<10 kHz).

Tantalum capacitors are formed by sintering Ta metal powder around a Ta lead wire to form a porous body that serves as the anode. The porous Ta is then coated with a semiconductive MnO<sub>2</sub> layer, which is coated with carbon and silver paints to form the cathode. A supporting T-bar is then welded to the lead wire, and the assembly is encapsulated. A wet electrolyte may be used in place of the MnO<sub>2</sub>. Tantalum capacitors are very stable over time and temperature.

Mica capacitors consist of mica, KAl<sub>2</sub>(Si<sub>3</sub>Al)O<sub>10</sub>(OH)<sub>2</sub>, plates with fired-on silver electrodes. The metallized plates are stacked together in a multilayer fashion. Mica capacitors are extremely stable over time, have low thermal coefficient of capacitance, and have relatively low loss.

Ceramic capacitors are fabricated in four general processes: thin film, thick film, single-layer, and multilayer. Thin film capacitors were developed to address a need to embed passive components into electronics packaging—hybrid

circuits. Dielectrics such as SiO, SiO<sub>2</sub>, Ta<sub>2</sub>O<sub>3</sub>, TiO<sub>2</sub>, titanates, and aluminosilicates can be vacuum deposited with a variety of electrode metallizations.

Thick film hybrid packaging consists of layers of screen-printed/fired dielectric and circuit layers. Here again, the desire to embed passive devices into the substrate drove the development of thick film capacitors. The screen-printed pastes consist of a high-K dielectric, usually BaTiO<sub>3</sub> based, a glass binder, and organic constituents such as binder, dispersant, and solvent.

Single-layer capacitors represent the simplest form of ceramic capacitors. These capacitors use a single layer of dielectric ceramic between two metal electrodes. The dielectric may be in the form of a disc, cylinder, or rectangular plate.

In general, capacitors are designed to take advantage of the material and geometric contributions to the capacitance. However, there are secondary properties of capacitors that drive the design. For example, high-permittivity materials are desired to maximize the energy density per unit volume, but the material must also exhibit some specified temperature response and possess low dielectric loss. For this reason, the material selection for a specific application is generally a compromise. Because capacitance is additive when individual capacitors are placed in parallel, it is desirable to use multilayer devices with interdigitated electrodes. To take advantage of the inverse relationship to dielectric thickness, there is a drive to improve processes and powder characteristics to achieve thinner dielectric layers.

Figure 3.10 shows the simple disc capacitor structure containing one layer of ceramic dielectric. This structure was the standard for ceramic capacitors for many years. The development of multilayer capacitors has eroded the market for single-layer discrete devices. The most efficient way to maximize capacitance is to stack many thin layers of dielectric in series and connect them electrically in parallel as shown in Fig. 3.11. When connected electrically in parallel,  $C_{\text{total}} = C_1 + C_2 + C_3 + \dots$

Two processes for forming MLCs are shown in Fig. 3.12. In both processes, the dielectric powders are mixed in a solvent solution with dispersant, organic binders, and plasticizers. In the tape process, the slurry is de-aired and cast into thin sheets using a doctor blade. The slurry is typically pumped into a reservoir. The leading edge of the reservoir has a small, adjustable gap. A metal belt or polymer film moves under the reservoir and doctor blade. As it does so, a thin film of slurry is carried along the belt. This thin film continues to move through a heated bed to gradually drive off solvents, leaving a flexible ceramic binder film, *green tape*. The end of the caster is typically equipped with a spooler so that the casting is a continuous process. The green tape is typically 50 to 60 volume percent ceramic and 25 to 30 volume percent organic binder. Dielectric sheets from 15 to 100 μm thick are typical. Sheets of the green tape are printed using a screen printer with a metal-organic paste, typically Ag or Ag-Pd based, to form the pattern of the internal electrodes. The pastes are dried, and the printed sheets are stacked and laminated at elevated pressure (1 to 4 Ksi) and temperature (50 to 90°C). Individual capacitors are diced from the laminated block prior to firing by a hot-knife or gang saws.

For thinner dielectric layers, 10 to 25 μm, a wet lay-down process is used. The wet lay-down process differs from the tape process in that the multilayer

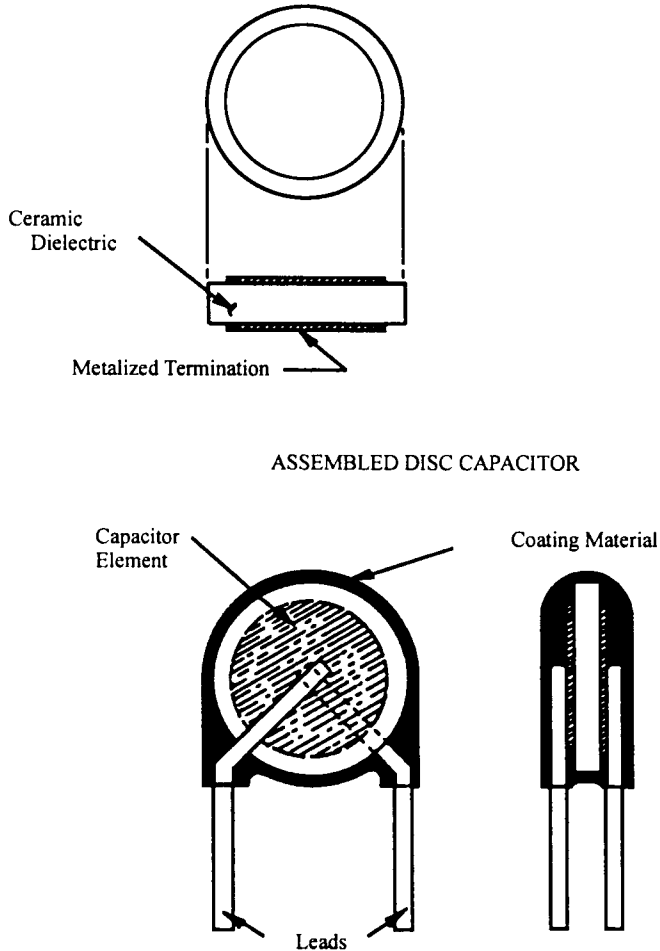


Figure 3.10 Simple disk capacitor design.<sup>16</sup>

structure is built up through a successive printing and drying process. Here, the slurry is printed onto a carrier plate in very thin layers. The printed dielectric is dried, and the process is repeated to avoid pinholes. The electrode print is applied to the dried dielectric layer. This process is repeated to build up the multilayer structure. The capacitors are fired in a variety of methods, but all go through some method of binder decomposition followed by sintering of the metal and ceramic particles. The fired capacitors are then terminated on two sides to achieve electrical connection to alternate layers.

### 3.3.1 Capacitor material classification

The Electronic Industries Alliance (EIA, formerly Electronic Industries Association) has specified a method of classifying capacitors based on their capacitance value and temperature sensitivity. Class 1 capacitors are highly stable

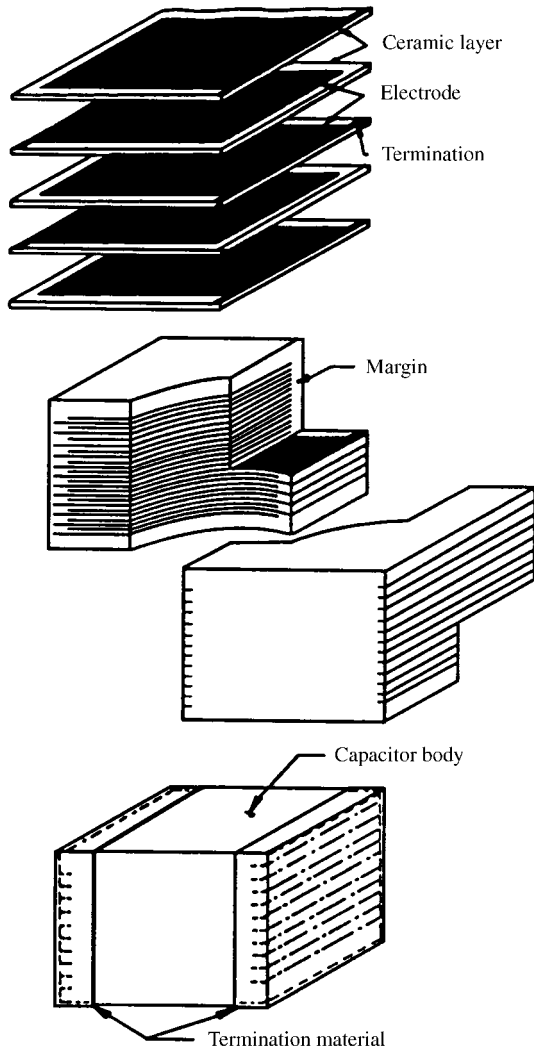


Figure 3.11 Multilayer capacitor design.<sup>16</sup>

with respect to temperature and time (i.e., no aging) and have low loss. Typically, these capacitors are made with titanates or tantalum. Class 2 capacitors are significantly more affected by temperature, time, and frequency; however, they are made from materials with much higher dielectric constants. Class 2 capacitors are typically made with ferroelectric materials and possess a broad range of stability. Therefore, EIA also set categories for temperature stability, outlined in Table 3.4. The classification of Class 2 capacitors is expressed in terms of three symbol codes. The first symbol represents the lower operating temperature, the second represents the upper operating temperature, and the third represents the change in capacitance over the operating temperature range.



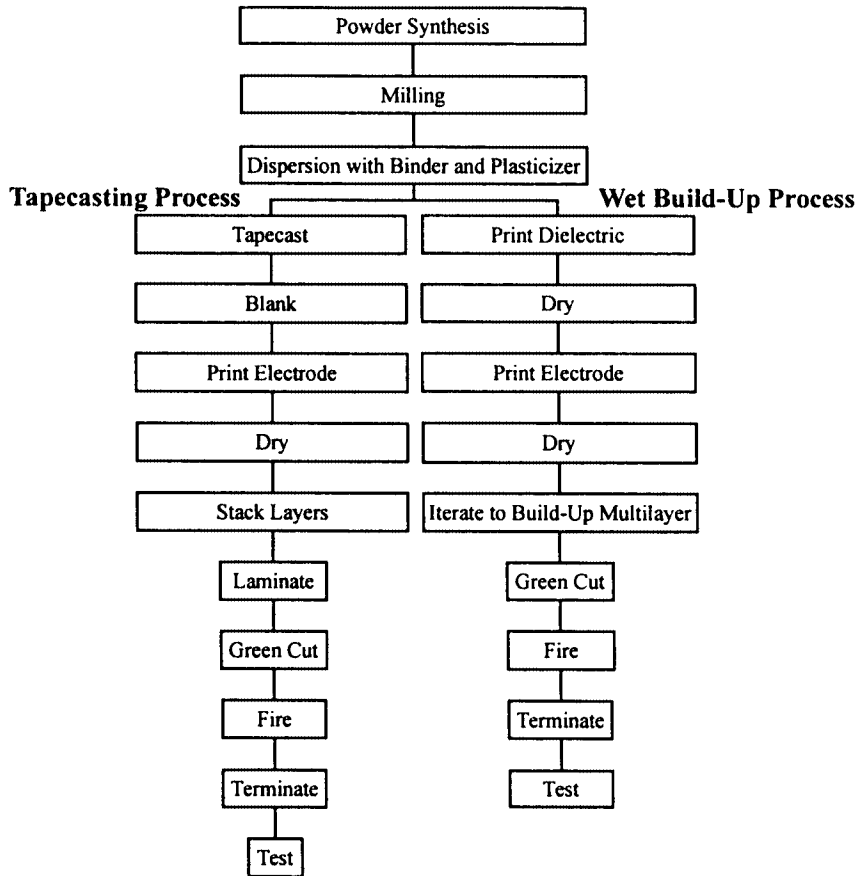


Figure 3.12 Multilayer capacitor fabrication steps.

Negative-positive 0-ppm/°C (NPO) devices are Class 1 dielectrics typically based on rutile  $\text{TiO}_2$ . These compositions can contain up to 50 percent  $\text{BaTiO}_3$ , which raises the dielectric constant and balances the negative temperature coefficient of rutile as shown in Table 3.5. Class 1 dielectrics are necessary for applications where a high degree of stability is necessary, as shown. Figure 3.13 shows the temperature stability for various classes of capacitors.

Class 2 devices are based on ferroelectric materials with considerably higher dielectric constants, such as those listed in Table 3.5. These materials exhibit shifts in dielectric constant as a function of time (aging). This phenomenon is a result of ferroelectric domain movement over time. A typical aging curve is shown in Fig. 3.14. The application of heat, voltage, or stress to the material will have a de-aging effect. Increasing frequency will result in reduced dielectric constant and increased dissipation factor in Class 2 dielectrics.

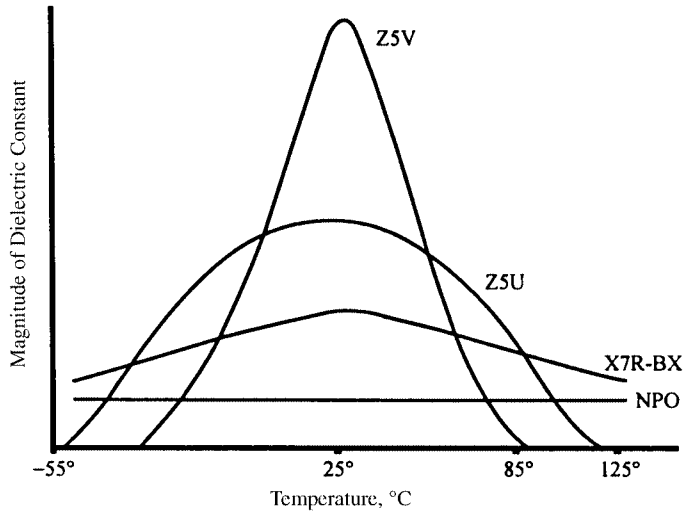
Applying DC voltage to a Class 1 dielectric results in a decreased capacitance and dissipation factor. AC voltages tend to raise the dielectric constant and dissipation factor (see Fig. 3.15).

TABLE 3.4 Electronics Industries Association (EIA) Capacitor Classifications and Examples

EIA code	Temperature range (°C)	Change in capacitance (%)	Typical dielectric constant	Typical dielectric loss (%)
X7	-55 to +125			
X5	-55 to +85			
Y5	-30 to +85			
Z5	+10 to +85			
D		±3.3		
E		±4.7		
F		±7.5		
P		±10		
R		±15		
S		±22		
T		+22 to -33		
U		+22 to -56		
V		+22 to -82		
<i>Examples</i>				
X7R	-55 to +125	± 15	3000–4000	<2.5
Z5U	-10 to +85	+22 to -56	8000–10,000	<4.0
Y5U	-30 to +85	+22 to -56	12,000–20,000	<4.0
Y5V	-30 to + 85	+22 to -82	12,000–25,000	<4.0
COG (NPO)	-55 to + 125	30 ppm/°C	up to 100	<0.1

Figure 3.16 shows the basic perovskite structure of  $\text{BaTiO}_3$ . The paraelectric perovskite is cubic and has an  $\text{ABO}_3$  form with one formula unit per unit cell. The A site is at the corners of the unit cell, the B site is at the unit cell center, and the oxygens are at the unit cell face centers. The ferroelectric perovskite phases are in the same arrangement as the cubic phase, but the unit cell is slightly distorted into a tetragonal, rhombohedral, or orthorhombic structure. The A site atoms are coordinated by 12  $\text{O}^{2-}$  atoms, and the B site atoms are coordinated by six  $\text{O}^{2-}$  atoms.

$\text{BaTiO}_3$  is the most common ceramic capacitor material as a result of its high permittivity, stability, and ease of doping. Figure 3.17 shows the unit cell dimensional change and associated dielectric constant change for  $\text{BaTiO}_3$  as a function of temperature. The diagram shows that stoichiometric  $\text{BaTiO}_3$  un-



**Figure 3.13** Temperature dependence of capacitance for various dielectrics.<sup>16</sup>

**TABLE 3.5 Ceramic Capacitor Materials**

Material	Relative permittivity	Dissipation factor (%)
TiO <sub>2</sub>	110	0.02–0.04
SrTiO <sub>3</sub>	285	<0.1
CaTiO <sub>3</sub>	130	<0.1
MgTiO <sub>3</sub>	16	0.01–0.03
Al <sub>2</sub> O <sub>3</sub>	10	0.04
MgO	10	<0.1
Steatite	6	0.03–0.1
BaTi <sub>4</sub> O <sub>9</sub>	40	0.01–0.03
BaTiO <sub>3</sub> (BT)	14,000	1–3%
BT + CaZrO <sub>3</sub>	5700–700	<3%
BaSrCaZrTiO <sub>3</sub>	11,500–14,000	<3%
Ba(TiZr)O <sub>3</sub>	10,000	<3%
PMN-PT	20,000–28,000	<3%
PFN-PFW	24,000	<3%

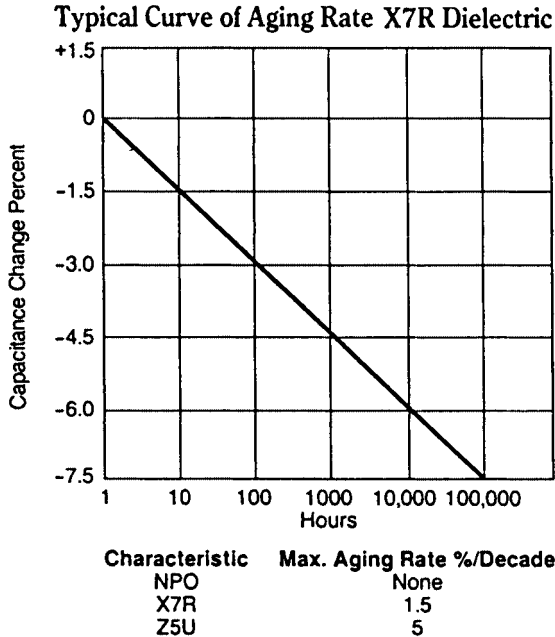


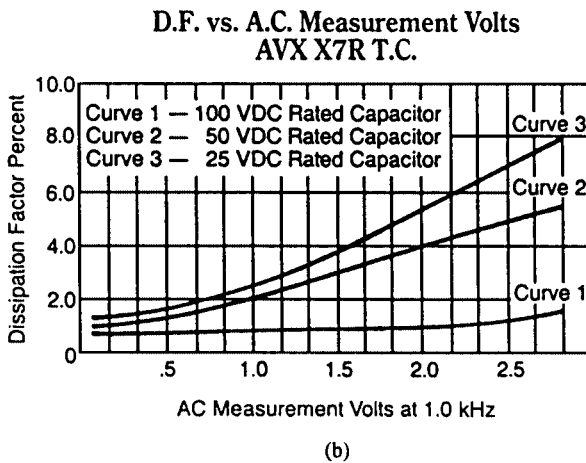
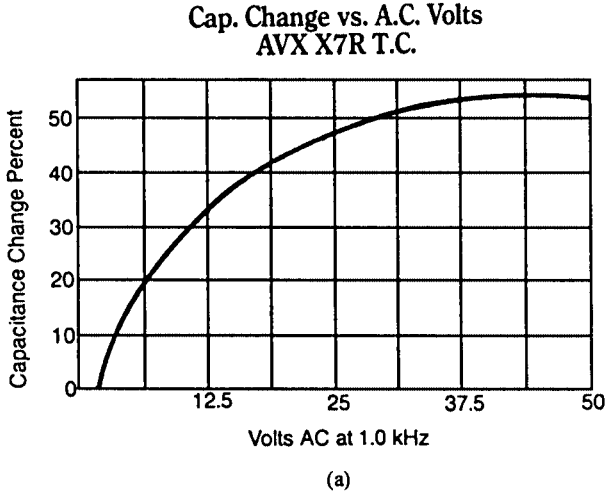
Figure 3.14 Aging behavior of various dielectrics.<sup>4</sup>

dergoes several phase transitions on cooling from high temperature. At approximately 110°C the high-temperature cubic phase converts from a paraelectric cubic phase to tetragonal ferroelectric phase. Cooling further results in conversion to an orthorhombic phase at approximately -10°C and a rhombohedral phase at approximately -100°C. At high temperatures, the lattice is expanded sufficiently to allow the B site ion to be centered in the cubic structure. As the material is cooled, the B site ion is shifted off center, creating a permanent dipole.

Perovskite  $\text{SrTiO}_3$  (ST) is also a base capacitor material with a dielectric constant of approximately 300 at room temperature. Pure  $\text{SrTiO}_3$  is paraelectric with a transition temperature near 0 K.  $\text{SrTiO}_3$  is frequently used in high-voltage applications, because its dielectric constant is relatively independent of electric field, shows virtually no electrostrictive strain at high field, and maintains high resistivity at high fields. It is therefore resistant to voltage breakdown (see Figs. 3.18 and 3.19). Commercial  $\text{SrTiO}_3$  compositions are typically donor doped to reduce oxygen vacancies and improve resistivities.

Calcium titanate,  $\text{CaTiO}_3$  (CT), is used in applications similar to those of ST; however, the dielectric constant is roughly half that of ST as shown in Fig. 3.18.  $\text{CaTiO}_3$  has a relatively flat dielectric constant over temperature and field. Both ST and CT are used in solid solutions with higher-permittivity materials to improve temperature and field stability.

Magnesium titanate,  $\text{MgTiO}_3$  (MT), is an ilmenite structure material with a low but stable dielectric constant ( $K = 16$ ). MT meets the EIA requirements for an NPO capacitor formulation of <30 ppm/°C over -55 to 125°C.



**Figure 3.15** Effect of DC and AC voltages on capacitance and dissipation factor.<sup>4</sup>

Lead titanate,  $\text{PbTiO}_3$  (PT), is a ferroelectric perovskite material with a Curie temperature near  $490^\circ\text{C}$ . PT is used extensively as a piezoelectric material; however, it is often used in solid solutions with other perovskites to improve capacitance and stabilize the perovskite phase. Modification of PT with  $\text{Sr}^{2+}$  substitutions for  $\text{Pb}^{2+}$  and  $\text{W}^{6+}$  and  $\text{Mg}^{2+}$  substitutions for  $\text{Ti}^{4+}$  yield excellent capacitor formulations with  $K = 5000$  at room temperature.

Lead magnesium niobate,  $\text{Pb}(\text{Mg}_{1/3}\text{Nb}_{2/3})\text{O}_3$ , is a ferroelectric relaxor material that is paraelectric at room temperature. The perovskite phase is typically modified with additions of lead titanate or barium titanate, which raises the Curie temperature to near room temperature. Very high dielectric constants can be achieved ( $>20,000$ ) but at the expense of temperature stability.

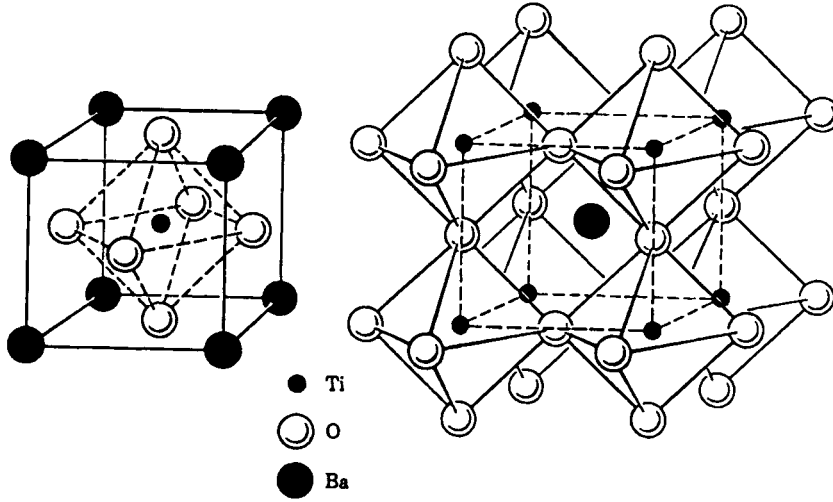


Figure 3.16 Perovskite  $\text{BaTiO}_3$  structure.<sup>14</sup>

### 3.3.2 Effect of additives

Sharp changes in dielectric properties as a function of temperature are generally impractical. The properties of perovskites such as  $\text{BaTiO}_3$  can easily be modified by additions of materials that form solid solutions in the perovskite structure. Isovalent substitutions on both the A and B site can be used to alter the transition temperature of perovskite materials. The ionic radii for the constituent and dopant ions are shown in Table 3.6 for the perovskite structure. In  $\text{BaTiO}_3$ ,  $\text{Pb}^{2+}$ ,  $\text{Ca}^{2+}$ ,  $\text{Sr}^{2+}$ , and  $\text{Cd}^{2+}$  are substituted on the larger A site (1.3 to 1.6).  $\text{Pb}^{2+}$  raises the phase transition (Curie temp) temperature,  $\text{Sr}^{2+}$  lowers  $T_c$ , and  $\text{Ca}^{2+}$  broadens the transition. These effects are predictable if one considers these substitutions as solid solutions in titanate form. For example,  $\text{PbTiO}_3$  has a higher (500°C) Curie point than  $\text{BaTiO}_3$ , and  $\text{SrTiO}_3$  is near 0 kelvins (K). Therefore, one would expect  $\text{Pb}^{2+}$  additions to raise the Curie point and  $\text{Sr}^{2+}$  additions to drop the transition temperature.  $\text{Hf}^{4+}$ ,  $\text{Zr}^{4+}$ , and  $\text{Sn}^{4+}$  can be used to substitute for  $\text{Ti}^{4+}$  on the smaller B site (0.6 to 0.75) of the perovskite structure. Isovalent substitutes have quite high solubility in the perovskite structures. Figure 3.20 shows the effect of isovalent substitutions on the transition temperature.

The effects of acceptor and donor ion substitutions in the perovskite structure was described by Jaffe, Cook, and Jaffe, as outlined in Table 3.7. Ion valences of the acceptor-type impurity atoms are lower than that of the constituent atoms. Oxygen vacancies are introduced to maintain charge balance. A decrease in DC resistivity has been attributed to the presence of charge carriers such as oxygen vacancies in the lattice. The decrease in resistivity ultimately leads to dielectric breakdown, but many ceramics fail because of the presence of voids or microcracks, which serve as initiation points

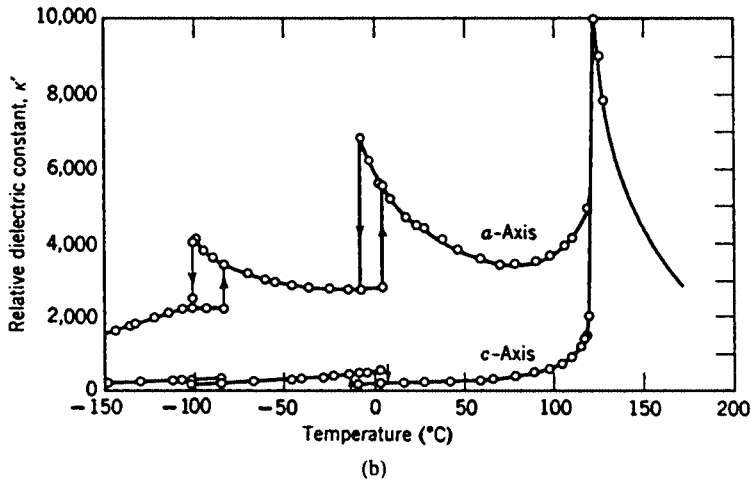
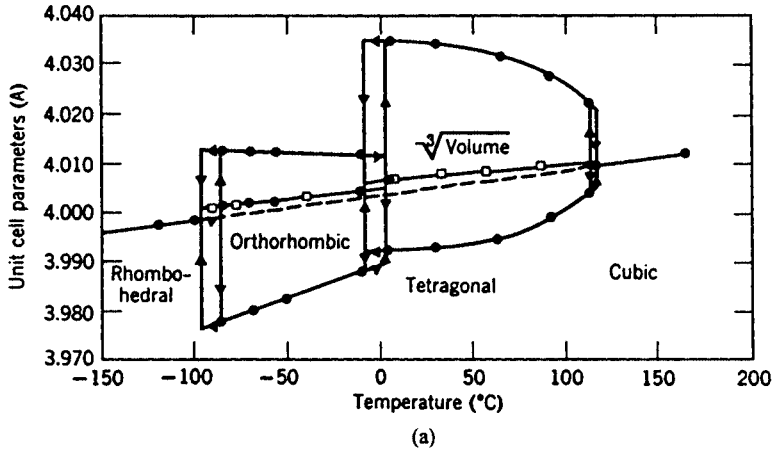


Figure 3.17 Unit cell dimensional and associated dielectric constant change for  $\text{BaTiO}_3$  as a function of temperature.<sup>14</sup>

for breakdown. Acceptor solubility is generally limited to <5 mol%. In  $\text{BaTiO}_3$ , acceptor dopants such as  $\text{Mn}^{2+,3+}$ ,  $\text{Co}^{2+,3+}$ ,  $\text{Fe}^{2+,3+}$ ,  $\text{Ni}^{2+}$ , and  $\text{Zn}^{2+}$  are substituted on the B site. The advantage of acceptor substitutions is that they lead to lower dissipation factors and inhibited grain growth. The distortion in the smaller unit cell caused by oxygen vacancies is believed to be the primary cause of such properties.

The ion valence of donor-type impurity atoms are higher than that of the constituent atoms, and A site vacancies are introduced. In perovskite  $\text{BaTiO}_3$ , donor atoms are known to suppress the peak dielectric and piezoelectric properties. This is believed to be a result of a compensating valence change of some of the  $\text{Ti}^{+4}$  to  $\text{Ti}^{+3}$ , because Ba is not volatile. In lead perovskites, such as lead zirconate titanate (PZT) or lead titanate (PT), it is believed that the excess lead created by the vacancies is allowed to leave the structure because of its

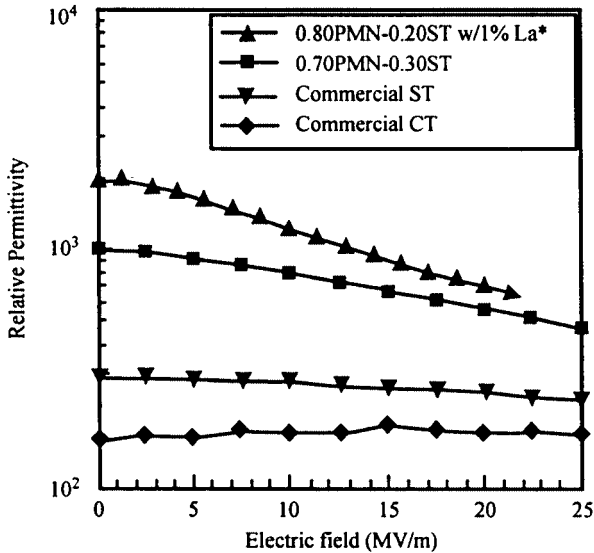


Figure 3.18 Permittivity vs. DC field for doped PMN, ST, and CT dielectrics.

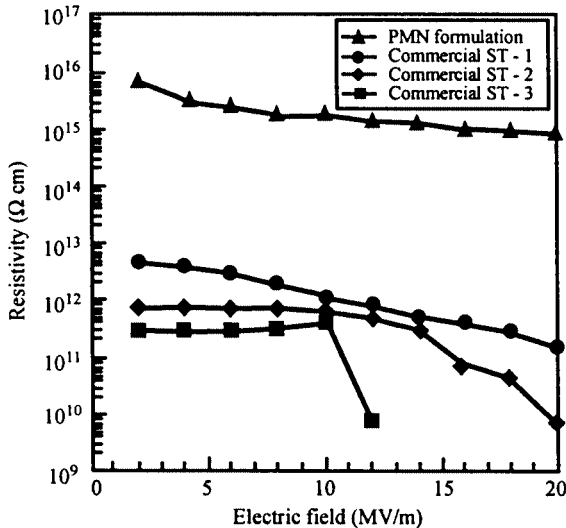


Figure 3.19 Resistivity vs. field for doped PMN and ST dielectrics.

high volatility so that the stoichiometry corrects itself. In these compounds, the peak dielectric constant and the piezoelectric properties are higher.

In  $\text{BaTiO}_3$ ,  $\text{Nb}^{5+}$ ,  $\text{Ta}^{5+}$ , and  $\text{W}^{6+}$  are substituted on the B site.  $\text{Bi}^{3+}$ ,  $\text{La}^{3+}$ , or  $\text{Nd}^{3+}$  is used on the A site. The properties in this case are generally explained by increased domain wall motion resulting from the A site vacancy. The ease with which these domains will switch results in a low coercive field to switch



**TABLE 3.6 Ionic Radii for Constituent and Dopant Ions**

Ion	Site	Coordination number	Ionic radii, Å
Pb <sup>2+</sup>	A	12	1.63
Ba <sup>2+</sup>	A	12	1.74
Sr <sup>2+</sup>	A	12	1.6
Ca <sup>2+</sup>	A	12	1.34
Zn <sup>2+</sup>	B	6	0.89
Nb <sup>5+</sup>	B	6	0.78
Ti <sup>4+</sup>	B	6	0.745
Li <sup>+</sup>	B	6	0.88
Mg <sup>2+</sup>	B	6	0.86
Fe <sup>3+</sup>	B	6	0.785
Ta <sup>5+</sup>	B	6	0.83
Sb <sup>5+</sup>	B	6	0.75
W <sup>6+</sup>	B	6	0.74

polarity and a reduced mechanical quality factor, because the domains will also move to cancel a small applied stress. The increased dielectric losses are also caused by increased domain wall losses. Lower aging rates are attributed to low residual stress as a result of the ease of domain wall movement. The higher DC resistivity is the result of the excess electrons countering p-type conduction.

The decrease in permittivity at high electric fields, dielectric saturation, is especially problematic in Class 2 dielectrics containing ferroelectric phases. It occurs because the ionic lattice distortion that produces the polarization has its limits. Tables 3.8 through 3.10 show typical capacitor formulations are used to achieve NPO, X7R, and Z5U performance, respectively.

### 3.4 Electromechanical Ceramics

Electromechanical materials are an interesting family of substances used for their ability to generate an electrical signal from a mechanical stimulation (passive devices) or generate mechanical displacements from electrical inputs (active devices). Passive devices include sensors such as sonar hydrophones, which give electrical signals as the sensor is stressed by sound waves. Advanced materials have been developed with very high electromechanical coefficients, enabling highly sensitive devices. New manufacturing processes

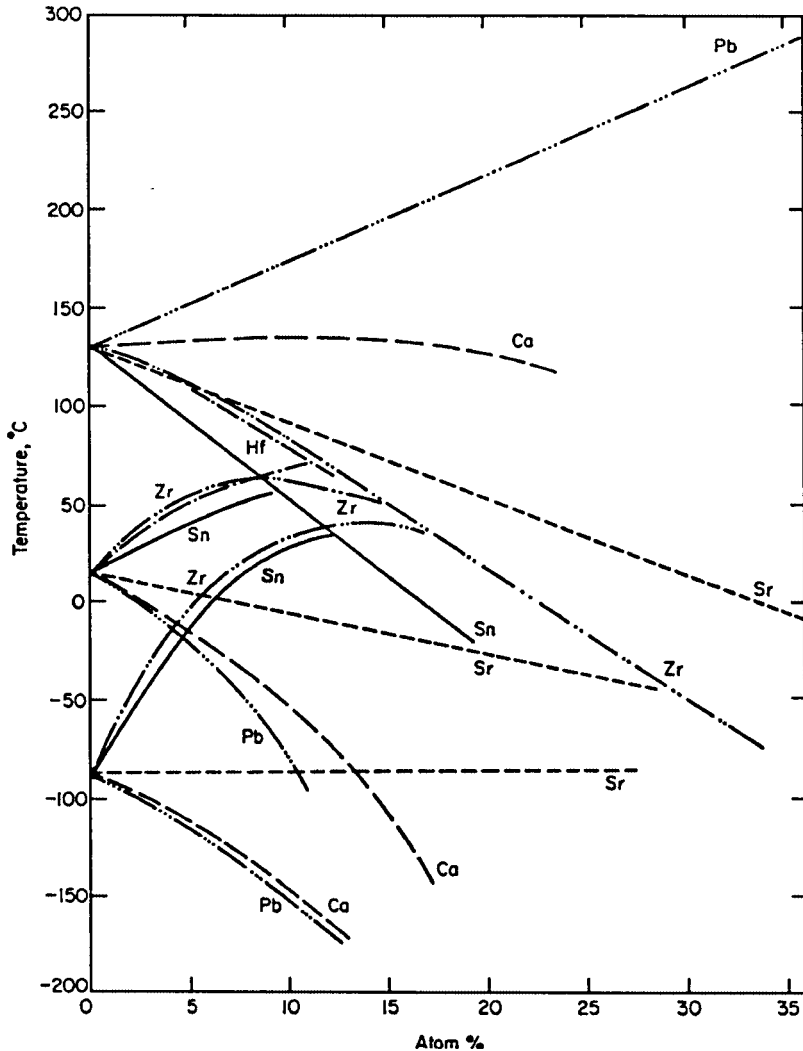


Figure 3.20 Effect of isovalent substitutions on the transition temperature of BaTiO<sub>3</sub> ceramic.<sup>13</sup>

allow complex arrays, composites, and multilayer stacks to be fabricated, further improving signal resolution. Other passive applications for electromechanical materials are ultrasonic sensors in medical devices and sensors in vibration-cancellation devices such as active suspensions in automobiles.

Active applications include microdisplacive devices and sonic projectors that output mechanical displacements as a result of applied electrical inputs. The high displacements, coupled with the high stiffness of ceramic electromechanical materials, allows generation of high forces. This allows vibration cancellation of relatively massive structures or generation of significant sonar source levels. Other active applications for electromechanical materials are actuators

**TABLE 3.7 Substitution Effects on Dielectric and Piezoelectric Properties**

Property	Isovalent substitution	Acceptor substitution	Donor substitution
Curie temperature	Lower	Higher	Lower
Dielectric constant	Higher	Lower	Higher
Dielectric loss	Lower	Lower	Higher
Electrical resistivity		Lower	Higher
Coercive force		Higher	Lower
Remnant polarization		Lower	Higher
Piezoelectric coefficient		Lower	Higher
Aging	Higher	Lower	Lower
Coupling coefficient		Lower	Higher
Mechanical quality factor		Higher	Lower
Elastic compliance	Lower	Lower	Higher
Strain hysteresis		Lower	Higher
Hysteresis squareness	Lower	Lower	Higher

**TABLE 3.8 Formulations for NPO Capacitors**

	Composition, wt%		
	1	2	3
BaTiO <sub>3</sub>	41–49	39–47	15–21
TiO <sub>2</sub>	48–54	41–47	26–34
ZrO <sub>2</sub>		8–13	
Nd(CO <sub>3</sub> ) <sub>4</sub>			59–45
Other	3–7	2–5	Small
$k'$ (25°C, 1 kHz)	35	30	62
$\tan \delta$	<0.002	<0.002	<0.002

used for precision positioning; pumps; vibration cancellation; loudspeakers; resonators and filters for radios and televisions; and ultrasonic generators for medical devices, milling, and cleaning. These applications range from the scale of semiconductor processing for electromechanical switches or miniature arrays to several-ton transducer arrays used in active sonar.

TABLE 3.9 Formulations for X7R Capacitors

	Composition, wt%			Comment
	1	2	3	
BaTiO <sub>3</sub>	90–97	85–92	86–94	Base material
CaZrO <sub>3</sub>	2–5	4–8		Shifter
BaCO <sub>3</sub>	0–5			Stoichiometry adjustment
SrTiO <sub>3</sub>		3–6		Shifter
Bi <sub>2</sub> O <sub>3</sub>			5–10	Depressor, flux
Other	2–5	1–4	2–6	
<i>k'</i> (25°C, 1 kHz)	1600–2000	1800	1400–1500	
tan $\delta$	<0.025	<0.025	<0.015	

TABLE 3.10 Formulations for Z5U Capacitors

	Composition, wt%			Comment
	1	2	3	
BaTiO <sub>3</sub>	84–90	65–80	72–76	Base material
CaZrO <sub>3</sub>	8–13			Shifter
MgZrO <sub>3</sub>	0–3			Depressor
SrTiO <sub>3</sub>		7–11	5–8	Shifter
CaTiO <sub>3</sub>		7–11	4–6	Depressor
BaZrO <sub>3</sub>		7–11	7–10	Shifter
CaSnO <sub>3</sub>			2–4	Shifter
Other	1–3	8–13	0–3	
<i>k'</i> (25°C, 1 kHz)	5700–7000	5500–6500	11,500–13,000	
tan $\delta$	≤0.03	≤0.03	≤0.03	

### 3.4.1 Piezoelectrics

The piezoelectric effect was first discovered in 1880 by Pierre and Jacques Curie in naturally occurring crystals such as quartz and Rochelle salt. The first significant application for piezoelectrics occurred during World War I, when Langevin developed a means of generating acoustic waves in water for signal-

ing and detection of German submarines. These early forms of active sonar employed the use of piezoelectric quartz. In 1920, ferroelectric behavior was discovered in Rochelle salt by Joseph Valasek. Because of its large piezoelectric effect, Rochelle salt became widely used in microphones, phonographs, loudspeakers, recorders, and oscillographs. In 1930, Sawyer and Tower developed a circuit to record the hysteresis behavior of this ferroelectric. The first polycrystalline piezoelectrics, based on  $\text{BaTiO}_3$ , were discovered by Von Hippel and others in the mid 1940s. R. B. Gray and S. Roberts were among the first to develop piezoelectric ceramics by “poling” ferroelectrics. The ferroelectric behavior of lead titanate was discovered in 1950. In 1952, piezoelectric behavior was discovered in tungsten-bronze structure lead niobate. In the mid 1950s, PZT (lead zirconate titanate) was developed and became the most widely used piezoelectric ceramic to date. The first piezoelectric polymer, polyvinylidene fluoride, was developed in 1969 by stretching it under high fields. More recently, a variety of complex niobate based piezoelectrics with very high piezoelectric coefficients have been developed. Multilayer and thin film processing have dramatically expanded the applications of this important group of materials.

### 3.4.2 Ferroelectrics

Polycrystalline piezoelectric materials exhibiting ferroelectric behavior are the center of attention, because they can be readily formed into various shapes and sizes using conventional processing. Ferroelectricity is the spontaneous alignment of dipoles as a result of their mutual interaction. At lower temperatures, the electric dipoles in a ferroelectric material create a local field that is stronger than the thermal energy required for randomization and spontaneous polarization results. Without external applied forces, the dipoles align in regions or domains. The various domains are then oriented along different crystallographic directions resulting in the lowest (strain) energy state and a net-zero polarization for the fired ceramic compounds of the perovskite structure shown in Fig. 3.16. These include  $\text{Pb}(\text{Zr}, \text{Ti})\text{O}_3$  (PZT),  $\text{BaTiO}_3$ ,  $\text{Pb}(\text{Mg}_{1/3}\text{Nb}_{2/3})\text{O}_3$  PMN, and  $\text{Pb}(\text{Zn}_{1/3}\text{Nb}_{2/3})\text{O}_3$  PZN. In addition, tungsten-bronze structures such as  $(\text{Sr}, \text{Ba})\text{Nb}_2\text{O}_6$ ,  $\text{PbNb}_2\text{O}_6$ , and  $\text{LiNb}_2\text{O}_6$  are often ferroelectric.

These compounds are typically cubic and therefore paraelectric at high temperature. As the material is cooled, a change to a ferroelectric phase occurs at the Curie temperature,  $T_C$ , and spontaneous polarization results. The perovskite ferroelectric phase is typically tetragonal or rhombohedral. Most of the perovskite compounds readily form solid solutions with one another, allowing substantial substitution to achieve optimal performance. Often, solid solutions are formed with perovskites of different crystal structures, which results in a composition range wherein two different ferroelectric phases are present—the morphotropic phase boundary. Figure 3.21 shows the effect of solid solutions between ferroelectric  $\text{PbTiO}_3$  and antiferroelectric  $\text{PbZrO}_3$ . It is generally desirable to develop compositions near the morphotropic phase boundary because, at this region, the dielectric and piezoelectric properties are maximized, as shown in Fig. 3.22.

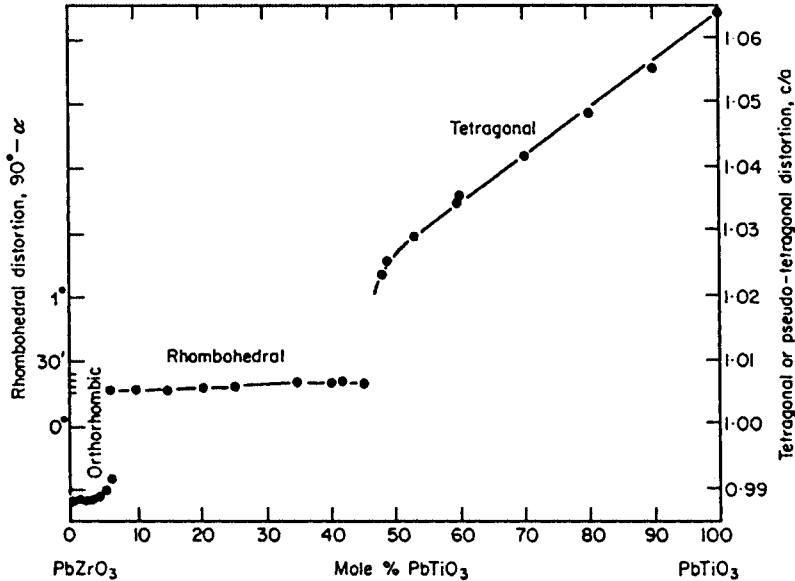


Figure 3.21 Unit cell dimension change vs. temperature in the PZT system.<sup>13</sup>

When a ferroelectric is cooled through its Curie region, the cubic lattice deforms to a polar phase. The polarization orients into regions, or domains, so as to minimize intergranular stresses. The dipoles of adjacent domains align along crystallographic axes.

Figure 3.23 shows how polarization changes with applied field in a ferroelectric material. At low initial fields, polarization increases nearly linearly with field. As higher fields are applied, the domains begin to align with the field and grow. The polarization increases more rapidly. Ultimately, a significant portion of the domains are aligned with the field, and little additional polarization results as the field is raised. The highest polarization achieved at high fields (>2 MV/m) with all dipoles aligned is the saturation polarization,  $P_S$ . When the external electric field is released, most of the dipole alignment remains, and there is a remnant polarization,  $P_R$ . The domain alignment can again be randomized to a net-zero polarization by reversing the polarity of the field. The field required to achieve this is the coercive field,  $E_C$ . As fields of opposite polarity are increased, the domains again align with the field, resulting in polarization of opposite polarity. This behavior under applied AC fields results in the hysteresis loop shown in Fig. 3.23. The hysteresis in the P-E relationship indicates energy lost in moving domain boundaries. The process of applying a high electric field to a polycrystalline ferroelectric to obtain a high remnant polarization, *poling*, is necessary to achieve strong piezoelectric behavior.

The piezoelectric expansion or contraction in the direction of an applied field results from alignment and stretching of dipoles in the material with the applied field. The expansion is linear and directly proportional to the magnitude

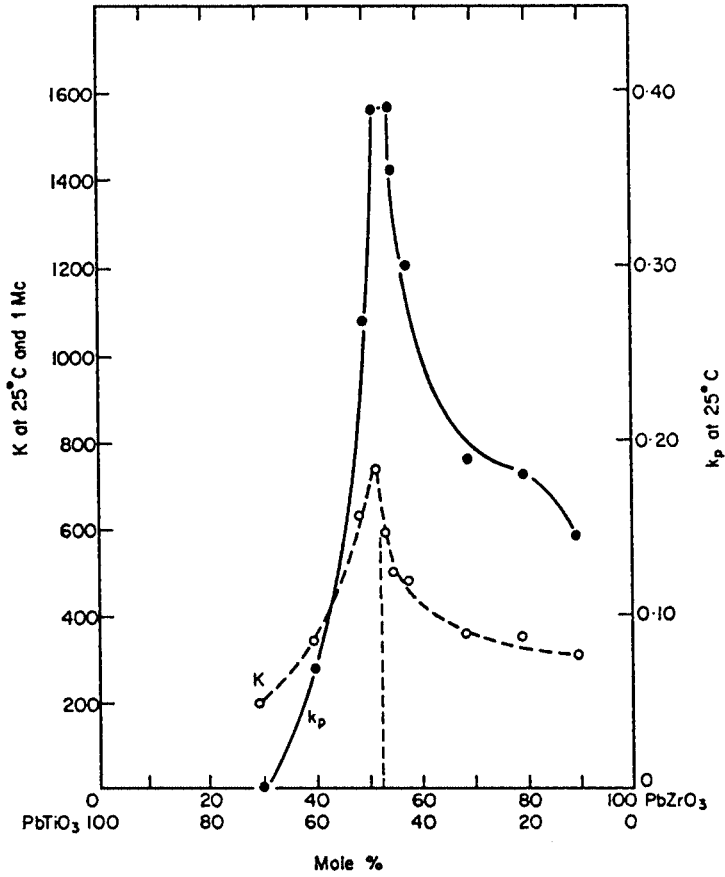


Figure 3.22 Dielectric constant and planar piezoelectric coupling coefficient for compositions near the morphotropic phase boundary in PZT.<sup>13</sup>

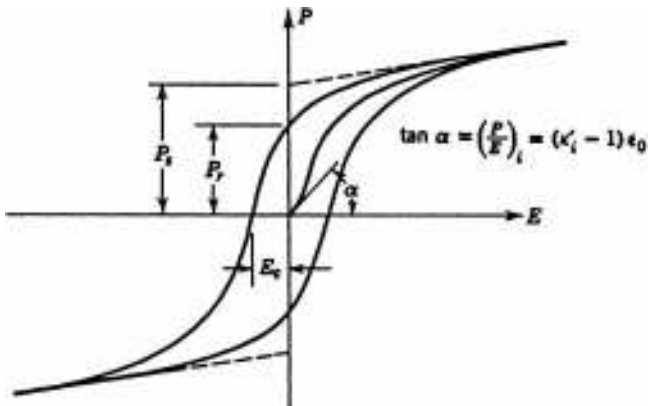


Figure 3.23 Electronic polarization vs. field for a ferroelectric material.<sup>14</sup>

and polarity of the applied field. Piezoelectric ceramics have reorientable dipoles; therefore, dipolar reorientation may occur if energy is added by electric fields, heat, or pressure. Reorientation by field (poling) is an integral part of the fabrication of a piezoelectric ceramic. Poling creates the initial remnant dipolar orientation in the material. Because all of the reorientation mechanisms involve energy inputs, there is an intrinsic energy loss during any reorientation; this energy loss is proportional to the hysteresis.

### 3.4.3 Electrostrictors

More recent developments of complex perovskite structures has resulted in a new class of electromechanical materials, *electrostrictors*. Purely electrostrictive materials are paraelectric and centrosymmetric; that is, they do not possess a polar axis and are typically cubic. The electrostrictive materials of most interest are ferroelectrics that are operated above or near their transition temperatures. The electrostrictive effect is a second-order phenomenon whereby an applied electric field results in a lattice distortion and mechanical distortion in the material.

During the 1980s, substantial research on electrostrictive materials, particularly PMN-based materials, occurred in the U.S. and Japan. Significant improvements in electrostrictive materials were made, achieving a pyrochlore-free perovskite near the morphotropic phase boundary. Researchers at Martin Marietta Laboratories<sup>4</sup> formed the perovskite phase using a sol-gel process and a mixed oxide process with barium titanate (BT) and strontium titanate (ST) additions. In particular, the base composition  $0.855\text{Pb}(\text{Zn}_{0.33}\text{Nb}_{0.67})-0.195\text{PbTiO}_3-0.05\text{BaTiO}_3$ , has yielded some of the highest effective piezoelectric coefficients available (i.e., low-field  $d_{33} = 500$  to  $750$  pC/N).

The field induced strain in piezoelectric and electrostrictive materials is on the order of  $10^{-4}$  to  $10^{-3}$  and is a function of applied mechanical stresses, electric fields, and thermal expansion. Under isothermal conditions, the net elastic strain in a material is given by

$$\varepsilon_{ij} = S_{ijkl}\sigma_{ij} + g_{ijk}P_k + Q_{ijkl}P_kP_l + \dots = S_{ijkl}\sigma_{ij} + d_{ijk}E_k + M_{ijkl}E_kE_l + \dots \quad (3.5)$$

where the  $S_{ijkl}\sigma_{ij}$  term describes the mechanically induced strain, the  $g_{ijk}P_k$  term describes the first-order piezoelectric response, and the second-order  $Q_{ijkl}P_kP_l$  term describes the electrostrictive contributions.

Figure 3.24 shows the transition region for a typical polycrystalline ferroelectric material. The material is cubic and paraelectric, and it exhibits purely electrostrictive behavior well above the transition region and piezoelectric, rhombohedral, or tetragonal below the transition. In the transition region, polarization is maximized as demonstrated in Eq (3.5).

Observing the strain response as a function of applied field across the transition region shows quadratic, low-hysteresis behavior at higher temperatures (Fig. 3.25). The dielectric permittivity is maximized at the transition region along with the dielectric loss. The polarization versus field plots show no hysteresis and no remnant polarization well above  $T_C$ . In pure electrostrictors, the first-order strain term in Eqs. (3.5) and (3.7) becomes negligible, and the



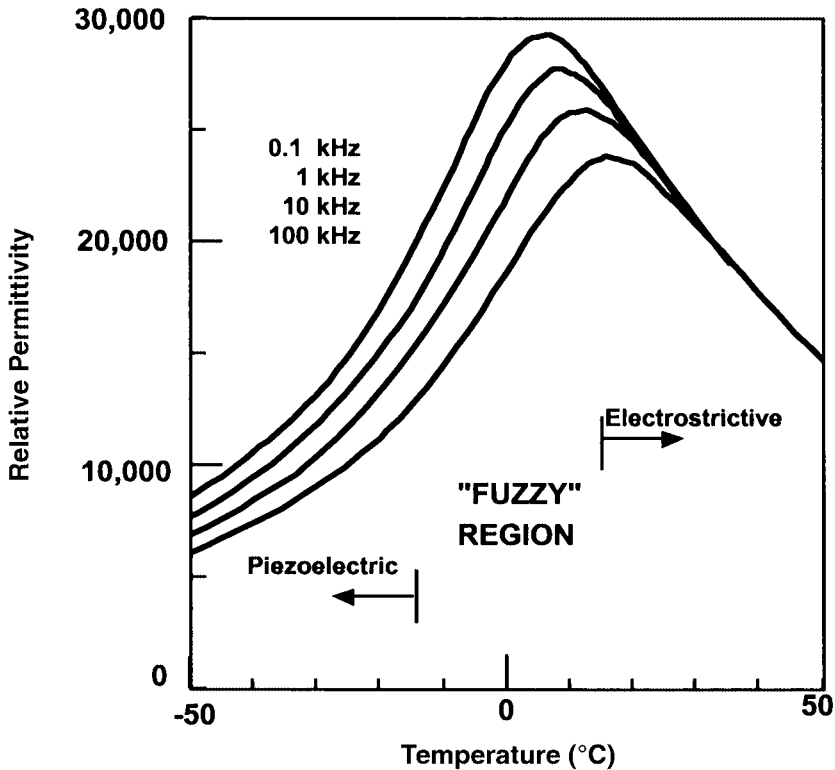
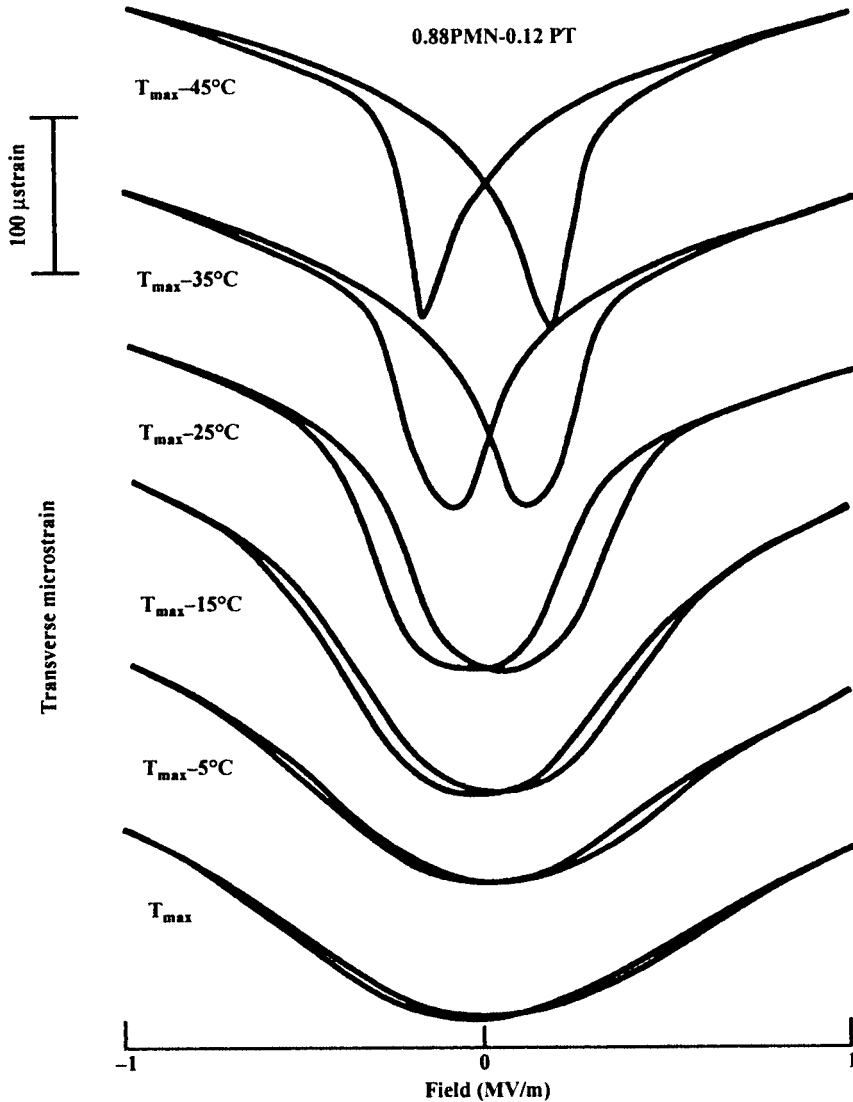


Figure 3.24 Schematic view of the weak-field dielectric properties of the relaxor ferroelectrics of interest.<sup>22</sup>

relation of strain to polarization or field becomes quadratic (at low fields). Electrostrictive strain is a result of a lattice distortion with applied field. Expansion of the material is observed in the direction of the applied field, regardless of the field polarity. Increasing polarization, strain, and hysteresis are observed as the material is cooled. Polarization and field-induced strain are maximized near the transition region. Ultimately, significant effects of the polar axis switching are observed; that is, large hysteresis and contraction with alternating fields (the butterfly response). Piezoelectrics expand under fields of the same polarity as the poling field but also contract under negative fields. Table 3.11 shows the properties of piezoelectric standards as well as common piezoelectric and electrostrictive materials.

### 3.4.4 Materials

“Hard” piezoelectric materials, Type I–IV, are typically formulated to operate well below the transition region. The piezoelectric phase is highly stable and typically formulated for high coercive force and minimal domain wall movement (minimal aging). This results in a material wherein the  $d$  coefficient is lower, but the hysteresis is relatively small as a result of minimal domain wall movement. This type of material is the most common electromechanical mate-



**Figure 3.25** Strain vs. field and temperature for a ferroelectric, showing piezoelectric response well below  $T_C$  and a more quadratic electrostrictive response as  $T_C$  is approached.<sup>22</sup>

rial, used in passive and active sonar as well as in many commercial applications where high induced force and stable response are needed.

“Softer” piezoelectrics, Type V and VI, are formulated to operate closer to the transition region, achieving higher strains with higher polarization. Typically, this results in corresponding higher hysteresis and dielectric losses, and they are more susceptible to pressure depoling and aging. These materials are attractive for high sensitivity passive transducers and actuator applications where high field induced strains are desired.

TABLE 3.11 Piezoelectric Standards and Properties of Selected Materials

Powder	Curie temperature (°C)	Room-temperature permittivity	Aging rate	$d_{33}$ or effective $d_{33}$ (pC/N)	Hysteresis (%) <sup>*</sup>
<i>Navy Standards</i>					
Type I	325	1275 ± 12.5%	-4.5 ± 2.0%	-4.5 ± 2.0%	1-3
Type II	350	1725 ± 12.5%	-1.5 ± 0.7%	-1.5 ± 0.7%	
Type III	325	1025 ± 12.5%	-4.0 ± 1.5%	-4.0 ± 1.5%	
Type IV	115	1275 ± 12.5%	-1.5 ± 0.5%	-1.5 ± 0.5%	
Type V	240	2500 ± 12.5%	-2.0 ± 1.0%	-2.0 ± 1.0%	
Type VI	180	3250 ± 12.5%	-2.0 ± 1.0%	-2.0 ± 1.0%	
MMC (129) PMN	25	23,000		760	1-4
MMC (100) PMN	33	18,000		850-1000	1-3
MMC PZN-PT-BT	144	3000-3500		650	10-11
0.91 PZN-0.09PT, single crystal	178	2200-4100		1500	
BaTiO <sub>3</sub>	120	1400-2000		191	
PbTiO <sub>3</sub>	500				
Pb(Ti <sub>0.48</sub> Zr <sub>0.52</sub> )O <sub>3</sub>				223	
U5H-32 <sup>†</sup> PZT	195	2500		600	11-12

<sup>\*</sup>Measurement taken at 20°C

<sup>†</sup>Ultrasonics Corporation, South Plainfield, NJ

Soft electrostrictors operate just above the transition region, where strains are maximized as a result of contributions of both piezoelectric and electrostrictive effects. This combined effect results in materials that achieve the highest electromechanical energy density and possess the highest degree of sensitivity. However, these materials are highly temperature sensitive and require high-power drivers in active roles because of the corresponding high capacitance and power dissipation.

Hard electrostrictors are formulated for low hysteresis and therefore operate well above the transition region where pure electrostrictive behavior is observed. These materials have excellent *shape memory* because of their low hysteresis and are well suited for precision positioning applications such as deformable mirrors.

Table 3.12 shows the properties of various piezoelectric transducer materials. Generally, materials with lower piezoelectric coefficients have significantly higher coercive fields, resulting in a more stable piezoelectric response.

TABLE 3.12 Properties of Piezoelectric Transducer Materials

Material	Dielectric Constant	$d_{33}$ (pC/N)	$d_{31}$ (pC/N)	$g_{33}$ ( $10^3$ m <sup>2</sup> /C)	$d_h g_h$	$k_p$
PbNb <sub>2</sub> O <sub>6</sub>	225	85	-10		2300	
Pb <sub>0.5</sub> Ba <sub>0.5</sub> Nb <sub>2</sub> O <sub>6</sub>		220	-90			
PbTiO <sub>3</sub>		51	-4			
BaTiO <sub>3</sub>		190	-79	13		0.36
PZT		223	-93.5			0.52
PZT	1800	450	-205		100	
.855PZN-.095PT-.05BT	3000-3500	540	-228		279	
.873PZN-.097PT-.03BT	1825	440	-196		143	
PLZT 2/65/35		150		23		0.45
PLZT 7/60/40		710		22		0.72
PLZT 7/55/45		405		15		0.56

In most electromechanical materials, dopants are used to tailor the properties for specific applications. Isovalent substitutions are often used to modify the dielectric properties of these materials. For instance, Ba<sup>2+</sup> or Sr<sup>2+</sup> substitution for Pb<sup>2+</sup> in perovskite and tungsten-bronze structures or Sn<sup>4+</sup> for Zr<sup>4+</sup> in PZT. The perovskite and tungsten-bronze structures will allow significant substitution with isovalent ions of similar size.

The Pb(Zn<sub>1/3</sub>Nb<sub>2/3</sub>)O<sub>3</sub> (PZN) materials are cubic above the transition temperature ( $T_C$ ), 140°C, and undergoes a diffuse phase transition to rhombohedral as it is cooled below  $T_C$ . PT is cubic above its Curie temperature of 490°C and undergoes a diffuse phase transition to tetragonal as it is cooled below  $T_C$ . The resulting solid solution of these results in a morphotropic phase transition between the rhombohedral and tetragonal phases at 9 percent PT. Additions of barium titanate (BT) to PZN-PT allow formation of pure perovskite near the morphotropic phase boundary where properties are maximized.

The ferroelectric phase of tungsten-bronze structure PbNb<sub>2</sub>O<sub>6</sub> is metastable; that is, it normally exists only at high temperatures, >1200°C. However, by doping and rapidly cooling from high temperature, the ferroelectric tetragonal phase can be retained to low temperatures.

Piezoelectrics have been the sensing and broadcasting element of underwater acoustics since its inception. Passive sensors are designed to detect acoustic signals by converting pressure waves or vibrations into electrical signals. Ignoring temperature, bias stress, and electrostrictive effects, Eq. (3.5) reduces to

$$\epsilon_{ij} = g_{ijk} P_k = d_{ijk} E_k \quad (3.6)$$

for a pure piezoelectric material, where

$$\begin{aligned} \varepsilon_{ij} &= \text{strain} \\ P_k &= \text{dielectric polarization vector} \\ E_k &= \text{electric field vector} \\ g_{ijk}/d_{ijk} &= \text{piezoelectric coefficients} \end{aligned}$$

The piezoelectric charge coefficients,  $d_{ijk}$ , are generally expressed using condensed subscripts, such as  $d_{33}$  and  $d_{31}$ , where the first subscript refers to the electric field direction or direction of polarization, and the second subscript refers to the stress or strain direction.

### 3.4.5 Applications of electromechanical materials

By definition, electromechanical materials provide a coupling between electrical and mechanical energy. The mechanical displacements are relatively small, but these materials can generate significant electrical and mechanical forces.

Actuators generate mechanical displacements with electrical inputs for applications that include precision positioning devices, miniature motors, fuel injectors, printer heads, precision machining, noise cancellation, and optical devices such as deformable mirrors. A variety of methods have been developed to achieve practical displacements with practical drive voltages. The practical maximum displacement for an electromechanical ceramic is 0.1 percent at fields of 1 to 2 MV/m. Therefore, 1 mm of material is needed to achieve a displacement of 1  $\mu\text{m}$ . A monolithic block of material would require 1 to 2 kV to achieve this displacement. Multilayer actuators as shown in Fig. 3.26 use ceramic capacitor processing and designs to reduce voltage requirements. The drive voltage required for a multilayer design is reduced by a factor equal to the number of layers. For instance, if the 1-mm thick actuator consisted of ten 0.1-mm layers, the drive voltages for the 1- $\mu\text{m}$  displacement would be reduced to 100 to 200 V.

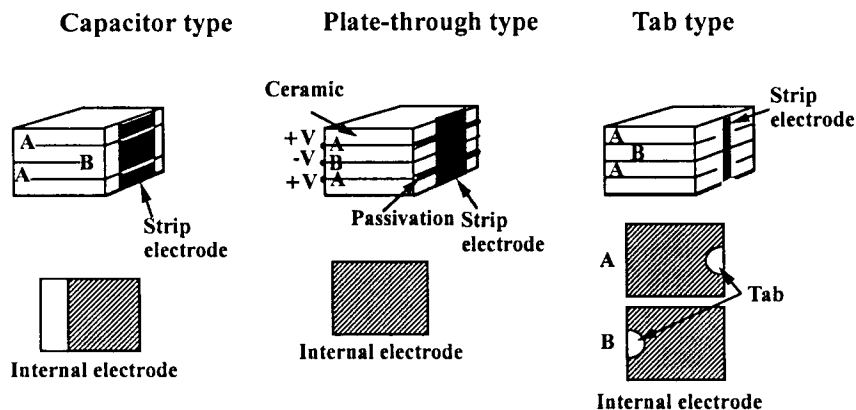
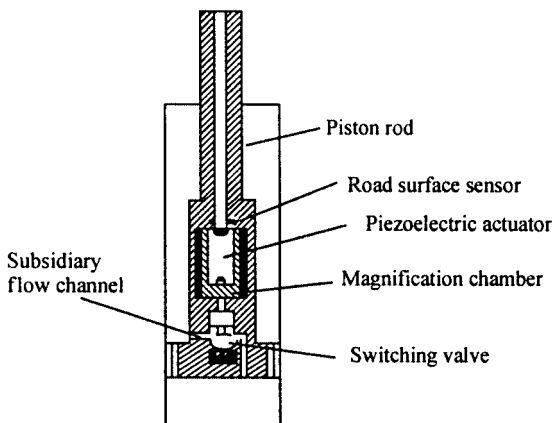


Figure 3.26 Actuator electrode and termination configurations.<sup>22</sup>

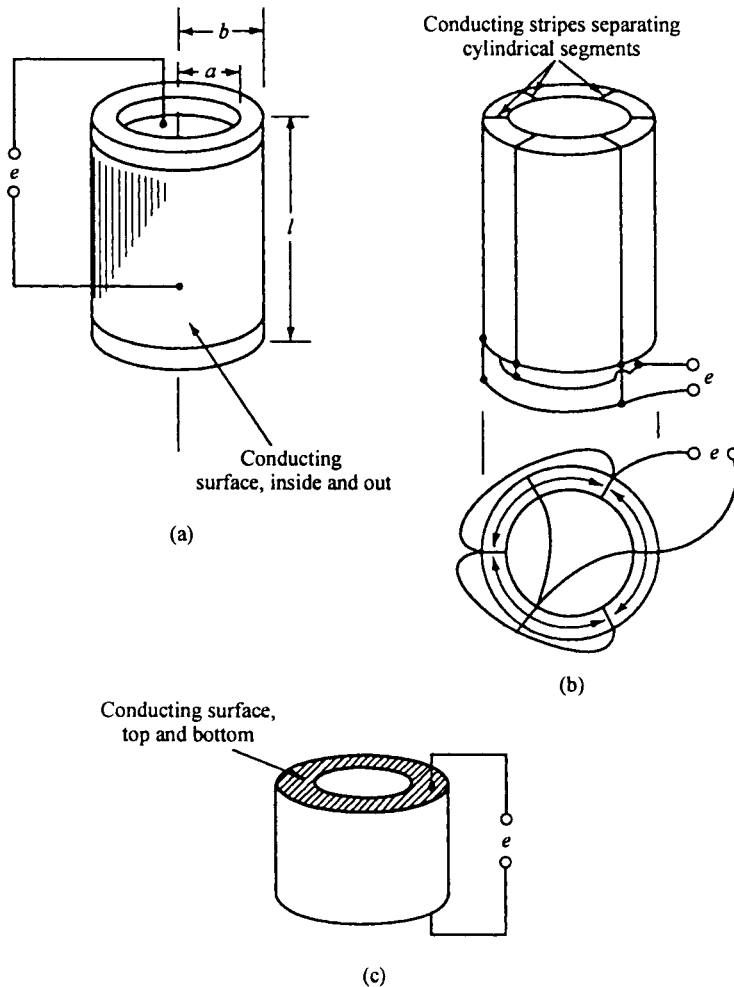
The Toyota Electronically Modulated Suspension (TEMS) uses piezoelectric sensors and actuators in a vibration cancellation role shown in Fig. 3.27. The system senses the road vibrations with a five-layer piezoelectric sensor. When rough roads or hard turns are encountered, the sensor is stressed and generates an electronic signal. The signal is amplified by a control unit that outputs a voltage to the 88-layer piezoelectric actuator. The actuator expands up to  $50\ \mu\text{m}$  on a hydraulic motion amplifier, which expands to 2 mm. This displacement stiffens the damping force of the shock absorbers, all within a 20-ms period.

Acoustic transducers convert electrical inputs into acoustic signals, i.e., projectors, or convert acoustic signals into electrical signals, i.e., sensors. Underwater acoustics applications have driven the development of piezoelectric ceramics. Hydrophones, such as those shown in Fig. 3.28, are the passive sensing devices in underwater acoustic applications. Hydrophones take advantage of the direct piezoelectric effect; that is, acoustic inputs in the form of pressure changes result in an electrical output. Hydrophones are designed for collecting inputs from a broad frequency band, 0.1 to 100 kHz. The higher frequencies allow higher resolution but are rapidly dissipated in water. Lower frequencies are therefore used for longer-range detection.

In sonar projector applications, acoustic power is applied to the water by an active surface. In most active sonar applications, the device operates at a natural resonant frequency so as to minimize the power requirements for large displacements. Projectors are the active devices for sound generation in underwater acoustics. Sonar projectors take advantage of the converse piezoelectric effect by converting large electrical signal inputs into mechanical outputs in the form of pressure changes, or sound waves. Projectors are typically designed to operate at resonance for maximum source level; therefore, the operating frequency band of individual devices is narrow. Often, arrays of projectors operating at different frequencies are used to produce broadband acoustic sources.



**Figure 3.27** Schematic of the Toyota Electronically Modulated Suspension (TEMS) shock absorber.<sup>21</sup>



**Figure 3.28** Ceramic cylindrical hydrophones: (a) radial mode, (b) tangential mode, and (c) longitudinal mode.<sup>6</sup>

Two types of sonar projectors are shown in Fig. 3.28. The Tompitz projector uses a stack of longitudinally poled piezoelectric slabs. The slabs are doughnut shaped so that a center bolt can be used to connect the head mass to the tail mass and prestress the multilayer ceramic stack. The slabs typically are metallized with thick film, fire-on metals with thicker metal shims separating slabs for better current carrying capability. The multilayer stack is electrically connected in parallel.

Flexensional transducers also contain a longitudinally poled stack of piezoelectric slabs, electrically connected in parallel and inserted into an elliptical metal ring. The metal ring is designed to have a center opening somewhat smaller than the ceramic stack so that the metal ring must be compressed along the short axis to insert the stack. This is an effective method for pre-

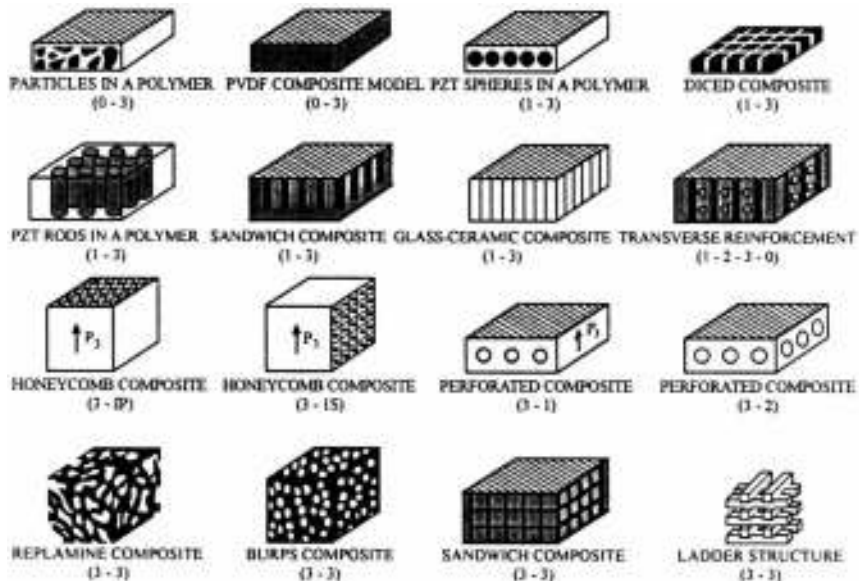
stressing the multilayer stack. The approximately 3:1 aspect ratio of the flextensional transducer amplifies the mechanical displacement along the minor axis. The flextensional transducer obeys conservation of energy laws, so the 3:1 amplitude improvement is at the expense of a 3:1 reduction in the force generated along the minor axis direction.

Ultrasonic transducers for medical imaging utilize piezoelectric ceramics and composites to generate an ultrasonic beam that can penetrate soft tissue. The same transducer then picks up the reflections off internal structures, organs, fetuses, and so on. These transducers most often consist of square cross-section piezoelectric rods in a polymer matrix. These are formed by a dice-and-fill process. Figure 3.29 shows various piezoelectric-polymer composites used to optimize the performance for various applications. The diced 1-3 composite is typically used in ultrasonic transducer applications.

### 3.5 Electro-optic materials

The electro-optic effect is simply a change in optical properties, namely refractive index, with an applied field. Changes in refractive indices are relatively small, on the order of  $10^4$ ; however, this is sufficient to modulate the phase or intensity of transmitted light. A half-wavelength change in phase is sufficient to modulate polarized light from 0 to 100 percent transmission.

The first observation of natural optical anisotropy was made in 1669, by Bartolinus, in calcite crystals, in which light travels at different velocities depending on the direction of propagation relative to the crystal structure. The electro-optic effect, electric field-induced anisotropy, was first observed in



**Figure 3.29** Piezoelectric-polymer composite configurations used to optimize ultrasonic transducer and hydrophone performance.<sup>16</sup>



glass, in 1875, by J. Kerr. Kerr found a nonlinear dependence of refractive index on an applied electric field. The “Kerr effect” is used to describe the quadratic electro-optic effect observed in isotropic materials. The linear electro-optic effect was first observed in quartz crystals in 1883, by W. Rontgen and A. Kundt. Pockels broadened the analysis of this relationship in quartz and other crystals, which led to the term *Pockels effect* to describe linear behavior. In the 1960s several developments in the areas of materials and processing led to the concept of electro-optic ceramics. The development of hot-pressing techniques enabled the fabrication of fully dense ceramic bodies with a high degree of transparency. The first electro-optic ceramics developed at Sandia National Laboratories were based on the solid solution of lead zirconate-lead titanate (PZT). By 1969, the first transparent ceramics of lanthanum-doped PZT (PLZT) were fabricated. G. Hartling and C. Land have extensively studied the electro-optic properties of PLZT and defined the composition dependence. The first single crystals of  $\text{Sr}_x\text{Ba}_{1-x}\text{Nb}_2\text{O}_6$  were fabricated in 1966 by A. Ballman and H. Brown. The large electro-optic coefficients were attractive for applications in laser modulation and deflection devices.

To sufficiently describe this effect, a review of optical properties of materials is necessary. The refractive index of a material is a measure of the reduction in the speed of light as it travels through a transparent material, that is,

$$n = \frac{c}{c_{\text{material}}} \quad (3.7)$$

where  $c$  = the speed of light in vacuum,  $3 \times 10^8$  m/s

Because  $\lambda = cv$ , a reduction in the speed of light results in a reduction in wavelength,  $\lambda$ .

The speed of light is affected as a result of the interaction with the electronic structure of the medium in which it is traveling. Materials containing large ions or negatively charge ions whose outer electrons are not so tightly bound (i.e., having high polarizability) have a stronger interaction with electromagnetic waves. In general, materials with more dense crystal structures lower the speed of light and result in higher refractive indices. The index of refraction of various transparent materials is shown in Table 3.13. Refractive index is somewhat dependent on the wavelength of the incident light. Typically, there is an increase in index at low wavelengths and a reduction at high wavelengths. Figure 3.30 shows the variation in refractive index for a variety of optical materials as a function of wavelength. The amount of light reflected or refracted at the interface between two different materials is determined by their refractive indices. The amount of light reflected at an angle equal to the incident angle is given by Fresnel's formula,

$$R = \left( \frac{n - 1}{n + 1} \right)^2 \quad (3.8)$$

for reflection in air.

TABLE 3.13 Index of Refraction for Various Transparent Materials

Material	Refractive index
Air	1.003
Soda-lime-silica glass	1.52
Fused quartz	1.46
Quartz	1.5/1.6
Calcite, CaCO <sub>3</sub>	1.56/1.74
ZnSe	2.62
SrTiO <sub>3</sub>	2.49
Strontium barium niobate	2.34
LA-doped lead zirconate titanate (PLZT)	2.50
BaTiO <sub>3</sub>	2.40
LiNbO <sub>3</sub>	2.31

The degree of refraction at the interface resulting from the change in light velocity is given by Snell's law,

$$\frac{\sin \phi_i}{\sin \phi_r} = \frac{n_2}{n_1} \quad (3.9)$$

where  $n_2$  is the refractive index of the material through which the light is refracted. Unpolarized (white) light contains randomly oriented electric field vectors, phases, and wavelengths. Both the reflected and refracted light undergo polarization of the electric field component vibrations. When unpolarized light contacts an interface, the reflected wave will have an electric field component whose vibrations tend to polarize perpendicular to the plane of incidence. This is illustrated in Fig. 3.31. The refracted wave vibrations tend to polarize parallel to the plane of incidence.

The direction of polarization in an isotropic material is always parallel to the applied field. The velocity of light travelling in an anisotropic material is dependent on both the direction of polarization and propagation. The optic axis is the crystallographic direction in which light will propagate at a speed that is independent of the polarization plane. When the electric displacement component of light vibrates at right angles to the optic axis, regardless of direction, the ray is called *ordinary*. For rays that vibrate parallel to the optic axis, *extraordinary* waves, the speed is dependent on the direction. The difference in refractive index between that of the ordinary wave,  $n_o$ , and the extraordinary wave,  $n_e$ , is the birefringence,  $\Delta n$ . Birefringence is a measure of the phase difference between the ordinary and extraordinary waves. The relative impermeability of a material is given by

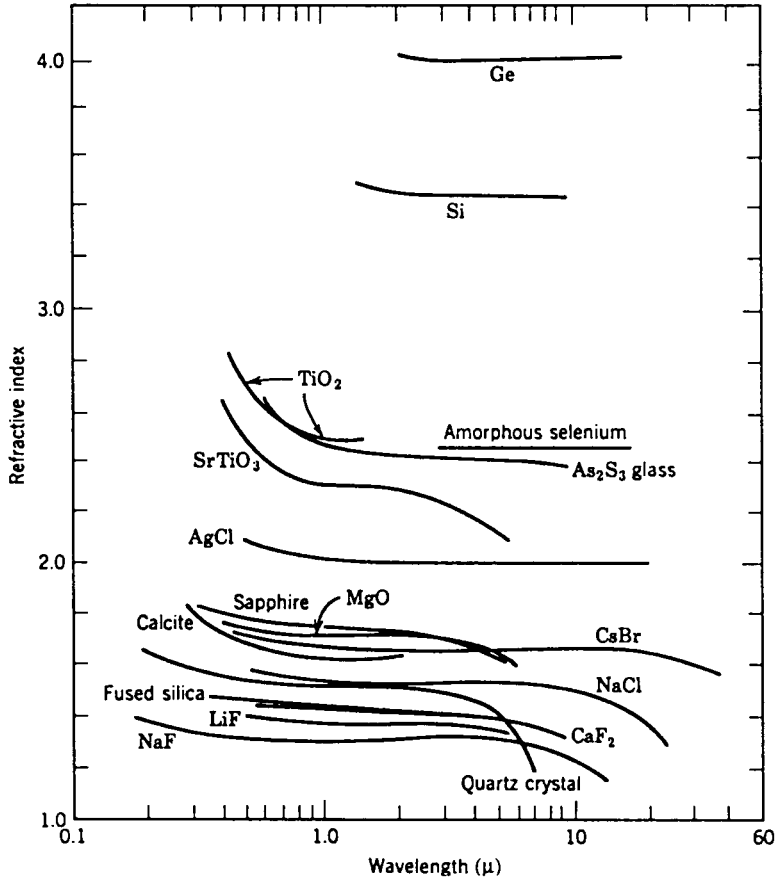


Figure 3.30 Change in refractive index with wavelength for several crystals and glasses.<sup>14</sup>

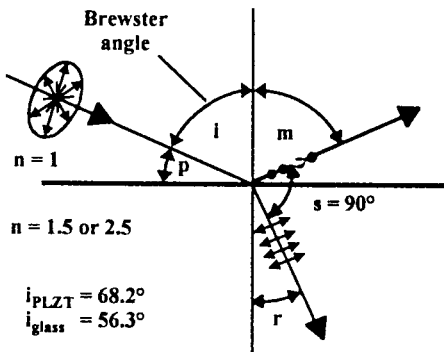


Figure 3.31 Polarization effects in unpolarized light on reflection and refraction.<sup>16</sup>

$$B_{ij} = \frac{1}{\epsilon_r} = \frac{l}{n^2} \quad (3.10)$$

where  $\epsilon_r$  = relative permittivity  
 $n$  = refractive index for the material

In reference to the principal axes of a crystal, the relation becomes the optical indicatrix,

$$B_{ij}x_i x_j = \frac{x_1^2}{n_1^2} + \frac{x_2^2}{n_2^2} + \frac{x_3^2}{n_3^2} = 1 \quad (3.11)$$

Application of a field causes a distortion in the optical indicatrix of  $\Delta B_{ij}$ . The electro-optic effect can be described in terms of the relative impermeability,  $\Delta B_{ij}$ , dependence on applied field,

$$\Delta B_{ij} = r_{ijk} E_k + R_{ijkl} E_k E_l \quad (3.12)$$

where  $r_{ijk}$  = linear Pockels electro-optic coefficients  
 $R_{ijkl}$  = quadratic Kerr electro-optic coefficient

When a field is applied to an anisotropic crystal, the change in refractive index is

$$\Delta n = \frac{-n^3 r_c E}{2} \quad (3.13)$$

where  $r_c = r_{33} - \frac{n_o^3 r_{13}}{n_e^3}$

These relationships describe the linear Pockels electro-optic effect.

When a field is applied to an isotropic crystal, the change in refractive index is

$$\Delta n = \frac{-n^3 (R_{11} - R_{12}) E^2}{2} \quad (3.14)$$

These relationships describe the quadratic Kerr electro-optic effect.

Just as the permittivity and polarization of a dielectric is dependent on the applied field, so is the refractive index; that is,

$$n = n_o + aE_o + bE_o^2 + \dots \quad (3.15)$$

The refractive index at no applied field is represented by  $n_o$ . The  $aE_o$  component represents the linear behavior between the refractive index and applied

electric field for materials that are noncentrosymmetric. The quadratic relationship between refractive index and applied field, the  $bE_o^2$  term, is seen in glasses and isotropic materials. In isotropic materials, the refractive index is the same, regardless of the direction of light propagation, and the polarization state of the incident light remains unchanged. As an electric field is applied, there is distortion of the electronic structure of the crystal, and the material will then exhibit different refractive indices. Therefore, light passing through the material will split into two rays having different velocities. As the rays recombine on exiting the material, there is interference, resulting in a rotation of the polarization direction. The phase shift, or retardation,  $\Gamma$ , is given by

$$\Gamma = \Delta n t \quad (3.16)$$

where  $t$  is the thickness of the electro-optic material through which the light propagates.

### 3.6 Materials

All electro-optic materials are ferroelectric; that is, they exhibit a spontaneous polarization below  $T_C$ . The material of greatest importance is La-doped  $\text{Pb}(\text{Zr}_z\text{Ti}_{(1-z)})\text{O}_3$ . The phase diagram for PLZT is shown in Fig. 3.32.  $\text{La}^{+3}$  substitutes on the A site of the perovskite structure in place of  $\text{Pb}^{+2}$ , acting as an electron donor. Charge neutrality is maintained by the formation of A or B site vacancies. Although the exact lattice configuration is still unknown, experimental results by Hartling et al. have shown that a significant number of lattice vacancies exist when PZT is doped with La. The result is a reduction in the  $c/a$  ratio and a drop in the  $T_C$ . As  $T_C$  is approached in a ferroelectric, the domain structure is more easily realigned, i.e., low coercive fields. PLZT com-

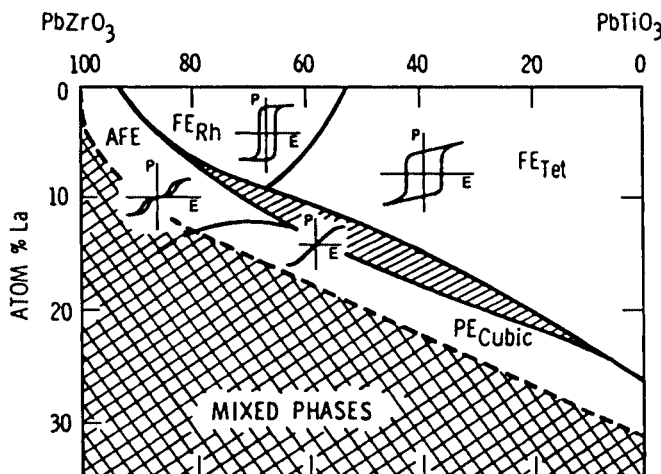


Figure 3.32 Room-temperature phase diagram of the PLZT system illustrating the phases present and typical hysteresis loops associated with each phase.<sup>16</sup>

positions used in electro-optic applications are nearly cubic, and the  $c/a$  ratio is approximately 1.01. Most often, compositions are chosen that lie close to the morphotropic phase boundary between tetragonal and rhombohedral phases where properties are maximized. Compositions on the tetragonal side of the boundary tend to be hard ferroelectrics, i.e., higher coercive fields. Compositions on the rhombohedral side are softer, i.e., lower coercive fields. Table 3.14 shows the electro-optic coefficients for some common electro-optic materials.

**TABLE 3.14 Electro-optic Properties of Various Materials**

Material (single crystals)	$T_C$ , °C	$R$ , $m^2/V^2$	$R_c$ , M/V	$E_c$ , kV/cm
BaTiO <sub>3</sub>	130		19–23	
LiNbO <sub>3</sub>			17.5	
LiTaO <sub>3</sub>			22	
2/65/35	320	$10^{-16}$		13.7
7/65/35	150	$10^{-16}$		5.3
8/65/35	65	$10^{-16}$		3.6
8.5/65/35		$38.6 \times 10^{-16}$		
9/65/35	5	$38. \times 10^{-16}$		0
9.5/65/35	–10	$1.5 \times 10^{-16}$		0
10/65/35	–25	$0.80 \times 10^{-16}$		0
11/65/35		$0.32 \times 10^{-16}$		0
12/65/35		$0.16 \times 10^{-16}$		0
8/90/10		$10^{-16}$		0
8/70/30	20	$11.7 \times 10^{-16}$		0
8/40/60	240		1.0	
8/10/90	355			37.5
12/40/60			1.2	
Sr <sub>0.5</sub> Ba <sub>0.5</sub> Nb <sub>2</sub> O <sub>6</sub>			2.10	
Sr <sub>0.75</sub> Ba <sub>0.25</sub> Nb <sub>2</sub> O <sub>6</sub>			14.0	
KH <sub>2</sub> PO <sub>4</sub>			0.52	
LiNbO <sub>3</sub>			0.17	
LiTaO <sub>3</sub>			0.22	

Transparency is a key requirement of electro-optic materials. Light scattering will occur at discontinuities such as porosity, phase boundaries, and grain boundaries. The best transmission is usually observed in isotropic materials

that are single phase, with a high degree of homogeneity, and fully dense. Although the properties of single-crystal electro-optic materials are superior to those of ceramics, polycrystalline ceramics have a number of advantages over single crystals. Process complexity and cost are perhaps the greatest advantages. Single crystals are typically grown from a molten bath and are limited in size. Polycrystalline materials can be formed in large sizes and complex shapes at relatively low cost. To approach the properties of single-crystal specimens, electro-optic ceramics are typically hot-pressed to achieve full densification. Improvements in homogeneity have occurred with the adoption of wet chemistry methods, such as sol-gel and precipitation, for preparation of the ceramic powders.

### 3.6.1 Applications

Electro-optic behavior falls into three categories: memory, linear, and quadratic. Figure 3.33 shows the characteristic polarization versus field behavior and the change in refractive index with applied field. Devices using the quadratic configuration are based on isotropic compositions with no applied field, such as 8 to 12 percent La additions in  $\text{Pb}(\text{Zr}_{0.65}\text{Ti}_{0.35})\text{O}_3$ . As a field is applied, a ferroelectric-type state is induced. These materials exhibit the quadratic, Kerr, dependence of birefringence on electric field.

Memory characteristic include soft ferroelectric behavior. Compositions exhibiting low coercive forces,  $<1$  MV/m, near the morphotropic phase boundary are typical, such as  $\text{Pb}(\text{Zr}_{0.65}\text{Ti}_{0.35})\text{O}_3$  doped with  $<8$  percent La. Typically, a large field is applied to achieve a large remnant polarization. Intermediate polarization states can be obtained by applying voltages.

Linear characteristics are achieved by forming compositions that are hard ferroelectrics, i.e., in the tetragonal phase region of PLZT, where the coercive fields are large ( $\approx 1.5$  to  $2$  MV/m). Typically, compositions for linear behavior are based on 8 to 12 percent La-doped  $\text{Pb}(\text{Zr}_{0.40}\text{Ti}_{0.60})\text{O}_3$ . To achieve the desired linear characteristics (Pockels behavior), the material first must be poled to achieve high remnant polarization.

Optical shutters utilize the properties of quadratic electro-optic materials as shown in Fig. 3.34. Switching from zero field to the field required for half-wave retardation results in a light shutter. If the electro-optic material is placed between crossed polarizers, polarized light is transmitted through the first polarizer. None of the polarized light is transmitted through the second crossed polarizer at zero applied field. Applying sufficient field causes birefringence and a net rotation of the polarized light by  $90^\circ$ , passing through the second crossed polarizer.

The voltage required to achieve  $90^\circ$  rotation of one wave component relative to the other is given by

$$V = \frac{\lambda t_{field}}{Rt_{prop}} \quad (3.17)$$

where  $\lambda$  = wavelength of the incident light

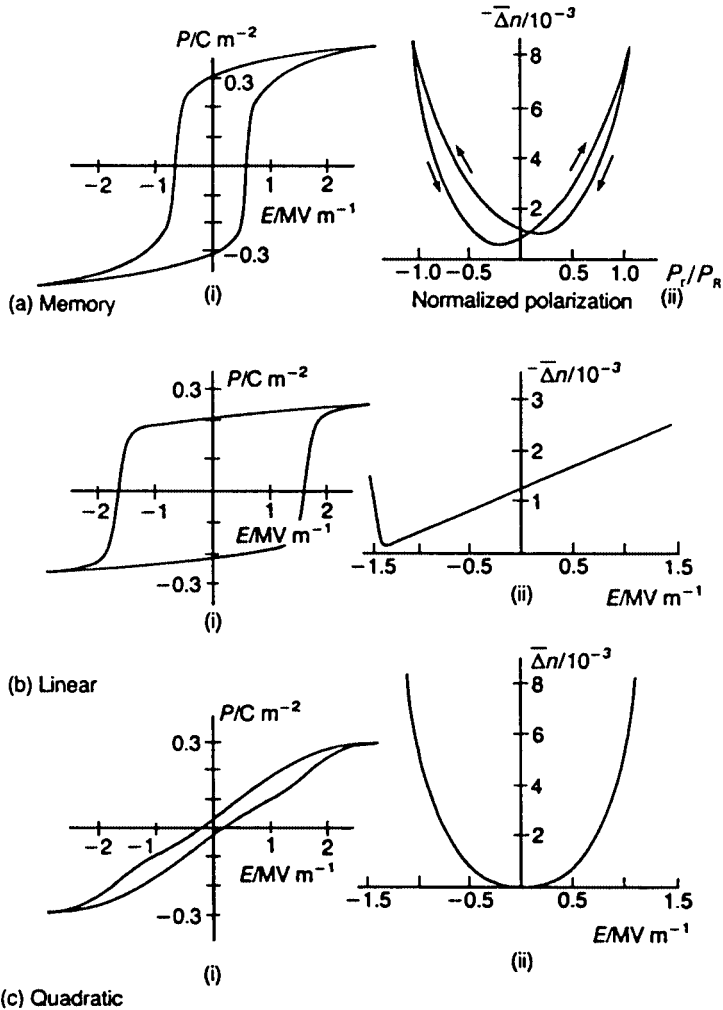


Figure 3.33 Hysteresis and electro-optic characteristics of the three main types of PLZT: (a) memory, (b) linear, and (c) quadratic.<sup>18</sup>

$t_{field}$  = thickness across which an electric field is applied  
 $t_{prop}$  = propagation distance

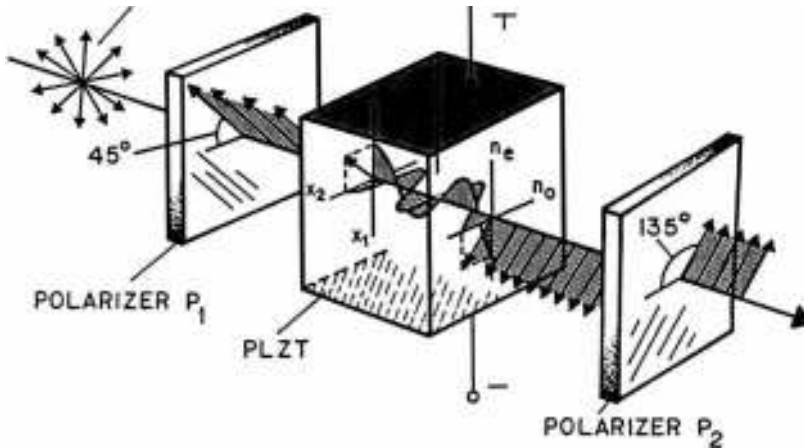
The required voltage can be reduced by increasing the electro-optic coefficient, reducing the material thickness in the applied field direction, or increasing the propagation distance.

The ratio of transmitted light to incident light in a cross-polarized light shutter is given by

$$I_t/I_i = \sin^2(\Delta n\pi/\lambda) \tag{3.18}$$

for monochromatic light of wavelength  $\lambda$ .





**Figure 3.34** Optical phase retardation in an activated PLZT electro-optic ceramic; the open state at half-wave voltage is shown for a crossed-polarizer configuration.<sup>16</sup>

However, when the incident light is white light, there is a retardation of different wavelengths as the electric field is increased. Figure 3.35 shows the Kerr optical interference color chart. It shows transmitted wavelengths and, therefore, colors with applied field for various material birefringence and thickness values.

Electro-optic thin film devices are of two types: one in which the propagation of light is along the plane of the film (optical waveguides), and the other in which the light passes through the film (optical memory and displays). An optical waveguide controls the propagation of light in a transparent material (ferroelectric thin film) along a certain path. For the waveguide to work properly, the refractive index of the film should be higher than that of the substrate. For light to propagate in the waveguide, the thin film should be optically transparent. A great deal of work has been done on making ferroelectric thin film waveguides from  $\text{LiNbO}_3$  and  $\text{Li}(\text{Nb,Ta})\text{O}_3$  using LPE, EGM, and MBE methods. PZT and PLZT thin films are even better candidates for optical waveguide applications because of their large electro-optic coefficients.

Ferroelectric thin films may replace the use of PLZT bulk ceramics for optical memory and display applications. The advantages offered by thin films for display applications include a simplification of the display device design and lower operating voltages as compared to PLZT ceramic devices. Optical memories using PLZT thin films will also need lower operating voltages.

### 3.7 Magnetic Ceramics

Magnetic ceramics differ from magnetic metals in that they are oxides that have lower magnetic moments, high resistivities, and a greater dependency of properties on microstructure; some types of magnetic ceramics, ferromagnetic and ferrimagnetic materials, exhibit remnant induction behavior. Magnetite ( $\text{Fe}_3\text{O}_4$ ) is a naturally occurring magnetic material (lodestone) that

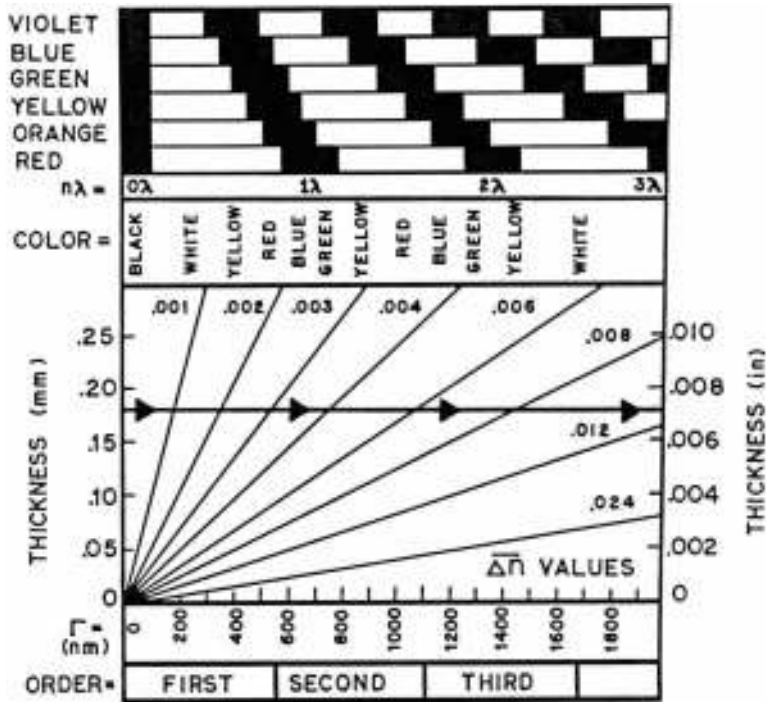


Figure 3.35 A Kerr retardation chart showing the origin of the Newton color orders.<sup>16</sup>

was used as primitive magnets thousands of years ago. Magnetite belongs to the spinel family of minerals, having the general formulation  $M\text{Fe}_2\text{O}_4$ , where M is typically a transition metal ion. Other important crystal structures in magnetic ceramics are iron garnets,  $M_3\text{Fe}_5\text{O}_{12}$ , and magnetoplumbite,  $M\text{Fe}_{12}\text{O}_{19}$ .

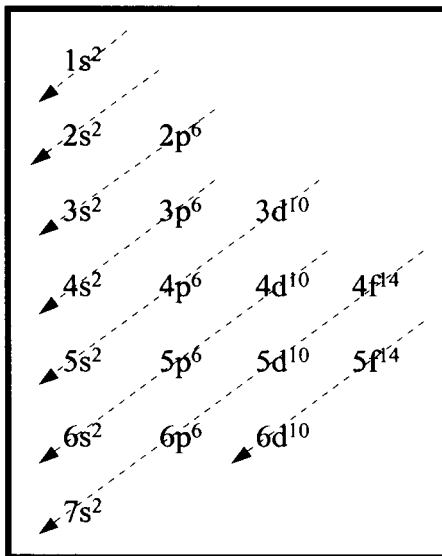
Investigations into the magnetic properties of various spinels began in the early 1900s (Hilpert). Throughout the 1930s, 1940s, and 1950s, there was increasing interest in developing ferrite materials as magnetic cores. These investigations led to the discovery of ferromagnetism (by Neel) in 1948, permanent magnet hexaferrites in 1951 (by Went), and ferromagnetic behavior in other structures such as orthoferrites and garnets. Magnetic garnets were discovered in the mid-1950s by Bertaut and Forrat. Volume production of Cu-Zn ferrite materials for magnetic core applications began in the 1930s. Applications for ferrite ceramics have expanded with the rapid growth of the electronics industry to include inductors, transformers, permanent magnets, magneto-optical devices, electro-mechanical devices, and microwave electronics devices.

A magnetic moment results from current loops. In a magnetic material, this can result from electrons orbiting atomic nuclei, electrons spinning on their own axes, and nuclei contributions. Nuclear magnetic moments are very small and typically are ignored.

The magnitude of magnetic moment for an orbiting electron is a Bohr magneton,

$$\begin{aligned}\mu_B &= \frac{eh}{4\pi m_e} = \frac{(1.602 \times 10^{-19} \text{ C})(6.623 \times 10^{-34} \text{ J/s})}{4\pi(9.109 \times 10^{-31} \text{ kg})} \\ &= 9.274 \times 10^{-24} \text{ Am}^2/\text{electron} \quad (9.274 \times 10^{-21} \text{ erg/Oe})\end{aligned}$$

In most ferrites, the electronic interaction in bonding is such that there is little electron orbital momentum (orbital quenching). The main contribution to magnetic moment is from electron spins that are free to orient with an applied field and that are not cancelled by antiparallel spins on other sublattices. Pauli exclusion principles allow only two electrons to occupy an energy level. These electrons will have opposite spins that cancel their magnetic moments ( $s = +1/2$ ,  $s = -1/2$ ). Permanent magnetic moments are found in solids containing ions with unpaired electrons, such as those containing conduction band electrons; an odd number of electrons; or transition, rare-earth, or actinide elements (because of their incompletely filled inner shells). Figure 3.36 shows the order in which electrons fill electron orbitals in an atom or ion. The superscript represents the number of electrons in each orbital. Electrons are oriented in four types of orbitals (s, p, d, and f) for which the space quantum number,  $l$ , equals 0, 1, 2, and 3, respectively. The orbital quantum number for all the electrons in an ion is equal the sum of the space quantum numbers,  $L = \Sigma l$ . The space quantum number is equal to  $-l, -l+1, -l+2, -l+3, \dots, +l$  for the number of electrons in each orbital. The spin quantum number for all the electrons in an ion,  $S$ , is equal to  $\Sigma s$ . Hund's rules can be used to determine the total magnetic moment for a given atom or ion. Hund's rules state the following:



**Figure 3.36** The order of electron orbital filling.

1. The number of unpaired spins is a maximum.
2. The  $L$  value is the maximum allowed.
3.  $J = |L - S|$  when the shell is less than half filled.
4.  $J = |L + S|$  when the shell is more than half filled.
5.  $\underline{J} = S$  when the shell is half filled.

The total magnetic moment for the ion is

$$\mu = 2[J(J + 1)]^{1/2} \mu_B \quad (3.19)$$

This relationship can be used to calculate the magnetic moments of various ions in a solid. Table 3.15 shows the electron configuration of ions in ferrite materials. Notice the unfilled 3d orbital for the transition metal ions.

**TABLE 3.15 Electron Configuration of Ferrite Constituent Ions**

Ion	Electrons	Electron configuration	Unpaired electrons
O <sup>2-</sup>	10	1s <sup>2</sup> 2s <sup>2</sup> 2p <sup>6</sup>	0
Fe <sup>2+</sup>	24 (23)	1s <sup>2</sup> 2s <sup>2</sup> 2p <sup>6</sup> 3s <sup>2</sup> 3p <sup>6</sup> 3d <sup>6</sup> (3d <sup>5</sup> )	4(5)
Mg <sup>2+</sup>	10	1s <sup>2</sup> 2s <sup>2</sup> 2p <sup>6</sup>	0
Al <sup>3+</sup>	10	1s <sup>2</sup> 2s <sup>2</sup> 2p <sup>6</sup>	0
Li <sup>+</sup>	2	1s <sup>2</sup>	0
Zn <sup>2+</sup>	28	1s <sup>2</sup> 2s <sup>2</sup> 2p <sup>6</sup> 3s <sup>2</sup> 3p <sup>6</sup> 3d <sup>10</sup>	0
Cd <sup>2+</sup>	46	1s <sup>2</sup> 2s <sup>2</sup> 2p <sup>6</sup> 3s <sup>2</sup> 3p <sup>6</sup> 4s <sup>2</sup> 4p <sup>6</sup> 4d <sup>10</sup>	0
Mn <sup>2+</sup> (Mn <sup>3+</sup> ) (Mn <sup>4+</sup> )	23 (22) (21)	1s <sup>2</sup> 2s <sup>2</sup> 2p <sup>6</sup> 3s <sup>2</sup> 3p <sup>6</sup> 3d <sup>5</sup> (3d <sup>4</sup> )(3d <sup>3</sup> )	5 (4) (3)
Cr <sup>2+</sup> (Cr <sup>3+</sup> )	22 (21)	1s <sup>2</sup> 2s <sup>2</sup> 2p <sup>6</sup> 3s <sup>2</sup> 3p <sup>6</sup> 3d <sup>4</sup> (3d <sup>3</sup> )	4 (3)
Co <sup>2+</sup> (Co <sup>3+</sup> )	25 (24)	1s <sup>2</sup> 2s <sup>2</sup> 2p <sup>6</sup> 3s <sup>2</sup> 3p <sup>6</sup> 3d <sup>7</sup> (3d <sup>6</sup> )	3 (4)
Ni <sup>2+</sup>	26	1s <sup>2</sup> 2s <sup>2</sup> 2p <sup>6</sup> 3s <sup>2</sup> 3p <sup>6</sup> 3d <sup>8</sup>	2
Cu <sup>+</sup> (Cu <sup>2+</sup> )	28 (27)	1s <sup>2</sup> 2s <sup>2</sup> 2p <sup>6</sup> 3s <sup>2</sup> 3p <sup>6</sup> 3d <sup>10</sup> (3d <sup>9</sup> )	0 (1)

The bulk magnetization,  $M$ , can be calculated using the formula

$$M = n \mu_B N_o d / A \quad (3.20)$$

where  $n$  = number of unpaired electron spins/atom  
 $N_o$  = Avagadro's number ( $6.023 \times 10^{23}$  atoms/mole)  
 $d$  = density  
 $A$  = atomic weight

Diamagnetic materials have electronic interactions that produce a net-zero magnetic moment. If a magnetic field is applied to these materials, a small magnetic moment is induced that orients opposing the applied field. These materials, which have closed electron shells, have negative susceptibilities on the order of  $10^{-5}$  to  $10^{-6}$ . Diamagnetic materials include most ceramics and metals with a closed electron shell, organics, and inert gases.

Materials containing ions with odd numbers of electrons, such as those from the rare-earth and transition series, possess a net magnetic moment. In the absence of an applied magnetic field, the orientation of these moments is random, with no mutual interaction, resulting in a net-zero magnetism. If a magnetic field is applied, the individual moments tend to align their polarity with the field, creating a net magnetism. Paramagnetic materials have a permanent magnetic moment with a positive but small susceptibility ( $10^{-3}$  to  $10^{-6}$ ). Thermal energy opposes this effect.

Ferromagnetic materials have large magnetization due to strong magnetic dipole interaction, spontaneously aligning without an applied field in small volumes of material. The magnetic dipole interaction is a result of electron exchange between  $O^{2-}$  ions and neighboring  $Fe^{3+}$  ions. These small volumes of material with aligned dipoles, Weiss domains, tend to randomly orient to the lowest energy state in the absence of an applied field. However, the net magnetization for the bulk material is zero because of the random orientation of the magnetization vectors between domains. Under applied field, those domains oriented in the direction of the applied field grow at the expense of oppositely oriented or perpendicular domains. The spontaneous magnetization is typically several orders of magnitude greater than the applied field, resulting in very high permeability.

Antiferroelectric materials have an exchange interaction between unpaired electrons, which results in antiparallel alignment of electron spins. The magnetic moments of ions in adjacent planes are equal in magnitude, aligned, but in opposite polarity; therefore, the result is no net magnetization. A few materials, such as FeO, MnO, NiO, and CoO, exhibit this behavior.

It is more common for materials to exhibit antiparallel alignment between two sublattices. These different sublattices have unequal numbers of antiparallel moments, resulting in a net magnetic moment for the crystal. These ferrimagnetic materials (ferrites) are the most broadly used magnetic material group. Both ferromagnetic and ferrimagnetic materials possess Weiss domain regions wherein there is a strong mutual interaction between magnetic moments, and spontaneous magnetization occurs. This spontaneous magnetization occurs along specific crystallographic directions that minimize the free energy of the material. Figure 3.37 shows how the successive breakup of magnetic domains keeps the magnetic flux within the material and lowers the energy level of the material. The boundary between adjacent domains has a finite width (approximately  $1\ \mu\text{m}$ ) and consists of a gradual change in magnetic moment from one orientation to the other, which minimizes the boundary energy. Figure 3.38 shows the behavior of a ferro- or ferrimagnetic material as a magnetic field is applied. The magnetic moments begin to align with the field; domain boundaries move so that domains aligned with field

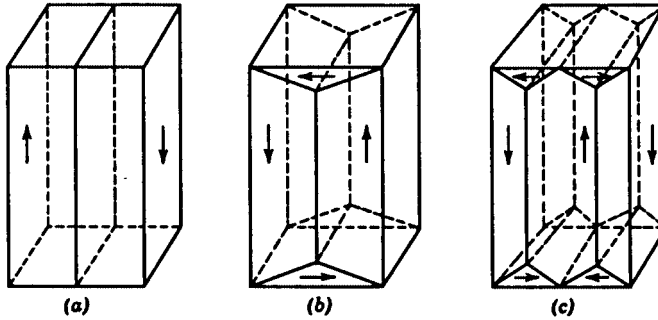


Figure 3.37 Several domain structures of a solid, each having a zero net magnetization but progressively lower energy.<sup>14</sup>

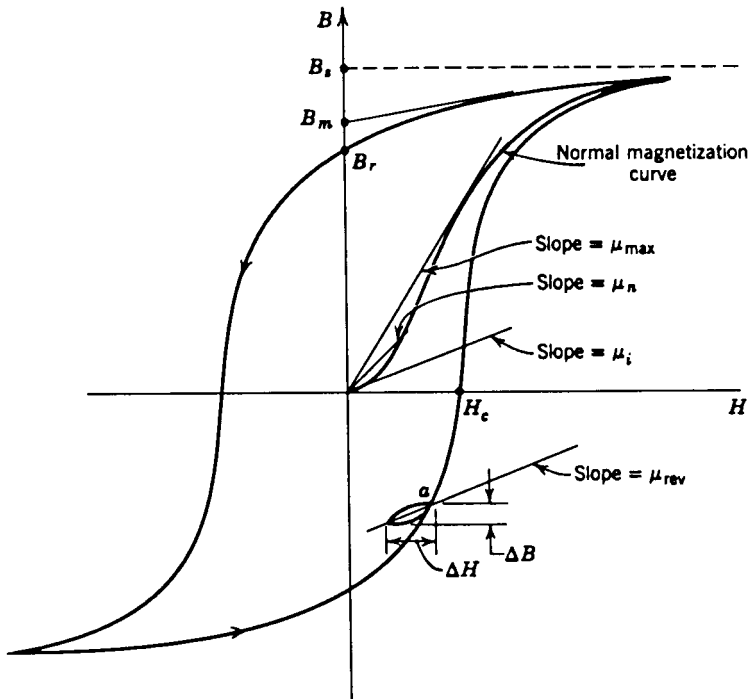


Figure 3.38 Magnetic induction vs. magnetic field for a ferrite.<sup>14</sup>

grow at the expense of others. This alignment results in increased magnetization as higher fields are applied. The ratio of the change in magnetic induction with applied field is the magnetic permeability; that is,

$$\mu = \Delta B / \Delta H \tag{3.21}$$

At high fields, the magnetization reaches saturation,  $B_s$ , as nearly all of the material aligns with the field. If the field is removed, a significant portion of

the domain alignment remains, creating a remnant magnetization (induction),  $B_r$ . If a reversed field is applied, the remnant induction is reduced. The field required to completely reverse the induced magnetization is the coercive field,  $H_c$ . If a large enough reverse field is applied, the domains will align in the opposite direction and ultimately saturate with reverse polarity. This cyclical behavior, hysteresis, is characteristic of ferro- and ferrimagnetic materials. This nonreversible B-H behavior represents an energy loss, in the form of heat, as a result of moving domain boundaries.

An applied magnetic field on a ferromagnetic material causes alignment of the magnetization vectors in the direction of the field. The magnetization,  $M$ , is the magnetic moment per unit volume and has units of tesla (weber/m<sup>2</sup>). Analogous to dielectric relationships, the relative permeability,  $\mu_r$ , can be defined as  $\mu'/\mu_0$ . The magnetic susceptibility,  $X_m$ , is defined as the amount of magnetization for an applied magnetic field,

$$X_m = M/H = \mu_r - 1 \quad (3.22)$$

Ferro- and ferrimagnetic materials obey the Curie-Weiss law; that is, magnetization drops as temperature increases as a result of the randomization of magnetic moments caused by the increased thermal energy. At the Curie temperature, spontaneous magnetization goes to zero, and the material becomes paramagnetic.

$$\frac{1}{X_m} = \frac{1}{C(T - T_C)} \quad (3.23)$$

where  $C$  = Curie-Weiss constant  
 $T_C$  = Curie temperature

The resultant magnetic induction (or magnetic flux density),  $B$ , as a result of a current loop on a nonmagnetic material is  $B = \mu_0 nI$ , where  $\mu_0$  is the magnetic permeability of vacuum,  $4\pi \times 10^{-7}$  H/m (1 G/Oe),  $n$  is the number of turns, and  $I$  is the current. If a coil is wound on magnetic material, amperian currents result ( $I_a$ ) from electron orbits and spin; this results in an additional contribution to the magnetic induction. The total magnetic induction (magnetic flux density) on a magnetic material is the sum of the magnetization and the external magnetic field.

$$B = \mu_0 nI + \mu_0 I_a = \mu_0(H + M) = \mu_0(H + X_m H) = \mu_0 \mu_r H = \mu' H \quad (3.24)$$

where  $\mu$  = permeability of the material

When an external field is applied to a ferrite shape, the material aligns to oppose the applied field, and magnetic poles are formed at the surfaces. The shape of the ferrite determines the magnitude of the field within the material. This internal field,  $H_i$ , is related to the applied field  $H_a$  and the demagnetizing field,  $H_D$  by

$$H_i = H_a - H_D = H_a - N_D M \quad (3.25)$$

where  $N_D$  = demagnetizing factor dependent on the device shape  
 $M$  = magnetization

If a uniform sphere of material is assumed,  $N_D$  is equal to 1/3, and the magnetic induction and will equal  $4\pi$ ; then,

$$B = H + 4\pi M \quad (3.26)$$

Typically, the total induction is expressed with the field subtracted out to equal  $4\pi M_s$ . In materials wherein saturation can be reached at relatively low fields, the saturation induction is equal to  $4\pi M_s$ . Therefore, the total magnetic induction in a material is given by

$$B = H + 4\pi M_s \quad (3.27)$$

In soft ferrites, the peak induction approaches the  $4\pi M_s$  value. Ferrites have lower saturation magnetization and higher resistivities than magnetic metals, primarily because of the amount of large, nonmagnetic oxygen ions.

Magnetic field strength and flux density are measured in terms of Gauss or Oersteds. 1 Oe = 79.7 A/m. 1 G =  $10^{-4}$  Weber/m<sup>2</sup>. One Weber/m<sup>2</sup> = 1 tesla = 796 emu/cm<sup>3</sup>. Permeability is given in terms of henry/m or erg/Oe. The elementary unit of magnetic moment, the Bohr magneton,  $\mu_B$ , is  $9.27 \times 10^{-24}$  Am<sup>2</sup>/electron =  $9.27 \times 10^{-21}$  erg/G.

### 3.7.1 Spinel

Spinel has the general chemical formula  $MFe_2O_4$ . The unit cell of the spinel crystal structure is composed of eight formula units, with the oxygen ions forming a cubic close-packed array as shown in Fig. 3.39. The oxygen array contains 64 tetrahedral (A sites) and 32 larger octahedral (B sites) coordinated interstices. Eight of the tetrahedral A sites and 16 of the octahedral B sites are filled; that is, 1 tetrahedral and 2 octahedral sites per formula unit are filled. The electronic spins of the ions on the A and B sites (and, therefore, their magnetic moments) are set up in opposing directions, antiferromagnetic. In normal spinel, such as  $MgFe_2O_4$ ,  $CdFe_2O_4$ , and  $ZnFe_2O_4$ , divalent ions occupy all eight of the available A sites, and trivalent Fe ions occupy the available B sites and have the chemical formula of  $(M^{2+}O)Fe^{3+}_2O_3$ . The tetrahedral site is smaller (0.55 to 0.67 Å) than the octahedral site (0.72 to 0.78 Å) and can more readily accommodate the smaller trivalent ions.

In inverse spinels, such as  $Fe_3O_4$  and  $CoFe_2O_4$ , all of the A sites and half of the available B sites are filled with trivalent ions; the remaining eight B sites are occupied by divalent ions and have a chemical formula of  $Fe^{3+}(Fe^{3+}M^{2+})O_4$ . The  $O^{2-}$  ions have a full 2p shell; the six electrons pair off with opposing spins that cannot contribute to a magnetic moment. Each  $Fe^{3+}$  ion has five unpaired 3d shell electrons whose spins are parallel and can contribute to a magnetic moment. In these antiferromagnetic materials, the unpaired



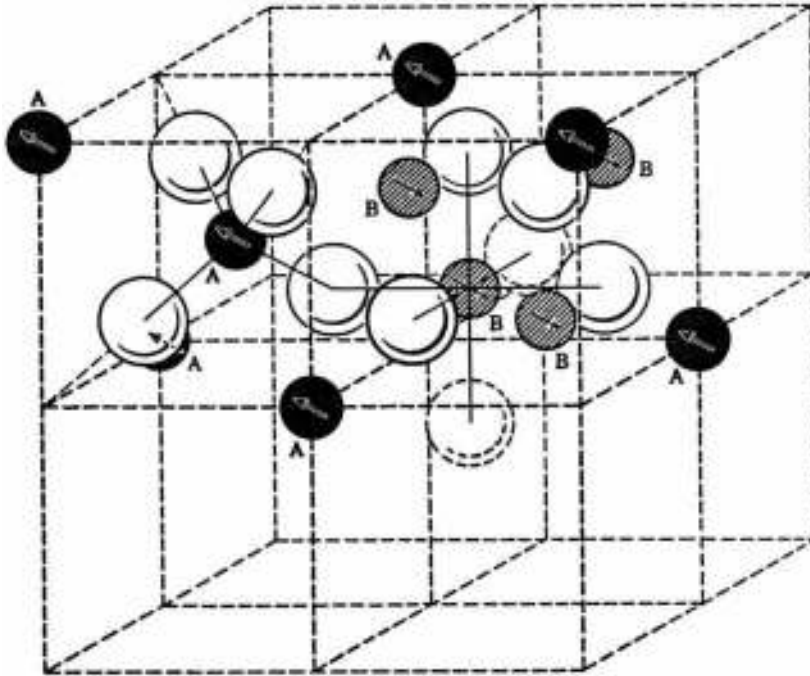


Figure 3.39 The crystal structure of spinel,  $AB_2O_4$ .<sup>14</sup>

electronic spins of the trivalent ions ( $Fe^{3+}$ ) on A site ions are antiparallel to those on the B site, canceling their magnetic moments. The net moment is a result of the remaining eight divalent ions on the B site. In  $NiFe_2O_4$ , the  $Fe^{3+}$  ions on the A site align antiparallel to those on the B site and mutually cancel. The net moment is the result of the remaining  $Ni^{2+}$  ions on the B site.

For a divalent M ion from the transition series with  $n$  electrons in the  $d$  shell, the magnetic moment for the ferrite is:

$$\mu_m = n\mu_B \text{ if } n < 6 \text{ or } (10 - n)\mu_B \text{ if } n > 5 \quad (3.28)$$

All of the metal atoms in the A and B sites will orient in the minimum energy configuration. Some ferrite formulations result in structures that are not fully inverse or normal, depending on the metal ion size, heat treatment, and atmosphere. If  $x$  is the fraction of divalent ions on the B site, then

$$\mu_m (\text{A site}) = (1 - x)n\mu_B + \times 5 \mu_B \quad (3.29)$$

$$\mu_m (\text{B site}) = (1 - x)5\mu_B + 5 + xn \mu_B \quad (3.30)$$

$$\mu_m (\text{net}) = \mu_m(\text{A site}) - \mu_m(\text{B site}) \quad (3.31)$$

Manganese ferrite is about 80 percent normal spinel and is not influenced much by heat treatment. Nickel ferrite is about 80 percent inverse and also is

not affected by heat treatment. In general, ferrites shift to the normal structure at higher temperatures. Magnesium and copper ferrite are normal spinel at high temperature; if quenched, the normal spinel structure is retained. If slow cooled, the spinel transforms to the inverse spinel structure.

Lithium ferrite,  $\text{Li}_{0.5}\text{Fe}_{2.5}\text{O}_4$ , requires an excess of  $\text{Fe}^{+3}$  ions to maintain charge balance with  $\text{Li}^+$ . Four of the 16 occupied octahedral sites are filled by  $\text{Li}^+$ . Gamma ferric oxide,  $\gamma\text{-Fe}_2\text{O}_3$ , is a special case of the spinel structure containing no divalent ions. For charge balance, only two-thirds of the normally occupied octahedral sites are filled with  $\text{Fe}^{3+}$ . This leads to an imbalance in the magnetic spins on the A and B sites, resulting in a net magnetic moment. Table 3.16 shows the magnetic moments for various ferrites calculated in this manner versus measured values. The differences are primarily the result of variability in ion location from the prediction, minor contributions from orbital momentum, and spin directions not being perfectly parallel. Table 3.17 shows the range of properties for ferrite materials.

**TABLE 3.16 Measured vs. Calculated Values for Magnetic Moments of Ferrites**

	Density, g/cm <sup>3</sup>	T <sub>C</sub> , °C	μ <sub>m</sub>	M <sub>z</sub>	B <sub>5</sub>
FeFe <sub>2</sub> O <sub>4</sub>	5.24	585	4	480	6000
ZnFe <sub>2</sub> O <sub>4</sub>	5.33	N/A	0		
MgFe <sub>2</sub> O <sub>4</sub>	4.52	440	0	110	1500
NiFe <sub>2</sub> O <sub>4</sub>	5.38	585	2	270	3400
CuFe <sub>2</sub> O <sub>4</sub>	5.42	455	1	135	1700
Li <sub>0.5</sub> Fe <sub>2.5</sub> O <sub>4</sub>	4.75	670	2.5	310	3900
MnFe <sub>2</sub> O <sub>4</sub>	5.00		5	400	6000
CoFe <sub>2</sub> O <sub>4</sub>	5.29	520	3	425	5300

Zinc substitutions for magnetic divalent ions can be used to raise the magnetic moment of the material.  $\text{Zn}^{2+}$  ions enter the tetrahedral A sites with no magnetic moment to orient antiparallel to the B site moments. The result is a larger uncanceled moment from the B site that contributes to the net magnetic moment. Figure 3.40 shows the measured effect of Zn additions to various ferrites.

Because  $\text{Fe}^{+3}$  and  $\text{Mn}^{+2}$  have the highest magnetic contribution of any ion,  $5 \mu_B$ , they have the highest potential contribution to the magnetization of a ferrite. Applications wherein the highest magnetic moments are needed typically contain  $\text{Mn}^{2+}$  or uncompensated  $\text{Fe}^{+3}$  additions. The magnetostriction coefficient for ferrous ferrite is positive, so additions of  $\text{Fe}^{+3}$  ions also reduce the magnitude of electrostriction in most ferrites. Replacing some of the  $\text{Mn}^{+2}$  ions

TABLE 3.17 Properties of Commercially Available Microwave Ferrites\*<sup>10</sup>

Major composition	Saturation magnetization, $4\pi M_s$ , G	Curie temp., $T_C$ , K	Resonance line width, $\Delta H$ , Oe	Landé $g$ factor	Coercive force, $H_c$ , Oe	Dielectric constant, $\epsilon$	Dielectric loss factor, $\tan \delta_\epsilon$	Dielectric density, $g/cm^3$
Y	1800	575	60					
Y	1780	555	45	2.00			<0.00025	5.06
Y	1780	555	55	2.01	0.75	16.0	<0.00025	
Y	1750	555	60	2.0		15	0.0005	
Y	1750	555	35	2.01		16.3		5.08
Y	1750	550	50			16.2	0.0005	
Y	1740	550	60	2.0				5.1
YGd	1600	540	60	2.0	1.1	16.0	<0.00025	
YAl	1540	550	50			14.8	0.0005	
YGd	1520	555	55	2.01			<0.00025	5.26
YAl	1470	525	40	2.01			<0.00025	5.04
YGd	1300	555	70	2.03			<0.00025	5.42
YAl	1220	515	55			14.6	0.0005	
YGd	1220	525	100	2.0		15	0.0005	
YGd	1200	555	85	2.00	0.75	15	<0.00025	
YAl	1200	535	60	1.99	0.5	15.5	<0.00025	
YGdAl	1200	525	55			14.8	0.0005	
YAl	1150	500	60	2.0				5.0
YAl	1120	485	40	2.01			<0.00025	5.03
YGd	1000	555	130	2.05			<0.00025	5.68
YGd	1000	555	120	2.00	0.8	15.5	<0.00025	
YAl	1000	525	60	1.99	1.2	15.0	<0.00025	
YAl	990	485	55			14.4	0.0005	
YAl	850	455	40	2.01			<0.00025	5.00
YGd	850	555	160	2.00	1.0	15.5	<0.00025	
YGd	840	525	200	2.0		15	0.0005	
YAl	800	505	65	2.00	1.2	15.0	<0.00025	
YGdAl	800	525	110			15.0	0.0005	

TABLE 3.17 Properties of Commercially Available Microwave Ferrites\*<sup>10</sup> (Continued)

Major composition	Saturation magnetization, $4\pi M_s$ , G	Curie temp., $T_C$ , K	Resonance line width, $\Delta H$ , Oe	Lande $g$ factor	Coercive force, $H_c$ , Oe	Dielectric constant, $\epsilon$	Dielectric loss factor, $\tan \delta_\epsilon$	Dielectric density, $g/cm^3$
YGdAl	750	525	80			15.0	0.0005	
YGd	750	555	200	2.08			<0.00025	5.85
YGd	725	555	220	2.03	1.0	15.5	<0.0005	
YAl	680	475	70	2.00	1.2	15.0	<0.00025	
YAl	680	455	45	2.00	1.0	14.5	<0.00025	
YGdAl	675	475	120	2.0				5.1
YGdAl	660	525	210	2.05			<0.00025	5.73
YAl	650	445	40	2.02			<0.00025	5.00
YAl	600	430	60	2.0		15	0.0005	
YAl	600	445	40			14.3	0.0005	
YAl	550	435	75	2.00	1.2	14.0	<0.00025	
YAl	475	430	50			14.0	0.0004	
YAl	400	405	45	2.01	1.0	14.0	<0.00025	
YAl	400	405	45			13.8	0.0005	
YAl	370	400	40			14.0	0.0005	
YGdAl	340	475	310	2.10			<0.00025	5.63
YAl	300	400	40	2.02	0.4	14.0	<0.00025	
YAl	290	390	40			13.4	0.0005	
YAl	240	370	40	2.03	1.0	14.0	<0.00025	
YAl	225	380	35			13.8	0.0004	
Nickel ferrites								
NiZn	5000	650	135	2.08	0.9	12.5	0.001	
Ni	3000	850	350	2.3				5.1
NiCo	3000	860	350	2.21	12	13.0	0.0025	
NiCo	3000	865	200	2.2		13	0.0005	
Ni	3000	865	500	3.3		12	0.0005	
NiCoAl	2440	826	260	2.33			<0.0005	5.05
NiTiAl	2200	825	500	2.45		12.0	0.002	4.80

TABLE 3.17 Properties of Commercially Available Microwave Ferrites\*<sup>10</sup> (Continued)

Major composition	Saturation magnetization, $4\pi M_s$ , G	Curie temp., $T_C$ , K	Resonance line width, $\Delta H$ , Oe	Landé $g$ factor	Coercive force, $H_c$ , Oe	Dielectric constant, $\epsilon$	Dielectric loss factor, $\tan \delta_\epsilon$	Dielectric density, $g/cm^3$
NiAl	2000	835	450	2.31	4	12.8	0.001	
NiCoAl	1800	820	1000	2.55	36	9.0	0.0015	
NiCoAl	1800	775	800	2.55	21	9.5	0.002	
Magnesium ferrites								
MgMn	2220	585	500	2.07			<0.00025	4.20
MgMn	2150	595	540	2.10	2.5	13.0	<0.00025	
MgMn	2100	575	425	2.0		12	0.0005	
MgMn	2000	555	350	2.0				4.3
MgMn	2000	575	400	2.07		12	0.0008	4.3
MgMn	1950	515	150	2.0				4.3
MgMn	1780	595	380	2.06	1.4	12	0.0005	4.15
MgMnAl	1760	565	490	2.11	2.1	12	0.0005	4.10
MgMnAl	1700	500	225	2.00	1.0	12.0	<0.00025	
MgMn	1650	575	650	2.0				4.3
MgMnAl	1550	515	375	2.0				4.3
MgMnAl	1250	439	155	2.00	0.4	11.5	<0.00025	
MgMnAl	1250	475	300	2.0				4.2
MgMnAl	1140	425	165	0.02				4.10
MgMnAl	1110	415	220	2.04	0.8	12	0.0003	3.95
MgMnAl	730	375	120	2.00	0.7	12	0.0004	3.90
MgMnAl	680	375	120	2.02	1.2	11.5	<0.00025	

\*Measurements made at X band.

SOURCE: *Handbook of Microwave Ferrite Materials*, W. H. von Aulock, Ed., © Academic Press, Orlando, FL, 1965, pp. xviii–xxi.

in  $MnFe_2O_3$  with  $Fe^{+3}$  ions has the effect of reducing the magnetic anisotropy to zero, raises the permeability, and decreases the resistivity. Additions of Co in most ferrites have the effect of making anisotropy more positive. Co is also added to improve power handling in ferrites.

Zn substitution in Mn and Ni ferrites increases the magnetic moments but also reduces the Curie temperatures, resulting in lower saturation induction values. Zinc additions also lowers magnetostriction and magnetocrystalline

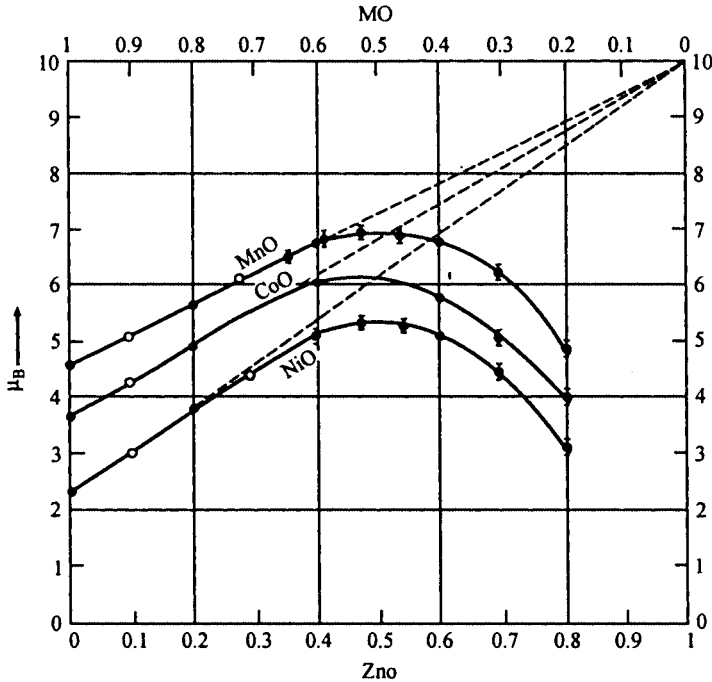


Figure 3.40 Effect of zinc substitution on magnetic moments of various ferrites.<sup>10</sup>

anisotropy. Most commercial ferrites are solid solutions of different ferrites, mixed ferrites, to optimize the properties for a particular application.  $\text{NiFe}_2\text{O}_4$  and  $\text{MgFe}_2\text{O}_4$  have lower magnetic moments but higher resistivities that are well suited for high-frequency applications.

### 3.7.2 Garnets

Garnets have the general structure  $\text{M}_3\text{Fe}_5\text{O}_{12}$ ,  $(3\text{M}_2\text{O}_3)(2\text{Fe}_2\text{O}_3)(3\text{Fe}_2\text{O}_3)$ , where M is a trivalent rare-earth or yttrium ion. The crystal structure is cubic, containing eight formula units per unit cell (Fig. 3.41). The oxygen array forms 24 tetrahedral (D site), 16 octahedral (A site), and 16 dodecahedral (C site) coordination interstices per unit cell. The  $\text{Fe}^{3+}$  ions occupying the tetrahedral are aligned antiparallel to the A and C sites. The net magnetic moment per unit cell is given by

$$\mu_m(\text{net}) = \mu_m(\text{A site}) + \mu_m(\text{C site}) - \mu_m(\text{D site}) \quad (3.32)$$

The rare-earth ions are large and therefore occupy the large dodecahedral sites. Because there are three D site  $\text{Fe}^{3+}$  for each two A site  $\text{Fe}^{3+}$  and three C site  $\text{M}^{3+}$  ions, and the moment for each  $\text{Fe}^{3+}$  ion is  $5\mu_B$ , the equation shortens to

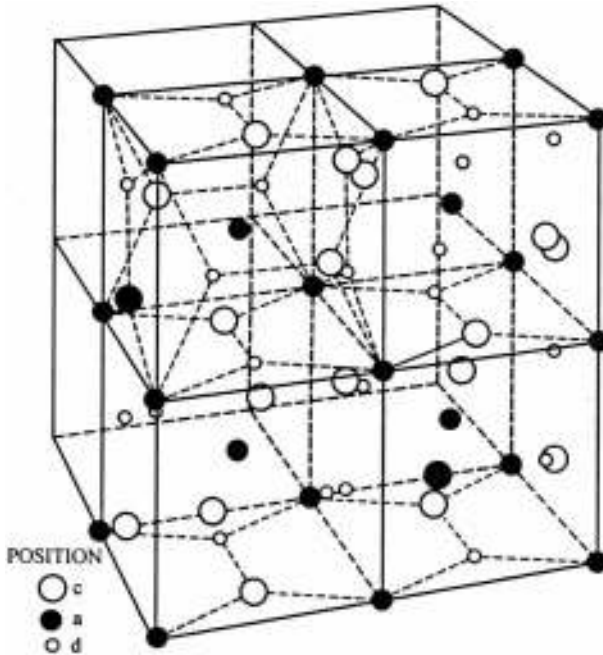


Figure 3.41 Unit cell of a rare-earth garnet.<sup>10</sup>

$$\begin{aligned}
 \mu_m(\text{net}) &= 2\mu_m(2\text{Fe}_A^{3+}) + 3\mu_m(2M_C^{3+}) - 3\mu_m(2\text{Fe}_D^{3+}) \\
 &= 3\mu_m(2M_C^{3+}) - 10\mu_B
 \end{aligned}
 \tag{3.33}$$

The  $\text{Y}^{3+}$  ion has no magnetic moment, because it has no unpaired spins (i.e.,  $4s^2 4p^6$ ), so the magnetic moment is due to the  $\text{Fe}^{3+}$  ions only. The rare-earth ions have unpaired 4f electrons that contribute to the magnetic moment. However, estimating the magnetic moment for garnets in this manner has some error caused by an electron spin-orbital coupling. This is the result of the 4f orbital surrounding full 5s, 5p, and 5d orbitals.

Substitutions are sometimes made for the  $\text{Fe}^{3+}$  ions to modify the properties of a garnet. Smaller ions, such as  $\text{Al}^{3+}$ , will occupy the smaller tetrahedral sites. This decreases the moment of the tetrahedral site and therefore the net moment of the garnet. Larger ions, such as  $\text{In}^{3+}$  and  $\text{Sc}^{3+}$ , occupy the larger octahedral sites. Again, these substitutions will decrease the moment for the site; however, the difference in the moment between the octahedral and tetrahedral sites is greater. These substitutions result in a higher net moment for the crystal.

### 3.7.3 Perovskites

The general formula for perovskite ferrites is  $\text{MFeO}_3$  where M is a rare-earth or  $\text{Y}^{3+}$ ,  $\text{La}^{3+}$ ,  $\text{Ca}^{2+}$ ,  $\text{Sr}^{2+}$ , or  $\text{Ba}^{2+}$  ion. The crystal structure is orthorhombic

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with face-centered oxygen ions; thus the name *orthoferrites*. The A and B site moments are aligned antiparallel; however, there is a slight canting, leading to a small net magnetic moment.

## 3.7.4 Hexagonal ferrites

Hexagonal ferrites have the general formula  $MFe_{12}O_{19}$  where M is  $Ba^{2+}$ ,  $Sr^{2+}$ , or  $Pb^{2+}$ . The crystal structure for magnetoplumbite consists of a hexagonal close-packed array of oxygen ions with two formula units per unit cell. The oxygen layers contain the  $M^{2+}$  ions, which can substitute for oxygen sites. The unit cell consists of ten  $O^{2-}$  layers with  $M^{2+}$  replacing  $O^{2-}$  on every fifth layer. Two layers contain  $M^{2+}$  ions, four layers contain four  $O^{2-}$  ions (one layer of three  $O^{2-}$  with one  $M^{2+}$ ), four layers containing all  $O^{2-}$  ions, and one layer containing three  $O^{2-}$  with one  $M^{2+}$ . The  $Fe^{3+}$  ions occupy two tetragonal sites, nine octahedral sites, and one five-coordination site. All of the tetragonal sites and two of the octahedral sites are aligned antiparallel to the remaining sites. The leaves four sites wherein the moment are not cancelled by antiparallel alignment. The net moment is  $4 \times 5\mu_B$  ( $Fe^{3+}$ ).

Hexagonal ferrite is used as a permanent magnet due to high magnetocrystalline anisotropy and high coercive fields. The easy direction of magnetization is the c axis.

## 3.7.5 Applications

Phase shifters are the enabling component for electronically scanned array radars (ESAs). In this application, a time delay in an RF signal is achieved by propagating through a magnetized waveguide or TEM through conductors embedded in the magnetic material. The degree of phase shift is controlled by varying the current applied to coil loops around the magnetic materials.

Magnetic garnets can be epitaxially grown in thin film form on nonmagnetic substrates. CTE differences result in a preferred magnetization direction perpendicular to the substrate. Magnetic domains form with spins up and spins down. These domains appear as bubbles in polarized light. These bubble domains provide binary inputs for digital computers (bubble memory).

## 3.8 Superconductive Ceramics

The phenomenon of superconductivity was discovered in 1911 by K. Onnes, in mercury metal, shortly after his development of a process for forming liquid helium. He found that resistance dropped sharply to near zero at a temperature of 4.2 K ( $-269^\circ\text{C}$ ). Later, the development of liquid helium enabled the discover of superconductivity in many compounds, because it allows the cooling of materials to near absolute zero (1 K) temperature. Meissner, in 1933, showed that superconductors exhibit not only zero electrical resistance but also diamagnetic behavior. Diamagnetic materials have electronic interactions that produce a net-zero magnetic moment. If a magnetic field is applied



to these materials, a magnetic moment is induced that orients in opposition to the applied field. These materials, which typically have closed electron shells, have negative magnetic susceptibilities on the order of  $10^5$  to  $10^6$ . The generation of the opposing magnetic field is the driving force for the high surface current (screening current) flow in the material.

When a magnetic field is applied to a superconductor below  $T_c$ , electric currents flow in the material without resistance, creating a magnetic field opposing the applied field—the Meissner effect. There is a critical current density,  $J_c$ , above which superconduction halts. The electric current density is a measure of the charge moving through an area of material over a given time.

$$J = nzev \quad (3.34)$$

where  $n$  = number of charged particles per unit volume

$e$  = electronic charge

$z$  = valence (in the case of ionic conduction)

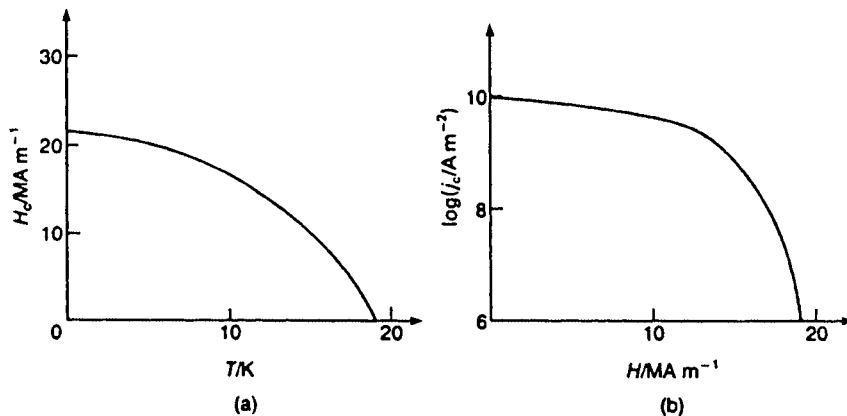
$v$  = drift velocity in units of cm/s

The ratio of the drift velocity to the local electric field,  $v/E$ , is defined as the charge mobility,  $\mu$ , in units of  $\text{cm}^2/\text{Vs}$ .

Electrical conductivity,  $\sigma$ , is a measure of the current density,  $J$ , with an applied electric field,  $E$ .

$$\sigma = J/E = nze(v/E) = nze\mu$$

There is a maximum magnetic field,  $H_c$ , above which superconduction ceases. In general, as the temperature is raised to  $T_C$ ,  $J_C$ , and  $H_C$  decrease as shown in Fig. 3.42 for  $\text{Nb}_3\text{Sn}$ . The desirable properties of a superconducting material are a high  $T_C$ , a high critical current density, a high critical magnetic field ( $H_c$ ), low cost, reliability, and manufacturability.



**Figure 3.42** (a) Critical magnetic field,  $H_c$ , as a function of temperature for  $\text{Nb}_3\text{Sn}$ , and (b) critical current density,  $J_c$ , as a function of magnetic field at 4.2 K for  $\text{Nb}_3\text{Sn}$ .<sup>24</sup>

In Type I superconductors, all magnetic flux is contained in a surface layer of the material—the *London penetration depth*. Metallic superconductors are Type I. In Type II superconductors, magnetic flux penetrates the interior of the material at a critical magnetic field. If the flux lines are not pinned, there is resistive energy loss, and the current density at which the magnetic flux moves into the interior determines  $J_C$ . If the flux lines are pinned along controlled crystalline defects, such as impurity inclusions or second phases, higher magnetic fields can be tolerated, leading to higher current density. The high-temperature superconductor (HTS) ceramics are Type II and are capable of withstanding much higher magnetic fields.

In the 1950s, Frohlich and Bardeen theorized that superconduction is a result of electron-phonon interactions that couple electron pairs. This pairing up can occur only at low temperatures where thermally induced motions of the electrons are sufficiently reduced. Later, L.N. Cooper showed how an electron pair, a *Cooper pair*, would have an combined energy level lower than conduction electrons in the highest energy state (the *Fermi level*). In 1957, J. Bardeen, L.N. Cooper, and J.R. Schrieffer further theorized the large-scale interaction of Cooper pairs, resulting in the *BCS theory*. The BCS theory describes how electron pairs in a superconducting metal interact such that their combined momenta is unchanged. Conduction scattering mechanisms, such as phonon interactions, have equal and opposite effects on each of the paired electrons. Therefore, there is no change in momentum and no resistance to the conduction of electron pairs. In 1950, B.T. Matthias attempted to establish criteria for good superconductors. Material requirements included a high concentration of Fermi-level electrons, the presence of soft phonons, and the proximity to a metal-insulator transition.

The quest for a room-temperature superconductor has spurred the development of thousands of compounds incrementally driving the critical temperature for superconduction to higher values. Table 3.18 shows various superconducting materials with their corresponding transitions temperatures below which the resistivity falls to infinitesimal levels. At present, the highest temperature for the onset of superconductivity is  $\approx 130$  K.

In 1966, the first superconducting ceramic was discovered in the perovskite structure  $\text{SrTiO}_{3-x}$  with a  $T_c$  of 0.5 K. The oxygen deficiency results in lattice vacancies that aid in the conduction—n-type conduction. Johnson et al., in 1973, documented the superconducting behavior of  $\text{Li}_{1+x}\text{Ti}_{2-x}\text{O}_4$  ( $0 < x < 1/3$ ) at  $\approx 14$  K. In 1986, J.G. Bednorz and K.A. Muller received the Nobel prize for their discovery of the superconducting behavior of perovskite-like  $\text{La}_{2-x}\text{Ba}_x\text{CuO}_{4-y}$  with a  $T_c$  of 35 K. The crystal structure consists of layers of perovskite formed by Cu-O separated by layers of rock-salt crystal structure formed by La, Ba-O ions. Their data, shown in Fig. 3.43a, sparked a significant amount of research in cuprate superconductors wherein  $\text{Cu}^{2+}$  and  $\text{Cu}^{3+}$  can coexist. Soon thereafter, Wu and Chu discovered compositions of  $\text{YBa}_2\text{Cu}_3\text{O}_{7-x}$ , the 123-cuprate material shown in Fig. 3.43b, with a transition temperature well above the 77 K boiling point of nitrogen, at  $\approx 93$  K. Superconductors that operate above liquid nitrogen temperatures enable the fabrication of practical devices that are cooled by much cheaper liquid  $\text{N}_2$ . These 123-cuprates are of

**TABLE 3.18 Transition Temperatures for Superconducting Materials**

Element/compound	$T_C$ (K)
SrTiO <sub>3-x</sub>	0.5
Sn	3.7
Hg	4.2
Pb	7.2
Nb	9.2
BaPb <sub>1-x</sub> Bi <sub>x</sub> O <sub>3</sub> ( $x \approx 0.25$ )	13
Li <sub>1+x</sub> Ti <sub>2-x</sub> O <sub>4</sub> ( $0 < x < 1/3$ )	14
Nb <sub>3</sub> Sn	18
Nb <sub>3</sub> Al <sub>0.5</sub> Ge <sub>0.2</sub>	20.9
Nb <sub>3</sub> Ge	23
Nd <sub>2-x</sub> Ce <sub>x</sub> CuO <sub>4</sub>	
BaKBiO	30
La <sub>2-x</sub> Ba <sub>x</sub> CuO <sub>4-y</sub>	35
PbSrCaLaCuO	55
YBa <sub>2</sub> Cu <sub>3</sub> O <sub>7-x</sub>	93
Bi <sub>2</sub> Sr <sub>2</sub> Ca <sub>2</sub> Cu <sub>3</sub> O <sub>x</sub>	110
Bi <sub>1.5</sub> Pb <sub>0.5</sub> Sr <sub>2</sub> Ca <sub>2</sub> Cu <sub>3</sub> O <sub>x</sub>	110
BiAlCaSrCuO	114
TiCaBaCuO	100–125
HgBa <sub>2</sub> Ca <sub>2</sub> Cu <sub>3</sub> O <sub>8</sub>	133 (150–160 pressurized)

the layered perovskite-type crystal structure shown in Fig. 3.44. Again, the superconducting behavior results from the existence of multivalence copper ions mixed with oxygen ions forming planar arrays separated by perovskite layers. The perovskite structure favors the existence of soft-mode phonons, as evident by its instability and morphotropic phase boundaries—one of the Matthias' criteria. The presence of multivalence ions and oxygen vacancies seems to favor superconductivity. The Cu-O distance is dependent on the oxidation state of the copper. Therefore, as an electron is transferred, the oxidation state of the copper changes, resulting in a lattice displacement. This is theorized to be the mechanism for the electron-phonon interaction described in the BCS theory.

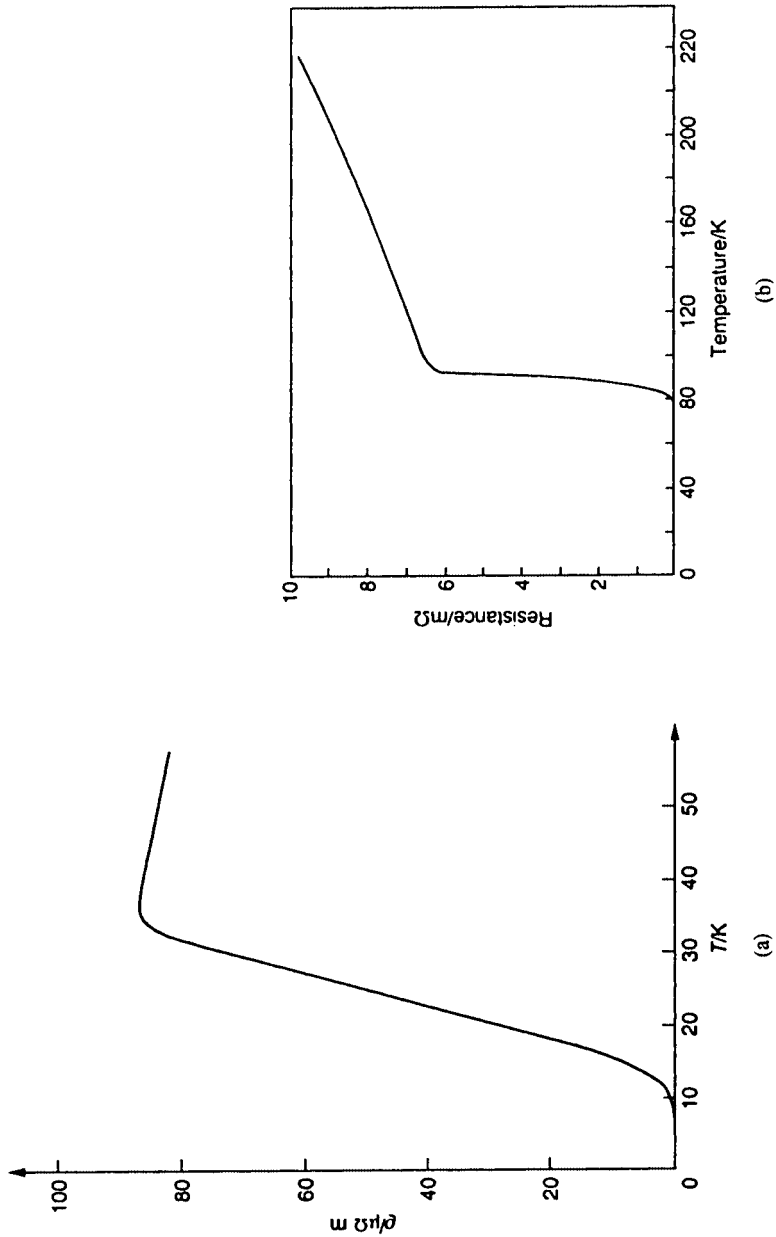


Figure 3.43 (a) Superconductivity in  $(La, BA)_2CuO_4$  and (b)  $YBa_2Cu_3O_{7-\delta}$ .<sup>18</sup>

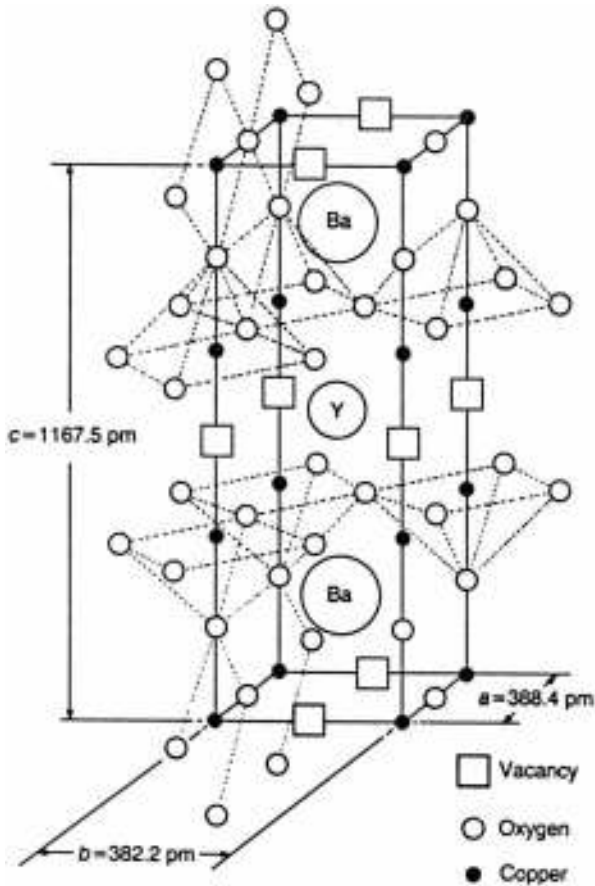
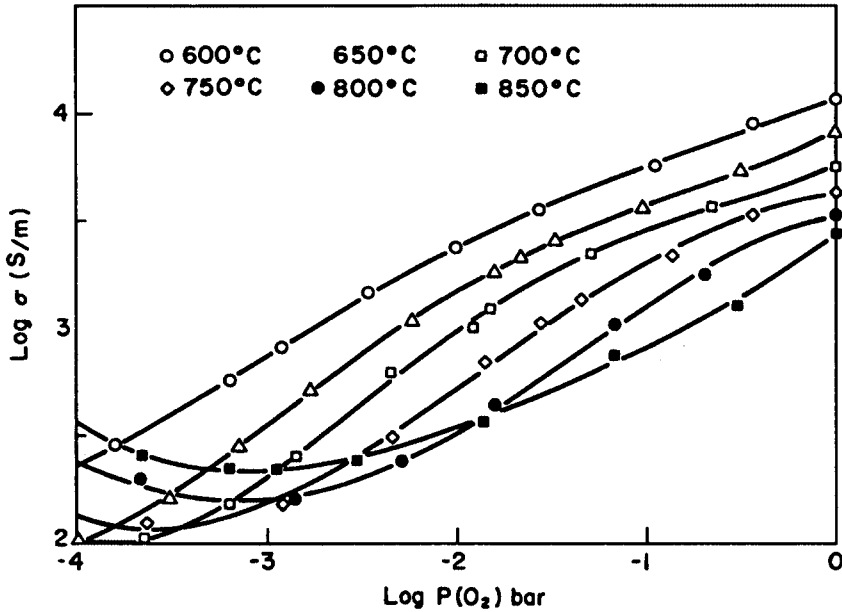


Figure 3.44 123-cuprate layered perovskite structure.<sup>18</sup>

In 1988, Maeda et al. discovered superconducting phases in the Bi-Sr-Ca-Cu-O system. Similarly, Sheng and Hermann discovered high  $T_C$  in the Ti-Ba-Ca-Cu-O system. The compounds contain Cu-O sheets interleaved with Ti-O or Bi-O sheets. The Bi-Sr-Ca-Cu-O system has three superconducting phases,  $(\text{BiO})_2\text{Sr}_2\text{Ca}_{n-1}\text{Cu}_n\text{O}_{2n+2}$ , where  $n = 1, 2, 3$ . Their respective critical temperatures are 7 K, 80 K, and 110 K. Deficiencies on any of the cation sites, creating hole conduction, have been found to significantly increase the critical current density. Figure 3.45 shows the change in conductivity as a function of oxygen atmosphere during processing for a 123-cuprate superconductor. In 1993, a series of mercury-based compounds were discovered with high critical temperatures has sparked new level of interest. The layered structure of  $\text{HgBa}_2\text{Ca}_2\text{Cu}_3\text{O}_8$  has been shown to have a  $T_c$  of approximately 130 K, or 164 K under high-pressure conditions.

Fabrication of these materials in large volumes with homogeneous phase and consistent properties has been a primary focus of superconductor research. Low critical current density,  $J_C$ , and poor mechanical properties have



**Figure 3.45** The equilibrium conductivity of  $\text{YBa}_2\text{Cu}_3\text{O}_x$  as a function of oxygen activity in the temperature range of 600 to 850°C.<sup>19</sup>

been the key problem areas. For most superconducting applications, a  $J_C$  of  $10^5$  to  $10^6$  A/cm<sup>2</sup> is required. The  $J_C$  of polycrystalline ceramics is generally much lower than that single crystals as a result of high-resistivity phases, microcracks, and changes in crystal orientation at the grain boundaries. Polycrystalline materials with  $J_C$  as high as  $5 \times 10^3$  A/cm<sup>2</sup> have been reported.

The highest-current-density materials have been fabricated in single-crystal or thin film forms. Critical current densities greater than  $10^6$  A/cm<sup>2</sup> have been achieved in single crystals and epitaxially grown thin films. Oak Ridge National Laboratory (ORNL) has demonstrated a Y-Ba-Cu-O coated conductor with the ability to produce 1 to 2 cm long, 0.3 cm wide conductors with critical current densities up to  $3 \times 10^6$  A/cm<sup>2</sup> at 77 K. Midwest Superconductivity Inc. (MSI) has produced high  $J_C$  results using MOCVD for Y-Ba-Cu-O deposition on a substrate produced by ORNL, resulting in a short sample with  $J_C$  of  $6.4 \times 10^5$  A/cm<sup>2</sup>.

The properties of ceramic superconductors are highly dependent on the concentration of charge carriers. Therefore, the properties are determined by the phase purity, crystal structure, composition, and defect structure of the material. The final oxidation state of these oxide superconductors is critical to achieving maximum performance and maximize  $T_c$ . Most device fabrications include an anneal in oxidizing atmospheres. A significant amount of research is focused on processing methodologies, final chemistry, and phase relations so as to achieve the desirable phase stability and purity. Polycrystalline ceramic superconductors are typically prepared by solid state calcination of oxide, nitrate, or carbonate precursors. Multiple milling steps are incorporated to

promote homogeneity. Chemical synthesis routes using organometallic salts and metal alkoxide precursors such as sol-gel, precipitation, and decomposition processing have also been used to achieve a high degree of homogeneity. For thin film superconductors, a variety of processes have had some degree of success, including chemical vapor deposition (CVD), spin coating, plasma spraying, molecular beam epitaxy, magnetron sputtering, laser ablation, and laser evaporation.

Grain-orienting processing techniques have been used to achieve anisotropic single-crystal behavior in polycrystalline ceramics. Current flows more easily perpendicular to the C axis of the crystals; therefore, a larger  $J_C$  and low onset resistivity is observed. Hot forging is a process similar to hot pressing; however, the material is unconstrained in the plane of the platens. The material is forced to densify or deform under a constant strain. Manufacturers of superconducting devices continue to strive for practical methods of forming useful superconducting circuits. The simple fact that the high-temperature superconductors are ceramic is a significant obstacle to forming wiring. However, processes such as plastic extrusion and tape casting are being used to fabricate superconducting coils. Polycrystalline wire formed by placing 123-cuprate in silver metal tubing is used to achieve current densities in the range of 2 to  $3 \times 10^3$  A/cm<sup>2</sup>.

### 3.8.1 Applications of superconductors

Superconductor materials are finding an increase in the number of applications. Most applications fall into one of three categories of functions: low-loss transmission electronics, high-magnetic-field generation, or high-current-carrying conductors for power delivery. Up to 15 percent of electrical power is lost through transmission line resistance between the power source and the end user. Superconducting transmission wires have the potential to eliminate this energy loss. The high current densities attained with superconducting coils enable the generation of large magnetic fields. Large magnetic field generation is required in medical diagnostic equipment, particle accelerators in nuclear energy research, and fusion containment magnets. Nuclear magnetic resonance (NMR) and magnetic resonance imaging (MRI) equipment uses superconductors for generation of the large magnetic fields used in these imaging systems. Efficient superconducting magnets are used to create magnetic fields as high as 20T. No-loss electrical transmission and high-speed signal processing have generated interest in the area of digital processing. Because of the diamagnetic behavior of the superconducting materials, the Meissner effect, they are being used in magnetic field shielding applications. Superconductors allow fabrication of highly efficient motors and generators. Magnetic levitation for efficient high-speed trains is now a possibility.

A superconducting quantum interference device (SQUID) is a superconducting instrument that is capable of detecting minute changes in magnetic fields. SQUID sensors can detect weak magnetic fields, as low as  $10^{-15}$  T. SQUID sensors have medical applications whereby magnetic fields resulting from electrical currents flowing in the human brain can be detected. Other ap-

plications include geological research and military applications such as submarine detection.

In 1962, B.D. Josephson predicted that the Cooper pairs in superconductors could tunnel through a 10-insulating barrier with no electrical resistance—the Josephson effect. A Josephson junction allows current to flow with no resistance with no applied field. However, at a critical voltage level, the Cooper pairs split up, and normal quantum-mechanical tunneling occurs with resistive losses. This effect enables the fabrication of microelectronic switches and transistors that operate faster and with lower power loss than semiconductor devices.

An example of high current transmission lines is shown in Fig. 3.46: the high-current transmission line fabricated by American Superconductor Corporation. This power transmission cable consists of HTS wires wound around a hollow core through which liquid nitrogen flows for cooling below  $T_C$ . The conductor is surrounded by conventional dielectric insulation. The efficiency of this design reduces losses. The cryogenic dielectric is a coaxial configuration comprising an HTS conductor cooled by liquid nitrogen flowing through a flexible hollow core and an HTS return conductor, providing even greater amp capacity, further reducing losses and entirely eliminating the need for dielectric fluids.

Motors and generators using HTS windings have twice the efficiency of conventional copper wire motors. Major motor applications include pumps, fans, and compressors as well as in the handling and processing of manufactured materials. According to the Department of Energy, this energy accounts for 70 percent of all the energy consumed by the manufacturing sector and over 55 percent of the total electric energy generated in this country.

Conductus Inc. fabricates high-performance RF filters and filter subsystems based on HTS technology for the telecommunications market. The ClearSite<sup>®</sup> line of front-end receiver subsystems for cellular and PCS base stations manu-

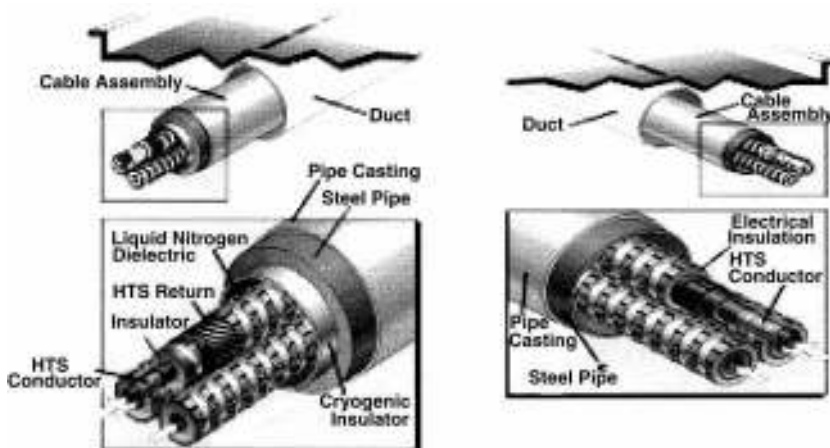


Figure 3.46 High-current transmission line from American Superconductor Corp.<sup>1</sup>



factured by Conductus contains microwave filters with as many as 19 poles, made from thin film HTS superconductors. Conventional filters are significantly larger than HTS filters, more inefficient, and limited to no more than nine poles, limiting the filtering capability. Conductus products are based primarily on YBaCuO thin films synthesized through sputtering, pulsed laser deposition, and co-evaporation.

IGC-Advanced Superconductors manufactures superconductive wire, cable, and tape used in MRI diagnostic systems, high-energy physics, and fusion power research. Products are based on NbTi, Nb<sub>3</sub>Sn, BSCCO 2212/Ag, and BSCCO 2223/Ag multifilament wire and tape.

Superconductor Technologies Inc. (STI) manufactures SuperFilter<sup>®</sup> Systems based on thin film superconductor receiver filters for use in wireless base stations.

## 3.9 Optical Fibers

### 3.9.1 Optical fiber basics

Today, most long-distance telecommunication occurs through optical fibers wherein data is transmitted via light through a glass rather than electrons through a metal fiber. Optical fibers carry information at higher frequencies and, therefore, higher speed and volume without the electromagnetic interference issues associated with metal wiring. The transmission of data through the use light rather than electrons or radio waves has had a dramatic impact on the capacity of telecommunication transmissions. The higher the transmission frequency, the higher the rate of data transmission. Communication at light frequencies was enabled by the advent of high-quality silica-based fibers that are capable of transmission of data over long distances with low attenuation.

Alexander Graham Bell patented an optical telephone system, the Photophone, in 1880. Throughout the early 1900s, a variety of discoveries were based on the idea of total internal reflection to transmit light through water, quartz rods, and Plexiglas<sup>®</sup> rods. The phenomenon of total internal reflection can confine light in a material surrounded by other materials with lower refractive index, such as glass in air.

Because the fibers were bare, light could be refracted outside the fiber, and the transmission was poor. In the 1960s, researchers found that cladding the fiber core with a material of higher refractive index dramatically improved its transmission. Snell's law for the critical angle for internal reflection is

$$n_1 \sin \Theta_1 = n_2 \sin \Theta_2$$

where  $n_1$  and  $n_2$  are the refractive index of the core and cladding, respectively. The critical incident angle is the minimum angle at which incident light will not be refracted into the cladding material; i.e., the refraction angle is 90°, and  $\sin \Theta_2$  is 1. The critical incident angle is  $\sin^{-1}(n_2/n_1)$ . Pure silica glass has a refractive index of 1.46. The typical difference in refractive index between the core and cladding is  $\approx 0.005$ .

The maximum launch angle is called the *acceptance angle*. If light enters the core at angles greater than the acceptance angle, a portion will be refracted into the cladding and result in attenuation of the signal. The *numerical aperture* (NA) is the square root of  $(n_{12}^2 - n_{22}^2)$ . Light entering at an angle greater than the NA will be refracted into the cladding. Typically, only a 0.4 percent difference in refractive indices is sufficient to achieve an adequate numerical aperture.

By 1960, the state of the art was approximately 1 dB loss per meter of fiber. This was adequate for medical applications using high-power lasers but much too lossy for consideration in communications. During the 1960s, the laser was invented, and there were significant advances in fiber technology. During this time, it was found that a substantial portion of the attenuation was the result of impurities in the glass fibers and that smaller diameter fibers allowed transmission of single-mode light. In 1970, researchers at Corning Glass designed and produced the first optical fiber with optical losses low enough to enable use in telecommunications. These early fibers had a goal of less than 20 dB loss per kilometer (<99 percent loss).

The impurity problems were solved by depositing fused quartz from the vapor phase using a cylindrical preform. In the mid 1970s, processes were refined to improve attenuation, and fibers with a refractive index gradient were developed for transmission of broader-band information—multimode fibers. The gradient is created through doping of the fiber with elements such as B, F, Er, or Ge to modify the refractive index. Multimode fibers carry multiple light rays or modes concurrently, each at a slightly different reflection angle within the optical fiber core. Multiple modes tend to disperse over long distances. Reducing the core diameter reduces multimode distortions. Single-mode fiber typically has a much smaller core (1 to 5  $\mu\text{m}$ ) than the multimode ( $\approx 100 \mu\text{m}$ ) and is used for long-distance transmission.

The first field test for telephone communication was done in 1977 using 850-nm wavelength light. In the early 1980s, the first undersea cable was developed using 1300-nm wavelength light in single-mode fiber. The attenuation was at a level of approximately 0.5dB/km. Typically, 600- to 1600-nm wavelength (visible and far infrared) signals are launched from laser or light emitting diodes and modulated to encode information.

Repeaters receive the optical signal, remove unwanted noise, amplify the signal, and retransmits it along the next segment. A repeater consists of a photocell, an amplifier, and a light emitting diode (LED) or infrared emitting diode (IRED).

Attenuation is the result of the absorption of light and secondary reradiation in different directions—Rayleigh scattering. This may be caused by inhomogeneities in the glass fiber. Intrinsic absorption of UV is the result of strong transition bonds in silica. Absorption may also occur because of impurities, transition metal ions, and residual  $\text{OH}^-$  ions. The light is reradiated at different wavelengths, causing attenuation at those wavelengths. Absorption of IR light ( $>1600 \text{ nm}$ ) causes atomic vibrations and a loss of energy as heat. For Ultraviolet transmission ( $\lambda = 300 \text{ to } 400 \text{ nm}$ ), pure silica cores are necessary. Silica has transmission of  $>90$  percent from 300 to 1800 nm. However, less

expensive glasses may be used in visible (400 to 700 nm) and infrared (700 to 2000 nm).

Corning and Lucent control 70 percent of the \$9 billion fiber market. The best fibers currently in development can handle 1.5 trillion bps. In March, 2002, Lucent Technologies' Bell Labs set a new fiber optic transmission record of 40 Gb/sec per channel transmitted over 64 channels over a distance of 4000 km. One gigabit of data is the equivalent of 1000 novels.

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**4.1 Considerations in Alloy Selection****4.1.1 Introduction**

Metals offer a wide variety of physical and mechanical properties for use in the electronics and electrical industries. Because of the demanding requirements on materials in electronic equipment, many trade-offs have to be made in selecting metals. Electrical conductivity must often be reduced to increase strength, while strength is sometimes reduced to obtain a target thermal expansion. These are only two simple trade-offs made in electronic design. Often, the selection involves even more mechanical and/or physical properties along with decisions on economics and manufacturability.

**4.1.2 Selection criteria**

The process of materials selection involves consideration of the functional requirements with respect to physical and mechanical properties. Feasibility and economics of manufacturing will always be a part of the equation. It does little good to select a material with optimal mechanical properties if the material cannot be fabricated into the desired shape at the required cost. The total design job requires consideration of all the factors of functional material properties and manufacturing processes. Some of the detailed factors to be considered are discussed below.

**4.1.3 Composition**

Chemical composition is the most commonly specified criterion for metals. This determines the basic mechanical properties and physical characteristics

## 4.2 Chapter 4

of the metal. Fabrication method and heat treatment will influence these properties, but the chemical composition provides fundamental characteristics. Many metals, such as aluminum and titanium, are used in essentially their pure state, with minor impurity elements. Addition of other elements to a basis metal is common to provide alloys with altered physical or mechanical properties. Alloying elements are controlled to specified limits so that the desired properties may be controlled to given limits. Standardized alloys are available with specified composition limits so that the designer may select the desired properties.

### 4.1.4 Product forms

The basic chemical composition of a metal or alloy provides the fundamental physical and mechanical properties. However, these properties are often influenced by processing during manufacture to attain the final shape. A material that is bought from a metal producer is generally subjected to a number of operations that will affect its final properties. It is important in many cases that the designer be aware of these variables when selecting a material.

Metals received into an electronics plant for use in manufacturing can be classified as in either cast or wrought forms. These are discussed separately below.

**4.1.4.1 Cast metals.** Cast metal forms are produced by pouring molten metal into a mold of the desired shape. No metal deformation occurs, and therefore the properties of the metal depend on the casting process (sand, investment, die, and so on), soundness of the casting, chemical composition, and heat treatment. Cast billets for machining into a final shape are sometimes purchased, but in most cases cast parts are molded to their final shape for most dimensions so that a minimum of machining is required to produce a finished part. Casting of complex shapes can often eliminate costly joining, machining, and forming operations, resulting in cost savings in the manufacture of such parts.

A major factor in the properties of cast metals is their soundness, i.e., lack of porosity and nonmetallic defects. Nearly all castings have some defects, such as porosity, gas holes, and shrinkage voids. These defects depend on foundry practice, mold design, pouring practice, and the design of the part. It is important that casting designers consult with foundries during design to reach agreement on defect limits, dimensional tolerances, degree of nondestructive evaluation (NDE), and so forth, because the allowable defects and dimensional tolerances will have an effect on the cost of the part.

The specified mechanical properties for castings are generally based on separately cast test bars. These test-bar values may vary widely from the actual strength of a casting because of existing defects in the casting. Where strength is critical, many foundries will guarantee properties in the actual casting in lieu of separately cast test-bar values. In any case, the properties required of the casting and the means of verification of the properties must be communicated to the foundry.

The cooling rate of metal has a major effect on the properties of the casting. The grain size of the metal decreases as the cooling rate increases, and small grain size generally means increased strength.

Cooling rate is affected by the thickness and mass of the metal shape being cast. Thus, a small, thin-wall casting will be of higher strength than a thicker-wall, massive casting of equal soundness.

The mold material will also affect cooling rate and thus strength. A metal mold (known as a *permanent mold*) will cool a part faster than a sand mold. The mass of the mold, preheating practice, and so forth will also affect the cooling rate.

Castings are widely used in the manufacture of many parts to allow the least amount of machining, joining, and forming. However, they require special care in specifying defect limits and property limits to ensure that required mechanical properties are met.

Not all metals can be readily cast into shapes of any great complexity, although practically all metals are cast into ingots for working into shapes by deformation methods. In the copper, aluminum, and magnesium alloy families, specific alloys have been developed for castings and for wrought alloys. There are exceptions where an alloy may be available as both a casting and as a wrought alloy, but the general separation remains.

In recent years, some special casting processes, such as semisolid metalworking and metal injection molding (MIM), have been used to produce near-net shape castings of low-thermal-expansion materials such as Al/SiC and tungsten-copper. The initial cost of the molds is relatively high for these processes. They are typically feasible where the number of part can justify the high initial cost or the performance achieved by these materials is critical to the application.

**4.1.4.2 Wrought metals.** The majority of metals and alloys are furnished in a wrought form; that is, the metal has been subjected to some shaping operation by deformation in the solid state. Among these operations are rolling, drawing, extruding, and forging.

Such operations will have major effects on the final properties of the material. These operations affect grain size, crystallographic orientation, homogeneity, soundness, size and shape of inclusions, size and shape of metallurgical phases, and so on. These factors affect strength and ductility, formability, directional physical and mechanical properties, as well as reaction to subsequent heat treatment.

The temperature at which the metal is deformed or worked is important in its effect on properties. Hot-working is defined as deformation done at temperatures above the recrystallization temperature of the metal. The recrystallization temperature is that temperature above which a metal will form new, strain-free grains as rapidly as the old grains are strained by the working process. At high temperatures, the metal is not hardened by the working process; thus, large amounts of deformation may be carried out without fracturing the metal.

Cold-working takes place below the recrystallization temperature and thus results in strain hardening of the material, because new grains cannot be formed to relieve the strain set up by deformation.

Wrought metals are formed to shape by either hot-working alone or by combinations of hot-working and cold-working. Simplified descriptions of some of the wrought product procedures follow.

**4.1.4.3 Extrusion.** This process generally uses a billet as raw material. In most cases, the billet is a casting. The billet is heated above the recrystallization temperature and then forced through a die of suitable shape to form the finished shape. As can be seen by the description, this is a hot-working process in essentially one direction. No appreciable work hardening occurs in this process. In some metals, the tensile strength is considerably higher than the compressive strength in the longitudinal direction. Often, it is the lowest-cost method to produce shapes with complex cross sections.

**4.1.4.4 Forging.** This is generally a hot-working process that starts with a cast billet that is shaped by hammering or pressing to form a shape. To obtain optimal properties, it is important that the cast structure be completely worked to form a grain structure and to close up shrinkage voids in the cast billet. The mechanical properties of forgings will depend to some extent on the flow direction of the metal during forging. For highest strength, forging suppliers should be consulted during design to ensure that the correct flow pattern can be attained.

**4.1.4.5 Rolling.** Sheet, plate, strip, and many bars and shapes are formed by rolling. This process accounts for the longest tonnage of metal produced.

Rolled parts typically begin with a large cast billet, which is heated well above its recrystallization temperature and reduced to a slab or billet by rolling. This slab or billet is then hot-worked to some thin long shape such as sheet. Hot-rolling helps to break up the large grains common to cast structures found in the ingot, replacing it with finer, uniform, recrystallized grains. The rolling also tends to close in voids, resulting in a more dense, defect-free metal. This is an essential step in getting a high-quality product.

Hot-rolled products tend to have relatively rough surfaces with some rolled-in scale. This, of course, is not desirable for most electronic purposes. The mechanical properties of hot-rolled properties are generally close to the annealed (or weakest) properties for that particular composition.

Some rolled products used in the electronics industry are given final shaping to finished dimension by cold-rolling after initial hot-rolling. This rolling results in better surface finishes, closer dimensional tolerances, and (under proper control) can result in higher strength as a result of cold-working. In some cases, this may result in a cost savings if the closer tolerance results in fewer machined surfaces. Many metals achieve their high-strength properties



via strain hardening by cold-working. Many aluminum, copper, magnesium, and nickel alloys, and all pure metals, cannot be strengthened beyond their annealed strength by any method other than strain hardening.

In metals and alloys that are hardened by strain hardening, the thickness of the section being used significantly affects the degree of strengthening. Thin sheet, which can be thoroughly deformed through the entire thickness, will have higher strength than thicker material, which does not get worked thoroughly. The designer should be careful not to assume that strengths shown for one thickness apply to all thicknesses.

Strain hardening can give desirable increases in strength, but it also reduces ductility and formability. Reduction in electric and thermal conductivity can result from strain hardening. Stress corrosion can be another detrimental effect of strain-hardened materials.

#### 4.1.5 Strengthening mechanisms

To adequately specify metals and their processing, the designer should have a knowledge of the strengthening mechanisms and the interactions of these mechanisms with the manufacturing process. The major hardening mechanisms are discussed below, along with some of the limitations and advantages offered by these methods.

**4.1.5.1 Strain hardening.** As discussed above, cold-working results in distortion of the crystal structure of metals, thus causing an increase in strength and hardness. Practically all metals strain harden to some extent, and it is the only way to strengthen some metals.

When strain-hardened metals are used in service, care must be taken that manufacturing processes do not exceed the recrystallization temperature of the metal. Such temperatures will result in loss of the strain hardening, and the metal will revert back to the annealed state. Such processes as welding and brazing are prime examples of heat sources that will reduce work-hardened materials back to their annealed state.

**4.1.5.2 Precipitation hardening (age hardening).** Many alloy compositions are such that the solid solubility of one metal into the other increases with temperature. By heating the alloy to a temperature at which the solubility is high and then quenching quickly to room temperature, the solute is retained in solution. Essentially, the alloying elements dissolve into the base metal. This process is known as *solution treating*. Subsequent aging at a suitable temperature precipitates out the solute uniformly throughout the crystallographic structure, causing lattice distortions that result in an increase in mechanical properties. Some alloys are aged to some degree at room temperature. Care must be taken not to exceed the specified time or temperature of the precipitation-hardening treatment. An overaged condition results wherein the mechanical properties are greatly reduced.

Materials of this type offer the advantage of allowing forming or other working in the annealed or soft condition, with subsequent heat treatment to produce higher strength. Also, parts may be welded, brazed, or otherwise heated during fabrication and then brought to high strength after these operations by solution treating and aging.

The sequence of solution treating and aging can be varied somewhat, depending on the circumstances. As mentioned above, both solution treating and aging may be carried out on the final assembly. One disadvantage of this procedure is that the fast cooling required for solution treatment may result in distortion. However, to get full strength from an assembly that has been heated above the aging temperature, this sequence is necessary.

Forming of metal in the solution-treated condition is done in many cases. The solution-treated condition is usually relatively ductile, thus permitting reasonable formability. After forming, a relatively low-temperature aging will result in full strength and hardness. Another variation of this procedure is to solution treat the raw stock just before forming. This takes advantage of the fact that solution-treated material is softest immediately after solution treatment. Examples of precipitation hardenable alloys include 17-4PH steel and 6061 aluminum.

**4.1.5.3 Phase-transformation hardening.** Some alloys, notably certain titanium alloys and many steels, are hardenable by manipulation of phase transformations. This mechanism takes advantage of the fact that a normally two-phase alloy can be converted to a one-phase alloy by heating to elevated temperature. Quenching from this temperature results in this single phase being retained at room temperature. Subsequent aging at moderately elevated temperature will cause the alloy to revert to the two-phase structure, but with much finer particles of each phase than would occur under equilibrium conditions. This fine structure results in increased strength and hardness.

Many metals are supplied with combined strengthening mechanisms. The most common instance is that of a material that is solution treated and then cold-worked by rolling or stretching, after which it is aged. This combination results in higher strength than could be attained by heat treatment or cold-working alone.

It is obvious that selection of a metal or alloy must take into consideration not only the final strength desired but also the feasibility of maintaining or attaining that property in fabrication.

#### 4.1.6 Mechanical properties

After chemical composition, the most commonly specified properties are the tensile properties. Usually, these consist of ultimate strength, yield strength, and percentage elongation as determined on a standard tensile test bar (per ASTM E8, for example). These properties are often all that need to be known to make a material selection for mechanical design. These values, however, represent data taken on machined test bars at room temperature under one

short-time loading. A number of factors that will reduce the design allowable stresses to well below the published tensile values are discussed below.

**4.1.6.1 Repeated loads (fatigue).** When loads are repeated, the allowable stress is reduced well below the tensile strength of the material. In other words, the metal will fail at stress levels well below the yield or ultimate tensile strength. With most nonferrous materials subjected to 10 million cycles of stress, the breaking stress can be one-third of the tensile strength. In considering fatigue data, attention should be paid to the type of specimen, the type of loading, and the condition of the test specimen with regard to notches. The presence of notches can further reduce fatigue stress to as low as one-fifth of the tensile strength. Improvement in fatigue has been brought about by improving surface finish and by various other methods.

The subject of fatigue is very complex and subject to some controversy. In designing for repeated loads, special attention should be given to the available data. Specific tests under service conditions are also recommended.

**4.1.6.2 Sustained loads.** Failure under long-time sustained loads may occur as a result of creep or fracture at stresses below the yield strength, as determined by the standard tensile test. Although this type of failure is thought of as occurring at relatively high temperatures, such phenomena do occur at room temperature.

**4.1.6.3 Temperature effects.** The strength of metals decreases as temperature increases. Ductility generally increases until temperatures near the melting point are reached. The reverse occurs on lowering temperature; that is, strength increases and ductility decreases. The decreasing ductility with decreasing temperature is not particularly severe with nonferrous alloys. No drastic embrittlement occurs, even at cryogenic temperatures.

It can be seen that the room-temperature tensile test values can be useful in the selection of materials, but the service conditions and type of loading can be important factors in selecting a safe design stress.

#### 4.1.7 Physical properties

Physical properties are a result of chemical composition, atomic arrangement, and temperature. In considering data on physical properties, the above factors should be considered. Practical situations in which significant changes in physical properties occur are briefly discussed below.

**4.1.7.1 Cold-working.** Slight decreases in electrical conductivity are experienced with cold-working on strain hardening.

**4.1.7.2 Heat treatment.** Heat treatment has various effects on the structure and distribution of alloying elements and phases and thus will often have major effects on physical properties, including electrical conductivity, thermal conductivity, density, thermal expansion, and sometimes elastic modulus. Many of these changes are insignificant for engineering purposes, but the electrical conductivity differences can be quite dramatic.

Precipitation hardenable alloys are especially prone to change in electrical conductivity with a change in heat-treat condition. The solution-treated condition usually has the lowest conductivity, because the alloying elements are in solution, a condition that gives low conductivity. Annealing results in conglomeration of the alloying elements, thus giving the effect of a mixture wherein the two phases may average out. Aging of solution-treated materials will usually result in some increase in electrical conductivity, but not to the extent that results from annealing.

Because of the crystal structure, some metals change in density when heat treated. Beryllium-copper is one such material. Beryllium-copper (UNS C17200, for example) is also an example of a material that undergoes a change in elastic modulus as a result of heat treatment.

**4.1.7.3 Temperature.** Physical properties change with temperature. Most of these changes are gradual. If the temperature changes result in a phase change, drastic changes in physical properties can occur. In magnetic materials, increasing temperature beyond the Curie temperature results in material becoming nonmagnetic.

It can be seen that, in using physical property data, attention should be paid to the details of service temperature and material condition.

#### 4.1.8 Manufacturing considerations

Selection of the material must always take into consideration the manufacturing processes to be used in fabricating the part. Material must be selected that can be processed to the final configuration economically.

Metallurgical properties of the materials selected will greatly influence the machinability, formability, and joining ability. Many times, compromises can be made to enhance manufacturing of the item. Knowledge of available fabrication equipment is also useful.

Some of the basic material characteristics that can be used to select materials for fabrication are discussed below.

**4.1.8.1 Formability.** The tensile test values for a material can be used as a reasonable guide for the selection of a formable material. The percentage elongation is a good indication of how much a material may be deformed. Also, a large difference between the ultimate tensile strength and the yield strength indicates good formability. Minimum recommended bend radii are also published for most materials and are sometimes included in specifications.

For drastic forming operations such as deep drawing, more sophisticated specifications of material properties are required. Grain size control is one of these. An optimal grain size along with a minimum elongation exists for most materials.

**4.1.8.2 Machinability.** Most metal alloys can be machined without great difficulty. Many alloys are made with specific chemical additions that improve machinability. These additions usually have the advantage that small chips are formed during machining. Many of these alloys have the disadvantage of being less formable, more brittle, and less weldable because of these additions. Care should be taken that the free-machining additions do not interfere with other fabrication techniques or sacrifice mechanical properties.

**4.1.8.3 Joining.** Alloy selection for joining is critical in designing a welded part. Often, the alloy selection determines the joining method, and vice versa. Bolt- ing, riveting, and other mechanical methods offer no real problem for most metals, but the metallurgical processes of welding, brazing, and soldering require considerable planning.

**4.1.8.4 Weldability.** The ratings on weldability are qualitative and are generally based on ability to be welded with conventional techniques. A metal or alloy may get a poor weldability rating for a number of reasons, including (1) tendency to crack during welding, (2) poor corrosion resistance of the weld, and (3) brittleness of the weld. To some extent, weldability becomes a function of the process that is used for welding. Much of the success in welding reactive metals such as aluminum, magnesium, and titanium is a result of the use of the inert-gas-shielded-arc methods of welding, wherein the molten metal is shielded from the air atmosphere by an inert gas. The development of the electron beam, with its narrow, deep-penetration weld, has resulted in successful welding of alloys and combinations of alloys that were formerly considered nonweldable. In addition, some solid state processes, such as roll bonding, explosive bonding, and friction welding, can produce an excellent metallurgical bond between dissimilar metals.

**4.1.8.5 Brazing.** Selection of an alloy to be brazed requires consideration of the melting point of the alloy to be brazed as compared to melting point of the brazing alloy. The relationship of the brazing temperature to the heat treating to be performed on the part should also be considered. If it is desired to have the final properties of the part in the heat-treated condition, the brazing alloy must have a melting point above the heat-treating temperature. The method to be used for brazing is important. Torch brazing locally heats the joint and may result in distortion. Furnace brazing requires heating of the whole part, resulting in less distortion but requiring fixturing in most cases. Induction

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brazing offers fast, localized heating. Dip brazing requires immersing the complete area to be brazed in a molten flux bath.

**4.1.8.6 Soldering.** Soldering is a low-temperature process that can be used on a wide variety of metals. Some nonferrous metals, such as aluminum and magnesium, are soldered with difficulty unless the surface is plated with a metal that is more easily soldered (tin, for example). Normal solders generally form galvanic cells with these alloys, and joints with poor corrosion resistance in the presence of moisture will result. These alloys may be plated with solderable coatings and then soldered much as other metals. Soldering is covered in detail in Chapter 5.

## 4.2 Comparative Data on Metals

It is obvious that, with the thousands of metal and alloy compositions available, and with the varying degrees of strain hardening, heat-treating conditions, and varying service temperatures, it is impossible to list all data for all conditions. A comparison of the range of properties available in an alloy group can usually narrow the selection greatly. Some general comparisons of a wide range of metals follow.

### 4.2.1 Yield strength comparisons

The yield strength of a metal is generally defined as the maximum stress to which a part is subjected in service. Figure 4.1 gives a comparison of the yield strengths of a number of alloys. It can readily be seen that there is a wide overlap of yield strength among the commonly used alloys. At stress levels below 40,000 psi, most alloy families have alloys that are adequate, and selection would be made on the basis of some other property or on cost factors.

### 4.2.2 Modulus of elasticity (Young's modulus) and stiffness

Figure 4.2 compares the elastic moduli of a number of alloys. Since this property indicates stiffness of a part, it plays an important design role. Note that there is little significant variation in elastic modulus for any one alloy family, even though yield strengths may vary as much as 20× in some alloy families.

Specific stiffness is calculated by dividing the elastic modulus by the density. In Fig. 4.3, various alloys are compared. Note that the commonly used structural metals such as aluminum, magnesium, and titanium are about the same, whereas nickel and copper alloys have somewhat lower values. The only standout material in this property is beryllium, with a value of 6 to 12 times that of common structural materials.

### 4.2.3 Strength-to-density ratios

In Fig. 4.4, the strength-to-weight ratios of a number of materials are compared. This figure shows that, when compared on a weight basis, some of the

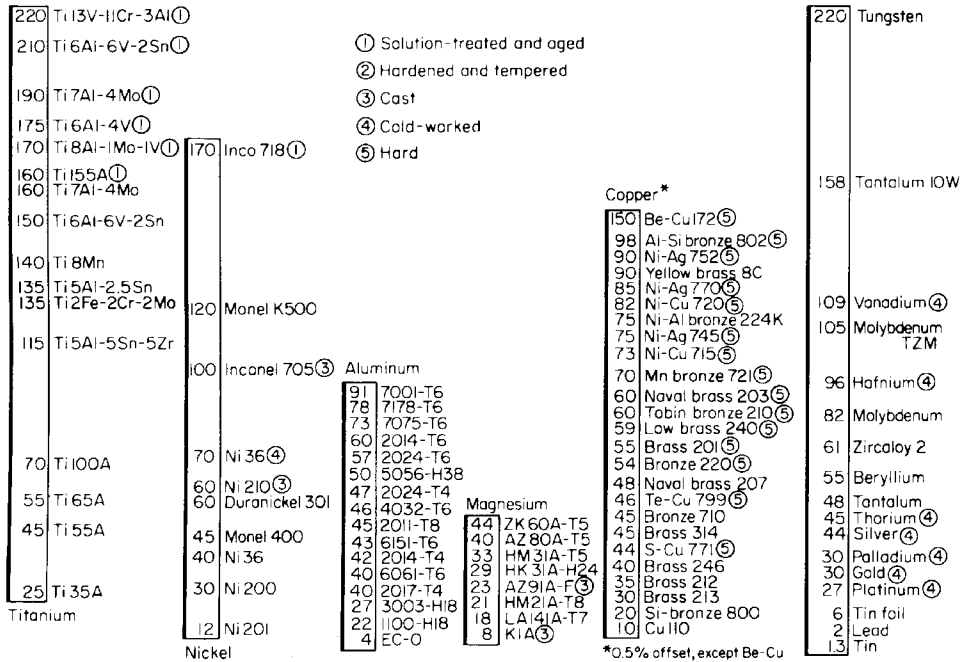


Figure 4.1 Tensile yield strengths of some nonferrous metals at room temperature (typical values  $\times 1000$ ).

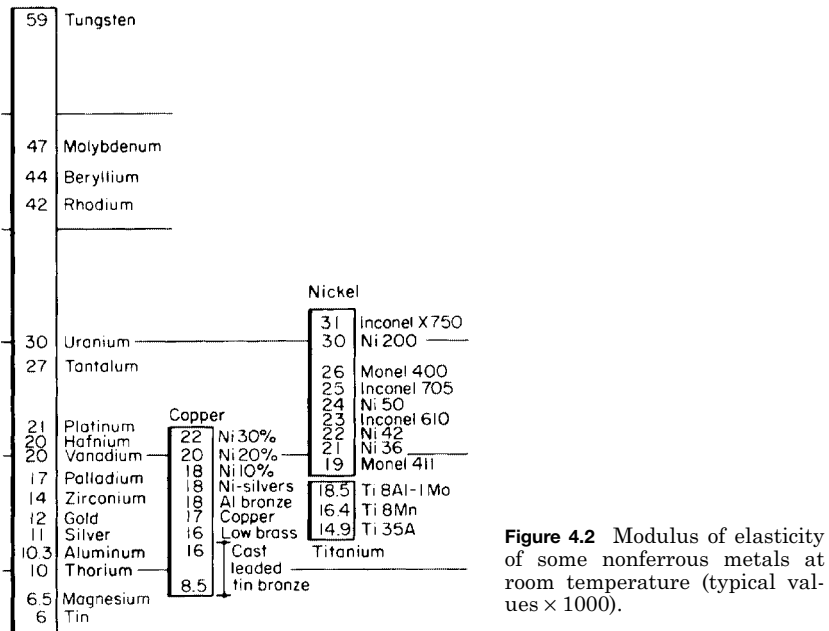


Figure 4.2 Modulus of elasticity of some nonferrous metals at room temperature (typical values  $\times 1000$ ).

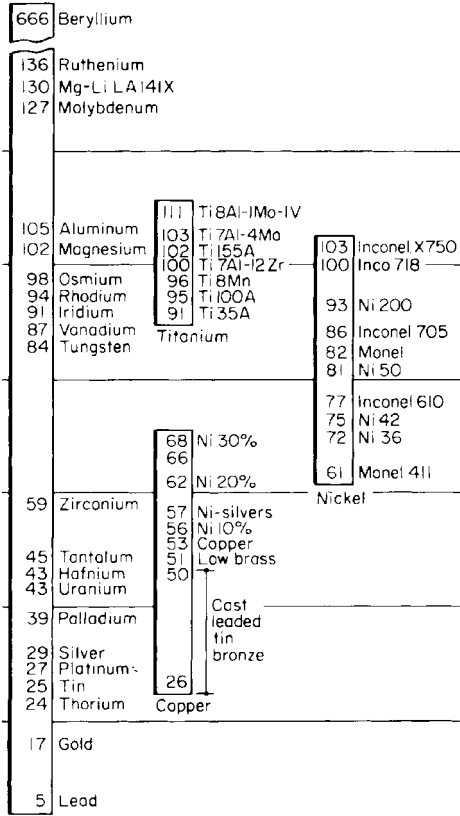


Figure 4.3 Specific stiffness of some metals at room temperature (typical values, modulus of elasticity × 10<sup>6</sup>/density).

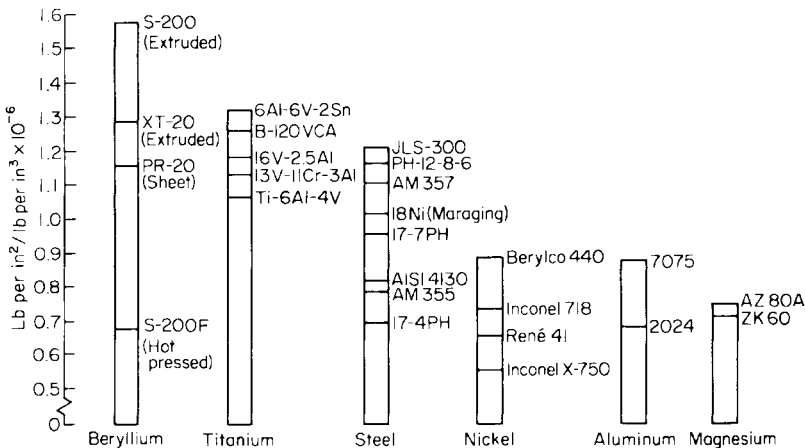


Figure 4.4 Ultimate tensile strength-to-density ratios of various structural materials at room temperature.



weaker, low-density materials are superior to the high-strength, high-density materials. Note that room-temperature comparisons do not necessarily hold at elevated temperatures.

#### 4.2.4 Thermal conductivity

In Fig. 4.5, thermal conductivities are compared. It can be seen that the pure metals—silver, copper, gold, and aluminum—have the highest thermal conductivities. Alloying in general lowers the conductivity, sometimes drastically.

#### 4.2.5 Electrical resistivity

Figure 4.6 graphs the comparative electrical resistivity of certain metals. Again, it should be pointed out that alloying will drastically affect electrical resistivity.

#### 4.2.6 Heat absorption

Figure 4.7 gives a comparison of the ability of metals to absorb heat. These values are for pure metals (with the exception of steel), and alloying can result in drastic changes. In addition, Table 4.1 lists the thermal properties of a

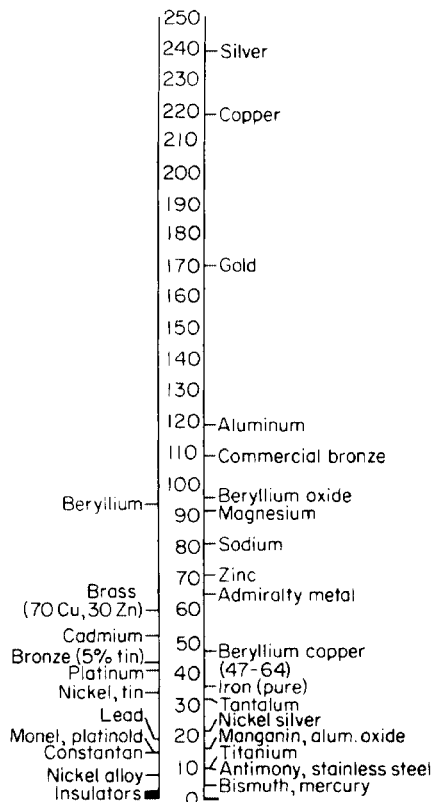
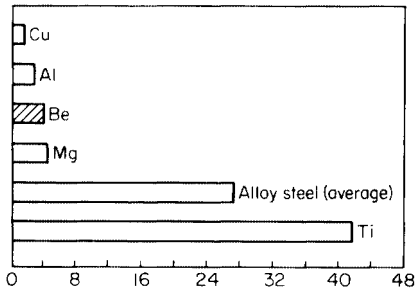
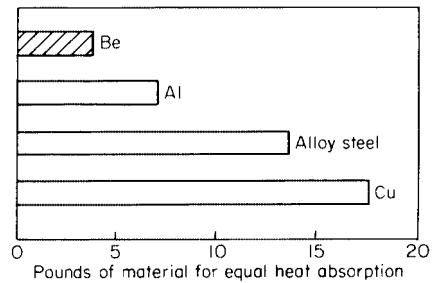


Figure 4.5 Thermal conductivity at 100°C for some materials.

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**Figure 4.6** Comparison of the electrical conductivities of several pure metals.



**Figure 4.7** Comparison of the heat absorption of several pure metals.

**TABLE 4.1 Thermal Properties of Several Pure Metals**

Property	Be	Mg	Al	Ti	Fe	Cu
Melting temperature						
°C	1277	650	660	1668	1536	1083
°F	2332	1202	1220	3035	2797	1981
Boiling temperature						
°C	2770	1107	2450	3260	3000	2595
°F	5020	2025	4442	5900	5430	4703
Thermal conductivity, cal/(sec)(cm <sup>2</sup> )(°C/cm)	0.35	0.367	0.53	0.41	0.18	0.94
Linear thermal expansion						
μin/(in)(°C)	11.6	27.1	23.6	8.41	11.7	16.5
μin/(in)(°F)	6.4	15.05	13.1	4.67	6.5	9.2
Specific heat, cal/(g)(°C)	0.45	0.25	0.215	0.124	0.11	0.092
Heat of fusion, cal/g	260	88	94.5	104*	65	50.6

\*Estimated.

number of pure metals. The above data were presented to give a first cut at comparisons among metals, in an effort to give the designer an idea of the range of properties available.<sup>8</sup>

#### 4.2.7 Ferrous metals (steels)

**4.2.7.1 General properties.** An alloy containing 50 percent or more of iron is considered to be a ferrous alloy. This section, however, also includes information on alloys that contain below 50 percent iron, because their specific desired properties are similar to those of the ferrous alloys. Ferrous alloys are divided into several categories such as typical compositions, specific properties, and standard trade designations. All three classes are employed; the class designa-

tions selected are those most commonly used in the industry. Many types of properties are sought from these alloys; i.e., magnetic properties, thermal expansion, electrical resistivity, thermal conductivity, corrosion resistance, and physical properties. Alloys discussed herein are classified by the following methods:

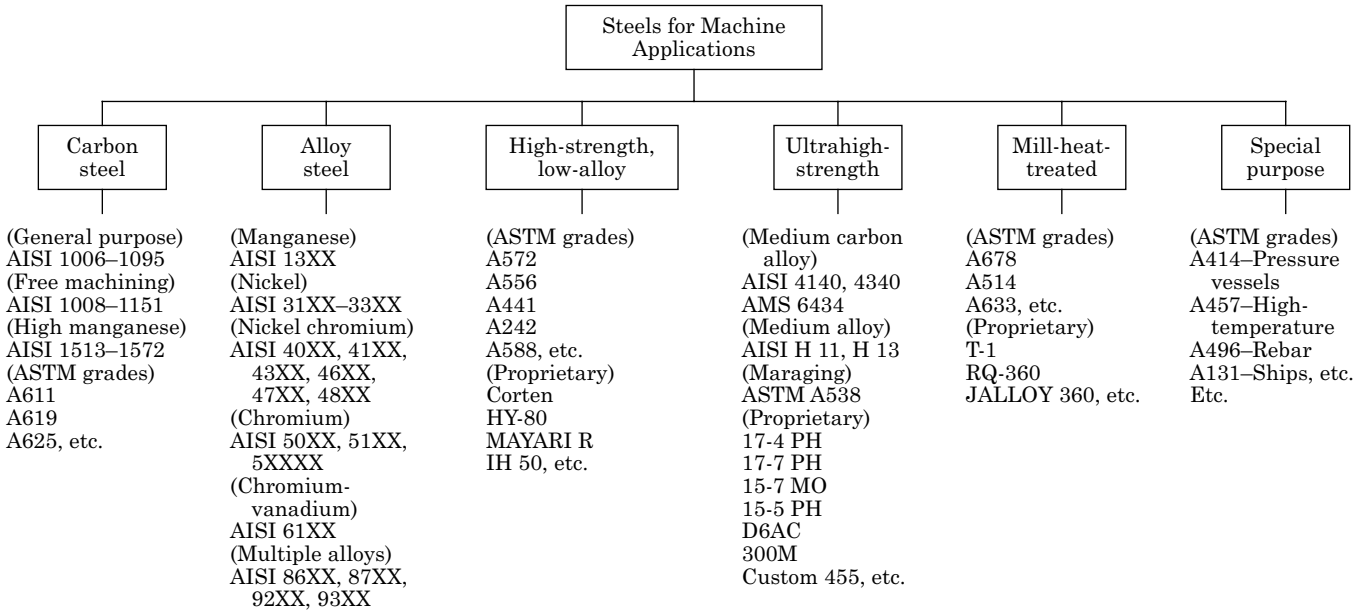
1. Typical composition when produced by two or more sources and each having a different brand name
2. Industry-designated brand names utilized by all sources such as the American Iron and Steel Institute (AISI)
3. Brand name if only available from one source

Various properties for these alloys are explained in terms commonly used in the industry. If the desired properties are not expressed in the units desired, conversion factors, in all probability, can be found. Properties not reviewed here may be available from producers of the alloys.<sup>9</sup>

**4.2.7.2 Alloy groups.** The high-strength, low-alloy, quenched and tempered, and some of the ultrahigh-strength steels were developed in recent years. They meet industry needs for weight reduction, higher performance, and, in many cases, lower costs. The disadvantage from the designer's standpoint is that it is becoming difficult to categorize steels in an orderly fashion to aid selection. The common denominator for the steel systems is use. They are the types of steels that would be used for structural components. Figure 4.8 outlines the categories. Even with the abundance of special-purpose steels, the workhorses are and for some time will continue to be the wrought ASTM, AISI-SAE carbon and alloy steels. Fortunately, these steels have an understandable and orderly designation system.

## 4.2.8 Composition-wrought ferrous alloys

**4.2.8.1 Carbon and alloy steels.** The most important identification system for carbon and alloy steels in the U.S. is the system adopted by the American Iron and Steel Institute (AISI) and the Society of Automotive Engineers (SAE). This system usually employs only four digits. The first digit indicates the grouping by major alloying elements. For example, a first digit of 1 indicates that carbon is the major alloying element. The second digit, in some instances, suggests the relative percentage of a primary alloying element in a given series. The 2xxx series of steels has nickel as the primary alloying element. A 23xx steel has approximately 3 percent nickel; a 25xx steel has approximately 5 percent nickel. The last two digits (sometimes the last 3) indicate median carbon content in hundredths of a percent. A 1040 steel will have a normal carbon concentration of 0.40 percent. The classes of steels in this system are shown in Table 4.2. In addition to the four digits, various letter, prefixes, and suffixes provide additional information on particular steels.



**Figure 4.8** Steel types used for machine applications.<sup>2</sup>

TABLE 4.2 Major Groups in the AISI-SAE Designation System<sup>2</sup>

Class	AISI series	Major constituents
<i>Carbon steels</i>	10xx	Carbon steel
	11xx	Resulfurized carbon steel
<i>Alloy steels</i>		
Manganese	13xx	Manganese 1.75%
	15xx	Manganese 1.00%
Nickel	23xx	Nickel 3.50%
	25xx	Nickel 5.00%
Nickel-chromium	31xx	Nickel 1.25%, chromium 0.65 or 0.80%
	33xx	Nickel 3.50%, chromium 1.55%
Molybdenum	40xx	Molybdenum 0.25%
	41xx	Chromium 0.95%, molybdenum 0.20%
	43xx	Nickel 1.80%, chromium 0.50 or 0.80%, molybdenum 0.25%
	46xx	Nickel 1.80%, molybdenum 0.25%
Chromium	48xx	Nickel 3.50%, molybdenum 0.25%
	50xx	Chromium 0.30 or 0.60%
	51xx	Chromium 0.80, 0.95 or 1.05%
Chromium-vanadium	5xxx	Carbon 1.00%, chromium 0.50, 1.00, or 1.45%
	61xx	Chromium 0.80 or 95%, vanadium 0.10 or 0.15% min.
Multiple alloy	86xx	Nickel 0.55%, chromium 0.50%, molybdenum 0.20%
	87xx	Nickel 0.55%, chromium 0.50%, molybdenum 0.25%
	92xx	Manganese 0.85%, silicon 2.00%
	93xx	Nickel 3.25%, chromium 1.20%, molybdenum 0.12%
	94xx	Manganese 1.00%, nickel 0.45%, chromium 0.40%, molybdenum 0.12%
	97xx	Nickel 0.55%, chromium 0.17%, molybdenum 0.20%
	98xx	Nickel 1.00%, chromium 0.80%, molybdenum 0.25%

**4.2.8.2 Stainless and specialty steels.** Stainless steels are an important class of alloys used for a wide range of applications and in many environments. They are used extensively in the power generation, pulp and paper, and chemical processing industries, but they are also chosen for use in many everyday household and commercial products. They are iron-base alloys that contain a minimum of approximately 11 percent Cr, the amount needed to prevent the formation of rust in unpolluted atmospheres (hence the designation *stainless*). Few stainless steels contain more than 30 percent Cr or less than 50 percent Fe. Carbon is normally present in amounts ranging from less than 0.03 per-

cent to over 1.0 percent in certain martensitic grades. Table 4.3 provides a useful summary of some of the compositional and property linkages in the stainless steel family.<sup>10</sup>

**4.2.8.3 Magnetic steels.** A wide range of magnetic characteristics are available from the many alloy combinations known to date. These magnetic characteristics are expressed in many specific parameters that have a significant meaning. To understand the information presented, one should be familiar with the general terms.

A general classification of magnetic alloys described herein is as follows:

1. High-permeability magnetic alloys
2. Permanent magnetic alloys
3. Stainless steel alloys
4. Temperature- compensator alloys

Magnetic parameters discussed here are typical for the respective alloy as determined by test methods having approval of ASTM Committee A-6, Magnetic Properties. An introduction to magnetic testing can be acquired by referring to ASTM Special Technical Publication 371, *Magnetic Testing: Theory and Nomenclature*. To discuss specific magnetic parameters of a given alloy, the method of test must be a standard test procedure that has been qualified by round-robin magnetic tests using an identical magnetic-core configuration. In cases for which a standard test does not exist, test methods must be identical, and the test equipment must be of identical circuitry. Reproducibility between test systems must be verified via the round-robin tests. This approach is employed in many instances between two or among several laboratories, because the ASTM standard methods of test do not provide all property information to predict performance in specific applications. Many nonstandard tests are employed today to express given properties in terms mutually agreed upon to express performance. These nonstandard test methods and procedures cover evaluations at all frequency levels, shapes of hysteresis loops, residual magnetism, types of magnetic field excitation, and the use of a selected magnetic-core configuration. If a magnetic core or magnetic-core section cannot be evaluated properly because of its shape, then a magnetic-core shape that is capable of being evaluated by standard methods of test can be subjected to the identical treatments. Standard magnetic tests will then provide property data in general terms.

Many magnetic materials, both high-permeability and permanent magnetic alloys, require thermal heat treatments or processes to achieve their designated optimal magnetic parameters. Each given magnetic material is capable of exhibiting a variety of magnetic properties as a result of heat treating and manufacturing processes; hence, it is necessary to specify details of heat treatment and test procedures. The manufacturing source must also control processing procedures so as to have minimal variation within a lot and from lot to lot.

**TABLE 1.8 Martensitic, Austenitic, and Precipitation Hardening Alloys** <sup>6</sup>

Martensitic alloys	
420	The basic martensitic alloy; corrosion resistant only in the hardened condition
410	Lower carbon content version of 420
440C	Higher carbon content version of 420; very hard and abrasion resistant
440A and 440B	Lower carbon content version of 440C; trades off some hardness to reduce brittleness
416	A free-machining variation of Type 410
420F and 440F	Free-machining variations of 420 and 440 C
430F	Free-machining variations of 430
430Ti	A small amount of titanium to is added to 430 to suppress all hardening during exposure to elevated temperature
Austenitic alloys	
302	The basic austenitic alloy containing 18% Cr and 8% Ni
304	Lower carbon content version of 302; better weldability and corrosion resistance
321, 347, 348	Type 302 with additions of titanium or columbium. The function of these added elements is to tie up all the carbon in the alloy so it cannot precipitate as chromium carbide. The columbium carbide is more stable than the titanium carbide (that is, more insoluble at higher temperatures), and for that reason the columbium alloy will withstand more severe conditions than Type 321.
304L	Even lower carbon version of Type 302, but still susceptible to sensitization; 0.03% C max.
303 and 303Se	Modifications of 302, to which sulfur or a combination of phosphorus and selenium are added to improve the machinability
302B	Type 302 with an addition 2% silicon; has a maximum operating temperature of 1800°F
308	Used mainly as a welding wire used to deposit an 18-8 analysis in the weld, allowing for some dilution during welding
310	The grade with the highest chromium content, chiefly known for its high scaling resistance
316, 316L, 317, 317L	Type 316 is generally considered to be the most corrosion resistant of all stainless steels. However, even Type 316 is considered borderline corrosion resistant when exposed to certain chemicals. An increase in the molybdenum content of approximately 1% (317) is believed to provide pitting and general corrosion resistance. Both of these molybdenum-bearing stainless steels find many applications requiring welding. 316L and 317L are the extra low carbon grades produced for these applications.
301	The corrosion-resistant grade includes a lower carbon level and a small increase in columbium to eliminate sensitization. The presence of copper improves the corrosion resistance in phosphoric acid solutions especially.
305	Low work-hardening rate alloy for cold-heading applications
201 and 202	200 series alloys were developed to conserve nickel during a time of nickel shortage. By substituting increased amounts of nitrogen and manganese for some of the nickel, it is possible to arrive at an analysis that has engineering properties very similar to the 300 series. The 200 series steels have slightly higher high-temperature strengths and room-temperature hardness due to the nitrogen. They also have higher work-hardening rates and are slightly less corrosion resistant.

TABLE 1.8 Martensitic, Austenitic, and Precipitation Hardening Alloys (Continued)<sup>6</sup>

Precipitation-hardening alloys	
17-4PH	The advantages of utilizing this precipitation hardening method rather than the phase change used in Type 410 include freedom from heavy scaling, freedom from warpage, and excellent surface quality, undamaged by heat treatment. In addition 17-4 PH exhibits corrosion resistance that is definitely superior to the Class I alloys and is equivalent to 18-8 in most corrosion environments.
17-7PH and PH 15-7 Mo	These semiaustenitic steels are austenitic at room temperature when they have been solution annealed at 1900–2000°F and rapidly cooled. As such, they are soft and ductile and can be formed or drawn. As with 17-4 PH, the hardness immediately after transformation is relatively low: Rockwell C 30. The final heat treatment once again consists of an aging or precipitation hardening heat treatment at 950–1150°F, and hardness from Rockwell C 38 to C 49 is possible. The precipitation hardening is achieved by the addition of about 1% aluminum. 17-7 PH serves in many general applications. In PH 15-7 Mo, the chromium was replaced with molybdenum to achieve higher creep and rupture strengths in the temperature range of 700–1000°F.

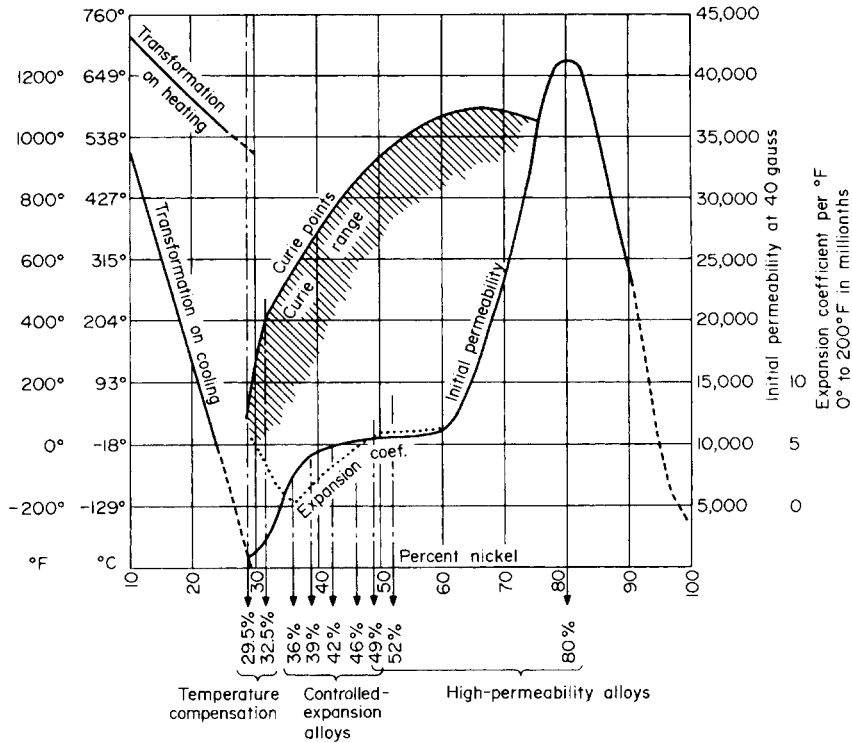
#### 4.2.9 High-permeability magnetic alloys

High-permeability magnetic alloys, also known as *soft magnetic alloys*, are required to have low magnetic hysteresis loss resulting from variations in the magnetic flux density produced within the alloy and a low residual magnetism after being subjected to a high magnetic field strength. This class of alloys does not retain permanent magnetic poles to any significant degree after being highly magnetized. Several alloy families produce magnetic properties that are of interest to the industry. Within each family, specific alloy compositions have been selected by the industry as standard grades because of best magnetic properties for a large number of applications.

**4.2.9.1 Nickel-iron alloys.** This family of alloys contains 30 to 80 Ni, with the balance Fe, and exhibits a variety of magnetic and expansion properties. In some cases, small percentages of other elements are added to obtain more desirable magnetic properties for certain applications. Figure 4.9 shows the effect of nickel content on initial permeability and Curie range and Curie points. All the nickel-iron alloys used for magnetic properties contain low carbon and cannot be hardened or have their hardness increased by thermal heat treatment. Hardness can be increased only by cold-working the alloy, and the higher the hardness, the lower the high-permeability characteristics. Thermal heat treatment will reduce the hardness, and the lower the hardness, the higher the high-permeability characteristics will be. Hardness, however, in the softest condition, is no reflection on the degree of optimal high-permeability melt to melt, or lot to lot from the same melt.

Producers of steel-mill products do not supply the alloys in the high-permeability condition in forms of bar and strip, because subsequent fabrication operations such as machining, bending, forming, and deep drawing reduce the high-permeability properties by the introduction of cold-work stresses. Parts





**Figure 4.9** Effect of nickel content on magnetic and expansion properties of some high nickel-iron alloys.

must be subjected to the thermal heat treatments to achieve most uniform desired magnetic properties.

High-permeability materials can be purchased in several types of physical conditions for easiest fabrication, depending on the part to be made.

Suggested physical conditions are as follows:

- Blanking of flat parts—Rockwell B-90 minimum
- Blanking and forming—Rockwell B-75/85
- Best forming or deep drawing—Rockwell B-75 maximum

Each alloy is capable of exhibiting a variety of magnetic properties. Lowest magnetic properties are observed in the cold-work or high-hardness condition; hence, any thermal heat treatment relieving cold-work stresses will improve the magnetic characteristics over those originally shown. Heat treatments should be conducted in a nonoxidizing, noncarburizing, noncontaminating atmosphere.

Atmospheres generally employed are dry hydrogen, dissociated ammonia, argon, dry nitrogen, and vacuum. It is recognized that the best atmosphere is dry hydrogen. The heat treatment is conducted in a sealed retort or equivalent. A continuous flow of atmosphere in the retort ensures the removal of un-

desirable gas compounds given off by the alloy, and this helps to improve the magnetic quality. Elements removed from the alloy are carbon, oxygen, and sulfur. It is necessary to study the magnetic properties of the heat-treated parts by varying temperature, time at temperature, and cool rate for establishing the treating procedure for a given facility.

Recommended heat treating for highest permeability in the nickel-iron family of alloys is as follows:

1. The retort should be capable of being gas tight or vacuum tight: i.e., a sealed retort.
2. Purge or flush the retort to free it of ambient atmosphere.
3. Introduce a protective or purifying atmosphere.
4. Heat the retort to 1120 to 1170°C.
5. Hold 2 to 4 hr at temperature.
6. Cool at a rate recommended for the alloy.
7. Use a protective or purifying atmosphere until the chamber is cooled to 200°C or less.
8. Introduce an inert atmosphere until cooled below 100°C.
9. Open the retort.

Typical magnetic properties of the most common high-permeability alloys are given in Table 4.4. Recommended heat treatments for obtaining these magnetic properties are shown for each alloy. These data apply to cold-rolled strip items of 0.030 in or thicker and bar items. Figure 4.10 provides the normal induction curves for the various alloys.

Alternating-current magnetic properties vary considerably, depending on lamination thickness, degree of interlaminar resistance, lamination shape, and frequency of the magnetizing current. Because each alloy exhibits a wide variety of AC magnetic characteristics, each commercial grade will be reviewed separately.

**4.2.9.2 80 Ni, 4 Mo, balance Fe.** This alloy is recognized as one of the highest initial permeability alloys and is used for its response to very low magnetizing forces. Trade names are 4-79 Permalloy<sup>1</sup> HyMu 80<sup>2</sup> and Hipernom.<sup>3</sup>

Magnetic-core and lamination manufacturers have applied various other brand names to the alloy. The most common application for this alloy is in the form of laminations 0.006 and 0.014 in. thick; hence, 60 and 400 Hz data are readily available. See Figs. 4.11 and 4.12 for typical data. Core loss data are given in Fig. 4.13. The alloy is available in strip form as thin as 1/8 mil (0.000125 in), which is used to manufacture small bobbin cores having specific square hysteresis-loop properties. Thicknesses in the range of 0.5 to 4 mils are used to manufacture numerous types of magnetic cores such as tape toroids

TABLE 4.4 Typical DC Magnetic Properties of Some Nickel-Iron Alloys

Property	45 Ni, bal. Fe	49 Ni, bal. Fe	49 Ni, 0.15 Se, bal. Fe	47 Ni, 3 Mo	78.5 Ni, bal. Fe	77 Ni, 1.5 Cr, 5 Cu	80 Ni, 4 Mo	80 Ni, 5 Mo
Heat treatment, Hz	←————1140/4/1————→				1040/2/ 600 Q	1140/4/1	←————1140/4/5————→	
$B_{40}$ permeability	5,000	7,000	3,200	4,000	8,000	20,000	50,000	70,000
Max. permeability	60,000	75,000	10,000	70,000	120,000	150,000	200,000	150,000
Approx. $B$ at max. permeability	8,000	7,000	6,000	5,000	3,000	3,000	3,500	3,500
Coercive force, oersteds	0.07	0.04	0.25	0.08	0.02	0.02	0.01	0.009
From $B$ , gauss	10,000	10,000	10,000	10,000	10,500	5,000	7,000	7,000
Saturation induction, gauss	15,000	15,500	15,000	163,500	13,000	6,500	7,700	8,500
Curie temp., °C	460	500	500	460	600	400	460	450
Electrical resistivity, $\mu\Omega$ -cm	45	48	48	80	20	60	58	63
Density, g/cc	8.17	8.25	8.25	8.27	8.45	8.50	8.74	8.75

Q = quench from temperature.

Heat treatment: 1140°C for 4 hr at temperature; 1°C/min cool rate (1140/4/1).

for high initial permeability and tape toroids having square hysteresis loop characteristics. Typical magnetic properties of strip at thicknesses of 1, 2, and 4 mils are given in Table 4.5.

TABLE 4.5 Typical Magnetic Properties of 80 Ni, 4 Mo, Balance Fe

Thickness, in	1-, 2-, and 4-mil square loop properties*					
	$B_{40}$ @ 60 Hz	$B_m$ , gauss	$B_m - B_r$ , gauss	$H_1$ , oersteds	$\Delta H$	$\mu$ @ $B_{40}$ and 15 kHz†
0.001	70,000	7,000	1,000	0.030	0.006	20,000
0.002	80,000	7,000	1,200	0.030	0.006	12,000
0.004	80,000	7,000	1,500	0.035	0.009	

\*Constant-current, flux-reset method of test per AIEE No. 432. Heat treatment: 1160°C for 0.5 hr at temperature, 1–5°C/min cool rate.

†Heat treatment: 1170°C for 1–4 hr at temperature; 5–15°C/min cool rate. Tape toroid ID/OD 0.80 ratio.

As stated previously, a wide variety of magnetic characteristics are obtainable by various heat treatments, as shown by 0.006-in lamination strip in Fig. 4.14. The magnetic properties will also be altered by time at temperature and

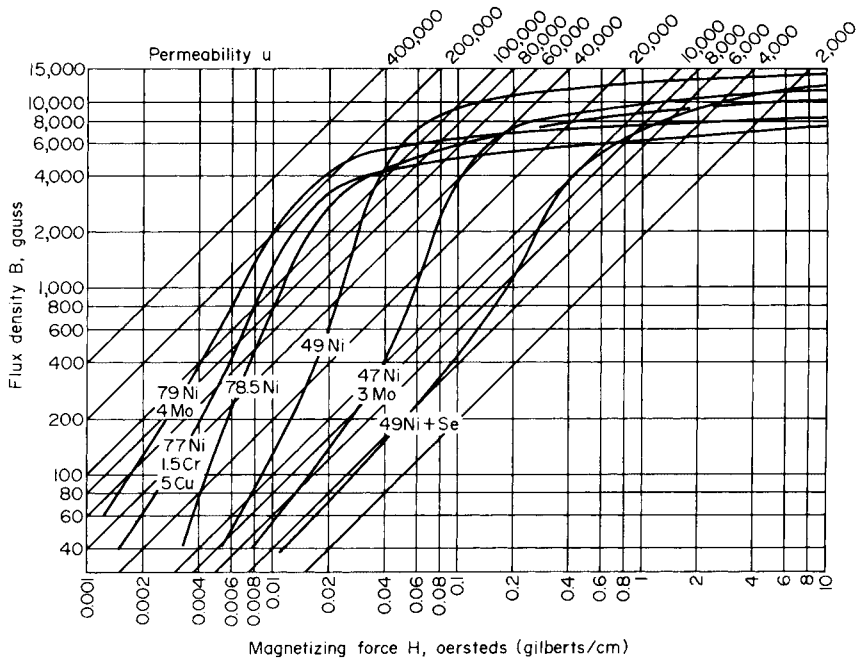
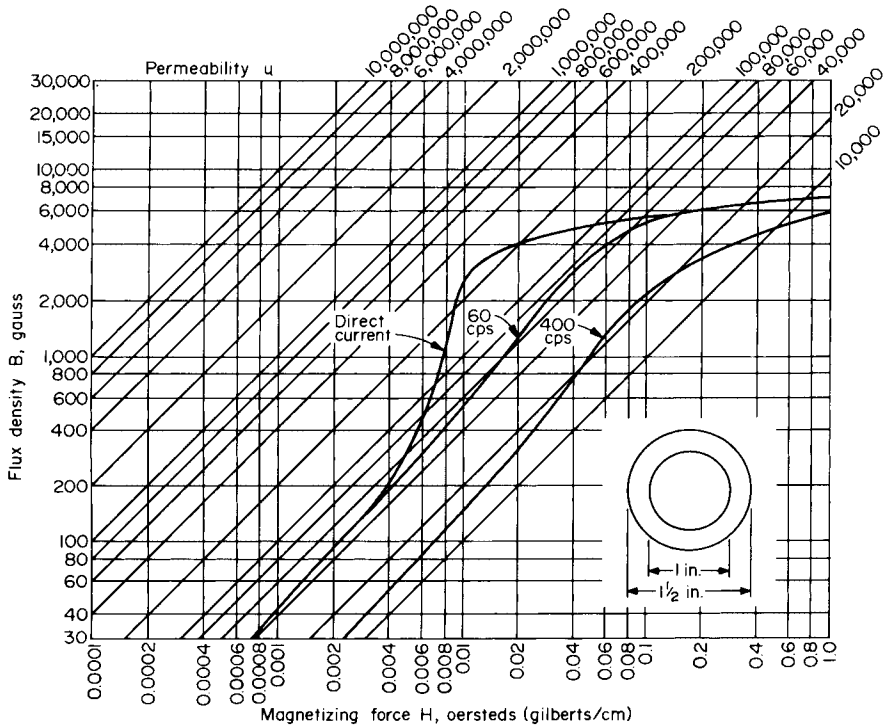


Figure 4.10 DC normal induction curves for some nickel-iron alloys.

cool rate; i.e., in some cases, magnetic-core parts are heat treated through the continuous furnace and produce acceptable magnetic properties for the given application. Because the alloy shows a very low hardness value (Rockwell B 50/55) after heat treatment, parts cannot be stressed or deformed without a loss and change in magnetic properties. Extreme care must be exercised during handling. Magnetic-core parts heat treated at lower temperatures are less strain sensitive.<sup>4</sup> General literature on other basic magnetic properties is available from the alloy producers in the U.S. such as Carpenter Technology.

**4.2.9.3 77 Ni, 1.5 Cr, 5 Cu, balance Fe.** This alloy has high initial permeability properties and is well known as Mumetal.<sup>1</sup> Its handling characteristics are similar to those of the 80 Ni, 4 Mo, balance Fe alloy. General magnetic characteristics for laminations, magnetic cores, and shields are available from the producer.

**4.2.9.4 49 Ni, balance Fe.** The alloy composition of 49 Ni, balance Fe is capable of producing a fairly high initial permeability with a moderately high magnetic saturation. Magnetic-core components are used where response is necessary in a fairly weak magnetic field; they have minimum residual magnetism where very small air gaps are in the magnetic circuit and show fairly good properties in AC magnetic fields. General usage is in the form of lamination strip, fabricated relay parts, and flux-carrying members and precision



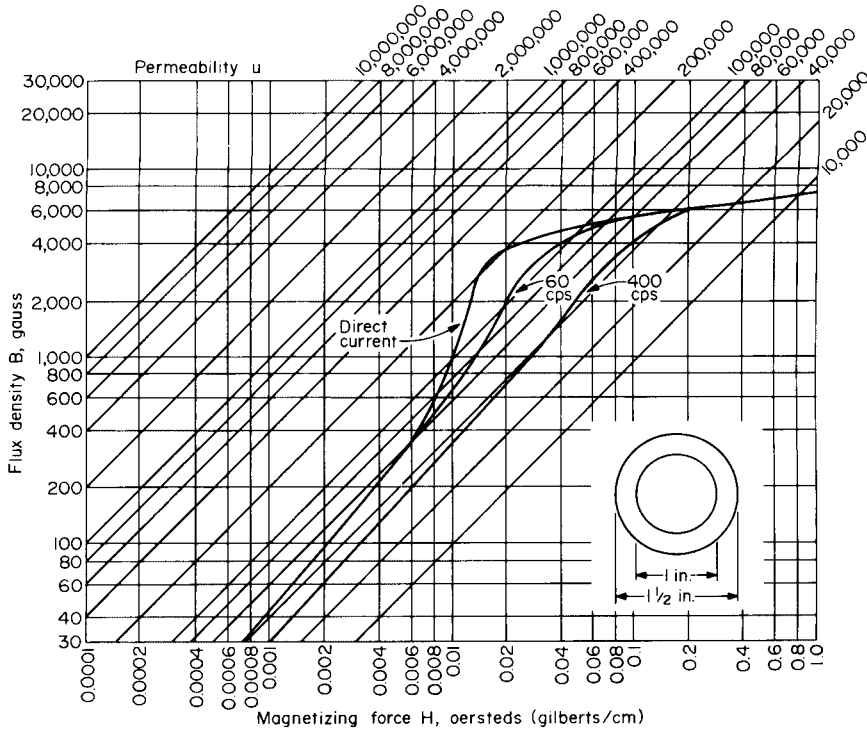
**Figure 4.11** DC and AC magnetic properties of 80 Ni, 4 Mo, balance Fe lamination strip, 0.014 in thick.

castings. A free-machining grade is available; however, there is a substantial sacrifice in the magnetic properties.

Through controlled melting practice and strip manufacturing procedures, several types of strip products are available in the industry to achieve specific types of magnetic properties that can be utilized in specific types of magnetic cores. This applies to strip products 0.020 in and less. The strip products are referred to as highly oriented, semioriented, and random-oriented. In each case, the strip product must be fabricated and heat treated as recommended to achieve the magnetic properties desired.

The semioriented grade is preferred for transformer lamination applications, because it has the highest magnetic properties when heat treated above 1000°C. Lamination strip AC properties are given in Figs. 4.15 and 4.16. Core-loss values appear in Table 4.6.

The random-oriented grade is recommended for rotor and stator laminations that must have minimal directional magnetism. The most suitable method of detecting this grade is a very fine grain size when heat treated at 1100°C (mean grain diagonal of 0.040 in). The semioriented grade will show a very coarse grain when heat treated under similar conditions. Basic magnetic properties of the random-oriented grade are slightly lower than those of the semioriented grade; however, they are superior to those of the semioriented



**Figure 4.12** DC and AC magnetic properties of 80 Ni, 4 Mo, balance Fe lamination strip, 0.006 in thick.

grade when heat treated below 1000°C. The effect of temperature on magnetic properties is shown in Fig. 4.17.

Highly oriented 49 Ni, balance Fe is marketed in strip form, from 0.5 to 14 mils, and is used for its square hysteresis loop properties after heat treating the fabricated cores. Laminations 0.006 and 0.014 in thick are available for certain types of magnetic cores.

Soft magnetic alloys are employed to shield magnetic components and electron beams from undesirable external magnetic fields that affect their function. This is accomplished by utilizing the soft magnetic alloy to deflect or carry around the undesirable magnetic field. Shields can also be used to contain undesirable magnetic fields by surrounding the undesirable source. Shielding efficiency in dB, a function of the magnetic alloy thickness, magnetic permeability, and shape of the shield, can be calculated for long, thin cylinders, using the equation

$$\text{S.E.} = 20 \log \mu t / 2R_o \quad (4.1)$$

where  $\mu$  = permeability  
 $t$  = thickness  
 $R_o$  = outer radius of shield

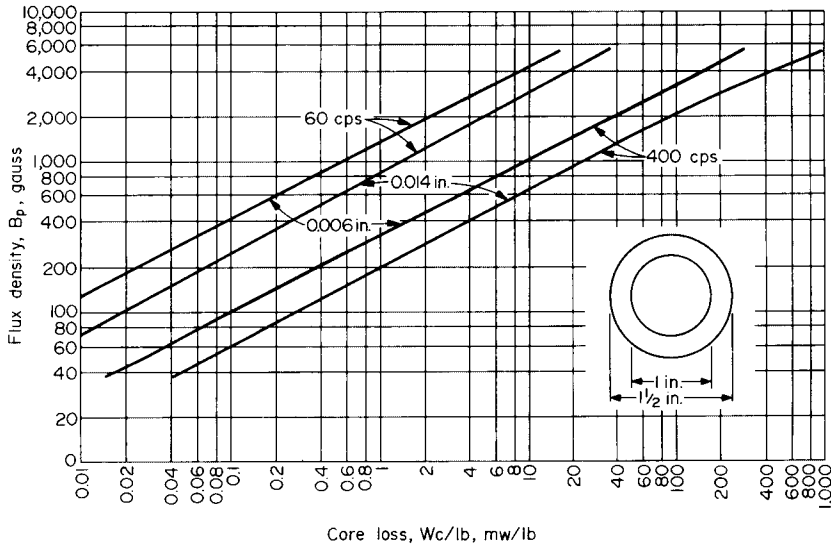


Figure 4.13 Core loss of 80 Ni, 4 Mo, balance Fe lamination strip.

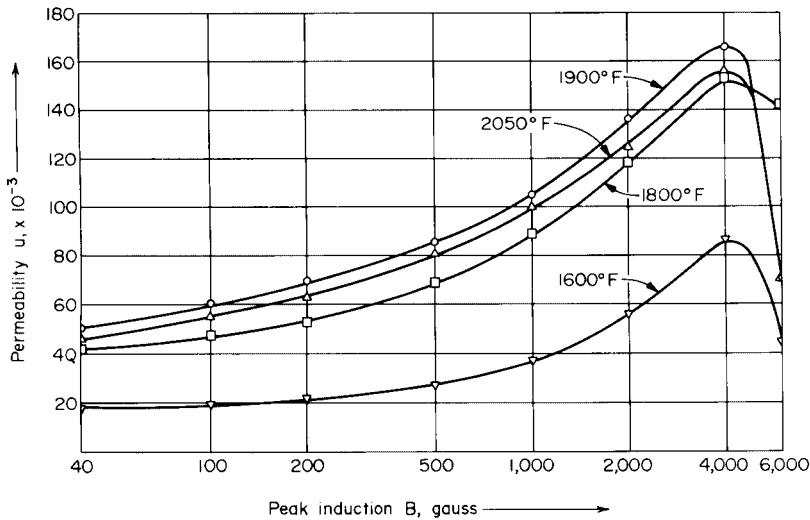
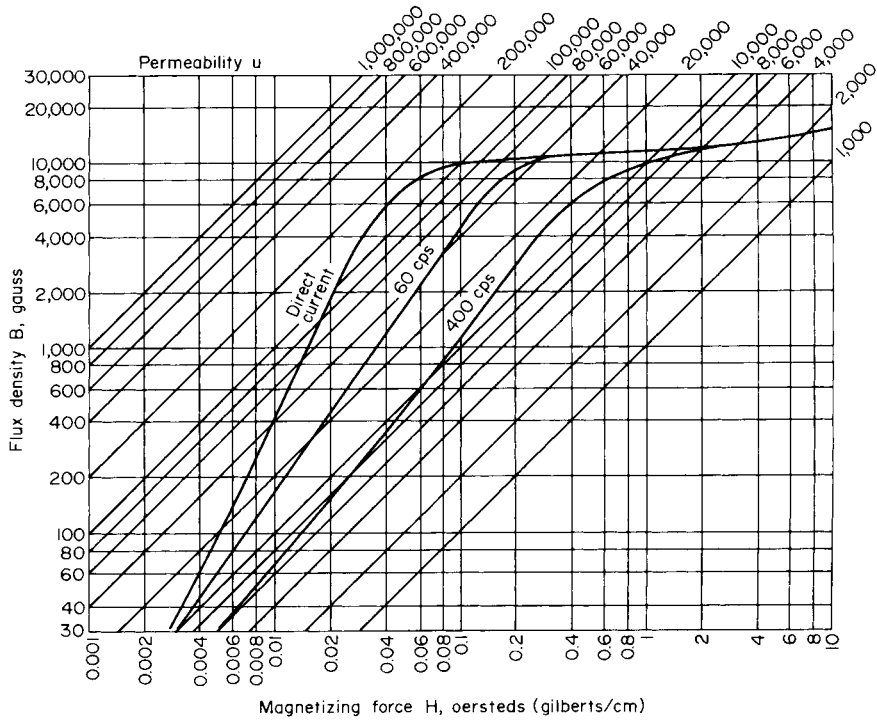


Figure 4.14 AC permeabilities vs. induction at 60 Hz for 80 Ni, 4 Mo, balance Fe, 0.006-in stamped rings for various 4-hr anneals.

This equation can be useful in determining how much the shield dimensions should be modified to compensate for a change in shield material permeability.

Laminated shields provide greater efficiency. To protect from very high-frequency fields, copper and soft magnetic alloy laminates are employed. Specific information regarding magnetic shielding is presented in Ref. 11.

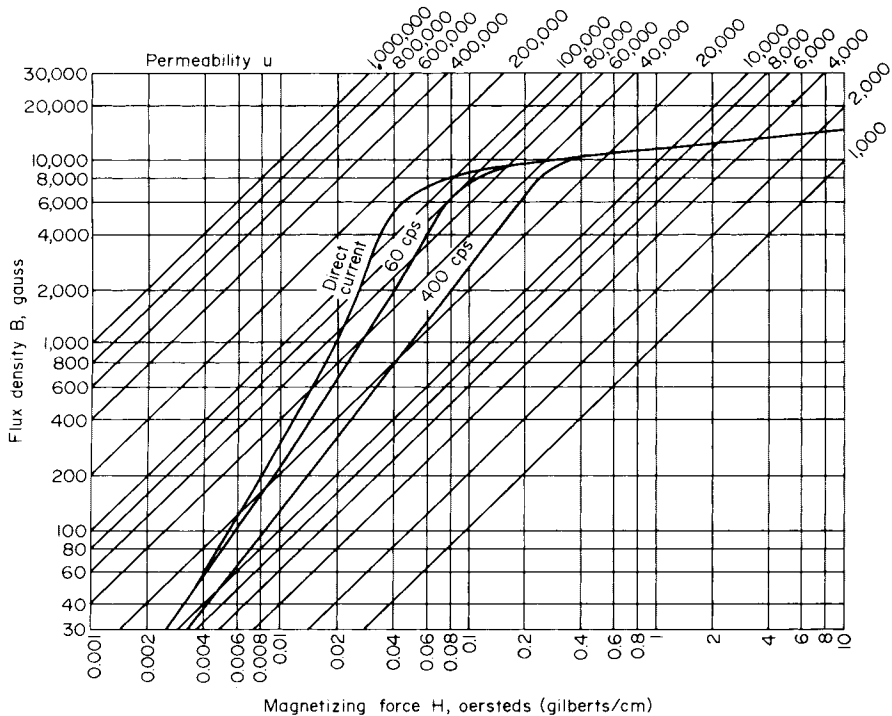


**Figure 4.15** DC and AC magnetic properties of 49 Ni, balance Fe semioriented lamination strip, 0.014-in strip.

**4.2.9.5 Silicon-iron alloys.** The family of silicon-iron alloys has a very important role in the field of magnetics because of their low cost and because of having been engineered into systems wherein an appreciable amount of electric power is involved. Even though their response to weak magnetic fields is inferior to that of the nickel-iron alloys, their magnetic characteristics surpass those of other alloys in the field of electronics under certain conditions. A considerable amount of property evaluation has been conducted for the electrical industry, and electric core-loss requirements have been established for the electrical sheet industry. Basic magnetic requirements of commercial grades are given in Ref. 11.

Three types of silicon-iron alloys in thick strip and bar forms are being fabricated into many shapes of magnetic cores and magnetic flux-carrying members. Machining operations, forgings, and precision castings make all shapes and sizes available. Commercial available grades have nominal silicon contents of 1, 2.5, and 4 percent. For improved machining properties, the silicon contents of 1 and 2.5 percent are available in free-machining grades. As with all other high-permeability alloys, a thermal heat treatment is required to obtain uniform magnetic properties from part to part. Magnetic properties improve with increasing heat-treating temperature.





**Figure 4.16** DC and AC magnetic properties of 49 Ni, balance Fe semioriented lamination strip, 0.006-in strip.

**4.2.9.6 Cobalt-iron alloys.** The family of cobalt-iron alloys and the various elements added to this family have been thoroughly investigated for basic magnetic properties.<sup>5,6</sup> Five basic alloys have found commercial application; however, only three are being manufactured in production quantities in various forms. These alloys are used primarily for their high magnetic saturation and relative low coercive force in AC and DC applications. Typical magnetic properties are given in Fig. 4.18.

**4.2.9.7 Commercial irons and commercially pure irons.** Many commercial irons are used for their magnetic properties because of their relative low cost in comparison to other, more expensive nickel-iron, silicon-iron, and cobalt-iron alloys. The magnetic properties obtainable vary considerably, depending on the heat treatment applied to the fabricated parts. Magnetic data on these alloys are very limited, as the properties are not too critical.

Applications requiring a minimal degree of nonmetallics and freedom of internal discontinuities demand a product that is manufactured by other procedures, such as consumable electrode melting and/or vacuum-induction melting. These methods of manufacture also ensure a very low carbon con-

**TABLE 4.6 Core Loss of 49 Ni, Balance Fe “Semioriented” and “Random-Oriented” Strip (60-Hz Core Loss, mW/lb)**

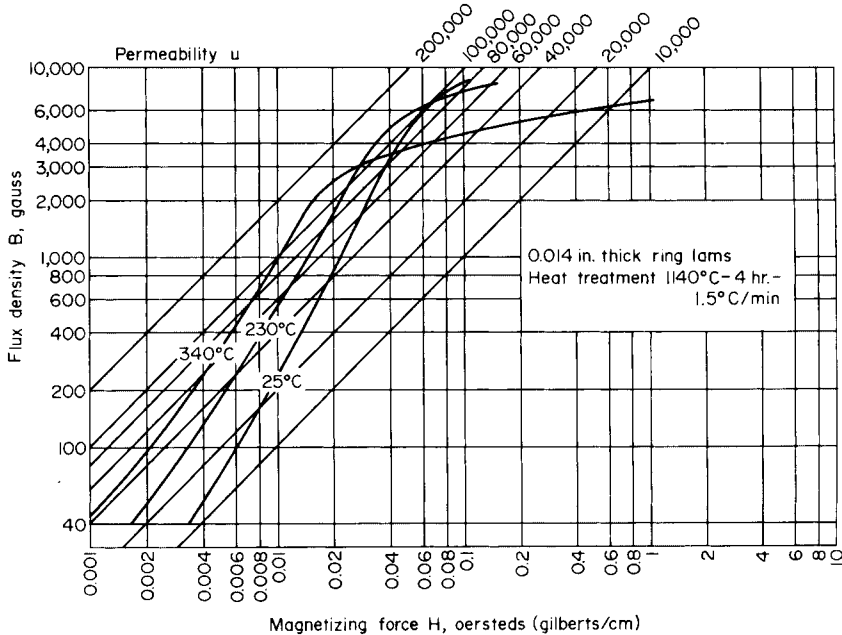
°C for 4 hr	<i>B</i> , gauss					
	1,000	2,000	4,000	6,000	8,000	10,000
0.006-in rings, semioriented grade						
920	9.60	26.3	68.5	120.0	173.0	240.0
982	2.66	8.45	26.6	52.0	85.5	135.0
1038	1.83	6.03	19.7	39.8	66.6	107.0
1093	1.51	5.20	17.8	36.4	60.0	101.0
1180	1.58	5.43	18.2	37.4	66.1	103.0
0.006-in rings, random-oriented grade						
870	6.21	18.5	67.0	85.7	131.3	193.0
920	4.42	13.44	51.5	66.8	104.1	154.5
982	3.26	10.2	41.8	54.8	86.5	131.6
1180	2.07	6.98	31.6	42.7	72.4	112.3
0.014-in rings, semioriented grade						
920	9.95	28.0	74.3	132.0	195.0	275.0
982	3.02	9.85	31.1	62.5	107.0	174.0
1038	2.69	8.91	28.8	58.0	99.9	164.0
1093	2.47	8.50	27.9	57.0	99.0	162.0
1180	2.64	8.90	28.6	57.6	99.5	164.0
0.014-in rings, random-oriented grade						
920	5.34	16.2	62.2	82.1	130.9	199.2
982	4.20	13.2	53.9	72.4	119.2	185.0
1180	3.61	8.97	40.2	55.0	93.3	151.3

tent, lowest gas content, and minimal residual elements. Their characteristics ensure the best performance in vacuum envelopes and minimal contamination over long periods of time.

With regard to mechanical properties and suggested machining information for magnetic alloys, general information has been compiled for some of the alloys reviewed. Thermal expansion properties are given in Table 4.7.

**4.2.9.8 Permanent magnetic alloys.** Permanent magnetic alloys are generally referred to as *hard magnetic materials*. These materials retain magnetic poles (north and south) after being subjected to a strong magnetic field. Magnetic property tests are generally conducted on specific bar shapes that have been heat treated. Most common magnetic parameters employed to compare and rate permanent magnetic materials are the following:

1. *Coercive force, H.* The demagnetizing force that must be applied to a magnet to reduce the magnetic induction to zero.



**Figure 4.17** 60-Hz permeability vs. temperature for 49 Ni, balance Fe random-oriented alloy.

**TABLE 4.7 Thermal Expansion Properties of Some Magnetic Alloys\***

Temp., °C	80 Ni, 4 mo, bal. Fe	77 Ni, 1.5 Cr, 5 Cu, bal. Fe	49 Co, 2 V, bal. Fe	27 Co, bal. Fe	1 Si, bal. Fe	2.5 Si, bal. Fe	4 Si, bal. Fe	Commercial iron
20–100	11.51	12.5	—	—	11.2	11.3	11.8	12.7
200	12.62	14.4	—	10.10	12.0	12.2	12.4	13.8
300	13.20	—	9.5	10.35	12.4	13.2	12.9	14.6
400	13.67	—	—	—	12.8	—	13.5	15.8
500	13.95	—	9.8	10.90	—	—	—	16.7

\*Coefficient of expansion = in/in  $\times 10^{-6}/^{\circ}\text{C}$ .

Note: Information for 36 Ni, bal. Fe and 49 Ni, balance Fe can be found in the text.

2. *Demagnetization curve.* The second-quadrant portion of the hysteresis loop relating induction in a magnet to its magnetizing force.
3. *Energy product,  $BH_{max}$ .* The product of  $B \times H$  in the second quadrant of the hysteresis loop. A figure of merit for a magnet. It is proportional to the amount of external energy available from a magnet of given dimensions.
4. *Residual induction,  $B_r$ .* The magnetic induction that is retained by a magnet after removal of a saturating magnetizing force.

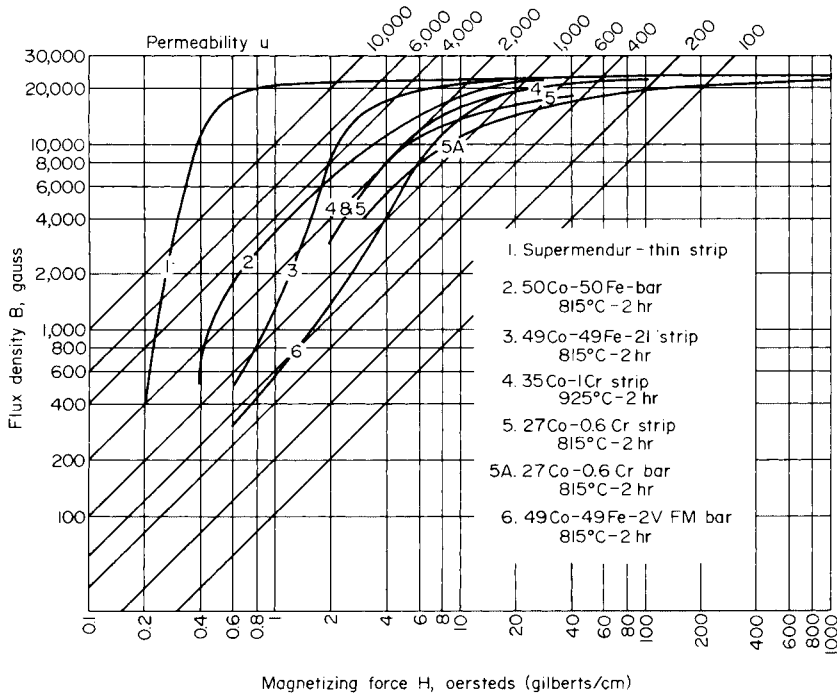


Figure 4.18 DC normal induction curves of Fe-Co alloys.

5. *Intrinsic curve ( $B - H$ )*. A plot of intrinsic induction in the second and third quadrants of the hysteresis loop. Intrinsic induction is not zero at the  $H_c$  point. This means that a field intensity  $H$  that is large enough to hold  $B$  at zero does not completely demagnetize the magnet, because of recoil. Complete demagnetization occurs only when  $B - H = 0$ .

Many alloy compositions have been evaluated for their permanent magnetic characteristics; however, the industry has standardized on certain compositions to meet the general requirements. Cobalt and chromium steels are available in wrought (rolled) and cast shapes. When permanent magnet units are very small (less than several ounces), the sintering manufacturing procedure may be preferred for economic reasons and to obtain higher physical properties. Because permanent-magnet alloys are very hard in the heat-treated condition, the unit cannot be machined or formed. Metal removal can be achieved only by grinding operations, and these must be conducted very carefully so as not to fracture the unit.

Ferrite magnets are also known as *ceramic magnets*. General composition is of a,  $M \cdot 6Fe_2O_3$ , where the  $M$  represents barium, strontium, lead, or combinations thereof. This type of magnet is very hard and brittle, is a good electrical insulator and a poor conductor of heat, and is chemically inert. Careful grinding procedures are recommended for removing material. Considerable development work is in progress on this type of permanent-magnet material, and it

is necessary to maintain constant contact with producers to ascertain new products commercially available.

**4.2.9.9 Stainless steels.** Stainless steels are divided into two groups: ferritic stainless steels (400 series) and austenitic stainless steels (300 series). Ferritic stainless steels are magnetic and can be further subdivided into martensitic (hardenable) and ferritic (nonhardenable) groups. Types 410, 416, 420, and 440 can be hardened by heat treatment and, in this condition, the alloy acts as a weak permanent magnet, as illustrated in Table 4.8 by the  $H_c$  values. In the full-annealed (low-hardness) condition, the magnetic values are considered to be weak, soft magnetic properties. Table 4.9 lists the general magnetic properties and includes the ferritic grades such as Types 430, 430F, and 446.

**TABLE 4.9 Typical DC Soft Magnetic Properties of Type 400 Stainless Steels**

Types	Hardness, Rockwell B	$\mu$ at $B$ gauss				$\mu_{\max}$	$H_c$ , oersteds from $10^3$ gauss
		500	1,000	5,000	10,000		
410 and 416*	80	200	380	900	1,020	1,080	5.0
430 and 430 F	75	400	550	1,600	1,600	1,840	1.7
446†	85	350	500	1,100	700	1,100	4.0

\*Heat treated at 815°C for 2 hr, furnace cooled.

†Heat treated at 900°C for 2 hr, furnace cooled.

Type 400 series stainless steels are employed for their magnetic properties when other soft magnetic alloys lack corrosion resistance to a given media and plated cores cannot be employed. Type 400 series stainless steels provide corrosion resistance to fresh water, mine water, steam, gasoline, crude oil, perspiration, alcohol, ammonia, soap, sugar solutions, and most foods.

Austenitic stainless steels (Type 300 series) are generally considered to be nonmagnetic alloys having good corrosion resistance to ambient conditions. All Type 300 series stainless steels have maximum permeabilities of 1.005 or less in the annealed (lowest hardness) condition. Cold work introduced through processing and fabrication will increase the maximum permeability. The rate of increase depends on the chemical composition and the stability of the austenite.<sup>7</sup>

**4.2.9.10 Temperature-compensator alloys.** As the nickel content in nickel-iron alloys increases above 29 percent, the Curie temperature increases (see Fig. 4.9). Commercial alloys containing 29 to 39 percent nickel are utilized as temperature-compensator alloys, because their magnetic saturation decreases with increasing temperature. This characteristic provides a means of controlling a DC magnetic flux density produced by a permanent-magnet or an electromagnet field which decreases with increasing temperature. To achieve this performance from the temperature-compensator alloy, the magnetic source

must produce a magnetic flux density in the alloy above the knee of the DC (B – H) curve. Most data available for these alloys have been determined at 46 oersteds, which is in the saturation range.

Generally, the magnetic pole strength of a permanent magnet decreases with increasing temperature. To achieve a uniform functional magnetic field, the temperature-compensating alloy is employed to shunt magnetic lines of force from the poles and away from the functional magnetic area. As the temperature decreases and the magnet pole strength increases, the compensating alloy shunts or robs more flux from the functional area. With increasing temperature and decreasing magnet pole strength, the compensating alloy shunts less flux. By proper selection of compensating alloys, thickness of the compensator cross section, and design of the shunt, the functional magnetic field can be controlled.

The temperature-compensating characteristics of these alloys can be varied by the amount of cold-work stresses introduced into the alloy. Cold work decreases the flux-carrying capacity and reduces the change in flux density per degree of temperature from that shown by the alloy in the annealed condition (condition generally supplied by the producer). Thermal treatments up to 480°C for several hours help to make the properties more stable with time and increase the flux-carrying capacity slightly. If the degree of cold work exceeds 10 percent reduction, it is recommended that the part be heat treated as recommended by the producer.

Temperature-compensator alloys are used to compensate permanent magnets in instruments, switches, watt-hour meters, tachometers, speedometers, microwave tubes, and so forth. These alloys can also be used for thermal switches and temperature regulators. Nominal flux density changes with temperature of commercial grades are given in Table 4.10.

**TABLE 4.10 Magnetic Flux Densities vs. Temperature of Temperature-Compensating Alloys at  $H = 46$  Oersteds**

Ni content, % Type *	29.0	29.8	29.8	32.5	36.0	38
	5	4	2	1		
Temperature, °C	Flux density, gauss					
-60	—	—	—	10,450	14,900	—
-40	4,000	5,450	5,650	9,900	14,400	—
-20	2,980	4,620	4,900	9,350	—	—
0	1,350	3,480	3,920	8,700	13,400	14,200
15	370	2,500	3,000	—	—	—
25	148	1,760	2,240	7,800	12,700	13,400
40	40	750	1,120	7,250	—	—
50	—	340	550	—	11,870	13,200
80	—	—	—	5,450	10,700	—
90	—	—	—	4,800	10,500	—
100	—	—	—	—	10,000	12,000
150	—	—	—	—	7,000	9,200
200	—	—	—	—	—	8,800

\*Carpenter Technology Corp. type numbers.

#### 4.2.10 Thermal expansion properties of alloys

Many ferrous alloys are used in various applications for their thermal expansion characteristics. All metals expand when the temperature is increased above 25°C (77°F) and contract when the temperature is decreased. The rate of expansion and contraction depends on chemical composition and physical condition; hence, a wide variety of thermal expansion characteristics are available from ferrous alloys. Typical thermal expansion properties of various alloys employed in the industry for this particular characteristic will be reviewed. Test procedures have been established by ASTM to determine the expansion characteristics of materials. Thermal expansion properties are typically expressed as the change in length per unit length resulting from a change in temperature of the material.

Data presented herein are expressed in the form of mean (average) coefficient of linear expansion in units per degree Fahrenheit. These data can be employed to calculate and plot the linear thermal expansion. From the linear thermal expansion, the instantaneous coefficient of linear thermal expansion can be determined.

**4.2.10.1 Nickel-iron alloys and related alloys.** This family of alloys has been thoroughly investigated for thermal expansion properties. The alloy containing 36 Ni, balance Fe (Invar) exhibits the lowest expansion properties of all metals (see Fig. 4.9); hence, the 36 percent nickel alloy is used predominantly in applications wherein minimum size change is necessary. The dimensional stability with time and thermal heat treatment to achieve same has been thoroughly investigated.<sup>12</sup> Investigations are in progress to reduce the expansion properties further by controlling the residual elements commonly found in commercial alloys. A free-machining grade, having slightly higher expansion characteristics, is available to realize lower machining costs. Invar itself is difficult to machine because of the gumminess of the alloy.

Figure 4.9 illustrates that, as the nickel content decreases below 36 percent and increases above 36 percent, the 25°C (77°F) coefficient of expansion increases; however, with increasing nickel content up to 65 percent, the Curie temperature increases. Below the Curie temperature, the nickel-iron alloys show fairly uniform coefficients of expansion; however, in the Curie range, the expansion properties increase. Above the Curie temperature, the alloys expand at a very rapid rate—similar to a true austenitic alloy having an instantaneous coefficient in the range of 9 to  $10 \times 10^6/^\circ\text{F}$ . To achieve specific expansion properties, other elements can be added, such as chromium. The addition of other elements increases the coefficient of expansion and lowers the Curie temperature. Expansion properties and physical properties of standard commercial grades are given in Table 4.11.

Expansion data, except for 36 Ni, balance Fe, are given for the annealed condition (free of cold-work stresses by heat treating at 1925°F for 2 hr in a nonoxidizing atmosphere). Expansion characteristics in conditions other than annealed are not reproducible, and they change as cold-work stresses are relieved.

TABLE 4.11 Thermal Expansion and Physical Properties of Nickel-Iron Alloys and Related Alloys

Type analysis and properties	36 Ni	36 Ni, FM	39 Ni	42 Ni	42 Ni, 6 Cr
Carbon*	0.03	0.05	0.05	0.03	0.06
Manganese	0.35	0.90	0.40	0.50	0.50
Silicon	0.30	0.35	0.25	0.25	0.25
Nickel	36.0	36.0	39.0	42.0	42.5
Other elements	—	Se 0.20	—	—	Cr 5.75
Iron	bal.	bal.	bal.	bal.	bal.
Physical constants					
Specific gravity	8.05	8.05	8.08	8.12	8.12
Density, lb/in <sup>3</sup>	0.291	0.291	0.292	0.293	0.294
Thermal conductivity, Btu/(hr)(ft <sup>2</sup> )(°F/in)	72.6	72.6	73.5	74.5	87.0
Electrical resistivity, Ω/cir mil-ft	495	495	440	430	570
Curie temperature, °F	536	536	644	716	563
Specific heat, Btu/(lb)(°F)	0.123	0.123	0.121	0.120	0.120
CTE, in/in × 10 <sup>-6</sup> /°F (annealed)					
At 77–212°F					
392	0.655 <sup>†</sup>	0.89 <sup>‡</sup>	1.22	2.57	3.64
572	0.956	1.62	1.48	2.54	3.94
662	2.73	3.33	1.88	2.71	4.59
752	3.67	4.20	2.60	2.78	5.02
842	4.34	4.93	3.34	3.14	5.56
932	4.90	5.45	4.01	3.83	5.89
1112	5.40	5.92	4.54	4.32	6.39
1292	6.31	6.67	5.33	5.50	6.99
1472	70.6	7.17	6.11	6.12	7.45
1652	7.48	7.56	6.64	6.66	7.87
1832	7.70	8.12	7.10	7.10	8.17
	—	—	7.45	—	—
Mechanical properties (as mill annealed)					
Tensile strength, ksi	65	65	75	82	80
Yield strength, ksi	40	40	42	40	40
Elongation in 2 inches, %	35	35	30	30	30
Hardness, Rockwell B	70	70	76	76	80
Elastic modulus, ksi × 10 <sup>3</sup>	20.5	20.5	21.0	21.0	23

\*Also available at carbon 0.01% (max).

<sup>†</sup>Unannealed.<sup>‡</sup>Fully aged.

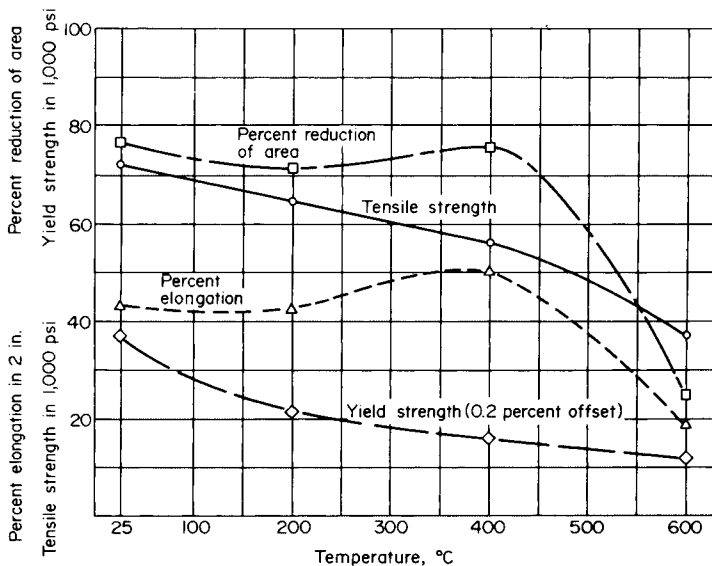


Thermal expansion properties below 77°F of several alloys are given in Table 4.12. For the effect of elevated temperature on the physical properties of a nickel-iron alloy, Fig. 4.19 provides nominal data observed on 42 Ni, balance Fe.

**TABLE 4.12 Coefficients of Thermal Expansion of Nickel-Iron Alloys Annealed at or below Room Temperature**

Temperature, °F	In/in $\times 10^{-6}/^{\circ}\text{F}$		
	36 Ni, bal. Fe	42 Ni, bal. Fe	49 Ni, bal. Fe
0–77	0.8	3.1	5.1
– 100 –	0.9	3.4	5.2
– 200 –	0.9	3.5	5.1
– 300 –	1.0	3.5	4.8

**4.2.10.2 Stainless steels (ferritic and austenitic).** Thermal expansion properties of ferritic stainless steels are presented in Table 4.13, and these properties are greater than those of the nickel-iron family, having 49 percent nickel and less. Lower cost and other specific properties favor these alloys in some applications. Exposure to high elevated temperatures can alter the expansion properties through metallurgical phase changes. The expansion properties are altered when austenite is formed in the alloy and the deletion of the austenitic phase is sluggish on cooling after being formed. As the chromium content increases, the ferrite is more stable with increasing temperature; titanium increases the ferrite stability.



**Figure 4.19** Physical properties of 42 Ni, bal. Fe (annealed).

TABLE 4.13 Thermal Expansion and Physical Properties of Ferritic Stainless Steels, Type 400 Series

Property	Type 410, Type 416*	Type 430, Type 430 F*	Type 430 Ti	Type 446	29% Cr alloy
Chromium content, %	13.0	17.5	18.2	24.0	28.0
Specific gravity	7.7	7.7	7.7	7.7	7.60
Density, lb/in <sup>3</sup>	0.28	0.28	0.28	0.28	0.27
Thermal conductivity at 32–212°F, Btu/(hr)(ft <sup>2</sup> )(°F/ft)	14.4	15.1	15.1	12.1	13.2
Electrical resistivity, Ω/cir mil-ft	343	361	361	385	385
Specific heat, Btu/(lb)(°F)	0.11	0.11	0.11	0.12	0.14
Structure	martensitic	ferritic	ferritic	ferritic	ferritic
CTE, in/(in)(°F), annealed					
At 77–212°F					
392	5.5	5.6	5.10	5.2	5.20
572	6.1	5.8	5.50	5.6	5.60
752	6.3	6.1	5.80	6.0	5.86
932	6.5	6.3	6.05	6.0	5.98
1112	6.7	6.5	6.30	6.2	6.19
1292	6.8	6.6	6.50	6.3	6.25
1472	7.0	6.8	—	6.4	6.46
1652	—	7.0	—	6.5	6.48
	—	7.1	—	7.0	7.09
Mechanical properties (as annealed)					
Tensile strength, ksi	70	75	75	85	85
Yield strength, ksi	45	45	45	55	55
Elongation in 2 inches, %	25	30	30	25	25
Hardness, Rockwell B	80	75	75	80	85
Elastic modulus, ksi × 10 <sup>3</sup>	29	29	29	30	30

\*S = 0.30 for better machinability.

Properties of several austenitic stainless steels are given in Table 4.14. Alloys in this series have very high coefficients of expansions; the values are slightly lower than the 22 Ni, 3 Cr, balance Fe alloy given in Table 4.11.

**4.2.10.3 Glass-to-metal sealing alloys.** A glass-to-metal seal is a vacuum-tight bond between a glass and a metal. The seal, depending on the design, is used to conduct a form of electricity into a chamber or to provide a structural advantage such as a transparent window or a support. To achieve a vacuum-tight and strong glass-to-metal seal, the glass and metal must have practically identically thermal expansion characteristics below the setting point of the glass so as to have minimum stress at the glass-to-metal interface and within

TABLE 4.14 Thermal Expansion and Physical Properties of Austenitic Stainless Steels, Type 300 Series

Property	Type 301	Types 303, 302, 304	Type 316	Type 347	Type 310	Type 330
Typical chromium content, %	17.0	18.0	17.0	18.0	25.0	18.0
Typical nickel content, %	7.0	10.0	12.0	11.0	21.0	35.0
Specific gravity	8.0	8.0	8.0	8.0	8.0	8.0
Density, lb/in <sup>3</sup>	0.29	0.29	0.29	0.29	0.29	0.29
Thermal conductivity at 32–212°F, Btu/(hr)(ft <sup>2</sup> )(°F/ft)	9.4	9.4	9.4	9.3	8.0	10.8
Electrical resistivity, Ω/cir mil-ft	435	433	445	438	469	600
Specific heat, Btu/(lb)(°F)	0.12	0.12	0.12	0.12	0.12	0.11
CTE, in/in × 10 <sup>-6</sup> /°F, annealed						
At -300 to +70°F						
-200	7.6	7.4	7.1	7.5	7.0	5.8
-100	7.8	7.7	7.4	8.1	7.5	6.5
-100	8.2	8.2	7.8	8.5	7.8	7.2
0	8.7	8.7	8.2	8.7	8.0	7.6
+70 to +200	9.2	8.8	8.9	9.0	8.4	8.1
300	9.4	9.0	9.2	9.2	8.6	8.3
400	9.5	9.2	9.3	9.4	8.8	8.5
500	9.6	9.4	9.4	9.5	8.9	8.7
600	9.7	9.5	9.6	9.7	9.0	8.9
700	9.8	9.7	9.7	9.8	9.2	9.0
800	9.9	9.8	9.8	9.9	9.3	9.1
900	10.0	9.9	9.9	10.0	9.4	9.3
1000	10.1	10.0	10.0	10.1	9.5	9.4
Mechanical properties (as annealed)						
Tensile strength, ksi	110	85	84	95	95	70
Yield strength, ksi	40	42	42	40	4	35
Elongation in 2 inches, %	60	55	50	45	45	30
Hardness, Rockwell B	85	80	80	85	85	85
Elastic modulus, ksi × 10 <sup>3</sup>	28	28	29	28	29	

the glass.<sup>13–15</sup> Metal parts, fabricated to the final shape employed in making the glass-to-metal seal, must have a thoroughly clean surface. The strongest seals are achieved when a tight metal oxide film is produced on the surface of the metal before the glass comes in contact with the sealing surface. This oxide can be generated by a prior thermal treatment or by heating the metal for sealing. The oxide roughens the surface of the metal and is soluble in the molten glass, thus increasing the area of contact. Small bubbles within the glass-to-metal interface are undesirable and are an indication of a weak bond. The bubbles can be eliminated by a prior treatment of the metal in a wet hydrogen

atmosphere to clean and/or decarburize the metal surface. After the sealing operation, an annealing treatment should be employed so that the nonequilibrium stresses within the glass are removed.

**Chromium-iron alloys.** Chromium-irons such as Type 430; Type 430Ti; Type 446; and 28 Cr, balance Fe are employed. Selection depends on the sealing temperature employed. Type 430 is not recommended for temperatures above 1700°F so as to avoid the formation of austenite in the alloy. The presence of austenite increases the degree of contraction on cooling and can result in cracked or overstressed seals. Type 446 will withstand higher sealing temperatures up to 2000°F, depending on chromium content and other elements in the analysis.<sup>16</sup> Type 430 Ti and 28 Cr, balance Fe have the most stable ferrite of the commercial grades. To obtain the strongest glass-to-metal seal, the parts should be heated in a wet hydrogen atmosphere to produce a greenish black oxide that is very tightly adherent to the base metal. Heating in air or a gas-firing flame for sealing to produce a sealing oxide is being used successfully.

**Nickel-iron alloys.**<sup>17</sup> Most common grades contain the nominal nickel contents of 42, 46, 48, and 50.5 percent. Most grades must be degassed in wet hydrogen before sealing. A typical treatment is to heat to 1750°F in wet hydrogen for 30 min. Preoxidizing treatments or flame oxidizing can be used. The 42 percent nickel alloy is generally used for ring (housekeeper type) seals with hard glasses whereby a feathered edge is inserted in the glass. This thin wall absorbs the expansion difference between the metal and the glass. The other alloys can be used for various internal, external, butt, and other types of seals, depending on the match with the various types of soft glasses—having a coefficient greater than  $2.8 \times 10^{-6}$  in/(in)(°F).

Gas-free types are available in several of these grades, and these have low carbon contents or other additives.

**42 Ni, 6 Cr, balance Fe.**<sup>18</sup> Because of the chromium content in this alloy, a very tight greenish black oxide can be formed on the alloy in a wet hydrogen atmosphere. Treatments to form the oxide range from 1950 to 2350°F, with varying time until the thin tight oxide is formed. This varies from facility to facility, each of which must be evaluated. To remove the oxide after cleaning, refer to the discussion of chromium-iron alloys.

**28 Ni, 17 Co, balance Fe.**<sup>19</sup> This alloy is most commonly used to make glass-to-metal seals with the hard glasses of the Pyrex<sup>®</sup> type; hard glasses are defined as having a coefficient of expansion less than  $2.8 \times 10^{-6}$  in/(in) (°F) up to 572°F. Because of the high sealing temperature, these alloys should be degassed as prescribed previously to produce good glass-to-metal seals. Preoxidizing or flame oxidizing can be employed before making the seal. If glass-to-metal seals are to be exposed to temperatures below -100°F, the alloy should be checked for phase transformation, which alters the expansion properties and could result in cracked or overstressed seals.

**Mild or low-carbon steel.** AISI 1010 can be used to make certain types of internal and external glass-to-metal seals. The expansion coefficient of expansion over the range of 77 to 572°F is  $6.95 \times 10^{-6}$  in/(in)(°F). This alloy is sometimes plated

before being subjected to a degassification treatment. Preoxidizing or flame oxidizing can be employed.

#### 4.2.11 General comments on metal fabrication

**4.2.11.1 Deep drawing.** The best ductility is exhibited by the nickel-iron alloys: 42 Ni, 6 Cr, balance Fe and the 28 Ni, 17 Co, balance Fe alloy. First draws of as much as 50 percent are achievable, with second redraws up to 25 percent. Less ductility is exhibited by the 28 Cr, balance Fe alloy, with which first draws should not exceed 20 percent.

**4.2.11.2 Welding.** With the exception of the chromium-irons, all grades can be welded by all techniques with precautions. Chromium-iron alloys can be spot-welded with precautions.

**4.2.11.3 Photochemical machining.** All grades can be photochemically machined with precautions. The vendor should be advised if this processing will be employed so as to achieve best performance.

**4.2.11.4 Ceramic-to-metal sealing alloys.** To obtain the best ceramic-to-metal seal, both ceramic and metal must have matching expansion characteristics. Generally, the bond is made with a brazing alloy. Precautions must be exercised during this treatment, because overheating may tend to cause excessive penetration of the brazing alloy into the metal. Intergranular penetration of the brazing alloy can be retarded by copper, silver, or nickel plating the metal in the area to be sealed.

**4.2.11.5 Constant modulus of elasticity alloys.** The iron-nickel-chromium-titanium alloy is age hardenable and exhibits a constant modulus in the temperature range of  $-50$  to  $+150^{\circ}\text{F}$ . The alloy is available in the forms of wire, rod, strip, round tube, and forgings. To achieve the lowest thermoelastic coefficient in the range of  $-10$  to  $+10 \times 10^6/^{\circ}\text{F}$ , the parts must be thermally aged as a final heat treatment. Through utilization of an annealing solution treatment of approximately  $1850^{\circ}\text{F}$  and rapid quench and/or percentages of cold reduction (if possible on the cross section), variations in high tensile strength, hardness, and near-zero thermoelastic coefficients are obtainable. Slight differences in chemical analysis between melts result in minor variations; hence, for very precise applications, adjustments in heat treatments are predictable through information available from the producer.

#### 4.2.12 Electrical-resistance alloys and electrical resistivity properties of some ferrous alloys

Electrical-resistance alloys are generally used to produce heat or to control electric current. In some cases, the electrical resistance or resistivity is a mi-

nor property for the selection of a given alloy. Standard procedures have been established to determine these electrical characteristics. Table 4.15 provides the electrical resistivity of some alloys and the effect of temperature on this property. The electrical resistivity of most alloys increases with increasing temperature.

Ferrous alloys and pure metals are not recommended for precision resistors because of their high-temperature coefficients. Several nonferrous alloy series are available for manufacturing wire-wound resistors to meet a variety of requirements.<sup>9</sup>

### 4.2.13 Aluminum and aluminum alloys

**4.2.13.1 General properties.** Aluminum and its alloys possess properties that find wide use in the electronics industry. Favorable physical properties, good strength-to-weight properties, good corrosion resistance, and low density, combined with economy in material cost and fabrication cost, make this alloy family a basic construction material for electronic assemblies.

**Electrical properties of aluminum.** Electrical conductivity of the higher-purity grades is 62 percent of that of pure copper on a volume basis and exceeds copper by approximately twice on a per-pound basis. Alloying to increase strength results in lower conductivity, but fairly strong alloys are available that still exceed the conductivity of copper on a weight basis.

**Thermal conductivity of aluminum.** The high thermal conductivity of aluminum is an advantage in dissipating heat, which is often a requirement in electrical apparatus.

**Density of aluminum.** The light weight of aluminum can often result in a reduction in weight as compared to materials that are stronger than aluminum on a volume basis. The fact that aluminum covers more area per pound when substituted gage for gage for copper alloys, nickel alloys, or steel, results in more favorable material costs, because the same weight of aluminum will cover a larger area than will the heavier alloys.

**Strength-weight of aluminum.** Although aluminum alloys cannot match high-strength steels, beryllium-copper, high-strength titanium alloys, or some nickel alloys in strength per unit area, its low density makes it competitive on a strength-weight basis at room temperature and at slightly elevated temperatures. At low temperatures, even in the cryogenic range, aluminum alloys retain good ductility and thus have found use in low-temperature pressure vessels.

**Corrosion of aluminum.** Corrosion resistance in aluminum is good to the extent that many applications require no protection. Corrosion resistance varies according to the alloying elements used, with the higher-purity alloys generally having best corrosion resistance. In severe environments, protection is needed, especially for the higher-strength alloys. This protection can be provided by anodizing or by conversion coating, either alone or in combination

**TABLE 4.15 Electrical Resistivities of Some Alloys and Factors for Calculating Values at Elevated Temperatures**

Composition	Resistivity at 68°F, Ω/cir mil-ft	Calculation factors at:											
		200°F	400°F	600°F	800°F	1000°F	1200°F	1400°F	1600°F	1800°F	2000°F	2100°F	
36 Ni, bal. Fe	484	1.09	1.185	1.25	1.3	1.35	1.386	1.42	1.45	1.48			
NiSpan C	625	1.03	1.06	1.11	1.16	1.23							
80 Ni, 20 Cr, 1.5 Si	650	1.016	1.037	1.054	1.066	1.070	1.064	1.064	1.066	1.072	1.078	1.084	
60 Ni, 15 Cr, bal. Fe	675	1.019	1.044	1.070	1.092	1.108	1.112	1.118	1.130	1.145			
35 Ni, 15 Cr, bal. Fe	600	1.029	1.067	1.105	1.137	1.167	1.187	1.206	1.223				
23 Cr, 6.2 Al, 1.9 Co, bal. Fe	836	1.002	1.005	1.009	1.014	1.020	1.024	1.028	1.037	1.045			
22.6 Cr, 4.5 Al, 2 Co, bal. Fe	812	1.002	1.005	1.009	1.014	1.020	1.024	1.028	1.037	1.045	1.050	1.055	
16 Cr, 5 Al, bal. Fe	800	1.007	1.018	1.032	1.053	1.084	1.116	1.137			1.055	1.053	
Types 302 and 304	435	1.08	1.18	1.28	1.37	1.44	1.50	1.65	1.75	1.82			
Type 316	445	1.07	1.17	1.26	1.34	1.41	1.59						
Type 321	435	1.10	1.25	1.36	1.45	1.55	1.62	1.68					
Type 347	440	1.09	1.20	1.25	1.35	1.46	1.52	1.58	1.64				
Type 309	470	1.07	1.17	1.26	1.35	1.42	1.48	1.53	1.58	1.62			
13 Cr, 4 Al	672	1.005	1.02	1.04	1.06	1.09	1.14	1.18					
Type 410	345	1.11	1.26	1.43	1.58	1.73	1.90	2.02					
Type 430	360	1.11	1.27	1.42	1.58	1.72	1.86	1.96					
Type 446	405	1.1	1.24	1.37	1.50	1.60	1.70	1.76					

Metals

with painting. Because aluminum is galvanically dissimilar to most common structural metals, it is necessary to pay special attention to applications in which it comes into contact with other metals.

**Availability.** Aluminum alloys are available in about every form, including sheet, plate, foil, pipe, tubing, forgings, and castings, as well as all types of extrusions and rolled shapes. Not all alloys are available in all shapes. This is especially true of castings, which are furnished in an entirely different group of compositions than are wrought alloys.

**Fabrication of aluminum.** The fabrication of aluminum can be carried out by all common means. Machining is very good, but the softer alloys and tempers tend to be gummy. Formability is excellent at room temperature.

**Joining of aluminum.** Joining can be accomplished by mechanical means such as bolts, screws, and rivets as well as by the metallurgical processes of welding, brazing, and soldering. However, precautions must be taken in selecting alloys for the metallurgical processes. Certain alloys are difficult to weld. The brazing alloys melt at a temperature that exceeds the melting point of certain of the commonly used alloys, thus making selection of materials to be brazed subject to careful consideration. Solders are available for aluminum, but corrosion by galvanic action between the aluminum and solder alloys may be a problem where moisture is present. Fluxes for brazing and soldering are highly active and will cause corrosion if left on the parts, thus making post-joining cleaning of paramount importance. Fluxless brazing has been done in vacuum furnaces and is currently under development. Successful fluxless soldering has been accomplished with ultrasonic devices. These processes eliminate the flux corrosion hazard.

**4.2.13.2 Aluminum alloy groups.** Table 4.16 shows the four-digit system for designating alloy groups on the basis of composition as devised by the Aluminum Association.

**TABLE 4.16 Wrought Designation System for Aluminum Alloys**

Series number	Primary alloying element	Relative corrosion resistance	Relative strength	Heat treatment
1xxx	none	excellent	fair	not heat treatable
2xxx	copper	fair	excellent	heat treatable
3xxx	manganese	good	fair	not heat treatable
4xxx	silicon	—	—	not heat treatable
5xxx	magnesium	good	good	not heat treatable
6xxx	magnesium and silicon	good	good	heat treatable
7xxx	zinc	fair	excellent	heat treatable



**4.2.13.3 Aluminum alloy temper designations.** For aluminum, there are two types of designations. The -H designations represent cold-worked conditions and are used for non-heat-treatable alloys. The -T designations are used for heat-treatable alloys that are primarily strengthened by heat treatment. It will be noted that the -T designations also include conditions that result from cold-working combined with heat treatment.

**4.2.13.4 Mechanical properties—wrought aluminum alloys.** In general, tensile values are above the specified minimum except for the annealed (-O Temper) values, which are below a specified maximum. These values are the most probable figures to be found when testing a large number of specimens.

The properties will also depend to a significant extent on the form in which the alloy is used. Thin sheet will generally have higher strength than thick plate of the same composition and heat treatment. Direction of loading will also influence the properties. In critical applications where safety margins are low, consultation with the producer for guaranteed properties is desirable. Standard specifications are available for most aluminum alloys in most forms. These specifications have minimum and/or maximum property limits that take into account section size, method of manufacture, and other process variables. Producers are able to guarantee compliance with these specifications.

**4.2.13.5 Effect of temperature on mechanical properties of aluminum alloys.** Elevated temperatures have an adverse effect on the mechanical properties of aluminum alloys. Other properties, such as fatigue strength and shear strength, will also show similar changes. It is obvious that moderately elevated temperatures over time can have appreciable effects on the mechanical properties of aluminum alloys. Note that alloys that are strongest at room temperature are not necessarily the strongest at elevated temperatures. Additional data is available through the Aluminum Association, Washington, DC.

**4.2.13.6 Physical properties of aluminum.** Table 4.17 shows a compilation of electrical properties at room temperature. These values will also change with change in temperature.

**4.2.13.7 Cast aluminum alloys.** Aluminum alloys can be cast by all available casting methods, including sand, die, investment, permanent mold, and plaster mold. Casting compositions are specifically designed for cast forms and differ significantly from those of the alloys used for wrought forms such as sheet, box, extrusions, and forgings. As a result, some of the highest electric and thermal conductivity values found in wrought alloys cannot be found in casting alloys. However, aluminum castings exhibit the favorable corrosion resistance and strength-to-weight ratio found in wrought alloys.

TABLE 4.17 Typical Thermal and Electrical Properties of Aluminum Alloys<sup>1</sup>

Alloy	Temper	Thermal conductivity @ 25°C (77°F)		Electrical conductivity @ 20°C (68°F), % of Intl. Annealed Copper Standard		Electrical resistivity @ 20°C (68°F)	
		Cgs units*	English units†	Equal volume	Equal weight	μΩ/cm	Ω/cir mil-ft
EC‡	All	0.56	1625	62	204	2.8	17
1060	0	0.56	1625	62	204	2.8	17
	H18	0.53	1540	61	201	2.8	17
1100	0	0.53	1540	59	194	2.9	17
	H18	0.52	1510	57	187	3.0	18
2011	T3	0.36	1040	39	123	4.4	27
	T8	0.41	1190	45	142	3.8	23
2014	0	0.46	1340	50	159	3.4	21
	T4	0.32	930	34	108	5.1	31
	T6	0.37	1070	40	127	4.3	26
2017	0	0.46	1340	50	159	3.4	21
	T4	0.32	930	34	108	5.1	31
2018	T61	0.37	1070	40	127	4.3	26
2024	0	0.46	1340	50	160	3.4	21
	T3, T4, T36	0.29	840	30	96	5.7	35
	T6, T81, T86	0.36	1040	38	122	4.5	27
2025	T6	0.37	1070	40	130	4.3	26
2117	T4	0.37	1070	40	130	4.3	26
2218	T72	0.37	1070	40	126	4.3	26
2219	0	0.41	1190	44	138	3.9	24
	T31, T37	0.27	780	28	88	6.2	37
	T62, T81, T87	0.30	870	30	94	5.7	35
3003	0	0.46	1340	50	163	3.4	21
	H12	0.39	1130	42	137	4.1	25
	H14	0.38	1100	41	134	4.2	25
	H18	0.37	1070	40	130	4.3	26
3004	All	0.39	1130	42	137	4.1	25
4032	0	0.37	1070	40	132	4.3	26
	T6	0.33	960	35	116	4.9	30
4043	0	0.39	1130	42	137	4.1	25
5005	All	0.48	1390	52	172	3.3	20
5050	All	0.46	1340	50	165	3.4	21
5052	All	0.33	960	35	116	4.9	30
5056	0	0.28	810	29	98	5.9	36
	H38	0.26	750	27	91	6.4	38
5083	All	0.28	810	29	98	5.9	36
5086	All	0.30	870	31	104	5.5	34
5154	All	0.30	870	32	107	5.3	32
5252	All	0.33	960	35	116	4.9	30

TABLE 4.17 Typical Thermal and Electrical Properties of Aluminum Alloys<sup>1</sup> (Continued)

Alloy	Temper	Thermal conductivity @ 25°C (77°F)		Electrical conductivity @ 20°C (68°F), % of Intl. Annealed Copper Standard		Electrical resistivity @ 20°C (68°F)	
		Cgs units*	English units†	Equal volume	Equal weight	μΩ/cm	Ω/cir mil-ft
5454	0	0.32	930	34	113	5.1	31
	H38	0.32	930	34	113	5.1	31
5456	0	0.28	810	29	98	5.9	36
5557	All	0.45	1310	49	159	3.5	21
6053	0	0.41	1190	45	148	3.8	23
	T4	0.37	1070	40	132	4.3	26
	T6	0.39	1130	42	139	4.1	25
6061	0	0.43	1250	47	155	3.7	22
	T4	0.37	1070	40	132	4.3	26
	T6	0.40	1160	43	142	4.0	24
6063	0	0.52	1510	58	191	3.0	18
	T1‡	0.46	1340	50	165	3.4	21
	T5	0.50	1450	55	181	3.1	19
	T6, T83	0.48	1390	53	175	3.3	20
6066	0	0.37	1070	40	132	4.3	26
	T6	0.35	1010	37	122	4.7	28
6070	T6	0.41	1190	44	145	3.9	24
6101	T6	0.52	1510	57	188	3.0	18
	T61	0.53	1540	59	194	2.9	18
	T63¶	0.52	1510	58	191	3.0	18
	T64	0.54	1570	60	198	2.9	17
	T65	0.52	1510	58	191	3.0	18
6151	0	0.49	1420	54	178	3.2	19
	T4	0.39	1130	42	138	4.1	25
	T6	0.41	1190	45	148	3.8	23
6262	T9	0.41	1190	44	145	3.9	24
6463	T1‡	0.46	1340	50	165	3.4	21
	T5	0.50	1450	55	181	3.1	19
	T6	0.48	1390	53	175	3.3	20
7001	T6	0.29	840	31	104	5.5	34
7039	T61	—	—	35	116	4.9	30
7072	0	0.53	1540	59	193	2.9	18
7075	T6	0.31	900	33	105	5.2	31
7079	T6	0.30	870	32	104	5.4	32
7178	T6	0.30	870	31	98	5.6	33

\* Cgs units = cal/(sec)(cm<sup>2</sup>)(°C/cm).† English units = Btu/(hr)(ft<sup>2</sup>)(°F/in).

‡ Electrical conductor grade, 99.45% minimum aluminum.

§ Formerly designated T42.

¶ Formerly T62.

In the design of castings, it is important to work with the foundry as early in the process as possible, because there is room for wide variation in the strength and quality of castings, depending on the factors mentioned above. The following major questions should be jointly answered by the purchaser and vendor:

1. How are mechanical properties to be determined? Are they to be determined on separately cast test bars or on test bars from the casting itself? Many specification properties are based on separately cast test bars, and the properties of the casting can be considerably lower than those specified. On the other hand, foundries will agree to guaranteeing properties of the actual casting in some instances.
2. What level of defects is to be allowed, and what means of inspection is to be used?

A procedure covering means of specifying and controlling these factors is outlined in AMS-STD-2175.

**Selection of alloy.** Casting alloy selection is not so straightforward as wrought alloy selection. The casting selection is complicated by the foundry characteristics of the alloy and by the foundry practice used in production. It may often be the case that a sound, inherently low-strength material will exceed the strength of a high-strength material of poor quality.

**4.2.13.8 Recommended aluminum casting alloys.** In electronics packaging, certain grades of castings may be recommended for specific purposes.

**General-purpose aluminum alloy.** Alloys 356 and A356 are the most widely used alloys in production. They have good foundry characteristics and very good mechanical properties. They are available in sand, permanent-mold, investment, and plaster-mold castings.

**Brazable compositions.** Alloys A612 and C612 are most commonly used for parts that must be brazed, because their melting points are high enough to withstand brazing temperatures.

**Low thermal expansion.** The high-silicon-content (18 to 20 percent silicon) alloys have thermal expansion rates close to that of alloy steel. These alloys are difficult to cast and must be carefully poured with special procedures.

**High-strength.** Some aluminum alloys have approached the strength of the higher-strength wrought aluminum alloys. Alloy 220 gives a tensile strength above 40,000 psi with good ductility, but it is difficult to cast.

The importance of close cooperation with foundries in early stages of casting design cannot be emphasized too strongly. Agreement should be reached on tolerance, quality standards, and strengths.

#### 4.2.14 Beryllium and beryllium alloys

Beryllium has a combination of physical and mechanical properties that make it a natural material for use in electronic packaging as a structural material

and as a material for thermal and electrical functions. The high cost of beryllium metal, combined with difficulties in joining and forming it, have made beryllium structures very expensive. In addition, the lack of ductility of the metal has precluded its use in many structural applications. A combination of beryllium and aluminum called AlBeMet\* can overcome, to some extent, the forming, joining, and ductility problems while retaining many of the desirable beryllium characteristics. Even with the addition of aluminum, material costs remain high. Despite its drawbacks, there are applications for which the high stiffness-to-weight and strength-to-weight ratios of beryllium and AlBeMet make their use cost effective in terms of weight reduction. Mirror blanks, gyro parts, airframe and missile body stiffeners, and control surfaces on airplane are examples of structural uses of these materials. The high thermal conductivity of pure beryllium, along with its high heat capacity, makes it a natural lightweight heat sink.

**4.2.14.1 Availability.** As mentioned above, beryllium is available in two basic compositions, these being essentially pure beryllium with various beryllium oxide contents and the material AlBeMet, which is a combination of beryllium and aluminum. The production methods for both of these alloys are advancing, with the result that products with improved properties are being developed, as well as capability for producing the materials in new forms. Aluminum-beryllium alloys are available in cast form. Close liaison with suppliers during the early stages of planning is recommended so that the most suitable product available is used. Aluminum-beryllium alloys are covered by three commercial specifications: AMS 7911, Aluminum-Beryllium Alloy, Hot-isostatic Pressed (HIP); ASE-AMS, 7912, Aluminum-Beryllium Alloy, Extrusions; and SAE-AMS 7913-97, Aluminum-Beryllium Alloy, Sheet and Plate 38AL-62BE.

A large amount of beryllium metal is produced in the form of hot-pressed block. This product is produced by first casting the metal into an ingot, which is then reduced to a powder stage by mechanical means. The powder is then compacted into a block by heat and pressure. Many beryllium parts are produced by machining from the hot-pressed block.

Extruded rod, tube, and bar produced by extruding hot-press block or billets are also available. Sheet that has been rolled from hot-pressed block is also procurable. In addition, sheet is being rolled directly from the cast ingot in some cases, and forged blocks are available.

The working done by extrusion and rolling results in material of improved properties (both strength and ductility) over the hot-pressed block. Beryllium is susceptible to developing directionality in properties because of working. Often, good ductility is present in one direction while being very poor in other directions. One method used in sheet production is to cross-roll. A designer should be aware of these directional properties and discuss specific requirements with the supplier.

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\* Registered trademark of Brush Wellman.

Aluminum-beryllium alloys are typically produced by extrusion in the form of bar and shapes. Dies for some simple structural shapes are easily fabricated. Consultation with the supplier on shape and size availability is recommended. Sheet and plate are produced by cross-rolling extruded rectangular bars.

**4.2.14.2 Chemical composition.** Beryllium is produced with controlled beryllium oxide content. It is typically supplied either as a commercially pure product or alloyed with aluminum. The major aluminum-beryllium alloy composition is the 62 percent beryllium, 38 percent aluminum composition.

**4.2.14.3 Physical properties.** Table 4.18 covers some physical properties of beryllium. Poisson's ratio is extremely low as compared to that of other structural metals. This value should be considered as provisional, and the supplier should be consulted as to actual values for available material, because there seems to be some conflict in data.

**TABLE 4.18 Some Physical Properties of Beryllium\***

Atomic diameter, A°	2.221	Latent heat of fusion, cal/g	250–275
Atomic number	4	Latent heat of vaporization	5390
Atomic weight	9.02	Magnetic susceptibility, gauss/oersted	
Density, g/cc	1.85	cgs	0.79
Density, psi	0.055	Thermal neutron absorption cross section, barn/atom	0.0090 ± 0.0005
Electrical conductivity, % IACS	38–40	Beryllium atoms per cm <sup>3</sup>	1.24 × 10 <sup>23</sup>
Electrode potential, V	–1.69	Thermal-neutron scattering cross section, barn/atom	7.0
Electrochemical equivalent, mg/coul.	0.04674	Slowing-down length, cm (fission energy to thermal energy)	9.9
Photoelectric work function, eV	3.92	Velocity of sound:	
Hall coefficient, cgs electromagnetic units	0.0024 ± 0.001	ft/sec	41,300
Mass susceptibility:		m/sec	12,600
–180°C	–0.72 cgs units	Entropy, S <sub>298.1</sub> , cal/(mole)(kelvins):	
+20°C	–1.00 cgs units	Solid	2.28 ± 0.02
+300°C	–1.20 cgs units	Liquid	32.56 ± 0.01
Melting point, °C	1285	Reflectivity (white light)	50/55
Melting point, °F	2345	Photoelectric work function, eV	3.92(9)
Boiling point, °C	2970	Poisson's ratio	0.25 ± 0.005
Boiling point, °F	5378		

\*SOURCE: Kawecki Berylco Industries, Technical Bulletin 304 03 PDI.

**4.2.14.4 Corrosion resistance and finishing.** Beryllium is susceptible to corrosion by chlorides. This factor alone makes it necessary to protect the metal from corrosion, because most equipment will be subjected to some chloride environment during service. Because field-performance data are practically nonexistent, it is recommended that testing be carried out under simulated service conditions.

Aluminum-beryllium alloys possess some of the favorable corrosion resistance of aluminum. Because the material is essentially a mixture of beryllium and aluminum, there exists a possibility of some galvanic corrosion effects. Service data on corrosion are not readily available, given that aluminum-beryllium alloys are typically coated to prevent corrosion or are used in space applications. As with beryllium, corrosion testing under simulated service testing is recommended, with due caution to safety with regard to the potential hazards of corrosion products.

**4.2.14.5 Protective coatings for beryllium and aluminum-beryllium alloys.** Both conversion coatings and anodic coatings are available for AlBeMet and beryllium. These coatings offer added corrosion resistance over that of the bare metals. Proprietary treatments are available from the metal producers.

Electroplating of beryllium is a production procedure. The common electroplated coatings may be applied. Typically, aluminum-beryllium alloys accept platings by standard techniques used for aluminum.

In general, it appears that both beryllium and aluminum-beryllium alloys—with suitable finish selected from conversion coatings, anodizing, or electroplating—can meet the corrosion-resistance requirements for most electronic applications.

## 4.2.15 Fabrication of beryllium alloys

**4.2.15.1 Toxicity.** Breathing of beryllium oxide dust particles generated from machining beryllium is a health hazard, so any operation that could create fine particles must be done under conditions that prevent any possible inhalation of these particles. The same precautions as taken with beryllium must be taken with aluminum-beryllium alloys. All machining operations must be done under conditions in which the particles created are collected at the tool and isolated in a container to preclude their discharge into the atmosphere. Heating operations such as welding and brazing must be similarly controlled. Before processing beryllium or aluminum-beryllium alloys, consultation with plant safety engineer, local government medical authorities, vendor safety department, and other cognizant safety or health officials is mandatory.

**4.2.15.2 Machining.** Beryllium can be machined by conventional machining methods. Tool wear will be high because of the abrasive nature of the material.

Most cutting-type operations leave a surface damage in the form of microcracks. These small cracks will act as failure initiation points. Removal of the surface layer by etching is required if structural integrity is to be maintained.

Aluminum-beryllium alloys can be machined by conventional techniques.

**4.2.15.3 Forming.** The brittle nature of beryllium makes forming a problem. Most forming is done at elevated temperatures.

AlBeMet has greatly improved formability over beryllium. Processes such as semisolid metalworking (SSM) have been used to form aluminum-beryllium alloys to near net shape, reducing raw material costs at the expense of additional tooling cost.

**4.2.15.4 Joining.** Mechanical fastening of beryllium must be done with care, because the drilling of holes will cause microcracks. Riveting operations may cause cracking of the structure.

AlBeMet may be joined satisfactorily by riveting, because its increased ductility will absorb impact, and surface damage from machining is not a major problem.

Welding of beryllium results in brittle welds that so far have not been considered satisfactory. AlBeMet appears to be weldable with either AlBeMet filler rod or with aluminum alloy filler rod.

Brazing of beryllium is practicable using either conventional aluminum brazing alloys or silver brazing alloys. AlBeMet may be brazed with aluminum brazing alloys.

**4.2.15.5 Cost.** Toxicity and high raw material costs are the two major issues to be considered when specifying beryllium. When performance standards such as low density, high stiffness, good thermal conductivity, and low thermal expansion are required, beryllium and aluminum-beryllium alloys should be considered. It is obvious that these materials must offer major design advantages to be cost effective in comparison with more conventional materials.

## 4.2.16 Copper and copper alloys

**4.2.16.1 General characteristics.** Copper and copper alloys to a great extent still dominate electrical-conductor applications in electronic equipment, even though aluminum and its alloys can show weight reduction and lower material cost. Among the characteristics that account for use of copper and its alloys are the following:

1. Pure copper has the highest electrical conductivity of any metal except silver when considered on a volume basis. As a result, copper electrical conductors require the lowest space for a given conductivity.
2. Forming characteristics of copper are exceptionally good and make economics of manufacture favorable.
3. Solderability of copper is good although, for most electric soldering, a solderable finish is required.
4. The application of finishes by electroplating is easy and reliable, as is the application of hot-dipped coatings.
5. The basic corrosion resistance of copper is good, and, again, finishes are easily and economically applied.



6. The availability of copper forms includes all sizes and shapes, including extremely fine wire, thin strip, and castings, as well as sheet, plate, bar, forgings, and extrusions.
7. Copper is suitable for many plant forming operations and lends itself to all machining operations. Such methods as electroforming and chemical milling are especially useful in shaping copper alloys.
8. The basic costs of copper and its alloys are still reasonable.
9. Thermal conductivity is high, offering a good means of transferring heat from components to a heat sink.

The above characteristics apply in general to copper and copper alloys. Note that alloying can drastically affect these properties. Some of the copper alloys have an electrical conductivity as low as 5.5 percent. Examine carefully all properties when selecting an alloy. Trade-offs sometimes will be required between such properties as strength and electrical conductivity. ASTM B152/B152M is a commercial specification that is commonly used for copper and copper alloy sheet strip and plate.

**4.2.16.2 High-electrical-conductivity alloys (UNS C10xxx and C11xxx).** Hundreds of copper alloy compositions are available. These range from high-purity copper to multiple alloys. Compositions are Copper Development Association/UNS designations. Alloys are distinguished by several characteristics.

The tough-pitch grades are probably the most widely used for electrical conductors. In the annealed condition, their electrical conductivities are approximately 100 percent International Annealed Copper Standard (IACS). The major drawback to these compositions, compared to the other high-conductivity coppers, is that they are subject to embrittlement by hydrogen at elevated temperatures of 700°F and above. This is because of the presence of oxygen in the metal, which will combine with hydrogen, resulting in internal cracking of the metal. Because most brazing operations involve hydrogen, either in the products of combustion of the heating gases or in furnace atmospheres, tough-pitch copper is not usually suitable where brazing is to be used in joining.

This problem can be overcome by use of copper with low oxygen content. Phosphorous deoxidized copper is one approach to solving this deficiency. The use of phosphorous as a deoxidizer results in a slight reduction of electrical conductivity and somewhat reduced formability.

Oxygen-free copper, which is produced without the use of metal deoxidizers, results in a product that is free from susceptibility to hydrogen embrittlement, retains 100 percent or better electrical conductivity, and has a formability equivalent to that of tough-pitch copper.

**4.2.16.3 Silver-bearing coppers (UNS C12500 to C13000).** High-conductivity coppers are also available with small amounts of silver present in the composition. These alloys retain the approximately 100 percent electrical conductivity,

with two additional advantages of improved creep resistance and resistance to softening at elevated temperatures. The latter advantage is useful if work-hardened material must be subjected to elevated temperatures during processing and it is desired to retain the work-hardened condition. The silver-bearing alloys will resist annealing at temperatures as high as 650°F, a temperature that will substantially anneal the pure coppers.

Other special-purpose, high-electrical-conductivity copper alloys are available with special properties. Among these are

1. *Zirconium-copper (UNS C15000)*. This is an alloy containing about 0.15 percent zirconium. It has improved creep strength at elevated temperatures and a small decrease in electrical conductivity.
2. *Tellurium-copper (UNS C145xx)*. The addition of small percentages of tellurium results in an alloy with a major improvement in machinability over pure copper while retaining an electrical conductivity of 90 percent IACS. Mechanical properties are moderately high as compared to those of copper.
3. *Sulfur-bearing copper (UNS C14700)*. The addition of sulfur to copper in small percentages results in a substantial increase in machinability while retaining a relatively high electrical conductivity of about 96 percent IACS.

It can be seen that a wide choice of compositions are available, with electrical conductivities in the 95 to 101 percent electrical conductivity range. Wide overlapping of properties, both physical and mechanical, can lead to many trade-offs in selection of materials. Very often, the selection will be one of economics of fabrication weighed against material costs. Material suppliers can offer aid in selecting a specific material.

**4.2.16.4 Brasses.** Brass, by definition, is an alloy of copper and zinc, but, in some cases, trade names have been given to brasses that suggest that they are bronze, which is by definition an alloy of copper and tin. There exists a wide range of compositions. Some generalizations may be made about the effect of zinc on copper. Among them are the following:

1. Tensile strength increases with increasing zinc content up to about 30 percent zinc.
2. Electrical and thermal conductivity decreases as zinc content increases.
3. Ductility of soft annealed material increases as zinc content increases up to about 30 percent zinc. In the harder tempers, ductility decreases in lean zinc alloys but begins to increase at around 10 percent zinc.

As indicated, these are generalizations that are subject to modification by cold-working and annealing sequences that affect grain size. For critical form-

ing or strength applications, it is desirable to work with the material supplier to select the specific set of properties tailored to the application and processing procedures.

**4.2.16.5 Leaded brasses.** Most of the brass compositions are available with lead added as a means of improving machinability. The lead exists in the matrix of the alloy as free lead, not as an alloy. The presence of lead results in production of fine chips in machining, thus producing a free-cutting condition. Lead contents vary from a nominal 0.5 percent to as high as 4.5 percent, with the highest percentage yielding the best machinability.

Lead has its detrimental qualities in that it reduces ductility. Problems may occur with the high-lead-content materials in forming operations. Terminals made from leaded alloys may crack in swaging and, in some cases, fracture during soldering. The latter problem is especially prevalent when the terminals are swaged to thick plastic terminal boards. Selection of one of the lower-lead-content alloys is a solution to this problem, although machinability may be reduced.

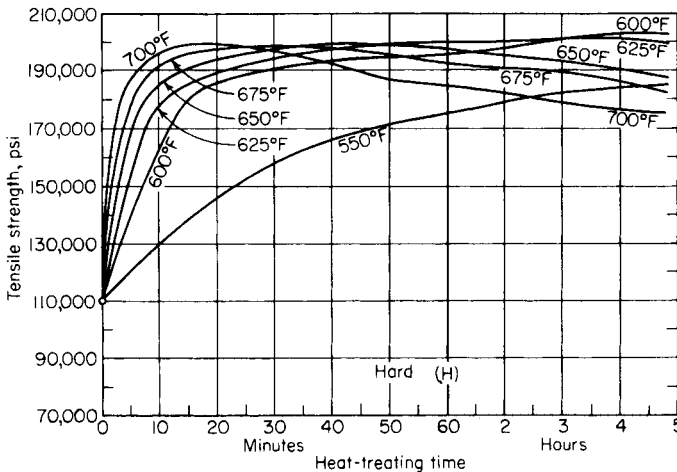
**4.2.16.6 Phosphor bronzes.** A series of bronzes containing 1 to 11 percent tin and 0.04 to 0.35 percent phosphorus is widely used for spring applications in electronics. These alloys are available in varying strengths up to a yield strength of 116,000 psi for the 10 percent tin alloy that has been cold-worked to the extra-spring-hard condition. However, this alloy has an electrical conductivity in the range of 11 percent IACS. The 1.25 percent tin alloy, on the other hand, has an electrical conductivity of about 48 percent, but its maximum attainable yield strength is 75,000 psi. This is an example of the trade-off that sometimes must be considered in reduced electrical conductivity so as to increase strength.

**4.2.16.7 Beryllium-copper (UNS C172xx).** Copper, when alloyed with beryllium, forms an alloy that is capable of being strengthened by precipitation hardening. It is capable of attaining tensile strengths in the range of 200,000 psi by proper heat-treating and cold-working procedures. At this hardness level, it still possesses good electrical conductivity in excess of 22 percent IACS. As a result of this combination of high strength and good electrical conductivity, beryllium-copper has become a widely used material for electrical spring applications.

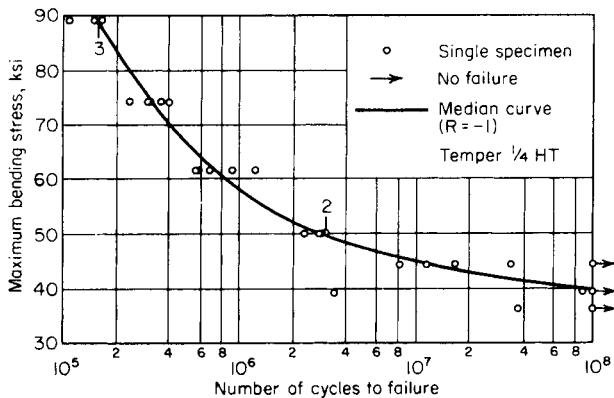
Because it is a precipitation-hardening alloy, beryllium-copper has processing advantages in forming. The material is subjected to a solution-annealing treatment, which leaves it in a relatively soft condition. Forming may be readily performed in this condition. A low-temperature aging treatment at about 600°F will result in increased strength with little distortion. For copper alloys, higher-strength alloys typically have the lower electrical conductivity. Effects on tensile strength and yield strengths brought about by variations in

aging temperatures are shown in Fig. 4.20. The 600°F aging is usually specified, because the time at temperature is not critical. Note that the aging time at 600°F can vary by several hours with little effect on tensile properties. At higher temperatures, a few minutes of excess time may result in overaging, with a resulting drop in properties. However, it is practical to use shorter aging cycles at higher temperatures if proper controls of material condition and heat-treating time and temperature are exercised. The cold-working history of the material between solution treating and aging is important in the aging response. Determination of aging cycles by test is desirable when deviation is made from the 600°F aging temperature.

Figure 4.21 shows the effect of repeated stress on the cycles to failure in fatigue for a 2 percent beryllium-copper alloy. Note that, at  $10^6$  cycles, the stress



**Figure 4.20** Effect of various aging times and temperatures on a typical 2 percent beryllium-copper alloy.



**Figure 4.21** Effect of repeated stress on strength of a typical 2 percent beryllium-copper alloy.

is about 40,000 psi and that, even at  $10^5$  cycles, the tolerable stress level is less than 90,000 psi even though the material has a yield strength of 150,000 psi. These data point out the importance of considering the number of load applications when designing for repeated loads.

#### 4.2.17 Magnesium alloys

Magnesium alloys have found acceptance primarily because they have the lowest density of any structural metal available today. The commonly used alloys have densities of about 0.065 lb/in<sup>3</sup>, and the recently developed magnesium-lithium alloys have densities of less than 0.050 lb/in<sup>3</sup>. These values may be compared to those of aluminum at approximately 0.100 and beryllium at approximately 0.066 lb/in<sup>3</sup>. Poor corrosion resistance and poor formability preclude the use of magnesium alloys in many applications. Procedures are available for overcoming these problems and providing economical and functional units for a variety of applications. Magnesium alloys are used in many applications for reduction in weight as compared to aluminum alloys and for lower cost than typical beryllium structures.

**4.2.17.1 Forms available.** Magnesium alloys are available in nearly all forms, including sheet, plate, bar, forgings, and extruded shapes. Extrusion is generally used for shaping bar, tubing, and other shapes. Castings are also available, but in compositions specifically developed for casting. All types of castings, including sand, die, permanent-mold, and investment, are available. Investment castings are available in any of the other casting compositions.

**4.2.17.2 Alloy designations.** Magnesium alloys are designated by a coding system that indicates the approximate nominal alloy percents of the two major alloying elements. Designations for alloys consist of not more than two letters representing the two alloys present in the largest percentages, arranged in order of decreasing percentages. The letters are followed by numbers representing the percentage of the alloying element rounded off to the nearest whole number. The most frequently used letters are as follows:

- A = aluminum
- L = lithium
- E = rare earths
- M = manganese
- H = thorium
- Z = zinc
- K = zirconium

An example designation is AZ31, which indicates an alloy of magnesium in which the two main alloying elements are aluminum and zinc, as indicated by

the AZ. The number 3 indicates 3 percent nominal aluminum, and the 1 indicates 1 percent zinc.

**4.2.17.3 Alloy availability.** The sheet alloy most commonly used is the AZ31 (3 percent aluminum, 1 percent zinc) composition. This is the general-purpose alloy for service near room temperature and is the most readily available alloy. The HK31 and HM21 alloys have been developed for improved strength at elevated temperature.

The LA141 alloy (14 percent lithium, 1 percent aluminum) is an example of the lowest-density class of alloys. Note that the strength of this alloy is relatively low, but the alloy possesses mechanical properties exceeding those of some commonly used metals such as annealed low-strength aluminum alloys. Other alloys based on the lithium-magnesium alloys are also available.

**Extrusion alloys.** Considerably more alloys are available as extrusions than as sheet alloys. The ZK60 alloys show the highest room-temperature properties of any magnesium alloys and compares favorably in terms of strength-to-weight ratio with the high-strength aluminum alloys. Compressive yield strength of magnesium alloy extrusions is significantly lower than the tensile yield strength of that same alloy. This is an excellent example of the directional properties found in certain alloys, as discussed previously. The magnitude of the difference between tensile and compressive yield strengths makes it mandatory that designers consider this difference in designs wherein stresses approach the yield strength.

**Elevated-temperature properties of wrought magnesium alloys.** As with all metals and alloys, the mechanical properties of magnesium are changed by temperature. Strength decreases as temperature increases, and ductility usually increases. Magnesium, being a relatively low-melting-point metal, can be drastically affected by moderately elevated temperature. For instance, the yield strength of AZ31B-H24 alloy decreases from 32,000 psi at room temperature to approximately 13,000 psi at 300°F. Alloys such as HK31A-H24 and HM21A-T8 are less affected by increases in temperature. HK31A-H24 has a yield strength of about 22,000 psi at 400°F, whereas HM21A-T8 retains a yield strength of about 13,000 psi at 600°F. Useful properties exist in selected magnesium alloys for moderately high-temperature service. Caution must be taken when using elevated-temperature properties, because the time at temperature, stress level, and the temperature itself also must be considered. Creep (deformation under a steady load) may occur well below the stress levels mentioned above. Consultation with suppliers for details about the properties for specific loading conditions and environments is recommended when designing for elevated temperatures. In some cases, tests simulating service conditions may be required.

**4.2.17.4 Magnesium alloy castings.** Magnesium alloy castings are poured in specific compositions primarily designed for casting. Usually, these alloys contain

higher percentages of alloying elements than are found in wrought compositions.

Investment casting practice has been developed to the extent that wrought-type alloys can be cast for special applications. AZ31 alloy has been cast for applications in which brazing was required.

K1A alloy, an alloy possessing a high damping capacity, is another specialty alloy. This alloy has been used for parts for which vibration damping is required. It is an alloy with about 1 percent zirconium. This alloy is available from most investment casting foundries. Mechanical properties are lower than those of most of the other magnesium casting alloys.

As with other castings, the question of guaranteed mechanical properties should be agreed upon via specification or drawing call-out, or specified on a purchase order. Most standardized specifications show mechanical properties of separately cast test bars and often allow the properties of the actual castings to be well below those specified. It is obviously important that the designer know whether the specified values are for test bars or for the casting itself. However, there is danger of unnecessarily raising the cost of castings if the maximum possible strength is specified for every section of the casting. A more reasonable procedure is to specify strength requirements in the critically stressed areas of the casting. This will allow the foundry to arrange its pouring and chilling practices to attain maximum soundness and strength in the critical areas.

**Elevated-temperature properties of magnesium castings.** Similarly to the wrought alloys, magnesium casting alloys suffer decrease in strength as temperature increases. The normal aluminum-zinc alloys such as AZ91 lose strength rapidly as temperature increases. EZ33A alloy maintains 50 percent of its room-temperature properties at 600°F, while HK31A-T6 still has 81 percent of its room-temperature strength at 500°F and 50 percent at 700°F. HK31A is another example of an alloy which is normally considered a wrought alloy but has found use in castings.

#### 4.2.17.5 Fabrication of magnesium alloys

**Forming.** Magnesium has a reputation of being difficult to form. However, under proper conditions, magnesium alloys may be formed to complex shapes by many techniques, including deep drawing. The use of elevated temperatures during forming is often necessary to accomplish such forming. Facilities that have been set up with heated dies have been very successful in forming magnesium alloys.

It is desirable, of course, to form material at room temperature for reasons of economy and convenience. Magnesium alloy AZ31A is capable of being formed as room temperature to a  $2T$  radius (where  $T$  = metal thickness) in thicknesses of 1/8 in and less. This compares favorably with some of the aluminum alloys.

**Joining.** Magnesium can be joined by most conventional joining methods, both mechanical and metallurgical, as discussed below.

*Riveting.* Riveting of magnesium is done by normal riveting practice. The riveting material recommended is aluminum alloy 5056. This alloy is sufficiently close to magnesium alloys in galvanic potential that no serious dissimilar metal problem exists. It is advisable that rivets be installed with a barrier such as zinc chromate primer which is applied wet to the rivet just before driving.

*Fusion welding.* Fusion welding of magnesium alloys may be readily accomplished with the tungsten inert-gas (TIG) process or with the metal inert-gas (MIG) process. Filler rods must be selected in accordance with the alloy being welded. The aluminum-zinc alloys (AZ) are usually welded with AZ9Z alloy as filler. The high-temperature alloys are often welded with EZ33 rod but also are welded with rod matching the material composition. Selection of rod composition will depend on the joint efficiency required, ductility required, and so forth. The individual magnesium supplier should be consulted for each specific case.

*Stress relieving of magnesium weldments.* The alloys containing aluminum and zinc as alloying elements are subject to stress corrosion. Because welding nearly always results in some residual stress, stress relieving is required after welding. Typical cycles are (1) 500°F for 15 min for AZ31 alloy annealed sheet and extrusions and as-extruded AZ61, ZK60, and AZ80; (2) 300°F for 60 min for AZ31 hard-rolled and ZK60 in the aged condition; and (3) 500°F for 60 min for cast alloys.

*Brazing.* It is possible to braze magnesium by the dip method, utilizing brazing fluxes similar to aluminum brazing fluxes. Filler metal is usually a 12.5 percent aluminum alloy. The removal of flux is a must, because the residues of flux are extremely corrosive to magnesium alloys. Most magnesium alloys may be brazed. A brazing process should be specified only after careful consultation with magnesium suppliers.

#### 4.2.18 Nickel and nickel alloys

Nickel alloys are characterized by good strength, corrosion resistance, and high ductility. The metal nickel has relatively good electrical conductivity, making it useful for electrical conductors for specialized applications. The magnetostrictive properties of nickel and high-nickel alloys make them applicable to various devices such as ultrasonic transducers. Nickel and nickel alloys have Curie temperatures that vary with alloy content. This transition from magnetic to nonmagnetic behavior has been used in control devices. The series of alloys based on nickel-copper are known as Monels.\* These materials show exceptional corrosion resistance in saltwater immersion service. Some of these alloys are age hardenable, notably the alloy K-500 and 500. The Inconel series of alloys is based primarily on nickel plus chromium plus iron with minor additions of other alloying elements. These alloys have exceptionally good elevated-temperature properties. Such alloys are useful at temperature ap-

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\* Registered trademark of Inco Alloys International.



proaching 2000°F. A specialty alloy of beryllium and nickel is age hardenable to strengths in excess of 200,000 psi. This material retains good strength at 600°F. It has found use as a spring material.

**4.2.18.1 Forms available.** Nickel and nickel alloys are available in most wrought forms. This includes all section sizes from ultra thin sheet and fine wire to heavy plate and forgings.

**4.2.18.2 Fabrication.** Nickel and nickel alloys have exceptionally good fabrication properties, as discussed below.

**Forming.** The ductility of nickel alloys makes forming by most conventional techniques extremely favorable.

**Joining.** Welding is practical for all nickel alloys by arc, gas, and resistance methods. Welding of nickel alloys to most steels as well as to some copper alloys is often performed.

**Brazing.** Brazing with the silver brazing alloys, copper, and nickel-base brazing alloys is readily accomplished by furnace, torch, induction, and resistance brazing.

**4.2.18.3 Physical properties of nickel alloys.** Table 4.19 shows values of a variety of properties of nickel alloys. The variety of magnetic and electrical properties obtainable by alloying makes nickel alloys extremely interesting to the electronics engineer.

**4.2.18.4 Mechanical properties of nickel alloys.** Nickel alloys may be supplied in various conditions (cold-drawn, annealed, and so on). These conditions will have ranges for properties. The ranges will depend on section size, manufacturing procedures, and heat-treating practice. Caution should be exercised when selecting materials of large section sizes, because it is likely that the highest-strength alloys will not be readily available.

#### 4.2.19 Titanium and titanium alloys

The chief attributes of the titanium family are excellent corrosion resistance, moderate density, and good strength, especially when considered on a strength-weight basis. Titanium alloys have densities about 60 percent of steel's, making the high-strength titanium alloys competitive with the high-strength steels when considered on a specific-strength (strength/density) basis. At temperatures around 600°F, titanium alloys surpass practically all other metals in reducing weight.

The electrical and thermal conductivities of titanium and its alloys are very low as compared to those of the aluminum, copper, and magnesium alloys.

TABLE 4.19 Physical Properties of Nickel and Nickel Alloys\*

Designation	Density, lb/in <sup>3</sup>	Modulus of elasticity, psi × 10 <sup>-6</sup>		Melting range, °F	Specific heat at 70°F, Btu/(lb)(°F)	Thermal expansion, in/(in)(°F) × 10 <sup>-6</sup>		Thermal conductivity, Btu/(hr)(ft <sup>2</sup> )(°F/in)		Electrical resistivity, Ω/cir mil/ft		Curie temperature, °F		Permeability @ 70°F (H = 200)		Poisson's ratio
		Tension	Torsion			70-200°F	70-500°F	70°F	500°F	70°F	500°F	Annealed	Age- hardened	Annealed	Age- hardened	
Nickel 200	0.321	30.0	11.0	2615-2635	0.109	7.4	7.9		374	57	126	680				0.31
Nickel 201	0.321															
Nickel 204	0.321	29.2				7.4	7.8			65		770				
Nickel 205	0.321									57						
Nickel 211	0.315					7.4	7.9	306	296	102	195					
Nickel 220	0.321															
Nickel 230	0.321															
Nickel 233	0.321															
Nickel 270	0.321	30.0		2650	0.11	7.4	7.8	655		43	125	667				
Permanickel alloy 300	0.316	30.0	11.0		0.106	6.8	7.9	400		94.5		600	563			
Duranickel alloy 301	0.298	30.0	11.0	2550-2620	0.104	7.2	7.7	165	211	255	310	60-120	200			0.31
Monel alloy 400	0.319	26.0	9.5	2370-2460	0.102	7.7	8.7	151	204	307	342	20-50				0.32
Monel alloy K-500	0.306	26.0	9.5	2400-2460	0.100	7.6	8.2	121	167	370	382	<-210	<-150	1.001	1.002	0.32
Monel alloy 501	0.306	26.0	9.5	2400-2460	0.100	7.6	8.2	121	167	370	382	<-210	<-150	1.001	1.002	0.32
Inconel alloy 600	0.304	31.0	11.0	2500-2600	0.106	7.4	7.8	103	127	620	639	-192		1.010		0.29
Inconel alloy 604	0.305					6.8	7.6	101	126	666	687	<-320		1.004		
Inconel alloy X750	0.298	31.0	11.0	2540-2600	0.103	7.0	7.4	83	104	731	754	-225	-193	1.002	1.0035	
Inconel alloy 751	0.298	31.0	11.0	2540-2600												
Inconel alloy 800	0.290	28.0	11.0	2475-2525	0.12	7.9	9.0	80	109	595	662	-175		1.009		0.30
Inconel alloy 801	0.287	29.0				8.1	9.0									
Inconel alloy 804	0.286	28.0				8.0				638		<-320		1.003		
Inconel alloy 825	0.294	28.0		2500-2550		7.8	8.4	77	103	678	719	<-320		1.005		
Ni-span-C alloy 902	0.293	24-29	9-10	2650-2700	0.12	4.2	6.0	84	114	611		340	380			

\*SOURCE: NASA contrace NAS8-21233, Final Report.

These low values are definite disadvantages in many applications but an advantage in applications where thermal isolation is desired or induced current from electric fields is to be minimized. Thermal expansion rates are slightly lower than for steels but generally are close enough to cause no appreciable problems. Physical properties are shown in Table 4.20. Titanium is available in commercially pure form (99 percent minimum Ti) and in a number of alloyed compositions.

Commercially pure titanium is available in several purities. This material ranges from 60,000 to 80,000 psi in tensile strength, depending on purity. It has the best heat-corrosion resistance, weldability, and formability of any of the titanium alloys. The pure metal is generally lowest in cost.

**4.2.19.1 Titanium alloys.** A number of alloying elements are used to enhance the properties of titanium. These include aluminum, vanadium, iron, manganese, tin, chromium, and molybdenum. Alloys are most often designated by nomenclature that starts with Ti, the chemical symbol for titanium, followed by a number that represents the nominal percentage of an alloying element, followed by the chemical symbol of the element. For example Ti6Al4V is titanium alloy containing 6 percent aluminum and 4 percent vanadium.

Three basic metallurgical types of alloys exist, namely, *alpha*, *alpha-beta*, and *beta*. The alpha type consists of alloys that retain the hexagonal crystal structure as found in pure titanium. On heating to 1625°F, unalloyed titanium transforms to a body-centered structure that is designated as the beta phase. Through the selection of alloying elements, the beta phase can be stabilized to the extent that it will exist at room temperature. Some alloys are alloyed to stabilize the entire structure in the beta phase at room temperature and thus are obviously called beta alloys.

Through proper selection of alloying elements, alloys have been developed that consist of a combined alpha and beta two-phase structure at room temperature. These alloys retain some of the advantages of both the alpha and beta phases and also render such alloys capable of heat treatment to higher strengths. Heat treatment consists of heating to temperatures that are high enough to transform the alpha phase to beta. Rapid cooling suppresses the natural transformation of beta to alpha. On subsequent aging, there is a transformation of some of the beta to alpha. This alpha is distributed throughout the beta matrix to give a fine structure that results in increased strength.

Some beta alloys can be heat treated by aging as well. During aging, fine particles of alpha and intermetallic compounds are precipitated out to provide strengthening. By alloying, the strength of titanium can be raised considerably above the strength of the unalloyed material. Yield strengths above 150,000 psi at room temperature are attainable with available alloys. Several factors other than mechanical properties must be considered when selecting an alloy. One of these is the availability of the alloy within the time required and in the quantity required. Metal distributors do not tend to stock many titanium and alloy products. The method of fabrication will also influence selection. Many of the alloys are not considered weldable, as welds are brittle.

TABLE 4.20 Typical Physical Properties of Titanium Alloys

Nominal composition, % (bal. Ti)	Density, lb/in <sup>3</sup>	Thermal expansion mean coefficient per °F × 10 <sup>-6</sup>			Thermal conductivity, Btu/(hr)(ft)(°F)		Instantaneous specific heat, Btu/(lb)(°F)		Electrical resistivity, μΩ-cm		Elastic moduli, psi × 10 <sup>-6</sup>	
		RT to 200°F	RT to 600°F	RT to 1000°F	RT	800°F	RT	800°F	RT	800°F	<i>B</i>	<i>G</i>
99.5 Ti	0.163	4.8	5.2	5.5	9		0.124		57		14.9	6.5
99.2 Ti	0.163	4.8	5.2	5.5	9.5		0.125		56		14.9	6.5
99.0 Ti	0.163	4.8	5.2	5.5	9.5–11.5	10.5	0.125	0.151	48–57	117.7	15.0	6.5
99.0 Ti	0.164	4.8	5.2	5.5	9.8–10.1	10.0	0.129	0.155	55–60	122.3	15.1	6.5
98.9 Ti	0.164	4.8	5.2	5.5	9.8		0.129		58		15.5	6.5
0.15–0.20 Pd	0.163	4.8	5.1	5.4	9.5		0.125		56.7		14.9	6.5
<i>Alpha alloys</i>												
5 Al, 2.5 Sn	0.161–0.162	5.2	5.3	5.3	4.5	7.2	0.125	0.152	157	180	16.0	7.0
5 Al, 2.5 Sn (low O)	0.161	5.2	5.3	5.4	4.5		0.125		157		16.0	
5 Al, 5 Sn, 5 Zr	0.166										16.0	
7 Al, 12 Zr	0.165										16.5	
7 Al, 2 Cb, 1 Ta	0.159										17.7	
8 Al, 1 Mo, 1 V	0.158	4.7	5.0	5.6					199	203	18.5	
<i>Alpha-beta alloys</i>												
8 Mn	0.171	4.8	5.4	6.0	6.3	9.0	0.118	0.152	192	140	16.4	7.0
2 Fe, 2 Cr, 2 Mo	0.171										16.7	
2.5 Al, 16 V	0.165										15.0	(aged)
3 Al, 2.5 V	0.162										15.5	
4 Al, 4 Mn	0.163	4.9	5.1	5.4	4.2	7.4	0.126	0.159	153	172	16.4	7.3
4 Al, 3 Mo, 1 V	0.163	5.0	5.3	5.5	3.9	6.8	0.132	0.142	165		16.5	7.0
5 Al, 1.5 Fe	0.162–	5.2	5.3	5.5							16.8	
2.75 Cr	0.163										17.6	(aged)
5 Al, 1.5 Fe, 1.4 Cr	1.162–	5.2	5.5	5.7	4.7	7.0			163	180	16.5	6.3
1.2 Mo	0.163										17.0	(aged)
6 Al, 4 V	0.160	4.9	5.1	5.3	4.2	6.8	0.135		171	187	16.5	6.1
6 Al, 4 V (low O)	0.160	5.3	5.3	5.3			0.135		171		16.5	6.1
6 Al, 6 V, 2 Sn	0.164	5.0	5.2	5.3	4.2		0.155		157		15.0	
1 (Fe, Cu)									157	170	16.5	(aged)
7 Al, 4 Mo	0.162	5.0	5.2	5.6	3.7	7.0	0.123	0.151	175	183	16.2	6.5
											16.9	(aged)
<i>Beta alloys</i>												
1 Al, 8 V, 5 Fe	0.168											
8 Al, 13 V, 11 Cr	1.175–	5.2	5.6	5.9	4.0	8.0	0.120	0.198	153		14.2	6.2
	0.176								142		14.8	(aged)

**4.2.19.2 Corrosion resistance of titanium alloys.** One of the major attributes of titanium alloys is corrosion resistance. The major commercial applications of these materials have been in the chemical field where the superior resistance to chemical attack has resulted in major economies as a result of the increased longevity of titanium parts as compared to that of other structural metals. Room-temperature atmospheric and saltwater environments are withstood well by titanium alloys. Stress corrosion in the presence of chlorides above 600°F is a problem, but such conditions are uncommon in electronic equipment, so this is not a serious drawback.

Titanium is the noble metal in a galvanic couple with most structural materials except stainless steel and Monel. Protection to prevent a galvanic couple may be needed when titanium is attached to other metals, especially aluminum alloys, magnesium alloys, or beryllium. As for most galvanic couples, consult MIL-STD-889 for guidance.

**4.2.19.3 Contamination.** Titanium and its alloys are subject to pickup of hydrogen, oxygen, and nitrogen, which will generally result in decreased ductility. Such contamination is most likely to occur at elevated temperatures. Thus, caution must be used in selecting atmospheres for heat treatment, especially above 1200°F. Selection of heat-treating atmospheres that are rich in one or more of the deleterious elements should be avoided. Inert gases such as helium or argon are most satisfactory as protective atmospheres, whereas a vacuum provides good protection and, in some cases, may be used to remove hydrogen that has been picked up from other sources. Plating and pickling are also sources of hydrogen pickup. Welding of titanium without fill shielding is another source of oxygen and nitrogen contamination.

**4.2.19.4 Forms available.** Titanium alloys are available in nearly any wrought form. Casting developments are underway, but casting has not become a common technique. Sheet, plate, bar, wire, strip, tubing, and extrusions are available in one alloy or another. Stock from a metal distributor may not be reliable, depending on the demand in a particular geographic region. Consultation with suppliers on the availability of alloys and forms available in that alloy is recommended before specifying a material for production.

**4.2.19.5 Fabrication of titanium.** Conventional processes are used for fabricating titanium parts. However, special precautions and revised techniques are sometimes required.

**4.2.19.6 Forming.** Titanium alloys have reasonable formability, similar to many other high-strength materials. Bend radii on commercially pure annealed high-purity sheet may be as low as 1 times the sheet thickness ( $1T$ ). The high-strength alloys in the solution-treated and aged condition may re-

quire radii as great as  $8T$  or more. Springback is particularly troublesome in titanium and its alloys because of their high yield strengths combined with relatively low elastic moduli. Hot-forming is often used with titanium alloys to minimize springback and decrease bend radii. Caution must be used in selecting temperatures for forming, because temperatures above the aging temperature will overage the material, resulting in lower strength.

**4.2.19.7 Welding.** Tungsten inert-gas welding of the weldable alloys is practical. The major precaution is that the heated weld area must be shielded from the atmosphere. Shielding gas should be supplied to both sides of the weld, and a trailing shield of gas is required to protect the weld during cooling. It may often be desirable to weld in an enclosure that is filled with inert gas. Glove box chambers for this purpose are commercially available.

Mechanical properties of welds are excellent. Most weldable alloys can be welded to 100 percent joint efficiency. The pure titanium grades and the alpha alloy grades are all weldable with good resulting mechanical properties and ductility. Certain of the alpha-beta alloys can be satisfactorily welded, but others are subject to formation of brittle welds. Caution should be used when specifying welding of these alloys, and the advice of materials suppliers should be sought on selection of welding rod, joint design, and welding procedures. Resistance weldability of titanium is excellent.

#### 4.2.20 High-density materials

Although, to a great extent, electronics engineers are interested in producing lightweight equipment, there are occasions when a high-density material is required so as to place a concentrated mass in a small volume. In some instances, the requirement for low thermal expansion and high thermal conductivity supersedes the weight requirement. A typical application is a counterweight.

Three categories of metals are available for these purposes. Of course, the moderately heavy metals, such as steels, nickel alloys, and copper alloys, can be used for such purposes if space is available. We will concentrate on the lead, tungsten, and depleted uranium metals, because they have higher densities than the aforementioned metals but still have reasonable economic feasibility as compared to high-density precious metals such as gold.

**4.2.20.1 Lead and lead alloys.** Lead, with a specific gravity of 11.35 g/cc (0.41 lb/in<sup>3</sup>) and a relatively low cost, is often a choice for counterweights. The low melting point of lead allows it to be cast using low-cost techniques, resulting in further economies.

The major disadvantage of lead is its low strength. The yield strength of relatively pure lead is around 800 psi, thus making it unsuitable for load-carrying applications. The creep rate of lead at room temperature is appreciable at stresses of 300 psi.

Antimony, when alloyed with lead in percentages of 1 to 9 percent, can appreciably increase the strength of lead. These alloys are also precipitation

hardenable by heat treatment. For the 4 percent antimony alloy, values of above 11,000 psi tensile strength have been reported. As-cast values of around 3,500 to 4,000 psi tensile strength have been found. Creep strengths do not appear to be drastically improved, however, indicating that sustained loads should be avoided.

Recently, dispersion-hardened lead has been developed. This material is available in the dispersion-hardened condition but will lose most of its favorable properties if melted.

**4.2.20.2 Sintered tungsten.** Sintered tungsten material is available with specific gravities in the range of 17 g/cc. These materials are usually tungsten particles mixed with other materials such as copper or nickel, after which they are compacted and sintered. The metals other than tungsten melt and braze the tungsten particles together. A wide variety of proprietary materials are available. Density and mechanical properties will vary, depending on the percentage of metals other than tungsten used.

The materials are available in bars and may be furnished in relatively complex shapes if quantities are sufficient to amortize dies.

**4.2.20.3 Depleted uranium.** This material, with a density in the range of 18.5 g/cc, has become available. With mechanical properties similar to those of low-carbon steel, it offers good structural properties. It is also capable of being cast to shape and worked by conventional tools, making economies of manufacture possible. Corrosion resistance of depleted uranium is poor, so it requires corrosion protection by the application of coatings.

#### 4.2.21 Refractory metals

Refractory metals, which are noted for their high melting points and ability to be useful at high temperatures, find some uses in electronic equipment at relatively low temperatures. These uses often are based on a combination of physical and mechanical properties. In addition, some of the metals have extremely good resistance to acids.

Table 4.21 summarizes the physical and mechanical properties of four important refractory alloys. It can be seen that a variety of properties are available among the metals tungsten, tantalum, molybdenum, and columbium. Alloys are available that modify these properties.

**4.2.21.1 Mechanical properties.** The most important of these alloys' mechanical properties is the useful strength that exists at elevated temperatures as high as 1000°C. This has been of major importance in consideration of these materials and structures.

**4.2.21.2 Modulus of elasticity.** The variation in modulus is wide, with tungsten possessing a value about twice that of steel, whereas columbium's modulus is

TABLE 4.21 Typical Properties\* of Refractory Alloys

Property	Tungsten	Tantalum	Molybdenum	Columbium
Atomic number	74	73	42	41
Atomic weight	183.92	180.88	95.95	92.91
Atomic volume	9.53	10.9	9.41	10.83
Mass				
Density at 20°C:				
g/cc	19.3	16.6	10.2	8.57
lb/in <sup>3</sup>	0.697	0.600	0.368	0.31
Thermal properties				
Melting point, °C	3400	2996	2625	2415
Boiling point, °C	5900–6700	7400	5560	3300
Linear coefficient of expansion per °C × 10 <sup>-6</sup>	4.0	6.5	5.45	6.89
Thermal conductivity at 20°C, cal/(sec)(cm <sup>2</sup> )	0.399	0.130	0.349	0.13
Specific heat, cal/(g)(°C)	0.34 (100°C)	0.036 (0°C)	0.061 (20°C)	0.065 (0°C)
Electrical properties				
Electrical conductivity, % IACS	31	13.9	36	13.3
Electrical resistivity, μΩ-cm	5.48 (0°C)	12.4 (18°C)	5.17 (0°C)	14.2
Temperature coefficient of electrical resistivity per °C	0.00482 (20–100°C)	0.00382 (0–100°C)	0.0047 (20–100°C)	0.0395 (0.600°C)
Mechanical properties				
Tensile strength, ksi:				
At room temperature	100–500	100–150	120–200	75–150
At 500°C	175–200	35–45	35–65	35
At 1000°C	50–75	15–20	20–30	
Young's modulus of elasticity, psi × 10 <sup>-6</sup>	59	27	46	12–15
At room temperature				
At 500°C	55	25	41	6.5
At 1000°C	50	22	39	
Working temperature, °C	1700 down	Room	1600	Room
Recrystallization temperature, °C	1300–1500	1050–1500	900–1200	900–1300
Stress-relieving temperature, °C	1200	900	800	800
Nuclear				
Cross section, thermal neutrons, barns/atom	19.2	21.3	2.4	1.1

\*Ranges only; data vary with type of sample and previous work history.



little higher than that of aluminum. The retention of high-modulus values at elevated temperatures is another factor in the use of these materials at elevated temperatures.

**4.2.21.3 Density.** The high density of tungsten and tantalum has resulted in their use as counterweights and as radiation shields. Molybdenum and columbium are slightly more dense than steel. The low thermal-expansion rates of tungsten and molybdenum make them good materials for use with some glasses and ceramics. Tantalum and columbium have expansion rates that are relatively low as compared to those of steels.

**4.2.21.4 Electrical properties.** The electrical properties of these metals, especially tungsten and molybdenum, make them applicable as electrical conductors. On the other hand, these alloys are also used as heating elements.

The characteristics shown in Table 4.21 gives a general view of the properties to be expected in alloys of this group. Alloys based on these metals will generally retain the properties of the base metal in terms of density, modulus of elasticity, and high temperature resistance. Attention should be paid, however, to the effect of alloying on electrical conductivity and thermal conductivity, as well as thermal expansion.

#### 4.2.22 Precious metals

The precious metals find rather frequent use in electronic equipment, generally for their physical and surface properties rather than for their mechanical properties. Physical properties such as electrical conductivity account for the use of such alloys as gold and silver. Their resistance to form surface compounds that interfere with electrical and/or optical properties of surfaces accounts for the use of such materials as gold, rhodium, and platinum.

Table 4.22 gives some of the physical properties of the most frequently used precious metals. These are typical figures for the pure metals. Most of these metals may be alloyed with other metals to enhance certain properties, but often with major effects on other properties. The form of the metal must also be considered. This is especially true of the electroplated form, because many of these metals find their major use as electroplates. Many electroplates have additives that are present for purposes of aiding in throwing power, smoothness, or luster, or for other reasons. These additives may have major effects on such properties of the deposited metal. In addition, many electroplates are actually alloys that may have drastically different physical and mechanical properties from those quoted for pure wrought metals. The density of electroplates varies somewhat also and will result in property variations.

**4.2.22.1 Silver.** Silver has the highest electrical conductivity and thermal conductivity of any of the metals. It has found use as electrical conductors and as

TABLE 4.22 Physical Properties of Precious Metals

Metal	Density, lb/in <sup>3</sup>	Melting temp., °F	Coefficient of linear expansion per °F × 10 <sup>-6</sup>	Thermal conductivity @ 212°F, Btu/(hr) (ft <sup>2</sup> )(°F/ft)	Specific heat, Btu/(lb)(°F)	Electrical resistivity @ 32°F, μΩ-cm
Platinum	0.775	3217	4.9	42	0.031	9.83
Palladium	0.434	2826	6.5	41	0.058	10.0
Rhodium	0.447	3560	4.6	50	0.059	4.51
Ruthenium	0.441	4190	5.1	—	0.057	7.6
Iridium	0.813	4447	3.8	34	0.031	5.3
Osmium	0.82	5432	3.6	—	0.031	9.5
Gold	0.698	1945	7.9	172	0.031	2.19
Silver	0.379	1761	10.9	242	0.056	1.47

a contact material. Probably the largest use of silver is as an electroplate on various types of pins, terminals, and contacts. The tarnishing of silver by sulfur compounds, which are present in most industrial atmospheres, is a major problem in the use of silver as a contact alloy or as a finish for terminals that must be soldered. The sulfide of silver interferes with electrical contact and makes soldering difficult. As a result, most silver surfaces are protected with an overplate of gold, which will protect the surface from sulfide formation. Problems have been encountered with this system of protection, because thin or porous electroplates do not offer sufficient protection to prevent sulfiding through the gold electroplate. At present, 50 millionths of an inch of gold is considered sufficient.

Silver is a low-strength material that is not suitable for most structural applications. Alloying with copper is a means of increasing the strength of silver. At 10 percent copper, which is known as *coin silver*, electrical resistivity increases to 2.2 Ω-cm as compared to about 1.6 Ω-cm for pure silver. The tensile strength of the 10 percent copper alloy in the annealed condition is almost twice that of silver in the annealed condition.

**4.2.22.2 Gold.** Gold is used widely as an electroplate to give corrosion resistance, to provide a contact surface with low resistance, and, in some special cases, as a conductor material. The low strength of gold makes it of little use as a structural or wear-resistant material. Alloys are available in both wrought and cast form and in the electroplated form. Alloys such as cobalt may increase the resistivity quite drastically. For instance, 1 percent cobalt increases the resistivity of gold by 710 percent.

**4.2.22.3 Rhodium.** The high reflectivity and low electrical surface resistance of rhodium, combined with its high hardness and the stability of the surface under corrosive conditions, make rhodium highly suitable for contact surfaces and mirrors. Rhodium is primarily applied by electroplating.<sup>8</sup>

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# Solder Technologies for Electronic Packaging and Assembly

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## 5.1 Introduction

### 5.1.1 Scope

What drives the end-use market are the continued convergence of computing, communication, and entertainment as well as the relentless growth of the wireless, portable, handheld digital electronics and optoelectronics. On the ever-changing technology landscape, the industry has responded and will continue to respond to competitive demands in the global marketplace. New electronic gadgets will be featured with increasingly higher functionality, further simplicity, lower cost, and greater operational ease. What has transpired from these market demands is continued technological innovation and an ever-shortening product life cycle. Environment-friendly manufacturing and the delivery of environmentally benign end-use products that are ultimately safe at the end of the product life cycle will become essential to technology-business competitiveness. This is a continuing challenge to the industry. Solder has served as the interconnecting material for all three levels of connections: die, package, and board assembly. In addition, tin/lead solder is commonly used as a surface coating for component leads and PCB surface finishes. In addition to solder materials, the process used to form solder joints to accomplish the vital function of electrical, thermal, and mechanical linkages between two metallic surfaces is equally important.

## 5.2 Chapter 5

This chapter addresses solder technologies in both material and process aspects for electronic packaging and assembly. Considering the established role of lead (Pb) and the demand in Pb-free materials, solder can be classified as either lead-containing or lead-free. In light of the global environmental commitment, this chapter will also cover Pb-free materials in terms of their properties and characteristics that are important to their applications in electronic packaging and assembly.

### 5.1.2 Surface mount technology

In this electronic and information age, we witness new technology developments and new product introductions to the marketplace almost on a monthly basis. One of the strongest trends, however, in the electronics interconnection and packaging segment is utilization of the surface-mounting concept to develop superior circuit board assemblies in both performance and cost. This concept has been utilized in hybrid assembly since the 1960s by interconnecting chip resistors, chip capacitors, and bare semiconductor dies on metallized substrates. Nevertheless, the potential of surface mounting was not fully explored and utilized until the early 1980s.

What is surface-mount technology? As the name implies, it is basically the application of science and engineering principles to board-level assembly by placing components and devices on the surface of the printed circuit board instead of through the board. Although this concept appears to be straightforward, the impact on the production floor is enormous, not only on components and design but also on materials and equipment. It also narrows the distinction between hybrid circuit assembly and printed circuit assembly. The specific benefits of surface mount technology in relation to through-hole technology include

- Increased circuit density
- Decreased component size
- Decreased board size
- Reduced weight
- Shorter leads
- Shorter interconnection
- Improved electrical performance
- Facilitated automation
- Lower costs in volume production

### 5.1.3 Industry trends

**5.1.3.1 Semiconductors.** Looking at the hierarchy of electronics, semiconductor devices have continuously exhibited improved reliability, reduced feature size,

increased wafer size, and doubled complexity every 18 months, in accordance with the Moore's law. As examples, wafer size increased from 3 to 4 in (75 to 100 mm) in the 1980s to 12 in (300 mm) this year; circuits have shrunk to sub-micrometer (0.1 to 0.25  $\mu\text{m}$ ) from several micrometers; IC pin count has increased from 40 to 80 to more than hundreds or tens of hundreds; IC fabrication techniques and equipment are developing in rapid pace from wet process and microanalysis to X-ray lithography and nanoanalysis.

At 45 years old, integrated circuits (ICs) are moving into another era of major developments. The new copper interconnect technology facilitates the implementation of deep submicron circuitry thus alleviating the RC delay problem. Copper has a significantly better conductivity than aluminum, which has been the backbone of IC circuits ( $\text{Cu} = 1.7 \mu\Omega\text{-cm}$ ;  $\text{Al} = 3.1 \mu\Omega\text{-cm}$ ). Copper is also known to have better electromigration resistance than aluminum. However, copper diffusion into silicon has been one of the major obstacles to the use of copper interconnect. Using IBM's proprietary barrier layer to prevent copper diffusion along with other companion technologies, the copper interconnect has become increasingly prevalent since 1999. IBM's Cu-connect ASIC technology (SA-12) also demonstrated 40 percent power savings by using 1.8 V rather than 2.5 V. The reduction in power consumption without sacrificing signal-to-noise quality is critical to the performance of portable electronics.

For example, it is reported that interconnects account for more than 70 percent of the signal delay in a 0.25- $\mu\text{m}$  chip. Interconnect RC delay increases as the square of the minimum feature size, thus determining the IC chip performance. As the feature size continues to shrink to 0.13  $\mu\text{m}$  or finer, RC delay issues become more critical.

In addition to the lower resistance offered by copper, a capacitance dielectric material lower than  $\text{SiO}_2$  is equally important to keep the interconnect RC delay in control for the nanoelectronics era. *System-on-a-chip* is another ongoing development. Fundamentally, the material innovations will be paramount to future generations of IC circuits. Combining deeper understanding in materials science with technology development, silicon crystals will get closer to perfection. Perfect silicon, obtained by eliminating crystal defects such as vacancies and dislocations, offers a new level of performance. Other silicon technologies continue to advance. IBM's *strained silicon* technology is reported to increase chip speed up to 35 percent while reducing power consumption without needing to shrink silicon circuits. The new strained silicon technology speeds the flow of electrons through transistors by stretching the material. The stretching concept may not be new, but the know-how to manufacture chips from this concept is a breakthrough. The process may seem simple enough, like stretching fabric, but the novelty is at the atomic level where one manipulates the atoms in silicon.

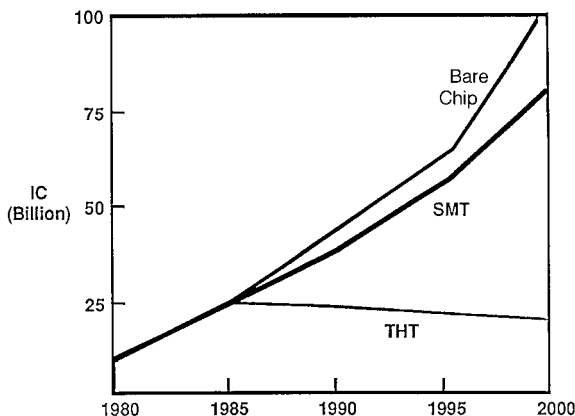
Up to now, electrons have been the workhorses for the electronic age and information era, making possible all modern products from ovens and cameras to computers and cell phones. Future technology may not only be derived from the conventional material theories of circuits, based on the mobility and conductivity of electrons and phonons, but also from photons. Nonetheless, elec-

tron transport will remain the main power behind future products in the foreseeable future.

**5.1.3.2 IC packaging and passive components.** With the known good die being a lingering issue for the board level assembly, the use of packaged surface mount devices continues to dominate. Across the two decades, the industry has evolved from dual in-line packages (DIPs) and pin grid arrays (PGAs) to 50-mil surface leadless ceramic chip carriers (LCCCs), plastic leaded chip carriers (PLCCs), small outline IC (SOIC), chip-scale packages (CSPs), and fine pitch quad flat pack (QFP), thin quad flat pack (TQFP), and array packages such as ball grid arrays (BGAs). The implementation of fine-pitch BGAs and CSPs continues to increase. Scanning over the package evolution, it can be categorized in three generic groups: Through-hole, surface mount, and chip-scale/direct die attach.

The use of surface mount devices finally exceeded that of through-hole devices in 1995, as shown in Fig. 5.1. It is projected that SMT will continue to enjoy a healthy growth rate at the expense of through holes, and the introduction of chip-scale (size) packages and direct chip attach will slowly fill the niche areas that require either maximal density and speed or minimal size and weight. Various packages are differentiated from one another by virtue of functional capabilities and/or physical characteristics. For example, package height of through-hole PGA in 3.5 mm compares with BGA in 2.3 mm; package-to-die size ratio for PQFP is around 8, and TBGA around 5. IC packages having high pin counts and new designs are expected to proliferate. Nonetheless, it is interesting to note that, despite the frequent introduction of new packages, SOIC/TSOP IC packages still occupy the largest market share at the present time and perhaps in the foreseeable future.

Array packages are primarily driven by high I/O count, board area savings, and the high radio frequencies required for wireless communication products.



**Figure 5.1** Market share of surface mount vs. through-hole.



The I/O pitch of BGAs generally falls in the range of 1.00 to 1.50 mm (0.040 to 0.060 in). PBGA, TBGA, and CBGA all have been adopted by chip makers for the high I/O counts required in workstations and minicomputers. Considering all factors in performance, economics, and reliability, a 250 I/O count is considered to be a break point in selecting between QFP and BGA. For products in which size and weight are critical to their marketability, CSP has been the center of attention since 1997. All six main CSP technologies (wire bond/rigid interposer, wire bond/flex interposer, flip-chip/rigid interposer, flip-chip/flex interposer, lead-frame/chip on lead, and wafer-level packaging) have been put to use.

The relative size of CSPs in comparison with other SMT packages can be clearly represented by the package area/die area ratio. CSP is generally accepted as less than 1.5, as opposed to BGA (1.25 mm pitch)  $\cong$  4, BGA (1.00 mm pitch)  $\cong$  2, QFP (0.4 mm pitch)  $\cong$  7, and QFP (0.5 mm pitch)  $\cong$  9.0. CSPs have made today's smaller portable electronics possible.

In addition to portable consumer electronics, the notebook computer is another application that drives the use of CSPs for relatively higher-I/O ASIC chips. CSPs have also been utilized in flash memory chips and extended to DRAM and SRAM packaging. However, the requirement of high-density PCB routing and the limited availability of package substrate materials have prevented the growth of high-I/O CSP technology to its fullest potential. The majority of CSPs have been for low-I/O applications. While a few specific CSP designs have emerged as "winners," the proliferation of new designs continues. As a renewed interest, flip-chip (wherein a bare chip with solder bumps on its surface is turned upside down and bonded directly onto the substrate without lead frame and wire bonding) has served as one of the base technologies to achieve chip-size packages, although CSPs can also be accommodated by wire bonding. As IC packages in conventional molded form or in chip size (scale) packages, or in flip-chip or in other advanced designs, are proliferating, the selection among various packages largely depends on the speed, heat dissipation, density (I/O), and cost desired. It is also end-use driven. For example, in the near future, while automotive ICs will use flip-chips and BGAs with high input/output (I/O), mobile and wearable electronics resort to ultra-thin CSP packages, stacked-chip packages, and system-in-package designs. Such packages will reach a higher performance level. Instead of 0.8-mm thickness, thinner CSP packages with a 0.5 mm thickness will be in demand. For stacked-chip packages, the goal is to put an entire cell phone in a single stacked package containing three vertically mounted dice. Because of heat management considerations, stacked-chip packages will remain limited in memory and other low-power uses in the near future.

In parallel, microelectromechanical systems (MEMS) will evolve by adding optical or mechanical components to a package, expanding the current end uses beyond vehicle airbag sensors, printer ink jet heads, and accelerometers. In this area, wireless applications will top the development list—for example, MEMS RF switches because of their advantage of low series resistance.

To meet wireless communications market demands, not only do IC packages need to be miniaturized, passive device manufacturers also must strive to

meet requirements for minimal real estate through chip size reduction or integration. In addition to physical miniaturization, increased capacitance values are also desirable for enhanced performance. To control and reduce cost, base metal electrodes, replacing noble metals, will increasingly find acceptance. For high-frequency applications, sustained capacitance and low equivalent series resistance (ESR) are increasingly important performance criteria for capacitors. The materials and processes that enable thinner dielectric layers to achieve higher capacitance values also will see increased demand. Additionally, high-frequency radio frequency (RF) circuits can make use of low-temperature ceramic co-fired materials, as they can reduce crosstalk between circuit elements. To alleviate the supply and cost concerns, niobium may be employed as a replacement for tantalum in capacitors.

We should begin to see a significant increase in the use of small 0402 and 0201 chips. Complementing discrete packages, other options are to integrate resistors, capacitors, and inductors in one package or to share the same package with ICs through thin or thick film technologies.

**5.1.3.3 Board-level assembly.** Ongoing efforts will be made to maximize yield, minimize defect rates, and improve performance by utilizing the technical knowledge, state-of-art equipment, and materials that have evolved in the industry. Constant assessment of new IC packages in conjunction with board design will become a part of the board-assembly business. Solder paste will remain the primary interconnection material, characterized by its established infrastructures, metallic nature, and fitness for automated manufacturing. Solder paste will only work not for SMT interconnections but also for certain through-hole components (paste-in-hole). Other solder deposition techniques, including solder jetting, will be assessed for specific packaging and assembly operations. Automation, SMT fitness (e.g., pick-and-place operations), and cost will be the determining factors for the viability and vitality of any new technology.

With the introduction of new packages and the increased number of package types for the PCB assembly and manufacturing processes, reflow profile in particular warrants further attention. Reflow profile not only affects the production defects and yield, it has an impact on the overall reliability of the assembly. A slower heating rate ( $<2^{\circ}\text{C}/\text{sec}$ , ideally  $<1^{\circ}\text{C}/\text{sec}$  in preheating zone) in conjunction with lower peak temperature exposure produces a good reflow profile. The same principle should also apply to rework and repair; using preheating and top/bottom heat source will facilitate the process and minimize any damage that may occur during rework. BGA rework processes and procedures are being established. The role of inert atmosphere ( $\text{N}_2$ ) soldering using low-nitrogen-consumption reflow ovens will be more prominent.

The accuracy and speed of placement equipment continues to improve. In addition, “gentle” placement capability, which allows manufacturers to work with small and fragile CSPs, is also in demand, including reliable feeding mechanisms and vision capability. To handle CSPs of 0.50-mm (0.020-in) pitch

or finer, positioning accuracy of  $\pm 0.05$  mm ( $\pm 0.002$  in) is required. Printing and dispensing systems for applying solder paste, underfill, adhesives, and coatings are characterized by increased automation and precision. New functional features continue to emerge to facilitate production operation and to enhance the end results.

Overall, flexible processes, agile manufacturing, and infrastructures equipped with hardware that offer versatile process capabilities are critical to the future success of SMT manufacturing.

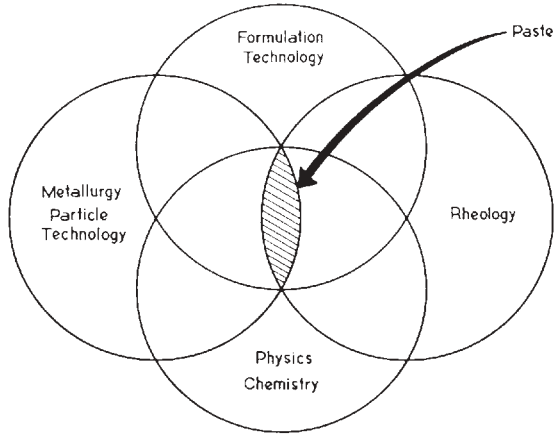
As the microelectronics and electronics industries continue to strive for higher quality and yield in every level of materials, designs, and processes, and as the density of board-level populations continues to increase, the demands on the soldering process and solder-paste materials will be increasingly stringent. Furthermore, environmentally friendly production will be a required part of future manufacturing. This includes CFC-free processes, reduced volatile organic compounds (VOCs), minimal waste, and lead-free solders.

In view of these trends, this chapter outlines the fundamentals of soldering and solder paste and the practical techniques and know-how in the key steps of soldering and solder-paste application, as well as new and emerging products and processes. It is hoped that this chapter will provide integrated knowledge in the soldering and solder-paste arena and stimulate much needed innovations in material, design, and processes.

#### 5.1.4 Interdisciplinary and systems approach

It has been said that the best science and technology are produced by a combination of four elements: an overriding commitment to scientific excellence, vision, intuition, and initiative. Soldering and solder-paste technology is no exception. Therefore, the objective of researchers is to meet demands for versatility in the soldering process and in solder-paste materials, and to continue to add to the pool of technology by applying and utilizing fundamental sciences and technologies.

From a technology point of view, pastes come from the interplay of several scientific disciplines. Figure 5.2 illustrates the spirit of paste technology.<sup>1</sup> Based on this technology, a number of existing and potential application product lines can be derived. These product lines are composed of organopolymeric vehicles and metallic and nonmetallic particulates, ranging from PM injection molding to EMI shielding composites, cermet thick film, polymer thick film, and solder paste, brazing paste, and adhesives. While each of these product lines has its unique qualities, one common fundamental is paste technology. Sciences and technologies to be utilized in paste technology include metallurgy and particle technology, chemistry and physics, rheology, and formulation technology. In addition, to meet the demands of the ever-changing electronics packaging industry and the accelerating pace of developments, a collaborative effort among users, material suppliers, and equipment manufacturers is much needed. They must be involved from the design state onward so as to develop the best suitable product or process system.



**Figure 5.2** Market share of surface mount vs. through-hole.

## 5.2 Solder Materials

### 5.2.1 Solder alloys

Solders are generally described as fusible alloys with liquidus temperature below  $400^{\circ}\text{C}$  ( $750^{\circ}\text{F}$ ).

The elements commonly used in solder alloys are tin (Sn), lead (Pb), silver (Ag), bismuth (Bi), indium (In), antimony (Sb), and cadmium (Cd). Their melting points are listed in Table 5.1. In addition to tin-lead alloys, binary solder alloys include tin-silver, tin-antimony, tin-indium, tin-bismuth, lead-indium, and lead-bismuth. Ternary alloys include tin-lead-silver, tin-lead-bismuth, and tin-lead-indium. The basic alloy for solder bumps at the die level (particularly the flip-chip) contains high temperature, high lead compositions such as Sn5/Pb95 or Sn10/Pb90. Eutectic or near-eutectic alloys such as Sn60/Pb40, Sn62/Pb36/Ag2, and Sn63/Pb37, have also been used successfully. The solder bump on the underside of the carrier CSP/BGA substrate, for example, can either be high temperature, high lead or eutectic, near eutectic tin/lead or tin/lead/silver materials.

**TABLE 5.1** Melting Points of Common Solder Elements

	Sn	Pb	Ag	Bi	In	Sb	Cd
$^{\circ}\text{C}$	232	328	961	271.5	156.6	630.5	321.2
$^{\circ}\text{F}$	450	620	1762	520	313	1167	610

Because of the temperature tolerance level of conventional board materials such as FR-4, board-level solder for attaching components and IC packages is

limited to eutectic, near-eutectic tin/lead, and tin/lead/silver solders. In some cases, tin/silver eutectic and low-temperature solder compositions containing bismuth (Bi) or indium (In) have been used.

Solder can be applied in various physical forms, including bar, ingot, wire, powder, preform, solder sphere and column, and paste, and in the molten state. The intrinsic properties of solder materials can be considered in three categories: physical, metallurgical, and mechanical. With the continued development of lead-free solders, new ternary, quaternary, and pentanary systems will proliferate.<sup>2</sup> The solidus and liquidus temperatures of some commonly used compositions are listed in Table 5.2.

Generally, the alloy selection is based on the following criteria:

- Alloy melting range in relation to service temperature
- Mechanical properties of the alloy in relation to service conditions
- Metallurgical compatibility, consideration of leaching phenomenon, and potential formation of intermetallic compounds
- Service environment compatibility, consideration of silver migration
- Wettability on specified substrate
- Eutectic versus noneutectic compositions

## 5.2.2 Metallurgy

For tin-lead binary alloys, the tin and lead elements have complete liquid miscibility and partial solid miscibility. The phase diagram in Fig. 5.3 shows solid solution regions represented by (Sn) and (Pb), a liquid region represented by L, liquid and solid solution regions represented by L + (Pb) and L + (Sn), and a solid solution mixture region, (Sn) + (Pb). As indicated, the eutectic point is 63 wt percent of Sn at a temperature of 183°C. The solubility of Sn in Pb increase as the temperature drops to the eutectic temperature and then decreases as

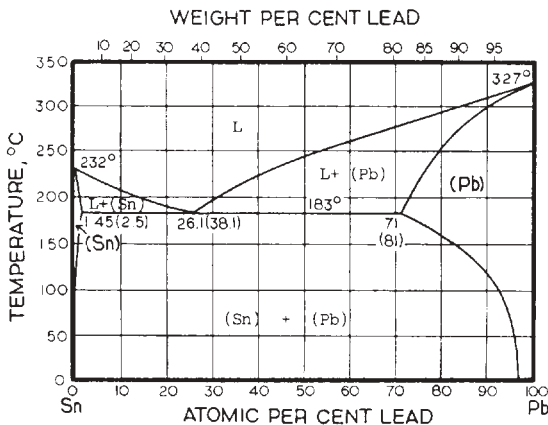


Figure 5.3 Phase diagram of Pb/Sn.

TABLE 5.2 Melting Range of Common Solder Alloys

Alloy composition	Melting range, solidus		Melting range, liquidus		Mushy range	
	°C	°F	°C	°F	°C	°F
70Sn/30Pb	183	361	193	380	10	19
63Sn/37Pb	183	361	183	361	0	0
60Sn/40Pb	183	361	190	375	7	14
50Sn/50Pb	183	361	216	420	33	59
40Sn/60Pb	183	361	238	460	55	99
30Sn/70Pb	185	365	255	491	70	126
25Sn/75Pb	183	361	266	511	83	150
10Sn/90Pb	268	514	302	575	34	61
5Sn/95Pb	308	586	312	594	4	8
62Sn/36Pb/2Ag	179	355	179	355	0	0
10Sn/88Pb/2Ag	268	514	290	554	22	40
5Sn/95Pb	308	586	312	594	4	8
62.5Sn/36Pb/2.5Ag	179	355	179	355	0	0
10Sn/88Pb/2Ag	268	514	290	554	22	40
5Sn/90Pb/5Ag	292	558	292	558	0	0
5Sn/92.5Pb/2.5Ag	287	549	296	564	9	15
5Sn/93.5Pb/1.5Ag	296	564	301	574	5	10
2Sn/95.5Pb/2.5Ag	299	570	304	579	5	9
1Sn/97.5Pb/1.5Ag	309	588	309	588	0	0
96.5Sn/3.5Ag	221	430	221	430	0	0
95Sn/5Sb	235	455	240	464	5	9
42Sn/58Bi	138	281	138	281	0	0
43Sn/43Pb/14Bi	144	291	163	325	19	34
52Sn/48In	118	244	131	268	13	24
70In/30Pb	160	320	174	345	14	25
60In/40Pb	174	345	185	365	11	20
70Sn/18Pb/12In	162	324	162	324	0	0
90Pb/5In/5Ag	290	554	310	590	20	36
92.5Pb/5In/2.5Ag	300	572	310	590	10	18
97.5Pb/2.5Ag	303	578	303	578	0	0

the temperature continues to drop. The same applies to the solubility of Pb in Sn.

The maximum solubility of Pb in Sn is 2.5 wt percent; of Sn in Pb, it is 19 wt percent. During soldering, the molten solder alloy wets the substrate with the aid of fluxes. Since the metallic surfaces involved in soldering tend to get oxidized or tarnished, the wettability depends to a large extent on the chemistry and reactions of fluxes. Nonetheless, the wetting phenomenon follows the basic wetting principle. For a system at a constant temperature  $T$  and pressure  $P$ ,

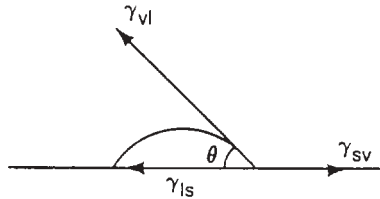
$$\left(\frac{\partial G}{\partial A}\right)_{PT} = \gamma$$

where  $G$  = free energy  
 $A$  = area  
 $\gamma$  = surface tension

Then, the thermodynamic condition for spreading to occur is

$$\Delta G < 0$$

The spreading of a liquid with negligible vapor pressure on a solid surface  $S$  is as follows:



Thus,

$$-\left(\frac{\partial G}{\partial A}\right)_{P,T} = \gamma_{sv} - (\gamma_{ls} + \gamma_{vl}\cos\theta)$$

where  $\gamma_{ls}$ ,  $\gamma_{vl}$ , and  $\gamma_{sv}$  are liquid-solid, liquid-vapor, and solid-vapor interfacial tension, respectively. Therefore, for spreading to occur,

$$\gamma_{sv} - (\gamma_{ls} + \gamma_{vl}\cos\theta) > 0$$

or

$$\gamma_{sv} > \gamma_{ls} + \gamma_{vl}\cos\theta$$

In general, for a system with liquid to wet the solid substrate, spreading occurs only if the surface energy of the substrate to be wetted is higher than that of the liquid to be spread.

## 5.12 Chapter 5

As the molten solder solidifies during cooling to form solder joints, the cooling process, including as the cooling rate, has a direct bearing on the resulting solder joint as to its microstructure and the development of voids. Figure 5.4 exhibits the SEM microstructure of 63 Sn/37 Pb melt under slow cooling, and Fig. 5.5 exhibits the microstructure under fast cooling, with other conditions being kept equal.

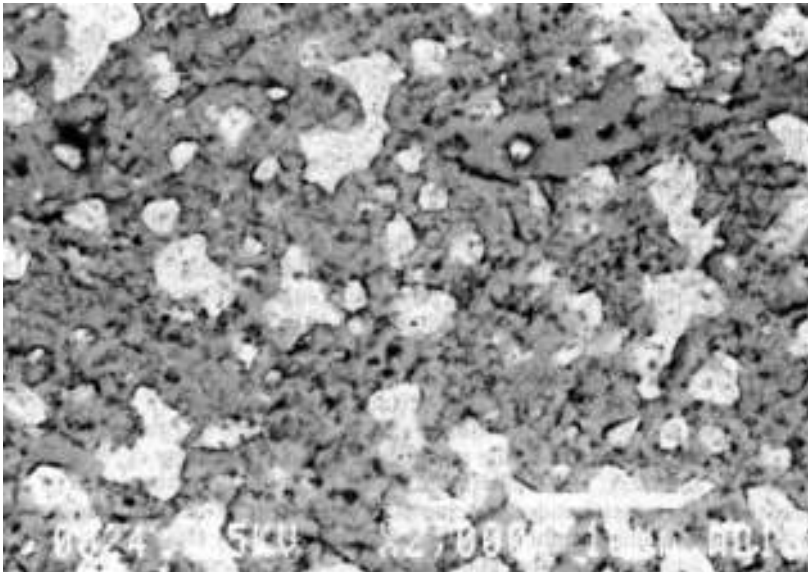
Because tin-lead solder alloys contain a solvus line and multiple solid phases, as shown in Fig. 5.3, they can be readily affected by heat treatment.

5.2.3 Solder powder<sup>2</sup>

Alloy powders can be produced by one of the common techniques—chemical reduction, electrolytic deposition, mechanical processing of solid particulates, and atomization of liquid alloys.

Alloy powders made from chemical reduction under high temperature are generally spongy and porous. The fine particles of noble metal powders are frequently precipitated by reduction of the salts in aqueous solution with proper pH. The precipitate slurry is then filtered, washed, and dried under highly controlled conditions. A mechanical method is generally used to produce flake-like particles. Metals possessing high malleability, such as gold (Au), silver (Ag), copper (Cu), and aluminum (Al), are most suitable for making flakes.

The electrolytic deposition process is characterized by dendrite particles, and it produces high-purity powders. The resulting particle sizes are affected by the type, strength, and addition rate of the reducing agent and by other re-



**Figure 5.4** SEM micrograph of 63Sn/37Pb under slow cooling.



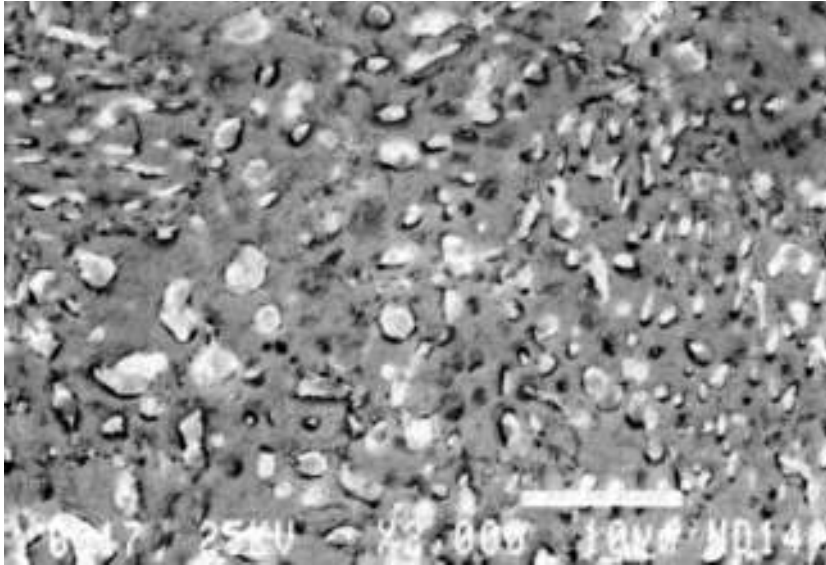


Figure 5.5 SEM micrograph of 63Sn/37Pb under fast cooling.

action conditions. The characteristics of the particles are also affected by current density, electrolytes, additives, and temperature. The principle of atomization is used to disintegrate the molten metal under high pressure through an orifice into water or into a gaseous or vacuum chamber. The powders produced by this method have relatively high apparent density, good flow rate, and are spherical in shape, as shown in Figs. 5.6 and 5.7. Powders to be used in solder paste are mostly produced by atomization because of its desirable inherent morphology and the shape of the resulting particles. Hence, the discussion that follows is concerned with the atomization technique only.

Figure 5.8 is a schematic of an inert gas atomization system with options of a bottom pouring system and a tilting crucible system. The system consists of a control cabinet, vacuum induction furnace, tundish, argon supply line, ring nozzle, atomization tower, cyclone, and powder collection container. The alloy is melted under inert gas at atmospheric pressure to avoid the evaporation of component ingredients. A high melt rate can be achieved. The molten material is then charged into the atomization tower. The melt is disintegrated into powder at atmospheric pressure by an energy-rich stream of inert gas. The process conducted in a closed system is able to produce high-quality powder.

In addition to inert gas and nitrogen atomization, centrifugal and rotating electrode processes have been studied extensively. The atomization mechanisms and the mean particle diameter are related to the operating parameters (diameter  $D$ , melting rate  $Q$ , and angular velocity  $\omega$  of the rotating electrode) and to the material parameters (surface tension at melting point  $\gamma$ , dynamic viscosity  $\eta$ , and density at melting point  $\rho$  of the atomized liquid). The relationships among these parameters are presented subsequently.

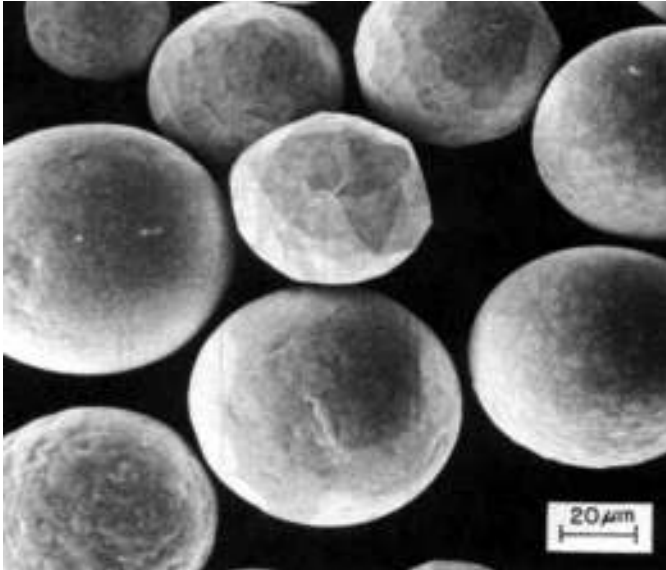


Figure 5.6 SEM micrograph of 63Sn/37Pb powder -200/+325 mesh.

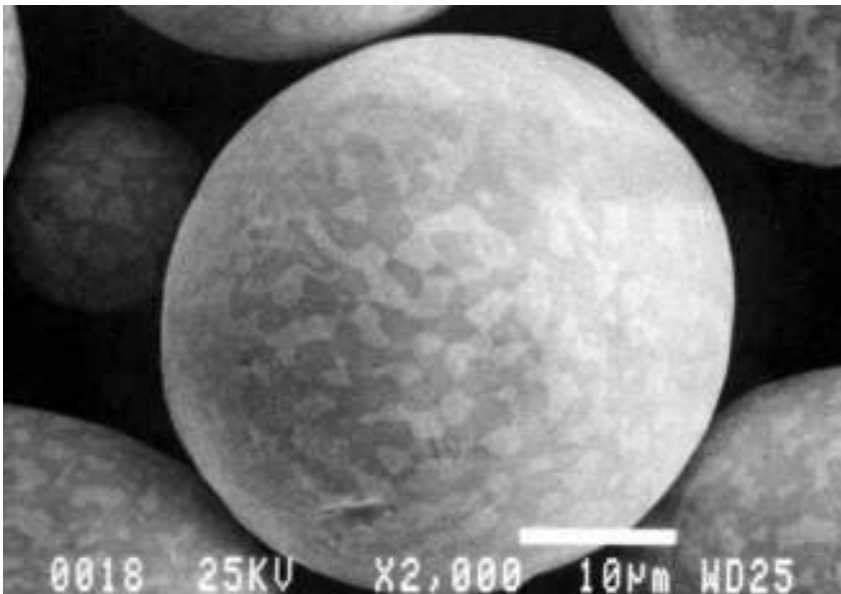


Figure 5.7 SEM micrograph of 63Sn/37Pb powder -325/-500 mesh.

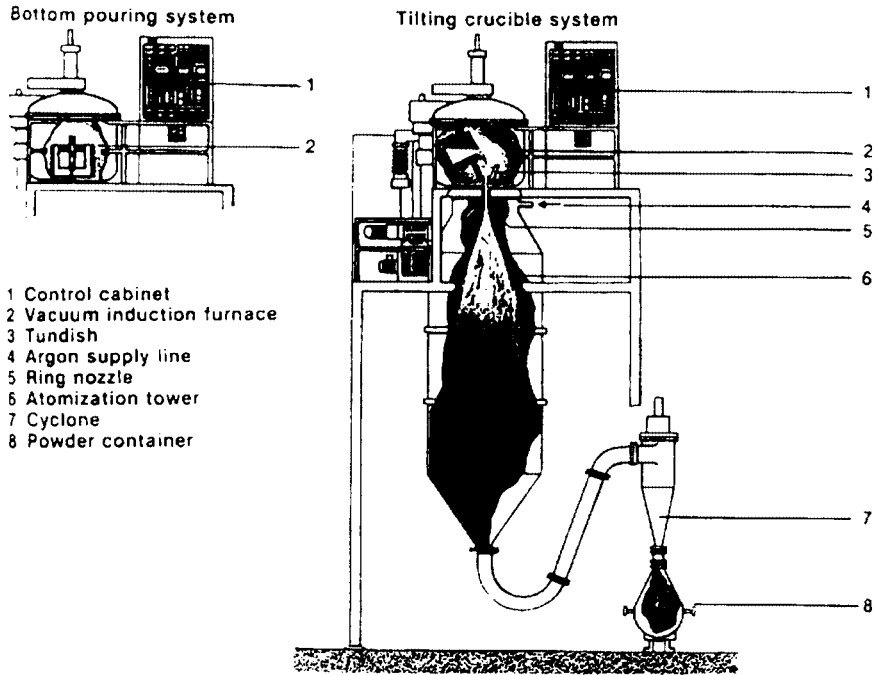


Figure 5.8 Schematic of an inert gas atomization system.

It has been found that the mean volume-surface diameter  $d$  is proportional to the surface tension of the atomized liquid and the melting rate but inversely proportional to the angular velocity of the rotating electrode, the diameter of the electrode, and the density of the atomized liquid, expressed by the following relation:

$$d \propto \frac{\gamma^{0.50} Q^{0.02}}{\omega^{1.03} \rho^{0.50} D^{1.05}}$$

where the symbols were defined earlier.<sup>3-5</sup>

The mass proportion of secondary particles  $P_s$  is directly related to the angular velocity of the rotating electrode, the density of the atomized liquid, and the melting rate but inversely proportional to the diameter of the electrode and the surface tension of the atomized liquid, expressed by the following relation:

$$P_s \propto \frac{\omega^{0.33} \rho^{0.56} Q^{1.24}}{D^{0.15} \gamma^{1.05}}$$

Metal powder can also be produced by vacuum atomization, which is believed to yield clean and finer particles. For superfine alloy powder, it is reported that a new atomizing technique is available using pulverizing energy produced by a

50-MPa water pump concentrated at the apex of a conical jet by which the thin stream of molten metal is disintegrated into superfine droplets.<sup>6</sup>

Ultrasonic gas atomization is another technique that produces metal powders successfully.<sup>7</sup> A process of two-stage spinning cup atomization with a liquid quenching is in development to produce fine particles with greater latitude in particle-size control.<sup>8</sup>

## 5.2.4 Mechanical properties

Three fundamental mechanical properties of solders include stress vs. strain behavior, creep resistance, and fatigue resistance.

Although stress can be applied by tension, compression, or shear force, most alloys are weaker in shear than in tension or compression. Shear strength is important, because most solder joints are subjected to shear stress during service.

Creep is a global plastic deformation that results when both temperature and stress (load) are kept constant. This time-dependent deformation can occur at any temperature above absolute zero. However, creep phenomena only become significant at “active” temperatures.

Fatigue is the failure of alloys under alternating stresses. The stress that an alloy can tolerate under cyclic loading is much less than that under static loading. Therefore, the yield strength, a measure of the static stress that solders will resist without permanent deformation, often does not correlate with fatigue resistance. The fatigue crack usually starts as several small cracks that grow under repeated applications of stress, resulting in a reduction of the load-carrying cross section of the solder joint.

Solder in electronic packaging and assembly applications normally undergoes low cycle fatigue (a fatigue life less than 10,000 cycles) and is subjected to high stresses. Thermomechanical fatigue is another test mode used to characterize the behavior of solder. It subjects the material to cyclic temperature extremes, i.e., a thermal fatigue test mode. Either method has its unique features and merit, yet both impose strain cycling on solders.

The ultimate tensile strength, 0.2 and 0.01 percent yield strength, and uniform elongation of common bulk solder alloys are listed in Table 5.3. In the group of Sn/Pb alloys, the strength decreases with decreasing tin content. This trend is expected, with the exception that the eutectic composition does not show the maximum strength. Its origin needs further confirmation.

The 96.5Sn/3.5Ag, 95Sn/5Ag, and 95Sn/5Sb compositions exhibit significantly higher strength and lower elongation. The composition 42Sn/58Bi is particularly strong, yet extremely brittle. In/Sn alloys with high indium content are extremely soft and lack adequate strength. It has been demonstrated that the solder joint strength may not coincide with that of bulk solder alloys because of other external factors, such as solder joint configuration, metallurgical reactions, interfacial wettability, interfacial effect, and the characteristics of other materials incorporated in the assembly.

Figures 5.9 through 5.30 show the creep behavior of solder alloys under a constant load of 920 g (equivalent to  $50 \times 10^6$  dyn/cm<sup>2</sup> initial stress) at an ambient temperature of  $25 \pm 3^\circ\text{C}$ .

TABLE 5.3 Tensile Strength and Uniform Elongation of Common Solders

Alloy composition	Liquidus, °C	Solidus, °C	Ultimate tensile strength, 10 <sup>3</sup> lb/in <sup>2</sup>	0.2% yield strength, 10 <sup>3</sup> lb/in <sup>2</sup>	0.01% yield strength, 10 <sup>3</sup> lb/in <sup>2</sup>	Uniform elongation, %
42Sn/58Bi	138	138	9.71	6.03	3.73	1.3
43Sn/43Pb/14Bi	163	144	5.60	3.60	2.77	2.5
30In/70Sn	175	117	4.67	2.54	1.50	2.6
60In/40Sn	122	113	1.10	0.67	0.53	5.5
30In/70Pb	253	240	4.83	3.58	3.08	15.1
60In/40Pb	185	174	4.29	2.89	2.06	10.7
80Sn/20Pb	199	183	6.27	4.30	2.85	0.82
63Sn/37Pb	183	183	5.13	2.34	1.91	1.38
60Sn/40Pb	190	183	4.06	2.06	2.19	5.3
25Sn/75Pb	266	183	3.35	2.06	1.94	8.4
10Sn/90Pb	302	268	3.53	2.02	1.98	18.3
5Sn/95Pb	312	308	3.37	1.93	1.83	26.0
15Sn/82.5Pb/2.5Ag	280	275	3.85	2.40	1.94	12.8
10Sn/88Pb/2Ag	290	268	3.94	2.25	2.02	15.9
5Sn/93.5Pb/1.5Ag	301	296	6.75	3.85	2.40	1.09
1Sn/97.5Pb/1.5Ag	309	309	5.58	4.34	3.36	1.15
96.5Sn/3.5Ag	221	221	8.36	7.08	5.39	0.69
95Sn/5Ag	240	221	8.09	5.86	3.95	0.84
95Sn/5Sb	240	235	8.15	5.53	3.47	1.06
85Sn/10Pb/5Sb	230	188	6.45	3.63	2.62	1.40
5Sn/85Pb/10Sb	255	245	5.57	3.67	2.26	3.50
95Pb/5Sb	295	252	3.72	2.45	1.98	13.70
95Pb/5In	314	292	3.66	2.01	1.79	33.0

Alloys of Sn/Ag, Sn/Sb, and 5Sn/85Pb/10Sb impart high creep resistance, as shown in Figs. 5.9 through 5.12. This is primarily attributed to solution hardening as substantiated by their high strength and low elongation. When load is applied, the deformation is hindered by means of either interaction of solute atoms with dislocations or interaction with the formation and movement of vacancies, resulting in the impediment of the dislocation movement. Figure 5.13 is a creep curve for the composition 85Sn/10Pb/5Sb, exhibiting relatively

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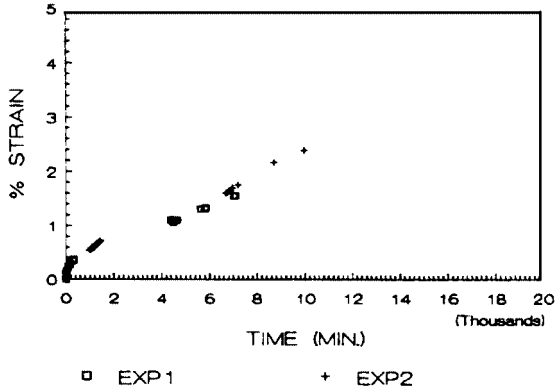


Figure 5.9 Creep curve of 96.5Sn/3.5Ag.

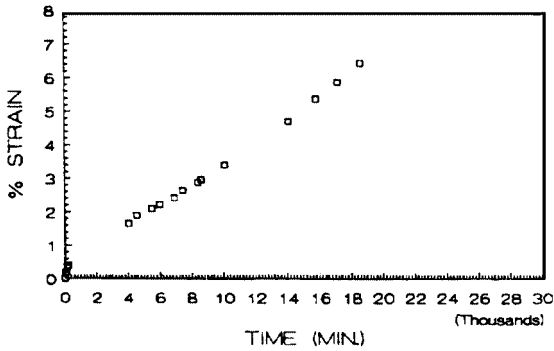


Figure 5.10 Creep curve of 95Sn/5Ag.

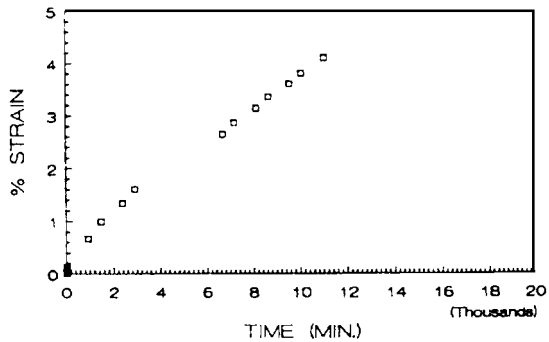


Figure 5.11 Creep curve of 95Sn/5Sb.

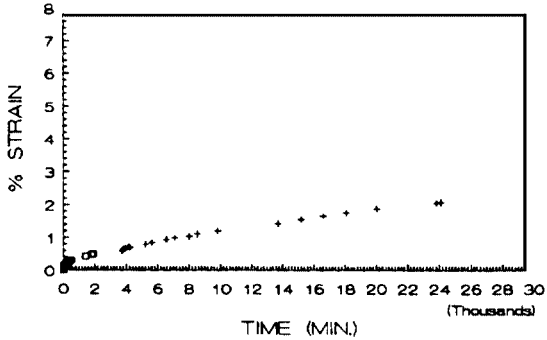


Figure 5.12 Creep curve of 5Sn/85Pb/10Sb.

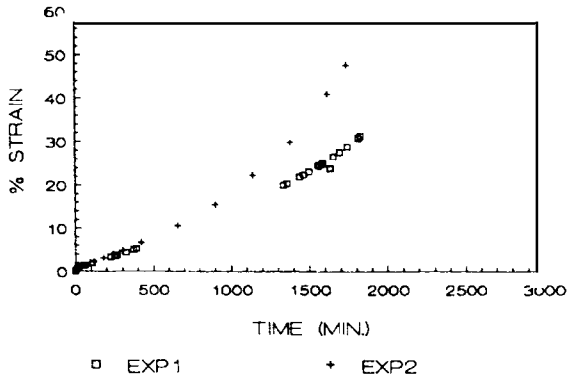


Figure 5.13 Creep curve of 85Sn/10Pb/5Sb.

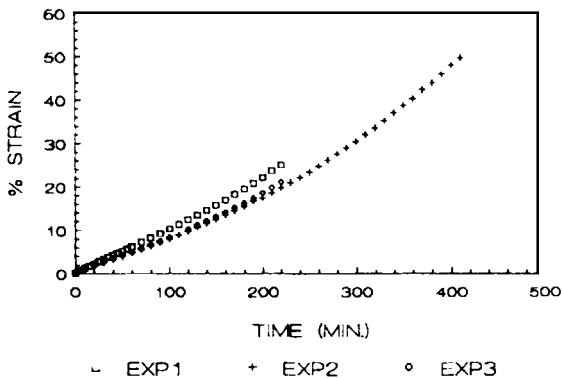


Figure 5.14 Creep curve of 63Sn/37Pb.

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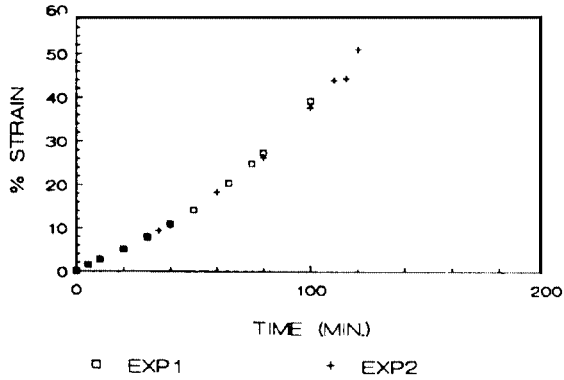


Figure 5.15 Creep curve of 60Sn/40Pb.

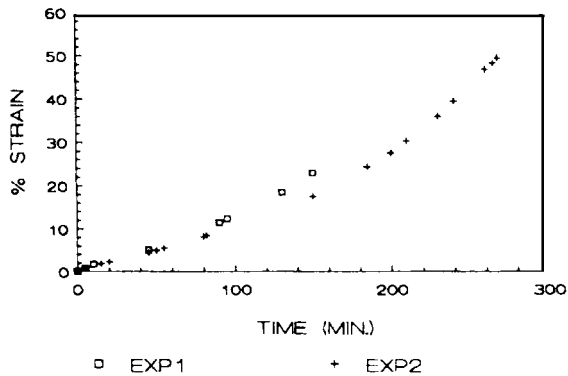


Figure 5.16 Creep curve of 80Sn/20Pb.

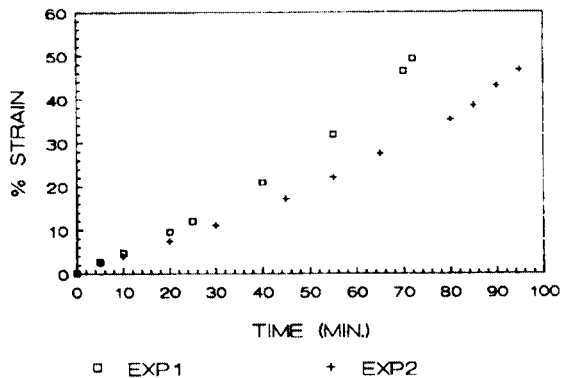


Figure 5.17 Creep curve of 25Sn/75Pb.



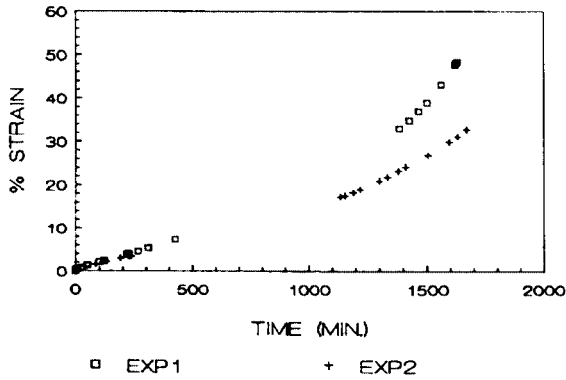


Figure 5.18 Creep curve of 10Sn/90Pb.

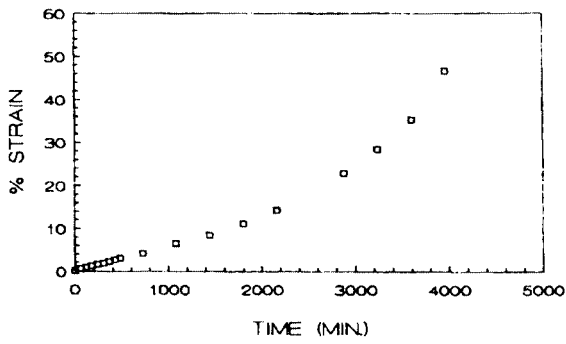


Figure 5.19 Creep curve of 5Sn/95Pb.

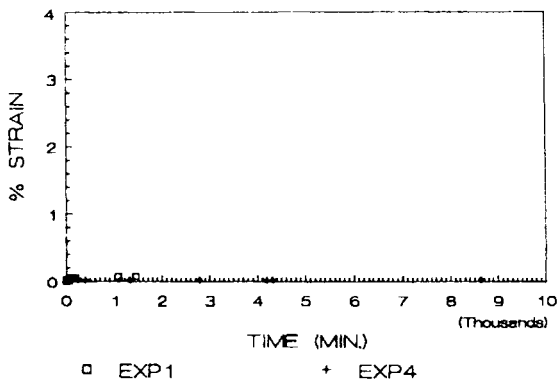


Figure 5.20 Creep curve of 62Sn/36Pb/2Ag.

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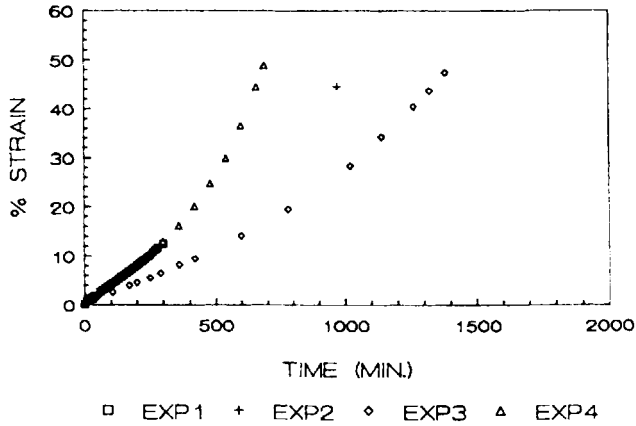


Figure 5.21 Creep curve of 15Sn/82.5Pb/2.5Ag.

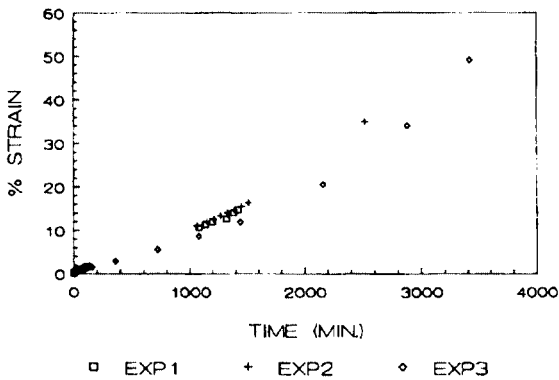


Figure 5.22 Creep curve of 10Sn/88Pb/2Ag.

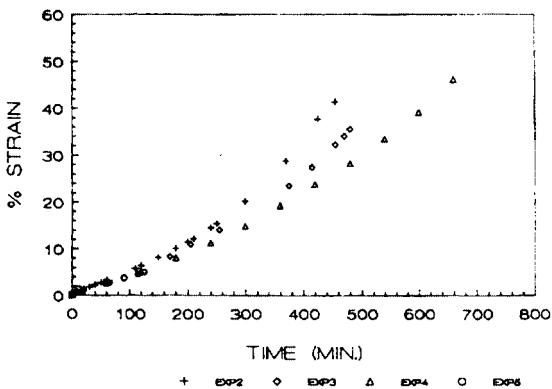


Figure 5.23 Creep curve of 5Sn/93.5Pb/1.5Ag.

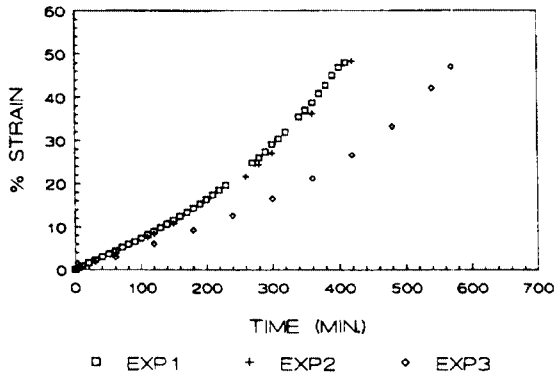


Figure 5.24 Creep curve of 1Sn/97.5Pb/1.5Ag.

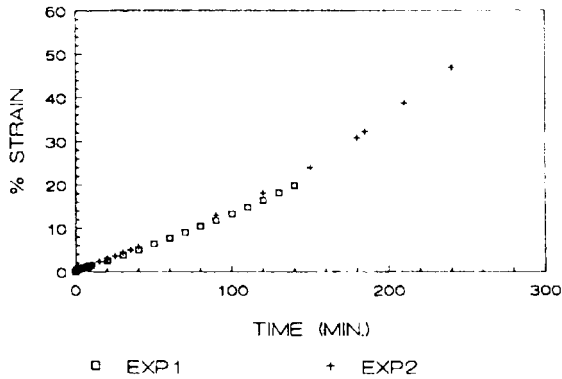


Figure 5.25 Creep curve of 42Sn/58Bi.

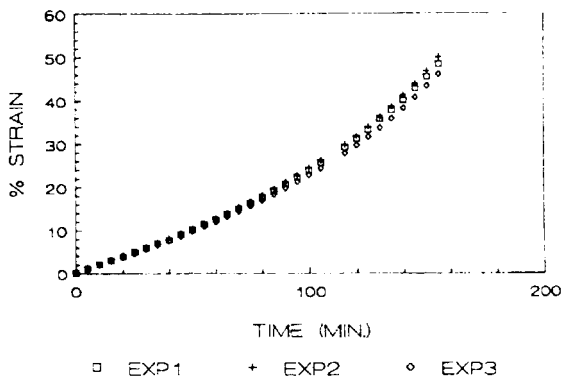


Figure 5.26 Creep curve of 43Sn/43Pb/14Bi.

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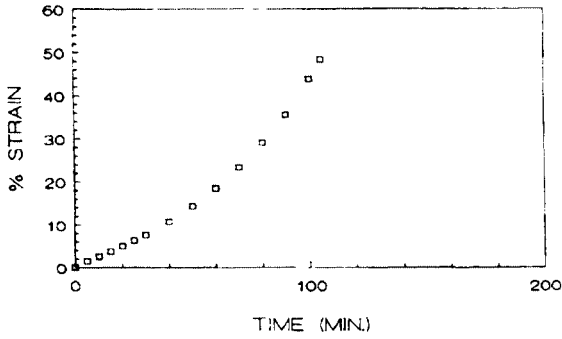


Figure 5.27 Creep curve of 30In/70Sn.

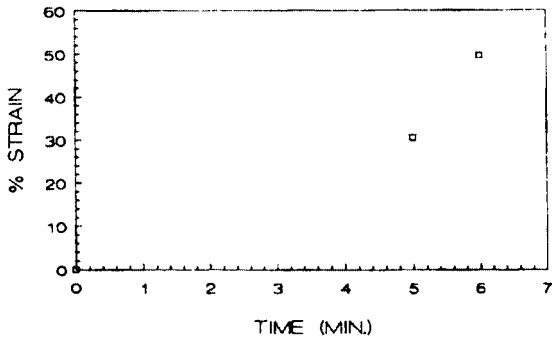


Figure 5.28 Creep curve of 60In/40Sn.

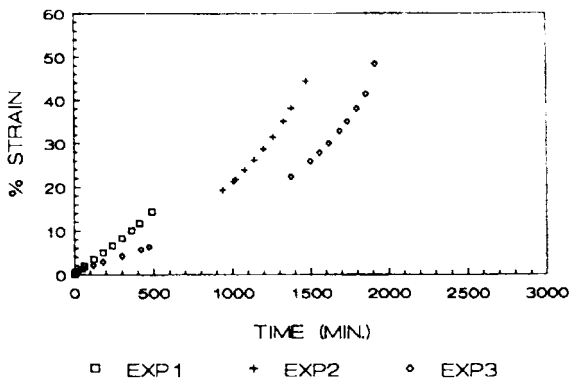


Figure 5.29 Creep curve of 30In/70Pb.

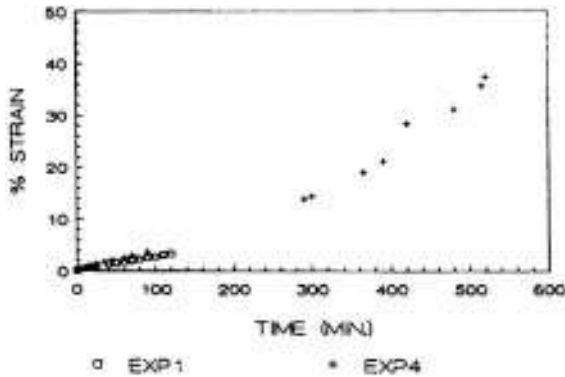


Figure 5.30 Creep curve of 60In/40Pb.

lower creep resistance than 5Sn/85Pb/10Sb. Their melting point may be a factor in creating such a difference.

Figures 5.14 through 5.19 show the creep curves for Sn/Pb compositions. Eutectic 63Sn/37Pb has higher creep resistance than noneutectic compositions 60Sn/40Pb, 80Sn/20Pb, and 25Sn/75Pb. Alloys 10Sn/90Pb and 5Sn/95Pb, however, benefited from the high melting point of their microstructural continuous phase, resulting in the more sluggish steady-state creep, as shown in Figs. 5.18 and 5.19. This is attributed to lower self-diffusion, although the alloys are ductile and have moderate strengths. The creep curves for Sn/Pb/Ag systems are shown in Fig. 5.20 through 5.24. 62Sn/36Pb/2Ag has the highest creep resistance. Its mechanism, whether through the impediment of grain-boundary sliding resulting from silver segregation or the result of high activation energy for the dislocation movement, is not substantiated.

Bismuth alloys, 42Sn/58Bi and 43Sn/43Pb/14Bi, though having high tensile strength, are found prone to creep. This may be primarily a result of their low melting temperatures and the predominance of the diffusion-controlled process. The corresponding creep curves are shown in Figs. 5.25 and 5.26. The In/Sn system has very poor creep resistance, as reflected in Figs. 5.27 and 5.28. The low melting point of their microstructural continuous phase is considered a main factor. While In/Pb compositions are ductile, as shown in the elongation data, the single-phase microstructure and moderate melting points provide moderate creep resistance, as shown in Figs. 5.29 and 5.30.

The creep resistance of the various solder alloys, as shown in Table 5.4, is ranked in five groups—low, low-moderate, moderate, moderate-high, and high. As the testing temperature or the applied load changes, a change in the creep behavior of the alloys may result.

### 5.3 Solder Paste

Solder paste, by its virtue of deformability and tackiness, is the primary material to make solder connections for surface mount and advanced surface mount processes when it is applied on the mother board (main circuit board)

**TABLE 5.4 Relative Creep Resistance of Common Solder Alloys**

Alloy composition	Rank	Alloy composition	Rank
42Sn/58Bi	Moderate	5Sn/95Pb	Moderate-high
43Sn/43Pb/14Bi	Low-moderate	62Sn/36Pb/2Ag	High
30In/70Sn	Low	15Sn/82.5Pb/2.5Ag	Moderate
60In/40Sn	Low	10Sn/88Pb/2Ag	Moderate-high
30In/70Pb	Moderate	5Sn/93.5Pb/1.5Ag	Moderate
60In/40Pb	Moderate	1Sn/97.5Pb/1.5Ag	Moderate
80Sn/20Pb	Moderate	96.5Sn/3.5Ag	High
63Sn/37Pb	Moderate	95Sn/5Ag	High
60Sn/40Pb	Low	95Sn/5Sb	High
25Sn/75Pb	Low	85Sn/10Pb/5Sb	Moderate
10Sn/90Sb	Moderate	5Sn/85Pb/10Sb	High

and/or when it is used for IC packaging on the module and package level. The deformable form of solder paste makes it applicable in any selected shape and size and readily adaptable to automation; its tacky characteristics provide the capability of holding parts in position without the need of additional adhesives before the permanent bonds are formed.

### 5.3.1 Definition

Solder paste, by one definition, is a *homogeneous and kinetically stable mixture of solder alloy powder, flux, and vehicle, which is capable of forming metallurgical bonds at a set of soldering conditions and can be readily adapted to automated production in making reliable and consistent solder joints.*

In terms of functionality, a solder paste can be considered as being composed of three major components. These are solder alloy powder, vehicle system, and flux system. The vehicle primarily functions as a carrier for the alloy powder, a compatible matrix for the flux system, and a basis for a desirable rheology. The flux cleans the alloy powder and the substrates to be joined so that high-reliability metallic continuity results and good wetting can be formed. Both vehicle and flux are fugitive or nonfunctional in nature after completion of the soldering. They are nevertheless crucial to the formation of reliable, permanent bonds. On a permanent basis, the alloy powder part is the only functional component in forming a metallurgical bond.

### 5.3.2 Characteristics

The chemical and physical characteristics of solder paste can be represented by the following parameters:

- Physical appearance
- Stability and shelf life
- Viscosity
- Cold slump
- Dispensability through fine needles
- Screen printability
- Stencil printability
- Tack time
- Adhesion
- Exposure life
- Quality and consistency
- Compatibility with surfaces to be joined
- Flow property before becoming molten
- Wettability
- Dewetting phenomenon
- Solder balling phenomenon
- Bridging phenomenon
- Wicking phenomenon
- Leaching phenomenon
- Quantity and properties of residue
- Residue corrosivity
- Residue cleanability
- Solder-joint appearance
- Solder-joint voids

### 5.3.3 Fluxes and fluxing<sup>9</sup>

The fundamental key to good solderability lies in ensuring that the surfaces to be joined are “scientifically” clean. Cleanliness must then be maintained during soldering so that a metallic continuity at the interface can be achieved. This cleaning process is called *fluxing*, and the material used is the *flux*.

Customarily, the flux is classified based on its activity and chemical nature, namely rosin-based such as RMA, water-soluble, and no-clean.

Fluxes are applied to the surface to react with metal oxides or nonmetallic compounds, thus “cleaning” them from the metal surfaces. Common metal surfaces that are soldered include Sn/Pb, Sn, Cu, Au, Ag, Pd, Au/Pd, Ag/Pd, Au/Pt, Au/Ni, Pd/Ni, and Ni. Each has its own associated fluxing chemistry.

The flux activity can be determined by the combined measurements in water extract resistivity, copper mirror test, halide test, and surface insulation test.

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To achieve fluxing, several approaches are available. Flux can be incorporated into the solder paste or inside the solder wire, it can be applied as a separate chemical directly onto the component and solder paste or inside the solder wire, or it can be applied as a separate chemical directly onto the component and solder pad surface, as with liquid flux used in wave soldering. Still another approach is gas-phase fluxing, which supplies a proper atmosphere to the soldering substrates. Other in-situ cleaning process may render the solder fluxless.

**5.3.4 Strength of fluxes**

The fluxing strength depends on the intrinsic properties of the flux agent or flux system as well as the external conditions. The factors include the following:

- Functional group and molecular structure of flux agent
- Melting point and boiling point of flux chemicals
- Thermal stability in relation to soldering conditions
- Chemical reactivity in relation to soldering conditions
- Surrounding medium of flux agent
- Substrates to be fluxed
- Environmental stability (temperature, humidity)
- Soldering conditions (temperature versus time, atmosphere)

The effects of molecular structure and medium on the strength of acids and bases are classified as inductive, resonance, hydrogen bonding, solvation, hybridization, and steric effects. For commonly adopted inductive effect, the electronic-withdrawing groups adjacent to the carboxylic group of molecules enhance the acidity strength of the carboxylic group as a result of anion stabilization. Conversely, electron-releasing groups decrease the acidity.

**5.3.5 Water-cleaning flux**

Water-cleaning flux is designed so that its residue after soldering can be removed by using either pure water or a water medium with the addition of a saponifier or an additive.

Considering performance, process, reliability, and cost, a flux chemistry that requires only water for removal (water-soluble) is the preferred choice. Special notes for using water-soluble solder paste are as follows:

- In the cleaning process, to avoid flux entrapment and incomplete residue removal, ultrasonic cleaning is an effective aid.
- In the soldering process, it is important to control the temperature profile, particularly in terms of peak temperature and dwell time at peak temperature to avoid overheating.



### 5.3.6 Gas-phase flux

Soldering under controlled-atmosphere conditions has been studied in recent years. Such controlled atmospheres can generally be classified as either *reactive* or *protective*.

The reactive atmosphere can help the fluxing agent clean component leads and solder pads. This approach has strong merits in solderability and leaves minimal residue. However, it should be cautioned that a reactive atmosphere is nonselective. It can react with all materials being exposed as long as the conditions meet thermodynamic and kinetic criteria. Therefore, all materials of an assembly must be compatible with the reactive atmosphere. With the wide variety of materials used in each assembly and the continued incorporation of new components and materials into assemblies, ensuring this compatibility can be quite a task. The protective atmosphere, on the other hand, primarily functions as an oxygen and moisture repellent during soldering without providing external chemical activity. Controlled atmosphere soldering is discussed in Sec. 5.4.6.

### 5.3.7 No-clean flux

From the user's point of view, no-clean flux (especially incorporated directly into solder paste) requires the following:

- Minimal amount of residue; ideally none
- Residue that is translucent and aesthetically acceptable
- Residue that will not interfere with bed-of-nails testing
- Residue that will not interfere with conformal coating where applicable
- Residue that is nontacky
- Residue that stays inert under exposure to temperature, humidity, and voltage bias
- Ability to flux effectively without solder-ball formation

Because of the wide variety of design and performance requirements in board assemblies, the acceptable amount of residue and the physical and chemical properties of the residue will vary from one application to another. An application-specific approach is needed. Success with a no-clean product requires close communication and collaboration between user and supplier to design a best-fit flux (material) and fluxing (process) system.

Common solder paste tests in chemical and physical characteristics continue to apply to no-clean systems. The industry's established test parameters and methods can be used to assess the quality and properties of the assemblies. These include ionic contaminant test and visual examination. However, the tests for no-clean system have one difference. These tests should be conducted after reflow or soldering. The solder paste chemical makeup measurement in terms of ionic mobility must be also taken after exposure to a specified reflow condition, not before exposure. This procedure is designed to

target the characteristics of the residue left on the board, not the as-is paste chemistry.

### 5.3.8 Comparison between water-clean and no-clean

With proper cleaning process and reflow parameters, a water-soluble process can produce clean assemblies in both function and appearance. In addition, the nature of its chemistry imparts wider fluxing latitude, better accommodating the inherent variations in solderability of components and boards. It requires initial equipment capital, added operating costs in energy and water consumption, and expenditures on consumables for a closed-loop recycle system.

No-clean (air) systems eliminate one process step, which is clearly an economic advantage. It should be noted that the cleaning process has been perceived as a step to remove residues from solder flux or paste, yet it actually has provided the cleaning function for components and boards for many operations without being noticed. It is not unusual for boards, before fluxing and soldering, to contain higher amounts of ionic contaminants than after soldering and cleaning. The level of as-received contamination may exceed the acceptable level, because most steps in board fabrication and component plating involve highly ionic chemicals.

For a no-clean system that requires soldering under a protective atmosphere such as  $N_2$ , the cost of  $N_2$  may offset or exceed the savings gained from no-clean operations, depending on  $N_2$  consumption and the unit cost of  $N_2$ , which varies with the location. Other factors that may also complicate the assessment of a no-clean system are solder ball effect and the acceptability of residue appearance.

Nonetheless, both water-clean and no-clean routes are viable application systems. A basic understanding of the principles behind each practice and the compliance with application requirements is essential to the success of implementing either manufacturing system. Table 5.5 summarizes the general feature comparison between water-clean and no-clean, and Table 5.6 illustrates viscosity and metal load of dispensing and printing pastes.

**TABLE 5.5 Comparison of Water-Soluble vs. No-Clean (Air)**

	Water-soluble	No-clean (air)
Merits	<ul style="list-style-type: none"> <li>• Clean assembly in function and appearance</li> <li>• Latitude for solderability variation</li> </ul>	<ul style="list-style-type: none"> <li>• One less process step</li> <li>• Lower operating and capital expenses</li> </ul>
Drawbacks	<ul style="list-style-type: none"> <li>• Extra step of process-cleaning</li> <li>• Operating cost—water, energy, and consumables</li> <li>• Initial capital expenditure</li> </ul>	<ul style="list-style-type: none"> <li>• Unable to remove contaminants from board and components</li> <li>• Often demand higher level of process control</li> <li>• Uncertainty in solder ball effect</li> <li>• Appearance issue</li> <li>• Possible limits for high-frequency application and/or uses that demand extraordinary extension of fatigue</li> </ul>

TABLE 5.6 Viscosity and Metal Load of Dispensing and Printing Pastes

Solder paste type	Viscosity, cP*	Metal load, wt%
Fine dot dispensing	200,000–450,000	To 88
Screen printing	450,000–1,000,000	To 92
Stencil printing	700,000–1,600,000	To 92

\*Centipoise, Brookfield RVT viscometer, TF/5 r/min, 3-min mixing/2-min reading.

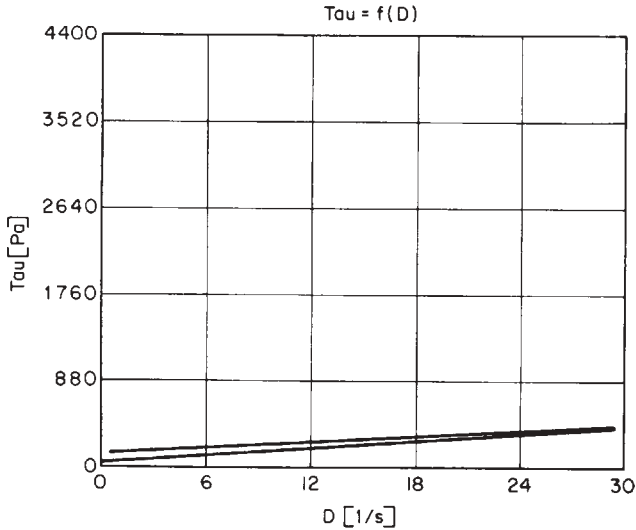
### 5.3.9 Rheology

Paste applicability depends on its rheology, that is, its flow and deformation behavior. The primary driving forces underlying the rheology of solder paste include both kinetic and thermodynamic contributions. Therefore, the rheology of solder paste may be affected by the following factors:

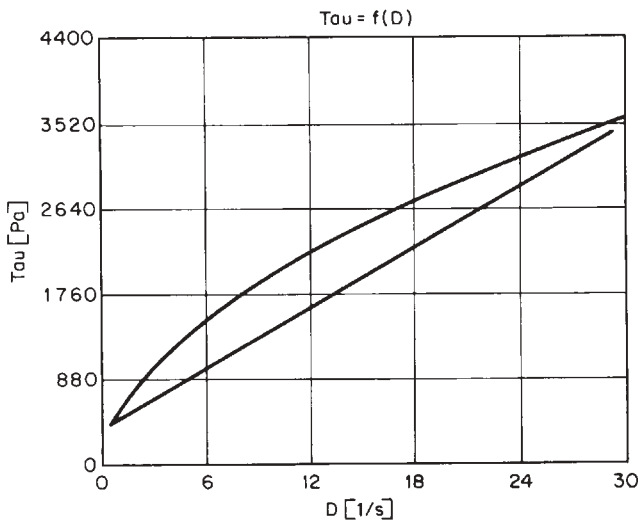
- Composition, shape, and size of suspended particles
- Chemical composition of suspending matrix
- Relative concentration of effective ingredients in matrix
- Structure of ingredients in matrix
- Interactions between matrix and suspended particles either physical or chemical in nature, including wetting and solvation
- Volume fraction occupied by suspended particles—usually, the higher the amount of particles, the more deviation from viscous flow
- Internal structure and its response to external forces
- Interactions among particles and resulting aggregates and flocculants
- Temperature

The difficulty of predicting the rheology of such a system is apparent and a result a lack of knowledge of the detailed structure and the nature of forces exerted by molecules or particles. However, its behavior can be characterized. It is also apparent that solder paste is not an elastic material, nor is it a pure viscous material. Viscoelasticity best describes the behavior of solder paste. The characterization of viscoelasticity and fundamental theories are covered in the literature.<sup>1,10</sup>

The common methods used to transfer solder paste consistently and accurately onto the intended solder pads include mesh screen printing, metal mask stencil printing, pneumatic dot and line dispensing, and positive displacement dispensing. Figures 5.31 and 5.32 illustrate the flow behavior of a dispensing paste and a printing paste, respectively.<sup>1</sup> The paste possessing a low yield point and very slight plastic behavior is found most suitable for dispensing applications, and a moderate yield point and thixotropy are generally associated with the printing paste. Table 5.6 lists typical viscosity and metal load percentages for dispensing and printing application techniques.



**Figure 5.31** Flow curve of dispensing paste.



**Figure 5.32** Flow curve of printing paste.

The size distribution of particles suitable for solder paste ranges from 45 to 74  $\mu\text{m}$  in diameter, corresponding to  $-200/+325$  mesh, are compatible with the printing standard of 0.050- to 0.25-in pitch land patterns, as well as with dispensing up to 20 gauge. For finer-pitch applications, smaller than 0.025-in pitch or 20 gauge, solder powder smaller than 45  $\mu\text{m}$  in diameter is needed.<sup>11</sup>

The printing thickness is another factor. Although the thicker paste deposit may impart a “better” joint, the maximum paste thickness for 0.050-, 0.025-,

and 0.012-in pitch land patterns are generally limited to 0.015, 0.008, and 0.004 in, respectively.

### 5.3.10 Formulation

As an example, a typical RMA solder-paste formula may contain 10 to 15 ingredients that provide various intended functions as shown in Table 5.7. The formula may appear to be straightforward. However, designing a viable product capable of delivering all the desired performance characteristics is complex and requires understanding the technologies.

**TABLE 5.7 Ingredients of Typical RMA Solder Paste**

Ingredient	Function
Rosin	Rosin system for designated softening point, acid number, thermal stability, fluxing activation, tackiness
Nonhalogen activator	Activator system for accomplishing fluxing action over a wide range of temperatures, rheology
Solvent	Solvent system to accommodate solubility, rheology, temperature compatibility, chemical compatibility
Binder	Providing compatible viscosity, rheology, tackiness
Fluxing modifier	Stabilizing and modifying flux
Rheology modifier	Contributing to targeted rheology

The following thinking steps are one route to take in developing a product:

1. Define performance objective.
2. Utilize fundamental technologies.
3. Select raw materials.
4. Understand and anticipate potential synergistic or antagonistic interactions between ingredients.
5. Balance performance parameters.
6. Fine-tune the formula to meet designated specifications.
7. Develop production process.
8. Produce consistent product.

A product involves many performance parameters, and some of them are trade-offs. For example, a high metal content is beneficial to solder joint volume and reduced voids and residue, yet it makes the paste more prone to drying and difficult to apply. A high-viscosity paste may improve flow control against temperature, but it causes the paste to be difficult to apply. Using

highly active fluxing chemicals may improve solderability in some cases, but their use may leave a more corrosive residue. In such cases, improving the solderability by selecting the proper ingredients without the use of highly active fluxing chemicals is the essence of technology. It should be noted that increasing the flux content does not always improve solderability in terms of wetting or the elimination of solder balling.

After the product has been designed, developing a reproducible process for making the paste with consistent characteristics is equally important. It is not an exaggeration, but an indication of the importance of the role of the process, to state that the identical composition formula can produce different results when the process is allowed to vary.

The design of water-soluble and no-clean products follows the same principle, but specific chemical ingredients differ.

### 5.3.11 Design and use of solder paste for system reliability

With the versatility of components and the vast variation in their solderability, it is tempting to formulate a flux chemistry with high activity. It is also convenient to incorporate the halide-containing organic ingredients to enhance the activity without adversely affecting the test results in the content of ionic species. This is because organic halides can be very effective fluxing agents in a very low dosage, thus relieving the level of elaboration (skills) in formulation technology. In addition, in various chemical makeups, low-dosage halides may be able to pass the “standard” tests. It is a well established fact that, among the chemical families, mobile halides are the most reactive species toward metals that make up the circuitry. Thus, their use should be discouraged.

Finer powder obviously facilitates the fine-pitch deposition via printing or dispensing. Undesirably, the paste with finer powder results in higher demand in the content, as well as in the activity of flux, and is more often prone to solder balling during reflow. Finer powder is also associated with higher cost.

Thus, it is always advantageous to use the coarsest powder that is allowable by a flux/vehicle system for achieving the printability and dispensability so that the reduced cost and proper flux activity can be obtained.

As the large or heavy array packages are incorporated in the assembly, the disparity of heat transfer is heightened. In those cases, increasing the temperature has indeed accommodated most reflow results. However, from a reliability standpoint, the approach may not be sound when considering the advent of heat-sensitive components, more complex PCB design, and increasingly versatile components contained in an assembly.

Reflow profiles based on slower heating and cooler temperature will be more in sync with today’s complex assemblies, minimizing in-process heat-induced damage as well as the level of residual stress, which may cause problems such as PBGA package cracking, board warpage, and board delamination. These three areas affect not only the production floor first-pass defect rate and yield but also the long-term performance of the assembly.

The principles of design and use of solder paste—mild flux, coarse powder, and low-temperature reflow profile—work in tandem, toward achieving the highest system reliability.

### 5.3.12 Quality assurance tests

Tests to assure the properties and performance of a solder paste can be grouped into five parts: paste, vehicle, powder, reflow, and post reflow. Table 5.8 summarizes the tests in each of the five parts.<sup>1</sup>

## 5.4 Soldering Methodology

### 5.4.1 Types

The commercially available reflow methods include conduction, infrared, vapor phase, hot gas, convection, induction, resistance, and laser. Each of these reflow methods has its unique features and merits in cost, performance, or operational convenience. For localized and fast heating, laser excels over other methods, with hot air in second place. For uniformity of temperature, vapor phase ranks first. For versatility, volume, and economy, convection and infrared are the choices. Conduction heating, however, is a convenience for low-volume and hybrid assembly. For conductive components requiring fast heating and high-temperature soldering, induction heating meets the requirement. Table 5.9 summarizes the strength and limitations of each method.

### 5.4.2 Reactions and interactions

During soldering, a series of reactions and interactions occur in sequence or in parallel. These can be chemical or physical in nature in conjunction with heat transfer. The mechanism behind fluxing is often viewed as the reduction of metal oxides. Yet, in many situations, chemical erosion and dissolution of oxides and other foreign elements act as the primary fluxing mechanisms. Using a more complex fluxing process in solder paste as an example, the primary steps are represented by the flowchart in Fig. 5.33.

### 5.4.3 Process parameters

With the prevalence of infrared and convection reflow, a few more words about furnace profile and furnace operating parameters are pertinent. It should be stressed that the reflow is a dynamic heating process in that the condition of the workpiece is constantly changing as it travels through the furnace in a relatively short reflow time. The momentary temperature that the workpiece experiences determines the reflow condition; therefore, the reflow results.

It is ultimately important to establish a correlation between the set temperature of a given furnace, the measured temperature of the workpiece at each specified belt speed, and the soldering performance. The resulting correlation between soldering performance and temperature setting or profile provides a “workable range” for the assembly.

**TABLE 5.8 Summary of Quality Assurance Tests for Solder Paste**

Paste
Appearance
Metal content and flux-vehicle percentage
Density
Viscosity
Viscosity versus shear rate
Cold slump
Hot slump
Molten flow
Tack time
Dryability
Dispensability
Printability
Shelf stability
Storage, handling, and safety
Flux/vehicle
Water extract resistivity
Copper mirror corrosion
Chloride and bromide
Acid Number
Infrared spectrum fingerprint and other spectroscopies
Solder powder
Alloy composition
Particle size, sieve
Particle size distribution, sedigraph
Particle shape
Particle surface condition
Dross
Melting range
Reflow
Solder ball
Solderability
Exposure time
Soldering dynamics
Post reflow
Cleanliness, resistivity of solvent extract
Surface insulation resistance, before and after cleaning
Solder joint appearance
Solder voids
Joint strength
Power cycling
Temperature cycling
Vibration test
Simulated aging
Thermal shock

Under mass reflow operation, both heating and cooling steps are important to the end results. It is generally understood that the heating and cooling rates of reflow or soldering process essentially contribute to the compositional fluctuation of the solder joint. This is particularly true when there are significant levels of metallurgical reactions occurring between the Sn/Pb solder and substrate metals. In the meantime, the cooling rate is expected to be responsible for the evolution of the microstructure.



TABLE 5.9 Outline of Benefits and Limitations of Reflow Methods

Reflow method	Benefits	Limitations
Conduction	Low equipment capital, rapid temperature changeover, visibility during reflow	Planar surface and single-side attachment requirement, limited surface area
Infrared	High throughput, versatile temperature profiling and processing parameters, easier zone separation	Mass, geometry dependence
Vapor phase condensation	Uniform temperature, geometry independence, high throughput, consistent reflow profile	Difficult to change temperature, temperature limitation, relatively high operating cost
Hot gas	Low cost, fast heating rate, localized heating	Temperature control, low throughput
Convection	High throughput, versatility	Slower heating, higher demand for flux activity
Induction	Fast heating rate, high temperature capacity	Applicability to nonmagnetic metal parts only
Laser	Localized heating with high intensity, short reflow time, superior solder joint, package crack prevention	High equipment capital, specialized paste requirement, limit in mass soldering
Focused infrared	Localized heating, suitable for rework and repair	Sequential heating, limit in mass soldering
White beam	Localized heating, suitable for rework and repair	Sequential heating, limit in mass soldering
Vertical reflow	Floor space saving, maintenance of desired throughput	Often more costly

The key process parameters that affect the production yield as well as the integrity of solder joints include the following:

- Preheating temperature
- Preheating time
- Peak temperature
- Dwell time at peak temperature
- Cooling rate

It should be stressed that the reflow in a furnace (infrared or convection) is a dynamic heating process in that the conditions of the workpiece are constantly changing as it travels through the furnace in a relatively short reflow time. The momentary temperature that the workpiece experiences determines the reflow conditions and therefore the reflow result.

Figure 5.34 illustrates a simulated reflow profile comprising three stages of heating:

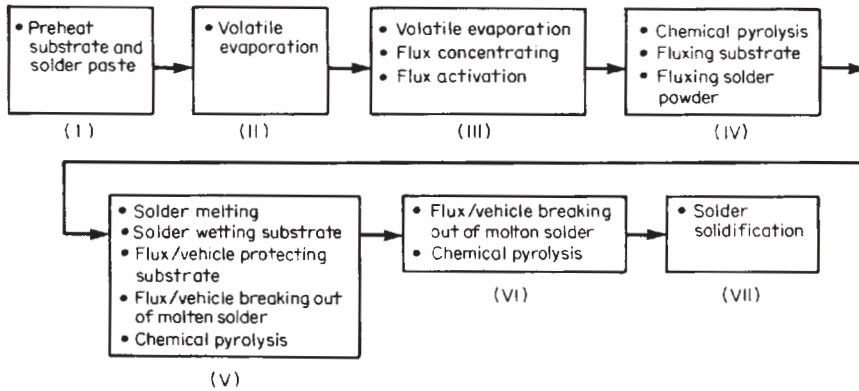


Figure 5.33 Flow chart of reflow dynamics.

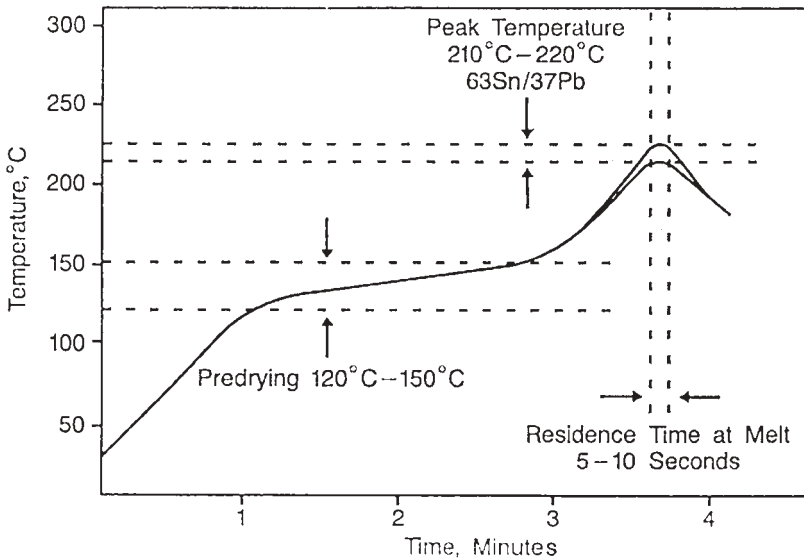


Figure 5.34 Reflow profile comprising three stages of heating.

1. Natural warm-up
2. Preheating/soaking
3. Spike and reflow

In the natural heating stage, the heating rate of reflow profiles being used in the industry falls in the range of 2 to 4°C. The parameters of the preheating/soaking stage are important to the reflow results. The desirable preheating rate is less than 1°C/s. During soldering dynamics, the heating process contributes not only to the effectiveness of wetting but also to the extent of

metallurgical reactions between solder and the substrates to which the solder interfaces, particularly the peak temperature and the dwell time at the temperature above the liquidus of the solder.

Several events occur during this stage, as shown in steps (2) and (4) of the flow chart (Fig. 5.33). These include temperature set to fit the specific flux activation temperature of the chemical system of the paste and the time at heat to fit the constitutional makeup of the paste. Inadequate preheating often causes a spattering problem that manifests itself as discrete solder balls. Too high a temperature or too long a time at the elevated temperature can result in insufficient fluxing and/or overdecomposition of organic, causing solder balling or hard-to-clean residue (if the no-clean route is adopted). The recommended general conditions for the second stage are 120 to 150°C for a duration of 45 to 150 sec. The third stage is to spike quickly to the peak reflow temperature at a rate of 1.0 to 4.0°C/s. The purpose of temperature spiking is to minimize the exposure time of the organic system to high temperature, thus avoiding charring or overheating. Another important characteristic is the dwell time at the peak temperature. The rule of thumb in setting the peak temperature is 20 to 50°C above the liquidus or melting temperature; e.g., for the eutectic Sn/Pb composition, the range of peak temperatures is 203 to 233°C.

The wetting ability is directly related to the dwell time at the specific temperature in the proper temperature range and to the specific temperature being set. Other conditions being equal, the longer the dwell time, the more wetting is expected—but only to a certain extent; the same trend applies at higher temperatures. However, as the peak temperature increases or the dwell time is prolonged, the extent of the formation of intermetallic compounds also increases. An excessive amount of intermetallics can be detrimental to long-term solder-joint integrity. Peak temperature and dwell time should be set to reach a balance between good wetting and to expel any non-solder (organics) ingredients from the molten solder before it solidifies, thus minimizing void formation.

For a given system, the cooling rate is directly associated with the resulting microstructure, which in turn affects the mechanical behavior of solder joints.<sup>2</sup>

It was found that the microstructural variation and corresponding failure mechanisms of solder joints that were made under various reflow temperature profiles are extremely complex. Nonetheless, some correlation between the cooling rate and the basic properties can be obtained.

The copper/solder/copper system is a good example, because it is still the most common material combination electronics assemblies. In this system, 63 Sn/37Pb solder joins copper pads (coated or uncoated) on the printed circuit board with the Sn/Pb coated copper leads of IC components.

For the tinned Cu-63Sn/37Pb-tinned Cu assembly, the reflowed solder joints are cooled in five different manners that deliver four cooling rates—0.1°C/sec, 1.0°C/sec, 50°C/sec, and 230°C/sec, respectively, as measured above 100°C. The fifth cooling mode was conducted in a two-step cooling, resulting an uneven cooling with an average cooling rate of 12°C/sec. Each of the five cooling modes produced a different development of microstructure of solder joint.<sup>2</sup>

#### 5.4.4 Reflow temperature profile

The reflow temperature profile, representing the relationship of temperature and time during the reflow process, depends not only on the parameter settings but also on the capability and flexibility of equipment. Specifically, the instantaneous temperature conditions that a workpiece experiences are determined by

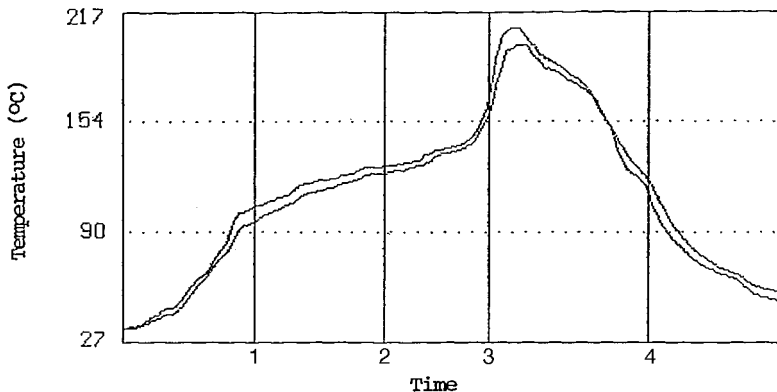
- Temperature settings to all zone controllers
- Ambient temperature
- Mass per board
- Total mass in the heating chamber (load)
- Efficiency of heat supply and heat transfer

For furnace-type reflow process, two profiles are taken to illustrate the effect of temperature profile on the reflow results.

Figures 5.35 and 5.36 show the actual temperature profiles of a convection oven, first with a relatively lower preheat temperature, as shown in Fig. 5.35, and then a higher preheat temperature, as shown in Fig. 5.36. The importance of the compatibility of solder paste chemistry and the assembly system with the reflow temperature profile can be easily demonstrated. For instance, if the solder paste and the assembly require the temperature profile of Fig. 5.35, performing reflow under the temperature profile of Fig. 5.36 may give rise to the following phenomena:

- Deficiency of flux, resulting in solder balls
- Overheating of organics, resulting in cleaning difficulty for processes that are designed to include a cleaning step

On the other hand, if the paste is designed for the higher preheat temperature and/or assembly requires additional heat, using the lower preheat temperature profile can produce the following phenomena:



**Figure 5.35** Convection reflow profile with lower-temperature preheating.

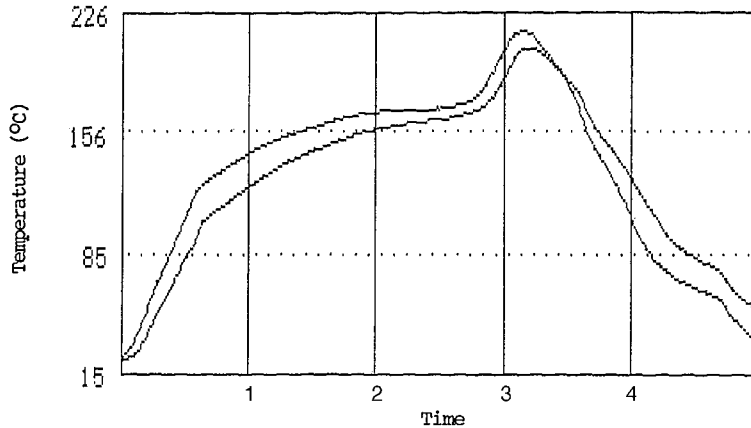


Figure 5.36 Convection reflow profile with higher-temperature preheating.

- Uneven soldering, resulting in cold solder joints
- An excessive amount of residue remaining or non-dry residue from no-clean paste

The temperature profile with boosted preheating conditions, as shown in Fig. 5.36 is most useful for the assembly that is densely populated with components with a large disparity in mass.

Depending on the type of conveyORIZED furnace, the mass of the assembly and the degree of loading, the major operating parameters to be monitored for effective reflow are the belt speed and the temperature settings of individual zones. The relationship between temperature settings and belt speed; increasing belt speed decreases the resulting peak temperature while other conditions are equal, as shown in Fig. 5.37. Because the required peak temperature is set at 20 to 50°C above the melting temperature of a solder alloy, the working range of peak temperature is always fixed. For every temperature profile, a relationship between peak temperature and belt speed can be

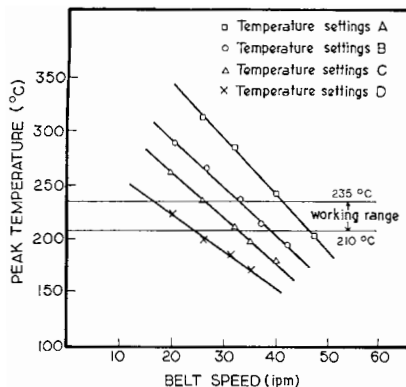


Figure 5.37 Reflow oven belt speed vs. peak temperature.

established, and usable range of belt speeds as depicted in Fig. 5.37 can be obtained.

#### 5.4.5 Effects of reflow profile

The reflow profile used for surface mount manufacturing has a direct bearing on manufacturing yield, solder-joint integrity, and the reliability of the assembly. Specific areas that are affected by reflow profile are listed below. Each area may be affected, to a different degree, by one or more of the three heating stages.

- Temperature distribution across the assembly
- Plastic IC package cracking
- Solder balling
- Solder beading
- Wetting ability
- Residue cleanability
- Residue appearance and characteristics
- Solder joint voids
- Metallurgical reaction between solder and substrate surface
- Microstructure of solder joints
- Board warpage
- Residual stress level of the assembly

**5.4.5.1 Uniformity of temperature distribution.** In a normal reflow environment, temperature differential across the assembly is inevitable. This results from the large disparity in mass and in the characteristics of the components coupled with the relatively short total reflow time (the entire cycle lasts only several minutes). A large temperature differential causes uneven soldering, resulting in localized cold joints or overheated joints. These problematic joints may contribute to manufacturing defects or jeopardize the long-term integrity of the solder joints under service conditions if they are not detected as manufacturing defects and corrected.

For a given oven, the rate of natural warm-up (in °C/sec) and the intended preheat temperature and time are the main factors that control temperature uniformity across the assembly. A slower heating rate in the warm-up state is desired to reach a more uniform board temperature distribution.

**5.4.5.2 Plastic IC package cracking.** Along with factors such as die size, the moisture sensitivity of the molding compound, and its thickness, reflow profile plays an important role in causing or preventing plastic IC package cracks. When the IC package (e.g., BGA, QFP, SOIC) absorbs a certain level of mois-

ture during storage, handling, or transit (without proper dry pack), the absorbed moisture may cause package cracking during reflow. Setting a proper reflow profile can mitigate the cracking problem; the heating rate from ambient temperature to 140 to 150°C is most critical.<sup>2</sup>

**5.4.5.3 Solder balling.** Elevated temperatures and excessive time at those temperatures during the warm-up and preheating stages can result in inadequate fluxing activity or insufficient protection of solder spheres in the paste, causing solder balling. In addition to the quality of solder paste, the presence of solder balls may be essentially related to the compatibility between the paste and the reflow profile. On the other hand, inadequate preheating or heating too fast may cause spattering, as evidenced by random solder balls. The two heating stages preceding the spike/reflow zone are primarily responsible for this phenomenon.

**5.4.5.4 Solder beading.** Solder beading refers to the occurrence of large solder balls (usually larger than 0.005 in [0.13 mm] in diameter) that are always associated with small and low-clearance passive components (capacitors and resistors). This problem will occur even when the paste may otherwise perform perfectly, i.e., free of solder balls at all other locations (components) on the board and with good wetting. The trouble with solder beading is that it may occur in most or all board assemblies, rendering the first-time yield to nearly zero. The current remedy on the production floor is to manually remove the beads.

The formation of solder beads near or under capacitors and resistors is largely attributed to paste flow into the underside of the component body between two terminations aided by capillary effect. As this portion of paste melts during reflow, it becomes isolated away from the main solder on the wettable solder pads, forming large discrete solder beads. With other factors, reflow profile is a contributor to this phenomenon. The practice of adopting a slower preheating rate and a lower reflow peak temperature can reduce solder beading. However, if the reflow profile is at its optimum, and the problem still persists, a new paste with a strengthened chemistry is the solution.

**5.4.5.5 Wettability.** The temperature setting and time spent in both preheating and spike/reflow affect wettability. However, each stage works by a separate mechanism. In the preheating stage, the range of temperature and the time spent in this range directly affect the activity of flux. Wettability, in turn, is affected by the fluxing action. However, in the spike/reflow zone, wetting on the “cleaned” surface is influenced by the peak temperature because of the intrinsic wetting ability of molten solder alloy. This ability increases on a wettable substrate with higher temperature. With all other conditions being equal, a longer dwell time can, to a limited degree, further enhance wetting. Modification of the spike/reflow zone may sometimes solve a minor wetting problem.

**5.4.5.6 Cleanability.** In the case of solder paste that is designed to be cleaned, particularly water cleaned, excessive heat may make it difficult for the residue to be removed, rendering a normal cleaning process ineffective. In this case, all stages of the reflow profile can be contributors.

**5.4.5.7 Residue appearance and characteristics.** The importance of the compatibility of the solder paste's chemical composition with the reflow profile can be readily demonstrated when using a no-clean soldering process. For instance, if the paste is reflowed with a temperature profile below the heat requirement, a higher amount of residue than expected will remain. In addition, the characteristics of that residue may range from being tacky to ionically active.

**5.4.5.8 Solder joint voids.** Incomplete outgassing (gases entrapped in the solder joint) is the main cause of voiding. In addition to design factors, the compatibility between the reflow profile and the chemical makeup of solder paste is important. There should also be sufficient dwell time in the molten state (above 183°C for 63Sn/37Pb) to ensure that the gases have enough time to separate and escape from the molten solder.

#### 5.4.6 Optimal profile

The heat transfer from the surrounding hot air to the various components on the board, such as leaded packages, array packages, and discretes, differs during the process such that a thermal equilibrium hardly exists. This disparity can be compensated for by either setting a reflow profile with a higher heat supply rate and higher temperature or one with a slower heating rate and lower temperature. On most manufacturing lines, unfortunately, a reflow profile with a higher heating rate and higher temperature is often used.

This disparity in the heat transfer may be heightened as large or heavy array packages are incorporated. Although increasing the temperature has accommodated most reflow results, the approach will not work well with heat-sensitive elements or with PCBs that contain increasingly versatile components.

The initial warm-up state plays a far more influential role in the quality and reliability of assembled boards than was first thought. An initial heating rate at less than 1°C/sec in conjunction with the heating rate for the rest of profile at not more than 3°C/sec is considered most beneficial and is recommended. Under SMT environments, the small degree of reduction in heating rate would not be a bottleneck for production throughput. By using the slower rate in the warm-up and preheating stages prior to reaching 183°C, the peak temperature can be maintained in the range of 210 to 215°C, in contrast to 215 to 230°C. The total dwell time above the liquidus temperature (183°C) falls in the range of 30 to 65 sec.

Reflow profiles based on slower heating rates and cooler temperatures will be more in line with today's complex assemblies, minimizing in-process heat exposure as well as residual stress.



### 5.4.7 Laser soldering<sup>1</sup>

Two types of laser have been applied to solder reflow—carbon dioxide (CO<sub>2</sub>) and neodymium-doped yttrium-aluminum-garnet (Nd:YAG). Both generate radiation in the infrared region with wavelengths of about 10.6 μm from the CO<sub>2</sub> laser and 1.06 μm for the YAG laser. The wavelength of 1.06 μm is more effectively absorbed by metal than by ceramics and plastics; the wavelength of 10.6 μm is normally reflected by conductive surfaces (metals) and absorbed by organics.

The main attributes of laser soldering are short-duration heating and high-intensity radiation, which can be focused onto a spot as small as 0.002 in (0.050 mm) in diameter. With these inherent attributes, laser reflow is expected to

- Provide highly localized heat to prevent damage to heat-sensitive components and to prevent cracking of plastic IC packages
- Provide highly localized heat to serve as the second or third reflow tool for assemblies demanding multiple-step reflow
- Require short reflow time
- Minimize intermetallic compound formation
- Minimize leaching problems
- Generate fine-grain structure of solder
- Reduce stress buildup in solder joint
- Minimize undesirable voids in solder joint

With these attributes in mind, laser soldering is particularly beneficial to soldering densely packed regions, where local solder joints can be made without affecting the adjacent parts, to soldering surface-mount devices on printed-circuit boards having heat sinks or heat pipes, and to soldering multi-layer boards. In addition, it also provides sequential flexibility of soldering different components and enhances the high-temperature performance of adhesives used for mounting surface-mount devices.

With respect to reflow time, laser soldering can be accomplished in less than 1 sec, normally in the range of 10 to 800 ms. The laser can be applied to point-to-point connections through pulsation as well as to line-to-line connections via continuous laser beam scan.

The fine-pitch flat-pack devices have been connected to printed wiring boards using YAG continuous laser beam scans on each side of the package. Both the use of prebumped solder pads and the direct application of solder paste are feasible. In directly reflowing solder paste, although using spattering and heat absorption problems have been observed, they are not incurable. To eliminate these problems, the preheating and predrying step is necessary. Location of laser beam impingement is another factor. In addition, compatible properties of solder paste have been designed to accommodate fast heating in relation to fluxing and paste consistency, coupled with the proper design of the equipment and its settings.

In using the laser, another concern is energy absorption by the printed-circuit boards, which leads to board damage. This is considered to have been corrected by switching from CO<sub>2</sub> laser to YAG laser. Due to the wavelength difference, the energy absorption by polymers can be minimized. Lish<sup>11</sup> has found that sometimes complications may occur. In assembling multilayer polyimide boards by using laser as a second-step reflow, burning was found in the board while it was moving under the laser. The burning was traced to the color pigments contained in the adhesive, which was used for attaching heat sinks. The problem was eliminated by using colorless pigment in the adhesive. This is another clear demonstration that a consideration of all materials in the reflow process is needed.

Regarding the resulting solder joint, a fine-grain microstructure and the formation of significantly reduced intermetallic compounds at the copper and solder (63Sn/37Pb) interface have been observed when laser soldering was used as compared to other reflow methods.<sup>12</sup> Stress buildup in the solder joint due to the difference in thermal expansion coefficients between the materials on both sides of the solder joint is expected when the reflow method requires the whole assembly to be exposed to the soldering temperature. Localized heating and exposure of short duration by using a laser are expected to generate less stress in the joint for the assemblies having materials of different thermal expansion coefficients.

## 5.4.8 Controlled-atmosphere soldering<sup>13</sup>

**5.4.8.1 Principle.** Based on its function, the atmosphere may be considered as either protective or reactive. A protective atmosphere normally is inert toward a specific soldering material under specific conditions, and a reactive atmosphere may involve either an oxidizing or a reducing function toward the subject system.

Broadly, chemicals that can provide oxidizing or reducing potential in relation to the specific metal-oxide system, and that can generate significant vapor pressure at an operating temperature, are expected to contribute to the functional nature of the total atmosphere.

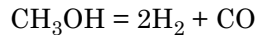
Following is a list of some commonly used atmospheres. Their corresponding nominal compositions are summarized in Table 5.10.

- Dry air
- Nitrogen
- Hydrogen
- Nitrogen-hydrogen blends at different ratios
- Dissociated ammonia
- Exothermic gas
- Nitrogen dopants at different concentrations

TABLE 5.10 Percentage Composition of Atmosphere Gases

Atmosphere	Carbon dioxide (CO <sub>2</sub> )	Oxygen (O <sub>2</sub> )	Carbon monoxide (CO)	Hydrogen (H <sub>2</sub> )	Methane (CH <sub>4</sub> )	Nitrogen (N <sub>2</sub> )	Trace
Air	—	21.0	—	—	—	78.1	0.9
Nitrogen	—	—	—	—	—	99.8–100	0–0–0.2
Hydrogen	—	—	—	99.8–100	—	—	0–0–0.2
Dissociated methanol	—	—	33.3	66.7	—	—	—
Dissociated ammonia	—	—	—	75.0	—	25.0	—
Exothermic gas (air/gas = 6/1)	5.0	—	10.0	14.0	1.0	70.0	—
Endothermic gas (air/gas = 2.4/1)	—	—	20.0	38.0	0.5	41.5	—

The thermal cracking of methanol essentially yields hydrogen and carbon monoxide at high temperatures, as represented by the chemical equation,



At low temperatures (below 800°C), side reactions may occur, leading to the formation of H<sub>2</sub>, CH<sub>4</sub>, CO<sub>2</sub>, and C.

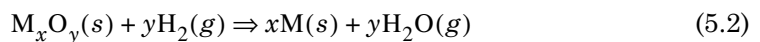
Each component of the atmosphere gases may function as oxidant or as reducing agent, depending on the temperature and its oxidation-reduction potential relative to that of the materials involved. Among the components of common atmosphere gases, oxygen, water vapor, and carbon dioxide normally serve as oxidants to most metals and metal oxides, and hydrogen and carbon monoxide serve as reducing agents. The ratio of oxidant content to reducing-agent content, in relation to that ratio at equilibrium, indicates whether the resulting atmosphere is oxidizing or reducing.

During soldering, the reactions and interactions of chemicals in the solder paste and between chemicals and the metal surface can be quite complex. In simple terms, the mechanisms may include evaporation, pyrolysis, oxidation, and reduction. The generalized oxidation and reduction reaction can be expressed as follows:

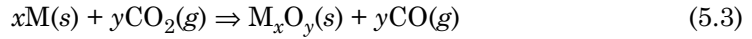
To obtain the thermodynamic equilibrium constant  $K$  for each of the preceding reactions,



$$K_1 = \frac{a_{\text{M}_x\text{O}_y}}{a_{\text{M}}^x a_{\text{O}_2}^y}$$



$$K_2 = \frac{a_M^x a_{H_2O}^y}{a_{M_xO_y} a_{H_2}^y}$$



$$K_3 = \frac{a_{M_xO_y} a_{CO}^y}{a_M^x a_{CO_2}^y}$$

Assuming that the compositions of solids remain constant and the gases behave ideally,

$$K_1 = \frac{1}{P_{O_2}^y} \quad K_2 = \frac{P_{H_2O}^y}{P_{H_2}^y} \quad K_3 = \frac{P_{CO}^y}{P_{CO_2}^y}$$

where  $a$  represents the activities of the individual reactants as well as the products of reactions (5.1), (5.2), and (5.3), and  $P_{H_2O}$ ,  $P_{H_2}$ ,  $P_{CO}$ , and  $P_{CO_2}$  represent the partial pressure of  $H_2O$ ,  $H_2$ ,  $CO$ , and  $CO_2$ , respectively.

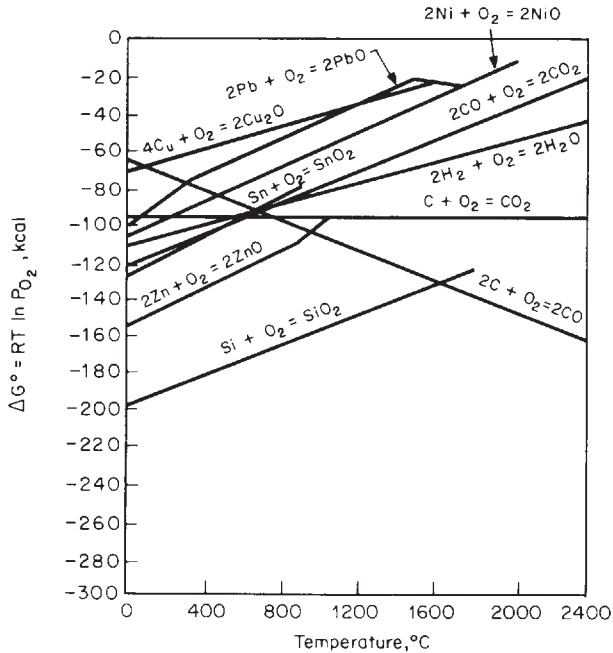
By introducing the relationship between the free energy  $\Delta G^0$  and the equilibrium constant,

$$\Delta G^0 = -RT \ln K$$

it is shown that reactions (5.1), (5.2), and (5.3) can proceed in the forward or reverse direction, depending on the temperature and the ratios of  $P_{H_2O}$ ,  $P_{H_2}$ ,  $P_{CO}$ , and  $P_{CO_2}$ .

Figure 5.38 shows the standard free energy of formation for some metal-metal oxide systems and  $CO/CO_2$ ,  $H_2O/H_2$ , and  $CO_2/C$  atmospheres as a function of temperature. Assuming that they are under equilibrium condition and at a soldering temperature of  $250^\circ\text{C}$ , lead oxide and copper oxide can be reduced by hydrogen. However, hydrogen is not effective for tin oxides until the temperature reaches  $600^\circ\text{C}$ . Equation (5.2) also indicates that the presence of too much water vapor in the furnace atmosphere will cause oxidation to certain metals. The partial pressure of water vapor should therefore be maintained at a constant and defined value.

At a given atmosphere, composition, and dew point, the gas flow rate and the flow pattern of the exhaust systems in the furnace are also important factors in soldering performance. The gas flow rate should be high enough to avoid localized atmosphere buildup as a result of local reactions. To achieve the best performance and cost results, the required flow rate is determined by the characteristics of the solder paste being used, the furnace belt speed, loading pattern, belt width, and other furnace parameters. The exhaust efficiency



**Figure 5.38** Standard free energy of formation for metal-metal oxide systems.

and its flow pattern, in combination with the flow rate, dominate the removal of volatile components generated from the pyrolysis and evaporation of chemicals in solder material, which in turn affects solderability.

It should be noted that a complete burn-out process is normally not feasible at the eutectic tin-lead or tin-lead-silver soldering temperature when using a solder paste. To obtain good solderability and quality solder joints, a metallic continuity at the interfaces between solder and substrate must be formed during soldering. When using a solder paste, a complete coalescence of solder-powder particles has to occur in synchronization with the development of metallic continuity at the interfaces. At the soldering temperature, the atmosphere surrounding the workpiece protects or interacts with the surface of substrates, the solder alloys, and the chemical ingredients in the flux-vehicle system. These interactions determine the chemical and physical phenomena in terms of volatilization, thermal decomposition, and surface-interfacial tension. A controlled atmosphere is expected to deliver a more consistent soldering process.

In addition to consistency, the inert or reactive atmospheres possess further merits. These include

- Solderability enhancement
- Solderability uniformity
- Minimal solder balling

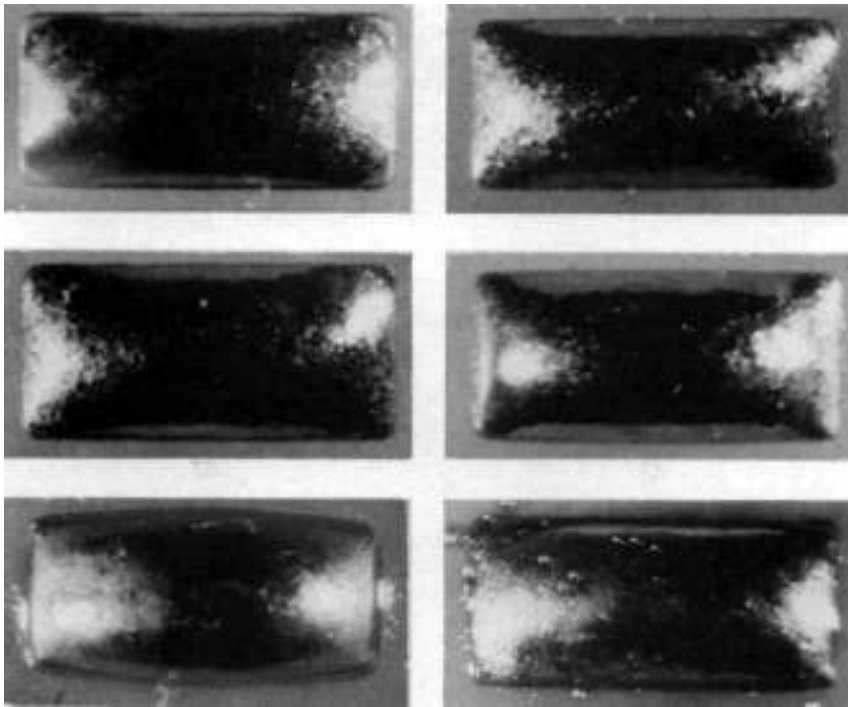
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- Irregular residue charring prevention
- Polymer-based board discoloration prevention
- Wider process window
- Overall quality and yield improvement

The inert and reactive atmospheres are expected to facilitate conventional fluxing efficiency during soldering. It should be noted, however, that performance results rely greatly on the specific atmospheric composition and its compatibility with the solder material, substrate, and chemicals incorporated in the system, which must also be compatible with the soldering temperature profile. Figure 5.39 shows that the solderability under  $N_2$  atmosphere is significantly improved, as solder balls that are formed under ambient air conditions are eliminated.

5.4.9 Process parameters<sup>15-18</sup>

**5.4.9.1 Gas flow rate.** The gas flow rate required to achieve a specific level of oxygen in the dynamic state of the reflow oven is largely controlled by the type

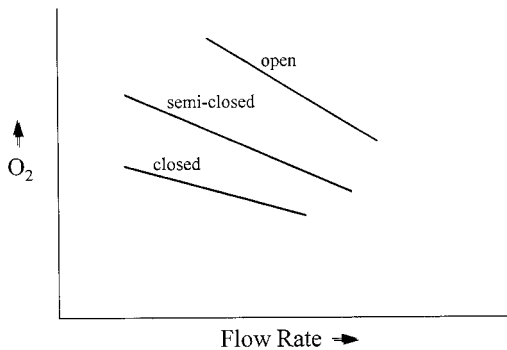


**Figure 5.39** Solderability performance of solder paste under  $N_2$  atmosphere vs. ambient air, reflowed under (a)  $N_2$ , (b)  $95N_2/5H_2$ , (c)  $85N_2/15H_2$ , (d)  $70N_2/30H_2$ , (e)  $H_2$ , and (f) ambient air.

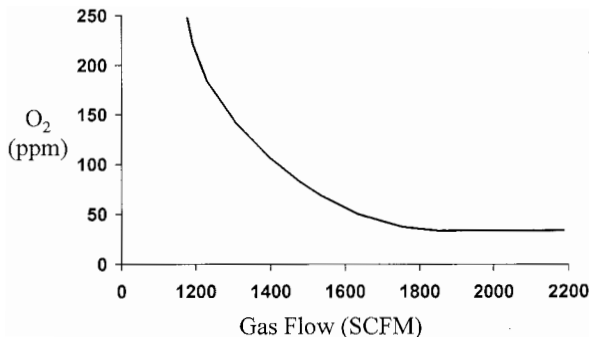
of oven, categorized as closed-system, semi-closed system, or open system. The relationship of the flow rate versus oxygen level within one type of oven and the relationship among the different types of oven are summarized in Fig. 5.40. For a given oven, the required flow rate increases when the allowable oxygen level is lowered. At a given flow rate, when the air tightness in oven construction is reduced, the achievable oxygen level will be higher.

As expected, for a given reflow system, the oxygen level is inversely related to gas flow rate as shown in Fig. 5.41. The gas flow rate also affects the temperature distribution and temperature uniformity of assembly. Figure 5.42 exhibits the temperature gradient between the component PLCC-84 and the board surface, indicating that a higher gas flow rate reduces the temperature gradient of an assembly.<sup>14</sup> However, the downside of using high flow rate goes to the higher gas consumption, therefore increasing cost. The cost impact may be mitigated when the design of oven is capable of internal gas recirculation in an efficient fashion.

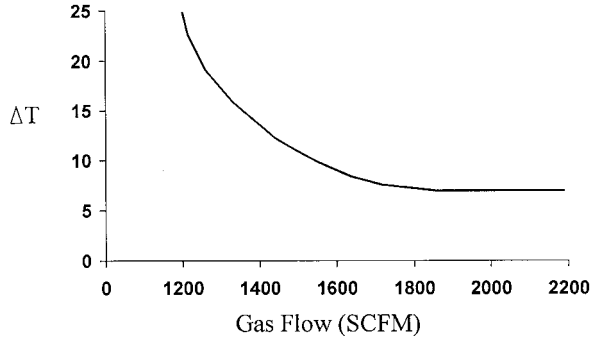
**5.4.9.2 Humidity and water vapor pressure.** Water vapor pressure inside the soldering govern can be contributed from the following:



**Figure 5.40** Oxygen level of three types of reflow oven.



**Figure 5.41** N<sub>2</sub> flow rate vs. oxygen level.



**Figure 5.42** Temperature gradient vs. flow rate.

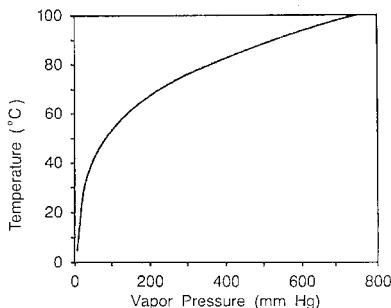
- The composition and purity of atmosphere
- The reaction product of flux/vehicle chemical system with metal substrates
- The moisture release from the assembly including components and board
- The ambient humidity

Because water vapor is essentially oxidizing to metal substrates that are to be joined by soldering, its partial pressure in the oven affects the overall function of the atmosphere.

The partial pressure of water vapor in an atmosphere gas is conveniently expressed as dew point—that is, the temperature at which condensation of water vapor in air takes place. The dew point can be measured by a hygrometer or dewpointer by means of fog chamber, chilled mirror aluminum oxide technique. The relationship of dew point with the vapor pressure is shown in Figs. 5.43 and 5.44. The relative humidity, RH, is related to the actual vapor pressure of water (or represented by dew point),  $P_w$ , and the saturated vapor pressure at the prevailing ambient temperature,  $P_s$ , as follows:

$$RH = \frac{P_w}{P_s}$$

The purity of incoming gas in terms of moisture is normally monitored by measuring the dew point.



**Figure 5.43** Dew point vs. vapor pressure (high).



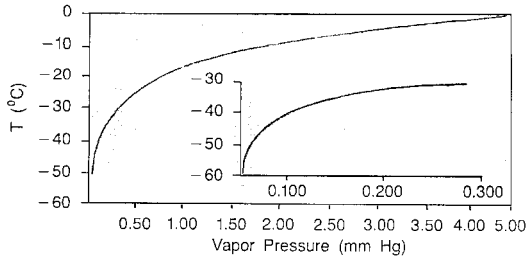


Figure 5.44 Dew point vs. vapor pressure (low).

**5.4.9.3 Belt speed.** For an evenly spaced loading on the belt, the belt speed not only determines the throughput, it also affects other operating parameters that can alter the soldering results. As examples, the parameters that are affected by the change of belt speed include

- Peak temperature—at fixed temperature settings, increasing the belt speed results in the decrease of peak temperature.
- Atmosphere composition—while other conditions are equal, the change of belt speed may alter the oxygen level (including moisture content).

**5.4.9.4 Temperature.** The operating temperature or temperature profile is an integral part of soldering process. It affects the physical activity and chemical reaction of the organic system in solder paste or flux. The operating temperature, particularly peak temperature, changes the wetting ability of molten solder on the metal substrate; wetting ability generally increases with increasing temperature. Chemical reactions and thermal decompositions respond to the rising temperature and the temperature profile.

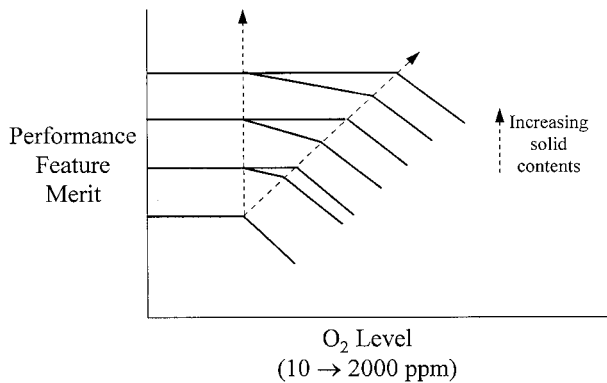
**5.4.9.5 Oxygen level.** Various studies have focused on the application of no-clean processes and on the determination of the maximum allowable oxygen level for using nitrogen-based no-clean soldering process in solder paste reflow and wave soldering.

Each study was performed with a specific solder paste and flux or with a selected series of paste and flux. Tests were conducted with specific equipment under a designated process. In view of the continued introduction of new equipment and the diversity of processes coupled with the versatility of solder paste and flux compositions, the test results are expected to represent the specific system (paste, oven, process, assembly) and at best to provide a guideline reference point. For example, a solder paste from the Vendor I to be used with Process A may require a maximum 20-ppm oxygen level to obtain good solderability, freedom from gross solder-ball effects, and acceptable after-soldering residue. To achieve similar results, the same paste to be used with Process B

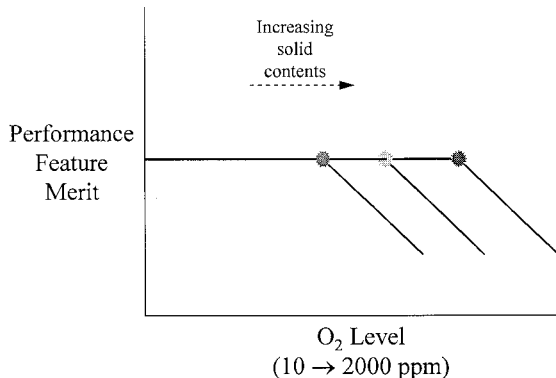
may need a maximum of 300 ppm oxygen. The same could be true for a different paste used in the same process.

The precise oxygen level requirement for a no-clean soldering is impractical to pin down. Instead, the general principle and trends in the relationship between the performance feature and the allowable maximum oxygen level can be derived. Figure 5.45 presents the trend of performance feature merit in relation to oxygen level for a series of solder paste containing various levels of solid contents. For a given performance feature, Fig. 5.46 shows the trend of the effect of solid content in no-clean paste on oxygen level requirement during reflow soldering. The performance feature denotes the solderability or the reduction in solder balling.

For convenience, solderability may be monitored by measuring wetting time, wetting force, meniscus rise, or wetting angle, or by visual wetting quality. The series of the curves represents the generic groupings of no-clean solder paste or flux by the level of solid contents. This is, however, based on the fact that the solid content possesses a good flux system. As shown in Fig. 5.45,



**Figure 5.45** Dew point vs. vapor pressure (high).



**Figure 5.46** Solid content in paste vs. performance feature.

the performance trend in the increasing solderability and decreasing solder balling is enhanced when the solid content increases, and, at a given solid content beyond a threshold of oxygen level, the performance will significantly drop. It should be noted that increasing solid content creates an increasing amount of after-soldering residue. The required oxygen level may fall in any place within the region, depending on other factors as discussed above. For a given level of performance, the allowable oxygen level will be relieved as the solid content increases, as depicted in Fig. 5.46.

**5.4.9.6 Optimal O<sub>2</sub> level.** In general, with levels higher than 2,000 ppm O<sub>2</sub>, the effect of nitrogen may hardly be detected. Below 20 ppm O<sub>2</sub>, the process will become difficult to control and, needless to say, too costly. For a given oven and process, the required O<sub>2</sub> level is essentially controlled by the chemistry and makeup of the solder paste. For example, a solder paste from Supplier A may require a maximum level of 800 ppm O<sub>2</sub> to obtain the desirable results (good wetting, no solder balls, etc.). To achieve similar results, solder paste from Supplier B may need a maximum of 200 ppm O<sub>2</sub>. In practice, O<sub>2</sub> levels in the range of 20 to 2,000 ppm should be able to accommodate most applications.

Soldering under nitrogen poses two additional demands: more stringent process control and higher operating cost. However, its potential effects on solderability, heat transfer, PCB materials, and process window may bring benefits in mounting large-area and heavy BGAs as well as in connecting small and delicate CSPs onto complex PCBs.

#### 5.4.10 Profile temperature measurement

At a steady state, and when properly used, the thermocouple can readily measure true temperature. However, in a dynamic environment, such as the reflow process, the response efficiency of a thermocouple may affect the accuracy of the temperature measurement.

To accurately measure the temperature on a solid surface (or a point), the thermocouple must be in a direct and firm contact with the surface to be measured. It is common to use attaching materials such as a high-temperature solder and high-temperature adhesive or Kapton<sup>®</sup> tape. The application of any of these materials inevitably introduces an additional mass into the contact area, which works as a thermal sink. The additional mass may skew temperature readings, resulting in an understanding readout. For cases in which the tip of the thermocouple is broken away from the surface contact, the oven air temperature, rather than the intended surface temperature, may be recorded. Thus, the amount of solder or adhesive used should be as small as possible, minimizing the barrier in heat transfer and thermal mass.

A more desirable technique, however, is to make contact without the use of extraneous material. One system (by Saunders Technology) has demonstrated its usefulness and performance. Its design features include a unique thermocouple probe mounted in a sliding ball joint and a detachable clamp. The probe serves as the temperature sensor, composed of a thermocouple hermeti-

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cally sealed in a nominally 0.020-in (0.51-mm) diameter stainless steel sheath. The sliding ball joint provides the positioning flexibility to reach a specific location on the board. Each clamp secures one or two probe sensors to the edge of the board, and multiple clamps can be used for simultaneously monitoring the temperature at selected locations. The probe can be readily connected to most commercially available profilers for data processing. A firm contact that can accommodate any possible shift during the temperature excursion is obviously a crucial element. A small-diameter probe tip also offers flexibility in access.

A low-mass, direct, firm contact, without the need for extraneous attachment material, provides a way to meet the criteria for achieving accurate temperature measurement.

## 5.5 Solderability<sup>1</sup>

### 5.5.1 Definition

Solderability, in a broad sense, is the ability of achieve a clean metallic surface on substrates to be joined during a dynamic heating process so that a good wetting of molten solder on the surface of the substrates can be formed. When using solder paste, solderability requires the additional ability to achieve a clean metallic surface on the solder powder so that a complete coalescence of the solder powder particles can be obtained. Solderability relies on the fluxing efficiency provided by fluxes or the solder paste and on the quality of the surface of the substrate.

### 5.5.2 Substrates

Among the common substrates to be soldered, the demand placed on the flux for good wetting depends on the intrinsic wettability of substrates. The wettability is ranked in the order of Sn, Sn/Pb > Cu > Ag/Pd, Ag/Pt > Ni. Solderability may change as a result of variations in the quality of the substrate surface. Therefore, using the same flux system may not produce the same results if the substrate surface condition varies.

The demand on flux strength also depends on the reflow temperature and techniques. Convection reflow operation under ambient atmosphere requires more fluxes than vapor-phase, hot air, or laser reflow. Inert or reducing atmospheres can modify the reflow performance in terms of wetting as well as residue characteristics.

### 5.5.3 Wetting phenomena

Good wetting is visualized as the formation of a smooth, uniform, and continuous solder coating on the surface of solder pads without dewetting, nonwetting, or pinholes.

*Dewetting* is the phenomenon of molten solder receding after it has coated the surface, leaving a rough and irregular surface with thick mounds of solder connected by thin solder film. In dewetting, the substrate surface is not ex-

posed. *Nonwetting* is defined as the phenomenon of molten solder not adhering to the substrate surface, thereby leaving the substrate surface exposed. The molten solder in such a case tends to form a high wetting angle ( $>90^\circ$ ).

#### 5.5.4 Solderability of components

Component leads are commonly made of copper, copper alloys, Alloy-42 (41 to 42.5 percent nickel, the balance iron), and Kovar (2 percent nickel, 17 percent cobalt, 53 percent iron, 1 percent others).

The leads are normally coated with a coating composition in a range of tin-lead alloys by means of aqueous plating or molten solder dipping. The plating process provides more uniform thickness, which is often porous, and molten solder dip produces a thicker and denser fused coating.

Ideally, device leads are pretinned to assure good solderability. But in practice, after tinning, most components undergo operations such as lead forming, encapsulation, or burn-in. These steps can degrade the surface quality of the lead significantly and, therefore, affect solderability. In summary, the solderability of tinned leads depends on the following factors:

- Composition of base lead materials
- Composition of coating
- Surface finish and condition of coating
- Age of coating
- Storage of coating
- Thickness of coating

A coating thickness of 0.0003 in (7.6  $\mu\text{m}$ ) is most prevalent, and a thin coating is often associated with poor solderability. Nonetheless, the ideal coating thickness depends on several practical factors.

The solderability of coated leads, under various shelf times and conditions, is a concern. Assuming that the coating is intact, this concern can be viewed from two aspects: (1) how is the solderability affected by the surface degradation due to oxidation or contamination during shelf time, and (2) how is the solderability affected by the interaction between lead material and tin-lead coating during shelf time or a treatment such as a burn-in test. The surface oxidation of tin-lead alloys normally is not an unsolvable problem, because the fluxing is able to take care of it.

The formation of copper-tin intermetallic compounds at the interface of copper-based leads and tin-based coating ( $\text{Cu}_3\text{Sn}$ ,  $\text{Cu}_6\text{Sn}_5$ ) can readily occur, although it would be extremely sluggish at room temperature, as indicated in the Cu-Sn phase diagram. With this interaction, the tin content at the coating-lead interface will be consumed gradually, resulting in solderability degradation. The consumption rate depends on temperature and time. In this regard, Alloy-42 and Kovar leads are expected to do better than copper leads with high-tin coating. However, high-tin coating normally provides better wettability.

It should be noted that, for leads coated by molten solder dip, copper-tin intermetallic compounds (namely,  $\text{Cu}_6\text{Sn}_5$ ) can be formed rapidly during coating. However, because of its intactness, the molten solder dip coating is expected to be relatively more stable during storage than electroplating. Leads made of Alloy-42 and Kovar may experience deterioration with age as a result of moisture permeation through the porous crystalline structure.

In either case, the degradation of the coating is driven by a kinetically controlled process and depends on other practical and environmental factors. Therefore, to assure the quality of the coated surface of leads, the shelf time and storage temperature must be minimized. Using freshly coated leads is ideal.

Component leads can also be coated with palladium. The compatibility of solder paste and reflow profile determines the solderability.<sup>2</sup>

### 5.5.5 Surface finish of PCBs

Section 5.8.5 provides a description of PCB surface finish characteristics.

## 5.6 Cleaning

### 5.6.1 Principle and options

After soldering, the residue surrounding the solder joint can be either removed (cleaned) or left as is. The decision about whether to clean up the residue depends on the property and activity of the residue and the reliability desired under specified service conditions.

Residual water-soluble chemistry left on or around solder joints after soldering need to be cleaned. The residue from liquid flux can be a simple system composed of a small amount of organic acid, high boiling solvents, surfactant, and reaction products. Residues from paste may contain a mixture of ingredients, including polar organics, nonpolar organics, ionic salts, and metal salts.

Key steps in a typical cleaning process are prerinse → wash → rinse → final rinse → drying. The parameters that affect the cleaning efficiency include

- Temperature of water
- Spray pressure
- Spray angle
- Wash time
- Flow rate
- Agitation aid

When a compromise among the parameters is needed, higher temperature and higher spray pressure often play more important roles than the flow rate and spray angle. In addition, mechanical agitation aids in dislodging foreign matter from the board and the clearance between components and the board. Ultrasonic agitation and centrifugal energy can provide effective mechanical

force. Centrifugal force that is directly proportional to the square of angular velocity and its parallel direction to the board assist the cleaning operation. Ultrasonic cleaning employs cavitation, defined as the implosion of microscopic vapor cavities within the solution, which is induced by the changing pressure differentials in the ultrasonic field. The pressure differentials are created by the exchange between negative and positive pressure in a liquid region. When the liquid with negative pressure is created, its boiling point drops, and many small vapor bubbles are formed. As the pressure changes to positive, the small bubbles implode with great violence. The mechanical wave is generated by high-frequency electrical energy released by a transducer. The cavitation phenomenon provides mechanical agitation and a scrubbing effect.

The effectiveness of ultrasonic cleaning depends on the cavitation intensity, which in turn is controlled by the magnitude of power or pulse width and by dissolved air in the solution. The effect of dissolved air has been illustrated and tested, indicating that it can act as an acoustical screen and energy absorber.<sup>19</sup> A deaeration step is needed to remove the air so as to obtain the true vaporous cavitation. It is suggested that the high audible noise level (a pronounced hissing sound) and minimal visible bubbles in solution, coupled with violent surface activity, are signs of ultrasonic efficiency. It is also suggested that the temperature of the solution is a factor in ultrasonic efficiency. The desirable temperature is approximately in the range of 80 to 98 percent of the boiling point of the solution.

Because of the concern that ultrasonics may damage wire bonding or other chip components, compatible process parameters are to be identified. Some guidelines are proposed as follows:

- Power of ultrasonic cleaner: 30 W per liter
- Ultrasonic range: 30 to 66 kHz
- Cleaning time: 3 min/cycle for five cycles (not to exceed a total of 15 min)

Because of the narrow gap (clearance) between the components and the board in surface mount assemblies, ensuring cleanliness has always been a problem. To solve the dilemma of cleaning process efficiency and the accuracy of cleanliness measurements, a functional test—the surface insulation resistance test—provides an indication of the cleanliness level for a given assembly. Cleaning efficiency on the production line, however, should rely on the established process and its stringent control, and the tests merely provide confirmation.

## 5.7 Fine-Pitch Application

In addition to the selection of solder paste, major factors contributing to the the results in printing solder paste include stencil thickness versus aperture design, stencil aperture versus land pattern, and stencil selection.

### 5.7.1 Stencil thickness vs. aperture design

When printing solder paste, proper design of the relative dimensions of stencil thickness and stencil aperture is required to achieve a balance between the printing resolution and the proper amount of solder deposit, thereby avoiding starved solder joints and pad bridging. For a selected stencil thickness, too small a stencil aperture width leads to open joints or starved joints. Too large an aperture width causes pad bridging. Table 5.11 provides guidelines for designing stencil thickness in relation to aperture.

**TABLE 5.11 Guideline of Stencil Thickness vs. Aperture Width**

Component lead pitch		Aperture width		Maximum stencil thickness	
inch	mm	inch	mm	inch	mm
0.050	1.26	0.023	0.58	0.0140	0.35
0.025	0.63	0.012	0.30	0.0075	0.19
0.020	0.50	0.010	0.25	0.0063	0.16
0.015	0.38	0.007	0.18	0.0043	0.11
0.008	0.20	0.004	0.10	0.0025	0.06

### 5.7.2 Stencil aperture design vs. land pattern

To make solder joints using a one-pass printing process, the stencil thickness must be selected such that it transfers a sufficient amount of paste onto the non-fine-pitch solder pads while avoiding an excessive paste deposits on the fine-pitch pads. Several options are available to achieve the deposition of a proper amount of solder paste on the land pattern to accommodate a mix of sizes of solder pads. These are enumerated below.

1. *Step-down stencil.* This is commonly achieved by chemically etching the non-fine-pitch pattern area from one side of the stencil while etching the step-down area for the fine-pitch pattern on the other side during a double-sided etch process. Alternatively, step-down area is etched into one foil, and a non-fine pitch pattern is etched into the other foil, after which the two foils are registered and glued together.

The practical step gradient is 0.002 in (0.05 mm), and some common combinations are

0.008 in (0.20 mm) for non-fine pitch

0.006 in (0.10 mm) for fine pitch

or

0.006 in (0.15 mm) for non-fine pitch

0.004 in (0.15 mm) for fine pitch



2. *Uniform reduction on four sides of apertures.* The dimensions of the fine-pitch aperture on stencil are reduced by 10 to 30 percent in relation to those of the land pattern. This reduces the amount of paste deposition on fine pitch land pattern and also provides some room for printing misregistration and paste slump, if any.
3. *Staggered print.* The opening in the stencil is only one-half the length of the solder pad and arranged in an alternating manner as shown in Fig. 5.47. For tin-lead coated solder pads, when the paste starts to melt during reflow, the molten solder is expected to flow to the other half of the pad, making the coverage complete. With a bare copper or nickel surface, the molten solder may not flow out to cover areas where the paste has not been printed.
4. *Length or width reduction.* The dimensions of the stencil opening are reduced along the length or width by 10–30 percent in relation to that of solder pads, achieving the reduction of the amount of paste deposited.
5. *Other shapes.* The stencil openings are made with selected shapes, such as a triangle or teardrop, to achieve the reduced solder paste deposition on fine pitch pattern.
6. *Compromise stencil thickness.* Instead of using the specific thickness that is considered to be the most suitable for a specific land pattern, select a thickness that is practical to both fine-pitch and non-fine-pitch patterns. For example,

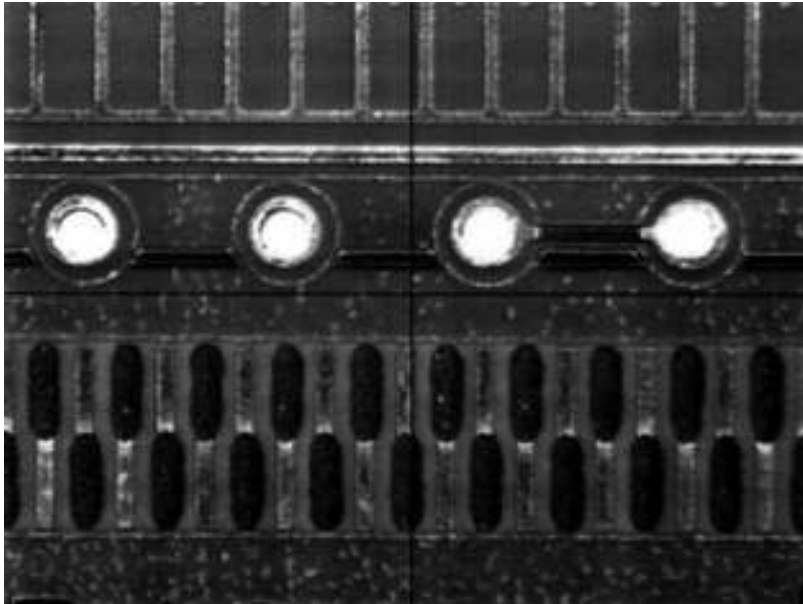


Figure 5.47 Staggered print.

Land pattern pitch combinations		Compromise stencil thickness	
mil	mm	inch	mm
50 and 25	1.26 and 0.63	0.007–0.008	0.18–0.20
50 and 20	1.26 and 0.50	0.006–0.007	0.15–0.18

### 5.7.3 Stencil selection

The performance of stencils is primarily driven by the foil metal and the process used to create the printing pattern. Currently, five types of stencil materials are commercially available—brass, stainless steel, molybdenum, Alloy-42, and electroformed nickel. The processes making the stencils may involve chemical etching, laser cutting, electropolishing, electroplating, and electroforming. Each type of foil or fabricating process possesses inherent merits and limitations. The key performance of a stencil is assessed in terms the straightness of the vertical wall, wall smoothness, and dimensional precision. In addition, durability, chemical resistance, fine opening capability, and cost are also important factors.

Table 5.12 compares various stencil materials, and Table 5.13 summarizes the relative performance characteristics of stencil-making techniques.<sup>2</sup>

**TABLE 5.12 Comparison of Stencil Materials in Key Performance Areas**

Performance	Brass	Stainless steel	Molybdenum	Alloy-42	Ni (electroforming)
Mechanical strength	unfavorable	favorable	favorable	favorable	favorable
Chemical resistance	unfavorable	favorable	unfavorable	favorable	favorable
Etchability	favorable	favorable	favorable	favorable	N/A
Sheet stock availability	favorable	favorable	unfavorable	favorable	N/A
Cost	favorable	less favorable	unfavorable	less favorable	N/A
Fine pitch (openings) capability	favorable	may need electropolishing	favorable	may need electropolishing	favorable
Unique feature	lowest cost	durable	self-lubricating, smooth wall	–	finest opening

## 5.8 Soldering-Related Issues<sup>2</sup>

### 5.8.1 Intermetallics vs. solder joint formation

Intermetallic compounds have often been observed at or near the solder/substrate interface as well as in the interior of solder joints. Metallurgically, an intermetallic compound is one type of intermediate phase that is a solid solu-

TABLE 5.13 Comparison of Techniques in Building Stencils

Techniques	Characteristics	Capabilities or features
Chemical etching	Most established process, sensitivity of fine pitch capability to process and control, sensitivity of aperture size and vertical wall control	Versatile, economical
Laser cut	Grainy wall surface; sequential cut, not concurrent formation of openings; higher cost; difficulty in making step stencil	Fine pitch capability, no photo tools or resist needed
Electropolishing	Complementary step to produce smooth wall surface	Smooth wall surface
Ni-plating on aperture wall	Reducing aperture opening, smooth surface	Finer opening
Electroforming	Additive process via electrode position, concern about foil strength, difficulty in making step stencil, suitable for stencil thickness of 0.001 in to 0.012	Gasket effect minimizing bleedout, capability of producing very fine opening, no need for electropolishing

tion with intermediate ranges of composition. Intermetallic compounds form when two metal elements have a limited mutual solubility. These compounds possess a new composition of a certain stoichiometric ratio of the two elements.

The new compositions have a different crystal structure from those of their elemental components. The properties of the resulting intermetallic compounds also differ from component metals in that they exhibit reduced ductility, density, and conductivity. Tin or tin/lead solder is metallurgically active with most metals that are commonly used in electronics packaging and assembly. Various intermetallic compositions have been identified under the equilibrium condition between tin and substrate metals, such as Au, Ag, Cu, Pd, Ni, and Pt. Indium-based solders also interact with these substrate metals, often forming intermetallics. One should note that thermodynamically stable compounds may not always be present, and some intermetallics that do not appear in the equilibrium phase diagram have been identified in soldered systems.

Relating to electronics packaging and assembly, intermetallic compounds may come from one or more of the following processes and sources:

- Intermetallics are formed at the solder/substrate interface during soldering.
- Intermetallics are present in the interior of the solder joint as the inherent metallurgical phases of a given solder composition, such as 95Sn/5Sb and 96Sn/4Ag solder.
- Intermetallics are developed during a service life either along the interface and/or in the interior of the solder joint.

When solder comes in contact with a common metal substrate for a sufficient amount of time at a high enough temperature, intermetallic compounds

may form. Below a solder's liquidus temperature, formation is primarily a solid state diffusion process and thus depends to a great extent on temperature and time. While solder is in a molten state, the solubility of the element from substrate into molten solder accelerates the rate of intermetallic formation.

External factors such as the temperature of exposure and the time at the elevated temperature also affect the rate of intermetallic compound formation. Thus, solder reflow conditions such as peak temperature, and the total dwell time at elevated temperatures, influence the rate and extent of intermetallic growth. Also, while in storage or service, the exposure of the assembly is a factor for intermetallic growth in systems.

The thickness of growth between eutectic tin/lead and copper is proportional to the square root of time, coinciding with the diffusion-controlled kinetics. As temperature rises, the rate of formation increases, with the longer time promoting the process.

The composition of intermetallics at the interface may differ from those of the solder joint interior. Furthermore, the surface condition of the substrate affects the kinetics of intermetallic development. For example, the oxidized surface may show a delayed development of the intermetallic phases, making a thinner layer as compared with a clean surface for a given amount of time. Unlike high-tin-content solder, which tends to form intermetallic compounds with small crystal structures, high-lead-content solder forms high, needle-like crystals.

In brief, the extent of intermetallic formation, the composition of the compounds, and their morphology depend on intrinsic factors. These factors include the following:

- The metallurgical reactivity of a solder with a substrate
- Soldering (reflow) peak temperature
- Dwell time at peak temperature
- The surface condition of a substrate—clean versus oxidized
- The post-soldering storage and service conditions

Intermetallics at the interface can be beneficial or detrimental. Wetting on the substrate followed by the formation of a thin layer of intermetallics is the prevalent mechanism in making permanent solder bonds. However, adverse effects may occur if the intermetallic layer becomes too thick. Generally acceptable thickness falls in the range of 1 to 5  $\mu\text{m}$ .

The morphology, size, and distribution of intermetallics in solder determine their beneficial or detrimental effects on solder-joint integrity. If they possess the correct properties, the intermetallics in the interior of the solder joint (away from the interface) act as a strengthening phase. In contrast, large and needle-shaped compounds generally weaken the mechanical properties of a solder joint.

The formation of excessive intermetallic compounds has proven to be a frequent source of solder joint failure. Cracks are often initiated around the in-

terfacial area under stressful conditions when an unacceptable amount of intermetallic materials develop along the solder/substrate interface.

The adverse effect of intermetallic compounds on solder-joint integrity is believed to be attributed to the brittle nature and thermal expansion properties of such compounds, which may differ from the interior solder. The difference in thermal expansion contributes to a solder's internal stress development. In addition, excessive amounts of intermetallic compounds impair the solderability of some systems, depleting one element of the contact surface. For instance, tin depletion from tin/lead coating on copper leads causes the exposure of  $\text{Cu}_3\text{Sn}$  to oxidation, resulting in inconsistent and/or poor solderability of component leads. In this case, the interface area is composed of gradients with  $\text{Cu}_3\text{Sn}$  phase next to the copper substrate followed by  $\text{Cu}_6\text{Sn}_5$  phase and lead-rich phase away from the interface line. Also, excessive intermetallics render a dull, rough look to solder joints.

A precise bonding process for die attach involving in-situ formation of Cu-Sn intermetallics from vapor-deposited copper-tin multilayer has been introduced. The unique feature of this bonding process is its fluxless nature and its control of intermetallic thickness. The resulting joint is composed of uniformly distributed Sn and  $\text{Cu}_6\text{Sn}_5$  with a joint thickness of 4.5  $\mu\text{m}$ .

The role of intermetallics, beneficial or detrimental, is determined by the design of an assembly, the service conditions in relation to that design, and the control of the soldering process. Understanding the relationship among them is the key to making reliable solder joints.

### 5.8.2 Gold-plated substrates vs. solder joint formation<sup>2</sup>

Using gold (Au) as a surface coating to resist the oxidation of underlying metals in semiconductor packages and electronics assemblies is a routine practice. Common applications include gold plating on PCBs, gold-containing thick film circuitry on hybrids, soft gold (24 karat) wire bonding, and hard gold (cobalt or nickel gold) for edge fingers as connectors. However, many in the industry are concerned or uncertain about the full role gold plays in solder.

When a gold-coated substrate is in direct contact with an Sn/Pb solder, the Au combines with the Sn of the solder at a rapid rate as a result of the metallurgical affinity between Sn and Au, forming Au-Sn intermetallics. Gold-tin intermetallics can affect a solder's physical and mechanical properties and alter a solder joint's appearance and microstructure.

An Au concentration below 10 percent by weight in Sn/Pb solder slightly increases that solder's initial tensile strength. However, beyond 3 percent, a solder's shear strength slowly drops. Normally, its hardness increases with the addition of gold. This effect is enhanced as the Au content exceeds 7 percent. A solder's ductility is slowly reduced with Au concentrations below 7 percent by weight and then drops rapidly as the Au content exceeds 7 percent by weight.

Gold can affect a solder's ability to wet and spread. Although a 2 percent Au concentration has no effect on 63Sn/37Pb, concentrations above 2 percent re-

duce the solder's spreadability and fluidity. For copper plated with Au, a pure Au coating has shown better wetting and spread than alloy Au when soldering with 63Sn/37Pb under identical conditions.

The dissolution rate of Au in solder depends on temperature, time, and solder composition. Foreign elements (e.g., Au, In, and Zn) in Sn/Pb solder retard this dissolution. During a reflow process with a long heating time, the quick dissolution of Au in molten solder causes that solder to wet directly onto the base metal and not the gold coating.

Although one might expect gold's inert nature to provide a base metal with full protection, tests on the aging of gold-electroplated Cu indicate that the solderability as measured by wetting time degrades with aging at a temperature of 170°C. Solderability degrades from the following causes:

- Diffusion of atmospheric contaminants through the porous Au film results in the oxidation the base material.
- Diffusion of base metal reaches the surface through the coating. The diffusion rate is associated with the Au coating grain size, with smaller grain sizes favoring diffusion.

Gold dissolved in solder alters that solder's microstructure. As the Au content reaches 1 percent by weight, the characteristic needle-shaped phase found in eutectic solder becomes readily detectable in the microstructure. The amount of hard phase increases with elevated Au concentrations. At room temperature, the composition of these intermetallics is a mixture of AuSn<sub>4</sub> and Sn.

The incorporation of Au may or may not change a solder's physical properties. At concentrations below 10 percent by weight, Au does not significantly affect a solder's electrical or thermal conductivity.

Gold can lower a solder's solidus temperature and increase its liquidus temperature, thereby widening the paste range or creating a pasty range for eutectic solder. This affects a solder's application performance, particularly for solder interconnections. Lowering a solder's softening temperature changes its mechanical response to rising temperatures. A eutectic solder is required for applications demanding high solder fluidity, whereas assemblies with a wide gap to fill find solder with a wide pasty range preferable.

Overall, Au has the most pronounced effect on solder joints in the following areas:

- Fluidity
- Wettability and spread
- Mechanical properties
- Phase transition temperature
- Microstructure
- Appearance

An overly thick Au coating results in a higher Au concentration in solder and an increase in material cost. If the coating is too thin, the surface protection effectiveness may suffer. One should also take into account that the surface condition of Au, particularly its porosity, is equally important to surface protection. An optimal Au application balances surface intactness, concentration in solder after dissolution, and cost.

When a solder's Au content is excessive, the following mechanical and/or metallurgical phenomena may occur:

- Premature solder joint fracture due to embrittlement
- Void creation
- Microstructure coarsening

The upper limit of Au concentration is assessed to be 3 percent by weight. Above 3 percent, deleterious effects could occur in one or more of the aforementioned areas. The 3-percent limit cited here is only a guideline. As a rule, one should verify the effect of Au concentration in solder for its performance in a specific electronics package and assembly under a given set of conditions.

To ensure that Au concentrations do not exceed acceptable levels, industry standards call for Au removal immediately prior to soldering. The general guidelines for Au removal are as follows:

- A double tinning process of dynamic solder wave must be used for proper Au removal.
- An Au removal procedure is unnecessary for through-hole components intended for dip or wave soldering, provided that the Au on the leads is less than 0.0025 mm.
- For surface mount parts, Au must be removed from at least 95 percent of the surface to be soldered.

### 5.8.3 Solder-joint voids

Voiding is one of the adverse phenomena in solder-joint integrity and reliability. It is generally expected that a low volume of small, well dispersed voids has little effect on solder-joint integrity; however, high-volume or large-size voids can degrade the joint with respect to its electrical, thermal, or mechanical properties.

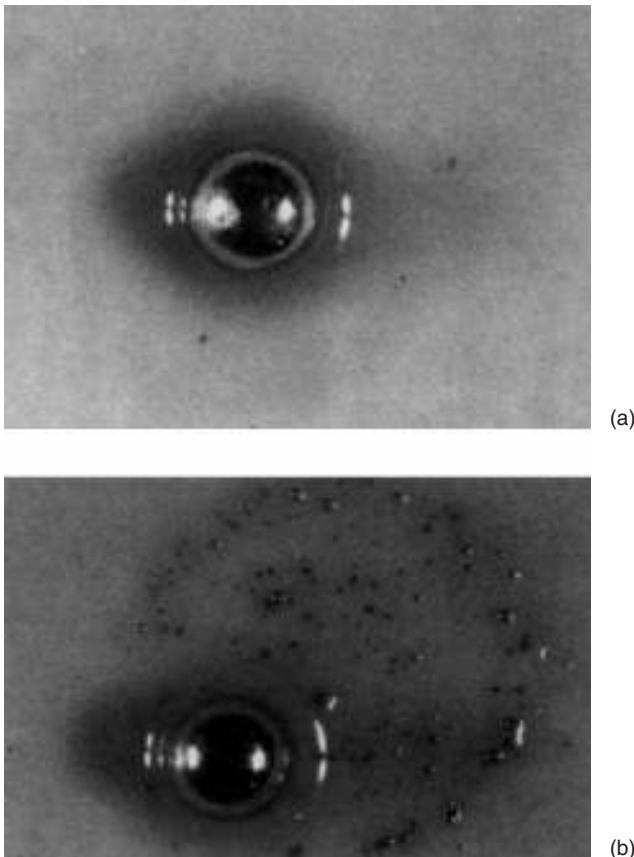
For solder joints made from solder paste, the flow characteristics and the thermal and physical properties of the vehicle-flux system, as well as the metal load, are important factors. To minimize voiding, the processing parameters and joint design should be optimized. These include the dosage of paste deposit, deposit thickness, joint configuration, reflow time, cooling rate, and wettability. The same paste could generate different voiding in size and concentration if used under varying conditions. A quality joint is, therefore, influenced equally by the solder-joint assembly process and the quality of the paste. Further discussion can be found in Ref. 2.

#### 5.8.4 Solder balling/beading

When using solder paste, solder balling in the reflow process is a common phenomenon. A continuous effort has been made through soldering process control, component and board quality assurance, and solder paste design to minimize the occurrence of solder balling.

The solder balling phenomenon can be defined as the situation that occurs when small spherical particles of various diameters are formed away from the main solder pool during reflow and do not coalesce with the solder pool after solidification, as shown in Fig. 5.48. Various manufacturing environments have revealed two distinct types of solder balling in terms of physical characteristics:

- A. Solder balling around any components and over the board
- B. Large solder balls associated with small and low-clearance passive components (e.g., 0805, 1206), with most of them being larger than 0.005 in (0.13 mm)



**Figure 5.48** Solder balling.



The type (A) solder balls normally can be removed during cleaning; type (B) solder beads, however, are difficult to remove using a normal cleaning process. With the implementation of a no-clean process, it is obviously desirable to avoid the occurrence of both types of solder balling. With the use of array packages (BGAs), solder balling also becomes more troublesome. In the presence of solder balls, the assembly may encounter the risk of electrical short when any solder balls become loose and mobile during service. Excessive solder balling may also deprive solder from making good solder joint fillet. In general, type A solder balls can be formed for different reasons. The following are the likely sources that should be considered:

- Solder paste with inefficient fluxing with respect to solder powder or substrate or reflow profile can result in discrete particles that do not coalesce, caused by either the paste design or subsequent paste degradation.
- Incompatible heating with respect to paste prior to solder melt (preheating or predry) can degrade the flux activity.
- Paste spattering caused by excessively rapid heating can result in the formation of discrete solder particles or aggregates outside the main solder pool.
- Solder paste that is contaminated with moisture or other high “energy” chemicals that promote spattering can produce solder balls.
- Solder paste that contains extra-fine solder particles that are carried away from the main solder by the organic portion (flux/vehicle) during heating can result in small solder balls.
- Interaction between solder paste and solder mask can cause the problem.

The appearance and distribution of solder balls often reveal the cause. Solder balls as a result of spattering are usually irregular and relatively large in size (larger than 20  $\mu\text{m}$  is not uncommon) and are scattered over a large area of the board; solder balls caused by fine powder in the paste often form a halo around the solder; ineffective or insufficient fluxing results in small solder balls that are scattered around the joint; and solder mask-related solder balls leave discoloration marks on the board.

Solder paste spattering during reflow can be caused by the following phenomena:

- Incompatibility between paste and reflow profile, such as excessively fast heating; high volatile content in the paste.
- The hygroscopicity of the paste; when the open time during assembly exceeds the capability of the paste or the paste is exposed to temperature and/or humidity beyond its tolerance level, the moisture absorbed by the paste can cause spattering.

To minimize solder balling during board assembly, several issues need to be addressed.

## 5.70 Chapter 5

- Selection of a solder paste that is able to deliver performance under the specific production conditions
- Understanding the characteristics of the solder paste selected
- Setup of the reflow process that best fits the solder paste selected
- Assurance of consistency and quality of the solder substrate, including boards and components
- Control of ambient conditions (temperature and humidity)
- Control of open time that the paste can accommodate
- Assurance of solder mask compatibility with the solder paste
- Assurance of a complete cure of the solder mask

For large solder beads associated with small passive components, formation is largely attributed to the paste slump and flow under the component body, between the two terminations, via capillary effect. The slump and flow dynamics can also be affected by the reflow temperature profile, the volume of paste, and component placement. To reduce the occurrence of these large solder beads, the following parameters are recommended for consideration:

- Solder paste rheology—minimizing paste slump
- Amount of solder paste deposit—avoiding excess paste
- Component placement—avoiding paste spread during placement
- Reflow profile—reducing preheating temperature exposure

## 5.8.5 PCB surface finish

For making sound interconnections, the characteristics and properties of the circuit board surface finish are as important as the component leads and termination.

Hot air solder leveled SnPb (HASL) has been used successfully as the surface finish for surface mount and mixed PCBs. As the need of a flat surface with uniform thickness becomes increasingly important to forming consistent and reliable fine-pitch solder joints, the HASL process often falls short. Alternatives to HASL include immersion Sn, electroplated SnPb (reflowed or non-reflowed), electroplated Au/Ni, electroless Au/electroless Ni, immersion Au/electroless Ni, immersion Pd, immersion Pb/electroless Ni, electroplated Sn-Ni alloy, and organic coating. When selecting an alternative surface finish for a PCB assembly, the key parameters to consider are solderability, ambient stability, high-temperature stability, suitability of the use as contact/switch surface, solder-joint integrity, wire bondability of assemblies that involve wire bonding, and cost.

**5.8.5.1 Basic process.** The three primary techniques to deposit metallic surface finish are electroplating, electroless plating, and immersion. Inherently, elec-

troplating utilizing electric current is capable of economically depositing thick coatings up to 0.000400 in, depending on metal and process parameters. Electroless plating, requiring the presence of a proper reducing agent in the plating bath, converts metal salts into metal and deposits them on the substrate. The immersion plating process, in the absence of electric current and reducing agent in the bath, deposits a new metal surface by replacing the base metal; plating stops when the surface of base metal is completely covered, so only a limited coating thickness can be obtained through the immersion process. For both electroless and immersion processes, the intricate chemistry and the control of kinetics are vital to the plating results. The chosen process parameters and chemistry, including pH and chemical ingredients, must be compatible with the solder mask and PCB materials.

**5.8.5.2 Metallic systems.** Available metallic surface finishes on copper traces include Sn, SnPb alloy, SnNi alloy, Au/Ni, Au/Pd, Pd/Ni, and Pd. The systems containing noble or semi-noble metals, such as Au/Ni, Au/Pd, Pd/Ni, and Pd/Cu, are capable of delivering a coating surface with uniform thickness. Those systems imparting a pure and clean surface also provide a wire-bondable substrate. In addition, wire bonding generally requires a thicker noble metal coating—more than 0.000020 in. A unique feature of the Au/Ni system is its stability under elevated temperature exposure during the assembly process as well as in subsequent service life. When in contact with a molten solder of SnPb, SnAg, or SnBi, surfaces coated with Sn and SnPb are normally associated with a better spreading and lower wetting angle than others. Of the metallic systems, those containing a Ni interlayer are expected to possess a more stable solder joint interface; in these systems, solder is expected to wet on Ni during reflow, because noble metals are readily dissolved in solder. The concentration and distribution of noble metals in solder need to be noted to prevent any adverse effect in solder joining integrity. For a phosphorus-containing plating bath, a balanced concentration of phosphorus in electroless Ni plating is essential. When the P content is too high, wettability suffers; when it is too low, thermal-stress resistance and adhesion strength are sacrificed.

Another characteristic important to solderability is the porosity of the surface. A thinner coating is more prone to porosity-related problems, but the surface density and texture can be controlled by the chemistry and kinetics.

**5.8.5.3 Organic coatings.** Benzotriazole has been widely recognized as an effective Cu, antitarnish, and antioxidation agent for decades. Its effectiveness, attributable to the formation of benzotriazole complex, is largely limited to ambient temperatures.

As the temperature rises, the protective function disintegrates. Azole derivatives such as imidazole (m.p. 90°C, b.p. 257°C) and benzimidazole (m.p. 170°C, b.p. 360°C) have been used to increase the stability under elevated temperatures. SMT assembly of mixed boards involves three stages of temperature ex-

cursion—reflow, adhesive curing, and wave soldering. The reflow step, however, is considered to be potentially the most harmful to the soundness of the organic coating, because it is the step that involves the highest temperature and longest exposure time.

Although the performance of an organic coating varies with the formula and process, the general behavior of organic coating falls within the following regimen:

- There is a need for compatible flux (generally more active flux).
- For mixed boards, there may be a need for more active flux in wave soldering.
- A thicker coating is more resistant to oxidation and temperature but may also demand more active flux.
- An organic coating needs to be employed as the last step of PCB fabrication.
- At temperatures higher than 70°C, the coating may degrade. However, the degradation may or may not affect solderability.
- The coating may be sensitive to PCB the prebaking process (e.g., 125°C for 1 to 24 hr).
- For no-clean chemistry, a N<sub>2</sub> atmosphere or higher solids content may be required in no-clean paste.
- The steam aging test is not applicable.
- It is not suitable for chip-on-board where wire bonding is required.

Nonetheless, when the fluxing activity and process are compatible, an organic coating can be a viable surface finish for PCBs. A bonus effect is that the bare copper appearance of the organic coated surface facilitates the visual inspection of peripheral solder fillets.

**5.8.5.4 Comparison of PCB surface finish systems.** Whatever its deficiencies may be, HASL provides the most solderable surface. However, comparing a metallic system with HASL, the latter subjects PCBs to higher temperatures (above 200°C), producing inevitable thermal stress in PCBs. Furthermore, HASL is not suitable for wire bonding.

To choose a valid replacement for HASL, many variables need to be assessed. Understanding the fundamentals behind each variable, in conjunction with setting proper priority of importance among these variables for a specific application, is the way to reach the best balanced solution.

When selecting an alternative surface finish for PCB assembly, the key parameters to consider are solderability, ambient stability, high temperature stability, suitable for use as a contact/switch surface, solder-joint integrity, and wire bondability for those assemblies that involve wire bonding, and cost.

Table 5.14 summarizes the relative performance of PCB surface finish systems.

TABLE 5.14 Relative Performance of PCB Surface Finishes

HASL	Au/Ni	Pd/Ni	Pd/Cu	Organic
<i>Pros:</i>				
Most solderable Uniform thickness	Uniform thickness Wire bondable Most stable T	Uniform thickness Wire bondable	Uniform thickness Wire bondable	Uniform thickness Low cost Easy inspection
<i>Cons:</i>				
Nonuniform thickness Potential IMC problem Unsuitable for COB PCB exposed to high temperatures	Higher cost	Higher cost	Higher cost (thicker coating)	Unsuitable for COB Flux and reflow process sensitive High T degradation Cu reaches upper limit in solder bath Required as a last board fabrica- tion step

## 5.9 Solder-Joint Appearance and Microstructure

### 5.9.1 Appearance

X-ray, laser thermal, and optical inspection techniques for solder-joint quality assurance have been developed extensively. Visual inspection is commonly used to verify solder-joint quality, and it is still required by military specifications. Thus, a few words are in order about the appearance of solder joints.

The factors affecting the solder-joint appearance, in terms of luster, texture, and intactness, are as follows:

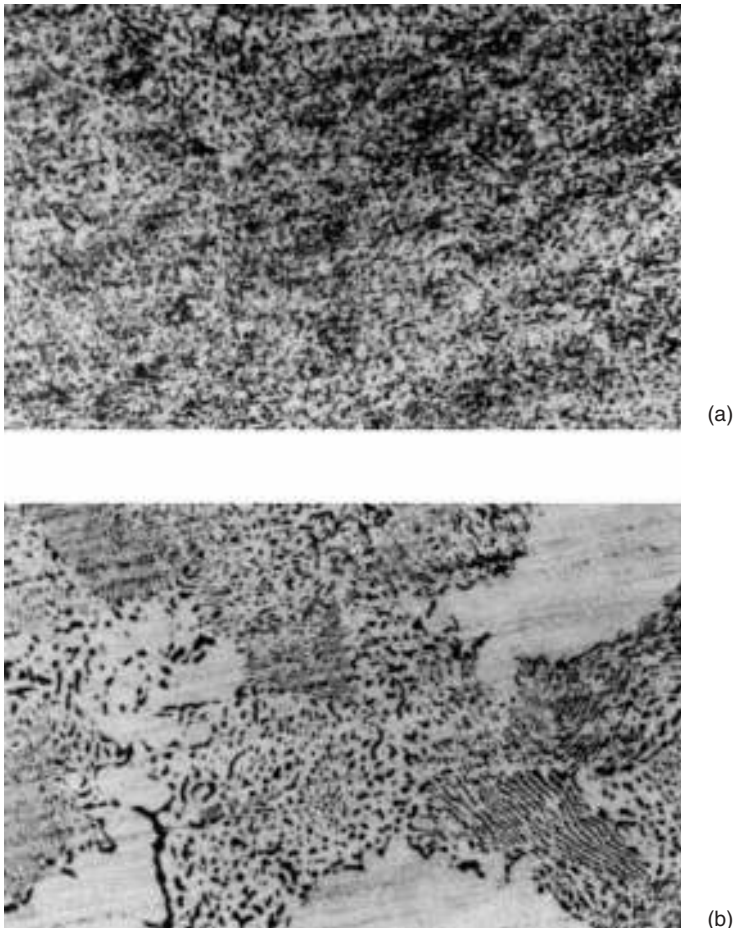
- Inherent alloy luster
- Inherent alloy texture
- Residue characteristics after paste reflow
- Degree of surface oxidation
- Completeness of solder powder coalescence
- Microstructure
- Mechanical disturbance during solidification
- Foreign impurities in the solder
- Phase segregation
- Cooling rate during solidification
- Subsequent heat excursion, including aging, temperature cycling, power cycling, and high-temperature storage

It is known that the process of solidification from melt is crucial to the microstructure development of an alloy, which, in turn, affects its appearance.

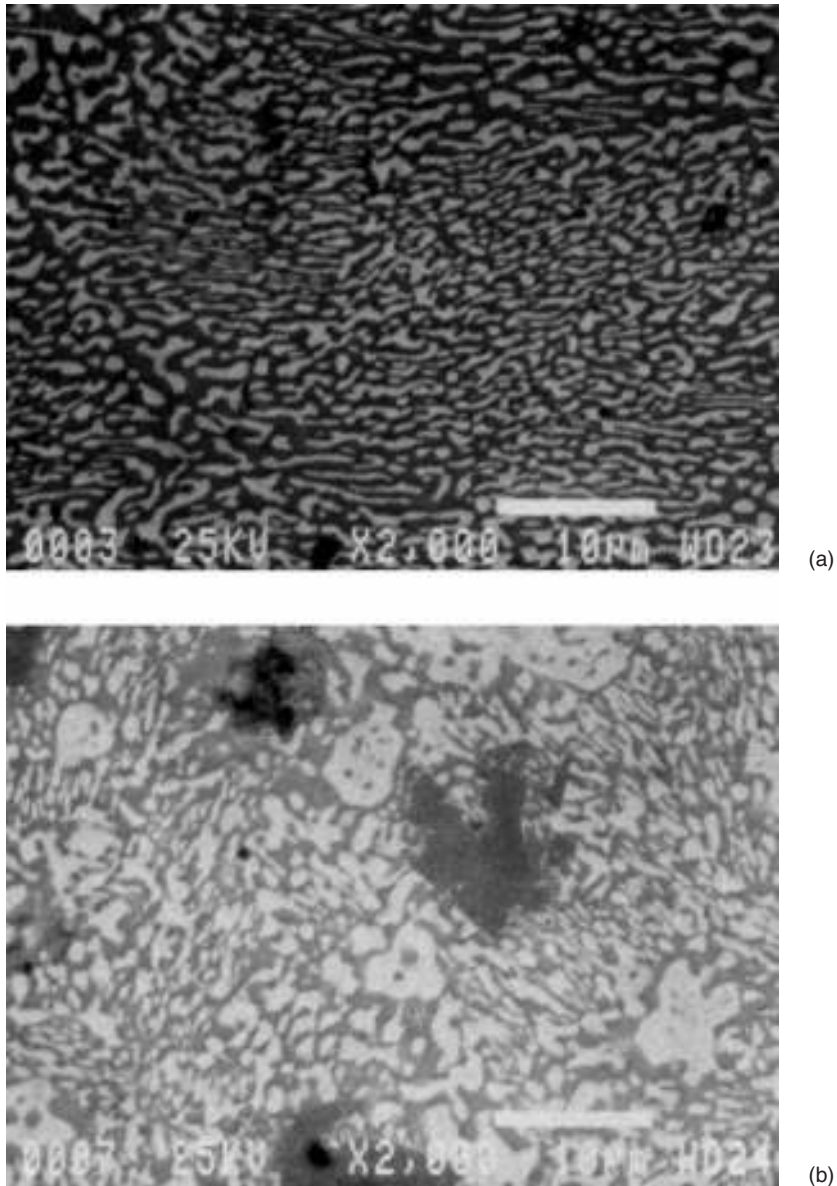
Figure 5.49b shows the 63Sn/37Pb off-eutectic microstructure of a two-metal powder mix, and Fig. 5.49a shows the eutectic microstructure of prealloyed powder reflowed under the same conditions. The difference is attributed to insufficient reflow in Fig. 5.49b; its microstructure reflects a slightly duller joint.

Microstructure is also related to alloy strength and failure mechanisms. It is observed that an ideal Sn/Pb eutectic structure, as shown in Fig. 5.49a, imparts a bright and smooth solder surface. Deviation from the eutectic microstructure is normally visualized as a duller joint.

The heating time at melt is another factor. Figure 5.50 shows the microstructure of two 63Sn/37Pb solder joint surfaces made under a regular infrared heating profile (Fig. 5.50a) and with prolonged exposure at peak temperature (Fig. 5.50b). Figure 5.51 shows the cross sections of these two joints; the excessively heated solder joint in Fig. 5.51b appears to be rough on the surface.

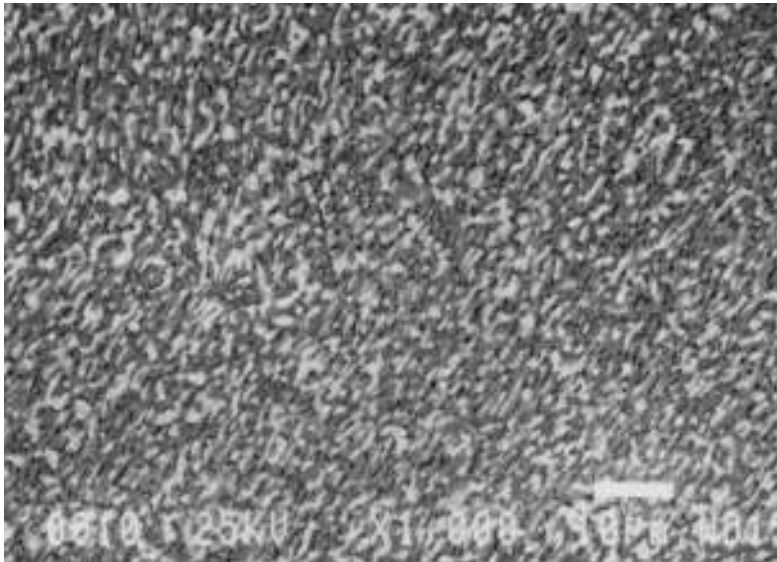


**Figure 5.49** SEM micrograph of 63Sn/37Pb structures: (a) eutectic and (b) off-eutectic.

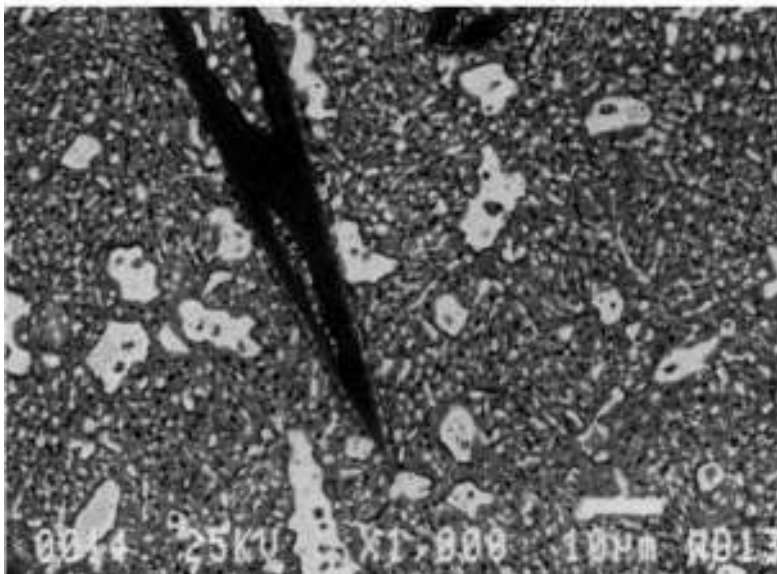


**Figure 5.50** SEM micrograph of 63Sn/37Pb solder joint surface reflowed under (a) regular and (b) prolonged heating.

The residue interference on the molten surface and during its solidification can contribute to a rough texture on the solder surface. Inadequate heating time or temperature will cause incomplete coalescence of solder particles, which also contributes to an unsmooth surface and possibly to an inferior solder joint. During cooling, any mechanical agitation that disrupts the solidifi-



(a)



(b)

**Figure 5.51** SEM micrograph of 63Sn/37Pb solder joint surface cross section reflowed under (a) regular and (b) prolonged heating.

cation process may lead to uneven solder surface. After the completion of reflow and solidification, heat excursion is expected to have a significant impact on solder-joint appearance, whether it is a surface reaction or internal structure change. Heat excursion can come from different sources, such as high-temperature storage, aging, temperature fluctuation during service, and power cycling during functioning.



In many cases, a duller or a rough joint may not be necessarily defective in a functional sense. Test may confirm that the duller and rougher joints have equivalent mechanical strength. However, one must be prudent in drawing a conclusion regarding joint reliability in relation to joint surface appearance. It should be noted that the surface condition of a metal is considered to be one of the variable that affect its failure mechanism. It should also be noted that the surface appearance may reflect the internal microstructure which, in turn, corresponds to the physical and mechanical properties of the solder joint. In the author's viewpoint, the level of smoothness and brightness that the alloy should show reflect a proper joint having been produced from a proper process.

### 5.9.2 Microstructure

When dealing with physical objects in the linear dimension larger than  $10^2 \mu\text{m}$ , we work on structure engineering. If we desire to view an object in the scale of  $10^{-10}$  to  $10^2 \mu\text{m}$ , we study material science and nuclear physics. As the scale shrinks to less than  $10^{-10} \mu\text{m}$ , the object becomes intangible and immeasurable. Microstructure essentially falls in the range of  $10^{-10}$  to  $10^2 \mu\text{m}$ . Hence, the understanding of solder joints within this range of dimensions is generally considered adequate for relating material properties to end-use applications.

Solders are normally polycrystallines that consist of an aggregate of many small crystals or grains. Most solder compositions contain multiple, physically distinct metallurgical phases that are formed and distributed according to given thermodynamic and kinetic conditions. For example, 63 Sn/37Pb is typically composed of lead-rich and tin-rich phases in solid state below eutectic temperature. The finer structure with features smaller than grains and phases is called the *submicrostructure*. Macrostructure is coarser than microstructure and is discernible to the human eye.

The parameters affecting the formation of a microstructure during the solder-joint creation process include heating and cooling. For an assembly prone to the formation of intermetallic compounds at the interface or in the intrinsic solder composition, prolonged heating may produce excessive intermetallic compounds at the interface or in the solder joint. When the solder is liquid, intermetallic compounds at the interface may continue to grow and migrate toward the solder joint interior. In extreme cases, intermetallics may emerge onto the free surface of the solder, causing a change in solder joint appearance. As to the cooling effect, the faster its rate, the finer the microstructure becomes. When the cooling rate is slow enough and approaches equilibrium, the microstructure of the eutectic composition normally consists of characteristic lamellar colonies. As the cooling rate increases, the degree of lamellar structure degeneration increases, and colonies eventually disappear. Although it is generally accepted that a faster cooling rate creates a finer grain structure in bulk solder, this rule is often complicated by the interfacial boundary and metallurgical reaction at the interface of solder joints. The nature of the substrate and its metallurgical affinity to solder composition can affect the solder joint Microstructure development. It would not be surprising to see the microstruc-

ture of the 63Sn/37Pb joint interfacing with a Ni-plated substrate differ from that of a Cu-plated substrate.

During service life, the integrity of joints made with sound fillet design and good wetting at the interfaces is affected by compatibility between the solder alloy and the substrate metal and subsequent in-circuit and external conditions such as heat dissipation, mechanical load, and environmental temperature fluctuation.

Heat, load, time, and extensive metallurgical interaction between the solder and the substrate metal cause changes in microstructure. Failed solder joints have revealed significant degradation in microstructure that is otherwise hidden in the as-solidified counterpart. In most cases in which the failure is a result of fatigue (fatigue-creep) phenomenon, grain (phase) coarsening has been observed to be a precursor of solder cracks.

If we assess the mechanical properties of a solder joint by using commonly established techniques, then shear strength, creep, isothermal low-cycle fatigue, and thermomechanical creep are the top four parameters. For a eutectic solder composition, the shear strength of the solder joint is improved by a very slow cooling rate, which results in the formation of a near-equilibrium lamellar eutectic structure. On the other hand, strength is also enhanced by using a very fast cooling rate, which produces grain size refinement. For plastic deformation under creep mode, creep resistance depends on the operating mechanism. When the lattice or vacancy diffusion process is predominating step, creep resistance is often lower, with a finer microstructure. This is the result of an increased vacancy concentration created by a faster cooling rate. Under an isothermal fatigue environment, the relationship between microstructure and fatigue resistance is more complex. Nonetheless, microstructure homogeneity is more important to low-cycle fatigue resistance. Thermal cycling fatigue resistance is often associated with decreased grain size.

To examine microstructural features, a 100 to 5000× magnification is needed. The characterization can utilize optical (light) or electron microscopy or, preferably, both.

For light microscopy, the solder specimen must be carefully prepared through metallagraphic techniques involving successive grinding and polishing. The technique uses ascending levels of abrasive particle fineness bonded on papers or used as slurry on a cloth-covered wheel. The size of the abrasive particles can range from 23  $\mu\text{m}$  to submicrometer size. Then, the specimen goes through an etching process. In comparison, scanning electron microscopy (SEM) requires little sample preparation when the sectioning (cutting) of the specimen is properly performed. Images from either secondary or backscattered electron signals can be readily obtained. Either provides informative characteristics with distinctive features. By combining information from both images, the microstructure and morphology of a solder joint can be better understood.

For solder joints, the two most information-revealing parameters are elemental composition and microstructure. For a given solder composition, the microstructure in the form of a quality microgram provides “sights” and “insights” into state of solder-joint integrity.

## 5.10 Solder-Joint Integrity

Solder-joint integrity can be affected by the intrinsic nature of the solder alloy, the substrates in relation to the solder alloy, the joint design or structure, the joint-making process, and the external environment to which the solder joint is exposed. Therefore, to assure the integrity of a solder joint, a step-by-step evaluation of the following items is warranted:

- Suitability of solder alloy for mechanical properties
- Suitability of solder alloy for substrate compatibility
- Adequacy of solder wetting on substrates
- Design of joint configuration in shape, thickness, and fillet area
- Optimal reflow method and reflow process in terms of temperature, heating time, and cooling rate
- Conditions of storage in relation to the aging effect on the solder joint
- Conditions of actual service in terms of upper temperature, lower temperature, temperature cycling, vibration, and other mechanical stress
- Performance requirements under the conditions of actual service
- Design of viable accelerated testing conditions that correlate with actual service conditions

### 5.10.1 Basic failure processes

In the real world, solder-joint failure often occurs in complex mechanisms involving the interaction of more than one basic failure process. Although creep-fatigue is considered to be a prevalent mechanism leading to the eventual solder joint failure, separate test schemes in creep and fatigue are often conducted to facilitate data interpretation and an understanding of the material behavior. The basic processes or factors that are believed to contribute to solder failure during service are as follows:<sup>1</sup>

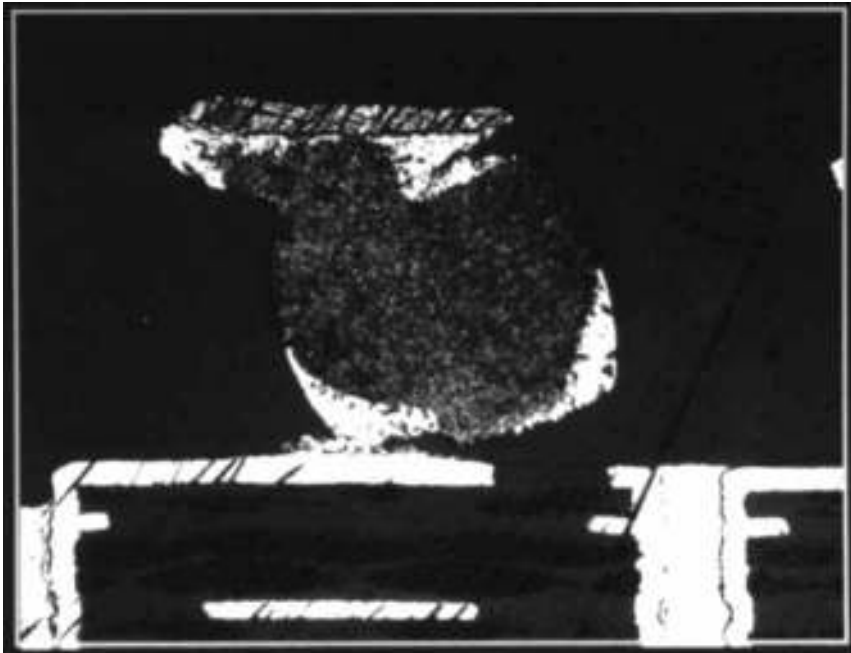
- Inferior or inadequate mechanical strengths
- Creep
- Mechanical fatigue
- Thermal fatigue
- Intrinsic thermal expansion anisotropy
- Corrosion-enhanced fatigue
- Intermetallic compound formation
- Detrimental microstructure development
- Voids
- Electromigration
- Leaching

### 5.10.2 Reliability of BGA solder interconnections

By virtue of array packages' attributes, BGA interconnections on the mother board generally consist of a relatively high number of solder joints per device in comparison with SOICs, PLCCs, and QFPs. The higher number constitutes a higher probability of defect occurrence. This, coupled with less accessibility for inspection, rework, and repair, makes the consistency of forming array interconnections and their quality and integrity critically important.

The main concern for the reliability of array interconnections stems from two areas. First, array solder interconnections are less compliant than conventional peripheral-leaded interconnections. The decreased compliance may contribute to reduced performance under a fatigue environment because of the cyclic thermal stress and strain imposed on the system by temperature fluctuation and in-circuit power on/off. The surface mount array interconnection is also relatively new, and its applications are still in the infant stage for board-level assembly. Statistically substantiated data are lacking in terms of field performance. A common failure mode of PBGA on PCB interconnection is shown in Fig. 5.52. Factors affecting long-term reliability of array solder joints are described below.

**Component package.** The temperature profile to which each solder joint is exposed is a major contributor to the distribution of thermal stress and strain among array solder joints. In addition to the external temperature change, the temperature profile depends on the functional characteristics of the die, the



**Figure 5.52** A common failure mode of PBGA on PCB interconnection.

ratio of die to package size, the thermal property of the carrier substrate, and power dissipation. A study of IC packages ranging from 81 to 421 pins under power cycling demonstrated that outermost solder joints reached 84.3°C while center joints were 98.9°C (1.2°C) below the junction temperature for an 81-pin package.

However, the 421-pin package, having a lower die-to-package size ratio, experienced a large temperature differential between the outer joints (56.2°C) and the center joints (98.5°C).<sup>20</sup> It was found that a 165-pin device that had the largest die size of the components under study had the earliest failure, and its cycle-to-failure was lower than that of the 225-pin device.

It was also found that the solder joints directly underneath the perimeters of the die failed first under temperature cycling. This indicates that solder-joint fatigue life depends more on die size than package size, and the relative location of solder joints to the edge of the die plays an important role in the fatigue performance of solder joints.

**Board materials.** The two characteristics of board materials that have the most influence on the long-term performance of solder interconnections are planarity and coefficient of thermal expansion (CTE). Poor board planarity adds to the coplanarity problem of the BGA package, contributing to the occurrence of solder joint distortion, which in turn may lead to early failure of the solder joint under cyclic stresses. The CTE of conventional board material (FR-4) is approximately  $15 \times 10^{-6}/^{\circ}\text{C}$ , while the ceramic carrier substrate of CBGA has nominal CTE of 6 to  $7 \times 10^{-6}/^{\circ}\text{C}$ . The CTE of solder material falls in the range of 21 to  $30 \times 10^{-6}/^{\circ}\text{C}$ , depending on the alloy. The differential in CTE between the board and carrier substrate results in an additional force of cyclic plastic deformation in solder joints under temperature-imposed conditions. Closely matching the board and carrier substrate CTE reduces thermally induced stresses.

**Solder composition.** The solder composition of the BGA carrier solder bumps affects the mechanical behavior of the solder interconnections. In general, a solder that is “stronger” in fatigue and creep resistance is expected to deliver a better service life. The thickness (height) of solder joints between the BGA and board is much larger than that of a fine-pitch QFP. The actual BGA solder joint height depends on the diameter of the bumps and the dimensions of solder pads; for example, the 0.022-in (0.55-mm) BGA solder height compares with a 0.003-in (0.08-mm) height for the QFP. Because the solder height for BGAs is larger, the effect of the intrinsic properties of BGA solder material is expected to be more pronounced than for QFPs.

**Solder joint configuration and volume.** The shape and configuration of solder joints can change the stress distribution and consequently affect failure mode development. Solder joint volume contributes to the kinetics of solder joint crack propagation. In addition, uniformity and consistency in volume and configuration among array solder joints within a package are important.

**Other material: underfill.** Several studies have demonstrated that an epoxy that fills the air gap between the solder and the underside of the component is ben-

eficial to the fatigue life of the solder joints. For plastic BGAs, the fatigue life of solder joints for over molded pad array carriers (OMPACs) under temperature cycles of  $-40$  to  $125^{\circ}\text{C}$  improved nearly two-fold with epoxy underfill.<sup>20</sup> The underfill around the chip and the solder of the SLICC (slightly larger than IC carrier) assembly, which is a combination of flip-chip and ball array technology, was used to enhance solder joint reliability.<sup>20</sup> The eventual solder joint failure under thermal shock of  $-55$  to  $125^{\circ}\text{C}$  was attributed to the separation of the underfill from the die surface. This loss of adhesion was further related to foreign contamination that was not thoroughly removed during the cleaning procedure.

A similar enhancement in solder joint performance by means of epoxy underfill was observed for the assembly of ceramic BGAs.

**Manufacturing process.** The above-described factors contribute to the long-term performance of solder joints during their service life. However, the ability to make high-quality solder joints at the point of production is equally important. Although an existing installed surface mount operation can be directly used to mount BGAs on a mother board, the setup of process parameters (particularly reflow temperature profile), control of the process, and proper ambient conditions are keys to making quality solder joints. High humidity and high temperature are generally detrimental to surface mount manufacturing.

Material behavior—in relation to temperature change, component effect, and design—is a significant factor in the reliability of interconnections. Understanding each of these areas in conjunction with establishing a quality manufacturing process is the means to full utilization of the merits of BGA packages.

### 5.10.3 Reliability of peripheral solder joints—component lead effect<sup>20</sup>

Consistency among components in their intended lead dimensions and consistency among the leads of a single component are crucial to the quality of solder joints and to the overall yield of manufacturing surface mount assemblies. Although specifications for lead dimensions exist, deviations from these specifications and variations within the specifications in commercial component suppliers often contribute to manufacturing problems in terms of quality and yield. This is because physical characteristics affect the long-term performance of solder joints. The effect can come from various sources as listed below:

- Lead material
- Lead length
- Lead width
- Lead thickness
- Lead height
- Lead co-planarity
- Lead material

Common lead materials include copper, Alloy-42, and Kovar. Lead stiffness varies with the design of the component package; however, the intrinsic stiffness follows the general order of

$$\text{copper} < \text{Kovar} < \text{Alloy-42}$$

It is believed that less stiff or more compliant lead materials are more favorable to the fatigue life of solder joints, other conditions being equal.

- *Lead length.* For QFPs, the lead length is measured from the toe to the contact point with the package body in a horizontal direction. The fatigue life of solder joints was found to increase by 67 percent as the lead length was increased from 0.085 in (2.13 mm) to 0.1125 in (2.82 mm).<sup>21</sup>
- *Lead width.* Figure 5.53 shows the effects of lead width on solder joint fatigue life;<sup>21</sup> fatigue life decreases as lead width increases. It was found that fatigue life is more sensitive to lead thickness than to lead width. The fatigue life drops rapidly as lead thickness increases, as shown in Fig. 5.54.
- *Lead height.* Figure 5.55 shows the effect of lead height as measured from the contact point of lead and package body to the solder pad in a vertical direction. As can be seen, solder fatigue life increases with increasing lead height.
- *Co-planarity.* Production defects are often related to the co-planarity of component leads, which includes starved solder joints and open joints. To avoid problems caused by poor co-planarity, it is advisable to maintain lead co-planarity in the range of 0.002 in (0.05 mm) for fine-pitch components, although 0.004 in (0.1 mm) seems to be an industry-accepted value, and

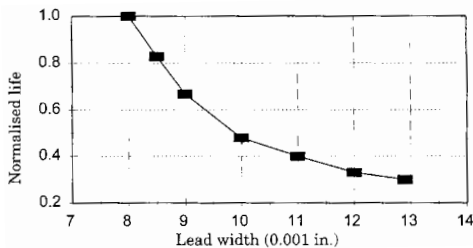


Figure 5.53 Solder joint fatigue life vs. QFP lead width.

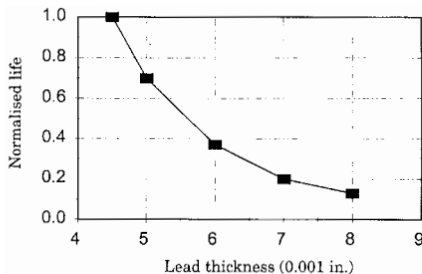
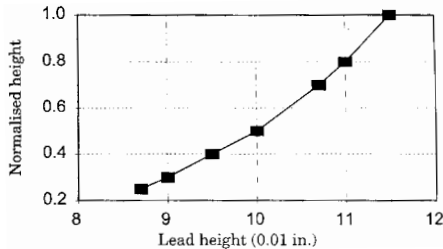


Figure 5.54 Solder joint fatigue life vs. QFP lead thickness.



**Figure 5.55** Solder joint fatigue life vs. QFP lead height.

0.003 in (0.075 mm) for fine-pitch devices. JEDEC 95 specifies co-planarity for individual components.

#### 5.10.4 Challenges in modeling solder joint life prediction

It is well recognized that solder joint reliability relies not only on intrinsic material properties but also on design, component type, the process that produces solder connections, and the long-term service conditions. As electronic IC packages and components continue to change at a rapid pace, it is highly desirable to have a model able to predict the service life and reliability of solder joints under a specific set of conditions. However, to derive such a model is an ever-daunting task. This is primarily because of the complex nature of solder materials in conjunction with the “active” service conditions. Solder materials display a more complex behavior in response to temperature, stress, and time than do high-temperature materials such as steel. Much remains to be understood. The challenges are further complicated by the high level of versatility in circuit boards in terms of various materials and designs.

For a given solder composition and design, the main physical factors affecting the solder material performance are temperature, ambient environment, strain range, strain rate, loading wave form, intrinsic microscopic structure, and surface condition of the materials. Furthermore, the solder joint is expected to behave differently from bulk solder materials. Hence, some established mechanical and thermal behavior of solders may not be applicable. This is presumably a result of the following causes:

- The presence of high ratio of substrate surface to solder volume, resulting in a large number of heterogeneous nucleation sites during solidification
- A concentration gradient of elemental or metallurgical composition when the solder joint is formed

Either of the above conditions may lead to a structure that is not homogeneous. As solder joint thickness decreases, the interfacial effect is more pronounced. Accordingly, the properties of solder joints may be altered, and the failure mechanism may be incongruent with that derived for bulk solder. It is generally accepted that, under cyclic strain conditions, the creep-fatigue process essentially accounts for the solder joint degradation, assuming that the interface problems, such as those caused by excessive intermetallics or poor wetting, are not the determining factors for failure. Consequently, most stud-



ies have been carried out under creep-fatigue testing mode. The goals in studying the creep-fatigue process are as follows:

- One needs to understand material behavior under cyclic strains, which one inevitably encounters during solder joint service life in electronic assembly.
- One also needs to develop or improve the resistance to degradation under cyclic strains by taking a system approach.
- It is also important to predict the fatigue life of solder joints so that performance reliability at a given set of service conditions can be designed and assured.

Many fatigue life prediction methods have been proposed, including the frequency-modified Coffin-Manson (C-M) method, strain range partitioning, fracture mechanics, and finite element analysis (FEA). The methodologies are largely borrowed from the established fatigue and creep phenomena of steels as a result of extensive studies coupled with the field data obtained over a longer period of time. Both the frequency-modified C-M method and fracture-mechanics-based methods are not capable of handling a complex loading wave form, although fracture mechanics can monitor the effect of interfacial crack initiation and propagation on life in a comprehensive manner, and the frequency-modified C-M method takes frequency effect into consideration. Strain range partitioning is able to deal with the strains in any wave form, yet separating the total inelastic strain range per cycle into creep strain and plastic strain is not easy. FEA also lacks the capability of including complex wave forms. Increased efforts in tailoring the basic life prediction models established for steels are burgeoning in electronics industry. Although these efforts may have generated models that apply to solder joints in comparative sense, a true working model has yet to be found.

Service conditions under which solder joints must perform in electronic packages and assemblies often involve random multiaxial stresses, which expose solder joints to creep range in addition to cyclic strains. At this time, sufficient and integrated data regarding solder joint behavior under such conditions, and corresponding damage evolution, are much lacking. Consequently, some important areas and conditions are grossly ignored in the modeling scheme. Listed below are the areas that either have not been included or not adequately covered. They are in turn considered to be the reasons that contribute to the limitations of the existing models to the real-world applications.

1. Effect of initial microstructure
2. Effect of grain size
3. Effect of microstructure that is not homogeneous
4. Change in microstructure versus external conditions
5. Multiaxial creep-fatigue

6. Identification of the presence or absence of crack-free materials at the starting point
7. Size of existing cracks, if present
8. Effect of interfacial metallurgical interaction
9. Joint thickness versus interfacial effect
10. Damage mechanism—transgranular or intergranular
11. Potential damage mechanism shift (from transgranular or intergranular)
12. Presence or absence of grain boundary cavitation
13. Effect of fillet geometry
14. Effect of free surface condition
15. Correlation of accelerated testing conditions with the actual service condition
16. Testing condition versus damage mechanism
17. Service conditioned to include possible variation in chip-power dissipation over time
18. Ambient temperature change
19. The number of on/off power cycles
20. Effect of variation in co-planarity among solder joints

Including the above-listed areas in modeling is not only overwhelmingly time consuming but also extremely difficult. It is a challenge indeed. However, the inclusion of all the above areas in devising a model is necessary to achieve a model's ultimate utility that predicts service life solder joints for a specific application. Until a universal model is validated, a practical system must be created using a combination of existing and experimental data.

#### 5.10.5 Creep and fatigue interaction

Serving as interconnections in electronics packaging and assembly, solder materials usually entail simultaneous exposure to more than one hostile environment, such as temperature. Most solder materials, even under ambient temperature (298 K), reach homologous temperatures ( $T/T_m$ ) well beyond 0.5. Under these service conditions, both creep and fatigue processes may exist and operate interactively. These situations would be equivalent to creep under cyclic loading or fatigue at high temperature.

Whether a “wear-out” phenomenon should be viewed as creep-aggravated fatigue or fatigue-accelerated creep depends on several factors. Generally, when the cyclic stress (or strain) amplitude is small in comparison with the mean stress (or strain), or the applied frequency is low and/or the temperature is high, the phenomenon can be treated as creep perturbed by fatigue. In con-

trast, when the cyclic stress amplitude is large, or the applied frequency is high and/or the temperature is low, the degradation phenomenon should be considered fatigue accelerated by creep behavior.

Solder material in electronic interconnections may undergo changes through one of the two interactive behaviors involving both creep and fatigue. The material properties for obtaining maximum creep resistance often differ from those for maximum fatigue resistance. The development of improved materials should be aimed at enhancing both creep and fatigue resistance.

## 5.11 Lead-Free Solders

The issue of lead in electronics has gone through more than 12 years of deliberation and debate by legislative bodies, manufacturers, and individuals around the world. Various ideas have been exhibited, particularly in U.S., and individual opinions expressed by both supporters and oppositions have been eloquent. On the global landscape, the tangible progress in technology and legislation differs in the three major continents—North America, the European Union, and Asia. Although a uniform consensus is still to be worked out, the technology has advanced, the business climate has changed, and, overall, the marketplace is striding into a highly environmentally-conscious playing field.

Various organizations have made dedicated effort to inform the industry about this pivotal issue. For instance, the Swedish Institute of Production Engineering Research (IVF) has developed the “Electronics Design-for-Environment Webguide,” which disseminates updated information to the industry regarding the development of legislation and technology. The International Tin Research Institute (ITRI) launched the Lead-Free Soldering Technology Centre, and IPC initiated the Lead Free Forum on the Internet. Professional organizations such as Surface Mount Technology Association (SMTA) and International Microelectronics and Packaging Society (IMAPS) have organized symposia dedicated to disseminating knowledge and information.

Global legislations in the three regions are described separately, below.

To producers and manufacturers, waste reduction, recovery, and recycling should be and inevitably will be treated as a long-term goal supported by an ongoing effort. A product should be designed for minimal environmental impact and with the full life cycle in mind. Life-cycle assessment includes all the energy and resource inputs to a product, the associated wastes, and the resulting health and ecological burdens. Overall the goal is to reduce environmental impacts from cradle to grave.

### 5.11.1 Status of worldwide legislation

**5.11.1.1 United States.** The Lead Exposure Reduction Act (S.391) was introduced in 1991, putting restrictions on lead solder, banning some and limiting lead content in others to less than 0.1 percent. In April, 1993, a sister bill

(S.729) to the Lead Exposure Reduction Act emerged. Under this Act, in addition to banning lead solders for plumbing, an inventory and concern list, new use notification requests, and product labeling were included. The EPA must inventory all lead-containing products and then develop a “concern list” of all products that may reasonably be anticipated to present an unreasonable risk of injury to human health or the environment. Any person can petition the EPA at any time to add a product to the “concern list.” Anyone who manufactures or imports a lead-containing product that is not on the inventory list must submit a notification to the EPA. The products on the “concern list” must be labeled.

On May 25, 1994, the Lead Exposure Reduction Act (S.729) passed the Senate floor. Furthermore, the Lead Tax Act (HR 2479 and S. 1357) was also introduced in June, 1993, placing a \$0.45 per pound tax on all lead smelted in the United States and on the lead content of all imported products.

The Resource Conservation and Recovery Act (RCRA) classifies solder skimmings and solder pot dumpings as scrap metal, not as hazardous waste, if can be shown that they are recycled. However, if they are disposed of as a waste, they must pass the Toxic Characteristic Leaching Procedure (TCLP) test with the established maximum concentration of lead by TCLP testing being 5 ppm; solder skimming and pot dumpings are expected to fail. Therefore, they are not exempted from RCRA hazardous waste regulations.

Waste solder materials are not considered hazardous if they are returned to a reclaimer or the supplier. A container with less than 3 percent by weight of its total content is considered empty and is not subject to hazardous waste regulation.

In 2001, the U.S. EPA tightened Toxics Release Inventory reporting requirement by reducing the reporting threshold for lead and lead compounds from 25,000 lb for manufacturing and processing (10,000 lb for other use) to 100 lb. This new EPA regulations under the Toxic Release Inventory (TRI) program requires all facilities that manufacture, process, or otherwise use 100 lb of lead or lead compounds to report their TRI lead releases annually, beginning July 1, 2002. The 100-lb lead threshold is approximately 270 lb of typical electronic solder based on 63Sn37Pb alloy. The new TRI lead rule mandates that releases be reported to within 0.1 lb, which is only 1.6 oz or 45.3 g. This is an extremely small amount over a one-year period, creating great demands on facilities as they calculate their annual lead releases.

**5.11.1.2 Japan.** The newly enacted legislation Home Electronics Recycle Law mandates the recovery of lead used in home electronics. Prompted by this law and the guidelines from the Japanese EPA and government to reduce lead and increase recycling, many Japanese electronic companies have announced voluntary plans to reduce or eliminate the use of lead in solder.

Some companies have implemented lead-free solders in commercial products. For example, Hitachi, Matsushita (Panasonic), and NEC announced intentions to reduce lead use to 50 percent of 1997 level by year 2002, and to stop using lead-containing solder in 2003.

Most companies, including Sony, Toshiba, NEC, Hitachi, and Matsushita, have their own programs for developing or selecting a suitable lead-free alloy composition.

**5.11.1.3 Europe.** Among the European Commission proposals, two main directives applicable to this industry are

- *WEEE*. Waste Electrical and Electronic Equipment Directive
- *RoHS*. The Restriction of Use of Hazardous Substances Directive

The European Commission Directive proposed implementation of WEEE by 2006 (2005).

According to the proposed document, WEEE stipulates "...components containing lead will have to be removed from any end-of-life electrical and electronic equipment (EEE) that is destined for a landfill, incineration or recovery..." where EEE was defined as equipment dependent on electric currents or electromagnetic fields to work properly, as well as equipment designed for use with a voltage rating not exceeding 1,000 V for AC and 1,500 V for DC.

The purpose of the WEEE Directive is, as a first priority, the prevention of waste electrical and electronic equipment and in the addition, reuse, recycling, and other forms of recovery of such wastes so as to reduce waste disposal of waste. It also seeks to improve the environmental performance of all economic operators involved in the life cycle of electrical and electronic equipment and in particular operators directly involved in the treatment of waste electrical and electronic equipment

The purpose of the RoHS Directive is to approximate the laws of the Member States in terms of restrictions on the use of hazardous substances in electrical and electronic equipment, and to contribute to the environmentally sound recovery and disposal of waste electrical and electronic equipment.

RoHS Prevention includes

- Lead
- Mercury
- Cadmium
- Hexavalent chromium
- Polybrominated biphenyls (PBB)
- Polybrominated diphenyl ether (PBDE)

In 1994, Nordic Ministers of Environment stated "...in the long run the phaseout of lead is necessary to reduce risk from lead exposure on human health and the environment...."

**5.11.1.4 Examples of implementation.** The legislative thrust in Europe and Japan is moving the industry toward "green manufacturing" and environmentally conscious workplaces. An exemplary lead-free manufacturing process

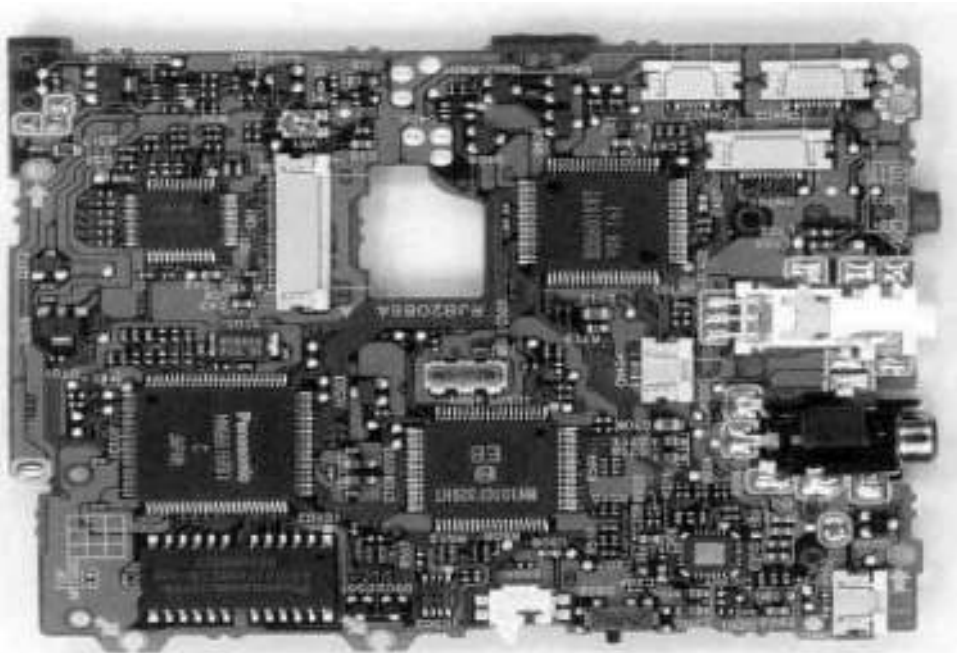
has been employed successfully to produce the Panasonic-Matsushita minidisk player models. It was reported by the manufacturer that the production enjoyed a relatively low melting point of 210°C while offering the same workability, and quality and reliability in the finished product is similar to that achieved with 63Sn/37Pb.

Figure 5.56 exhibits the main circuit card of the Panasonic MR100, which evolved from player types (MJ30, MJ70) to this player/recorder. The main cards for all three products were produced in lead-free manufacturing with Sn/Ag/Bi/Cu alloy compositions.

### 5.11.2 Technology and approaches

Looking back to approximately 12 years ago, when the industry started to “seriously” explore and conduct research in lead-free solders for making electronic products, this author indicated that any viable lead-free solders intended to replace Sn/Pb eutectic or near-eutectic compositions could not escape from being an Sn-based system (i.e., a minimum of 60 wt percent of tin).

This conclusion was based on both fundamental and practical perspectives. Fundamentals include metallurgical bonding capability on commonly used substrates, dynamic wetting ability during reflow process, and metallurgical “interactions” or alloying phenomena between elements. Practical factors include the availability of natural resources, manufacturability, toxicity, and cost.



**Figure 5.56** Main circuit card of Panasonic minidisk player MR100.

My another query back then was, “What constitutes futuristic solders?”<sup>22</sup> Is the environmentally friendly and failure-free solder joint technology a utopia or ultimately achievable performance? Solder alloys of Sn/Pb eutectic, along with near-eutectic or containing 2 percent Ag, have successfully served the function of making mechanical, electrical, and thermal connections for decades. However, the operating temperature (above room temperature) of electronic products is well above the “homologous” temperature. Based on the material principle, even at the ambient operating temperature, it is the highest application temperature that any engineering materials have ever endured. It thus comes as no surprise that local fatigue micro-cracking and global creep micro-cracking can occur in solder joints during their service life.

It is reasonably well substantiated that the common thermal fatigue failure is linked with the Pb-rich phase. It is therefore expected that the absence of Pb-phase in a properly designed lead-free tin-based solder may impart improved mechanical behavior, resulting in strengthened solders. With increased requirements on the integrity and reliability of interconnections in electronic and microelectronic assemblies, a better solder should always find its useful place.

The two crucial material characteristics for selecting the constituent elements and their specific dosages in the design of lead-free solders are (a) the elements’ ability to alloy with Sn and (b) their melting point lowering properties while alloying with Sn.

Based on metallurgy, elements such as In, Bi, Mg, Ag, Cu, Al, Ga, and Zn are the candidates that can lower the melting temperature of Sn to create Sn-based alloys that possess the required properties for electronic packaging and assembly. Table 5.15 tabulates the speculative melting point reduction with Sn at the selected temperature ranges for the candidate elements.<sup>30</sup>

**TABLE 5.15 Estimated Melting Temperature Reduction of Sn by the Selected Elements at the Specified Temperature Ranges**

Element	Melting temperature reduction		
	160 to 183°C	183 to 199°C	200 to 230°C
In	2.3	2.1	1.8
Bi	1.7	1.7	1.7
Mg	–	–	16.0
Ag	–	–	3.1
Cu	–	–	7.1
Al	–	-	7.4
Ga	2.6	2.5	2.4
Zn	–	3.8	3.8

**5.11.2.1 Alloy strengthening principles.** From a material point of view, the crystalline alloys can deform via one or a combination of the following mechanisms:

1. Slip
2. Dislocation climb
3. Shear on grain boundary
4. In-grain vacancy or atomic diffusion

It is generally understood that fatigue failure and material cracking is often caused by dislocation slip and the localization of plastic deformation. It is also generally understood that plastic deformation kinetics follows the power-law dislocation climb-controlling mechanism under high-stress/low-temperature conditions. In a low-stress region at high temperature, the grain boundary sliding becomes a rate-controlling process. Therefore, to strengthen the performance of conventional solders that are subject to stressful conditions as a result of external temperature fluctuation and/or-in-circuit power dissipation and power on-off electronic circuit boards, several approaches, as listed below, can be considered.

**5.11.2.2 Strengthening approaches.** Under high-temperature conditions (above room temperature) to which solder joints are normally exposed, the mobility of atoms increases, and so do dislocations. Other crystalline defects such as vacancies also increase. Additional slip systems are introduced, and metallurgical stability is unfavorably affected. In addition, environmental effects (oxidation, corrosion) become more pronounced.

Approaches that can potentially hinder the above material phenomena are expected to enhance the performance of solders, which in turn will achieve the performance levels required for new and future applications. Such approaches include

1. Microscopic incorporation of nonalloying dopant
2. Microstructural strengthening
3. Alloy strengthening
4. Macroscopic blend of selected fillers

These approaches involve both process and material factors.<sup>23–27</sup> For example, solid solutioning where solute atoms normally reduce the stacking fault energy and favorably control the diffusion behavior is one widely adopted strengthening mechanism. In any of these approaches, the objective of the alloy design is to set the proper parameters to achieve the following properties:

- Phase transition temperatures (liquidus and solidus temperature) as close to Pb bearing counterparts as practical



- Suitable physical properties—specifically, electrical and thermal conductivity and thermal expansion coefficient
- Metallurgical properties that are compatible with the interfacial substrates of components and boards
- Adequate mechanical properties, include shear strength, creep resistance, isothermal fatigue resistance, thermomechanical fatigue resistance, and microstructural stability
- Intrinsic wetting ability
- Environmental shelf stability
- Relatively low (or no) toxicity

**5.11.2.3 Alloy design.** For a Sn-matrix, candidates that can serve as viable alloying elements are quite small in number, practically limited to Ag, Bi, Cu, In, and Sb. However, doping elements may extend to a larger group of elements and compounds. Metallurgical interactions (reactions) and microstructure evolution in relation to temperature rise provide the critical scientific basis for developing new lead-free solders.

Binary phase diagrams provide general information about the conditions and extent of metallurgical interactions, although complete phase diagrams beyond the binary system are scarce. Nonetheless, binary phase diagrams offer a useful starting point.

After a decade of research, we found that the actual test results of the designed multiple-element alloy compositions came very close to the anticipated features in terms of properties and performance between a candidate element and Sn-matrix.<sup>24–28</sup>

To illustrate the point, as examples, Se and Te were found to readily embrittle the Sn-based alloys. Sb in an improper amount quickly jeopardizes the alloy's wetting ability. The distribution of In atoms in the Sn host lattice is sensitively reflected in the fatigue performance. An improper dosage of Bi may result in Bi second-phase precipitation, which can render the solder extremely brittle. The formation of intermediate phases and intermetallic compounds between Sn and Cu, Ag, or Sb, remarkably affect the strength and fatigue life of the alloy, which in turn depends on the concentration of each element as well as on the relative concentration among the elements.

The general performance is as predictable as stated, but a high-performance alloy composition demands a stunningly intricate balance of the elemental constituents. In each of compositional system, the useful products are often a specific composition or a narrow range of compositions at best.<sup>32–34</sup> Over the past decade, many compositions have been developed and disclosed. More than 75 patents on lead-free solder alloys have been issued worldwide. Among them, most compositions made public are not ready to be used in commercial applications. However, lead-free alloys exist that can be put to use, delivering desirable performance that is superior to that of their lead-containing counterparts.

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New solder alloys must possess the characteristics that are compatible with the practical manufacturing techniques and end-use environment. The basic material properties such as liquidus/solidus temperature, electrical/thermal conductivity, intrinsic wetting ability on surfaces that are commonly used, mechanical properties, and environmental shelf stability, must be gauged. Under the current framework, conductivity and shelf stability are not as sensitive to the makeup of a specific system as intrinsic wetting ability, mechanical performance, and phase transition temperatures. Ability to optimize these properties through in-depth application of materials science and metallurgical phenomena is the key.

### 5.11.3 Pb-free solder vs. Pb-bearing solder<sup>29-31</sup>

The driving forces behind the lead free solders are primarily performance demands and environmental/health concerns. It is reasonably well substantiated that common thermal fatigue failure for solder interconnections is linked to the Pb-rich phase. This Pb-rich phase cannot be effectively strengthened by Sn solute atoms because of limited solubility and Sn precipitation. At room temperature, the limited solubility of Pb in an Sn matrix renders it incapable of improving the plastic deformation slip. Under temperature cycling (thermo-mechanical fatigue) conditions, this Pb-rich phase tends to coarsen and eventually leads to the solder joint crack. It is therefore expected that the absence of Pb-phase in a properly designed lead-free tin-based solder may impart improved mechanical behavior, resulting in strengthened solders. The new alloys selected and listed below manifest improved performance over 63Sn/37Pb.

On the international landscape, some companies have implemented lead-free solders in commercial products. Many manufacturers have initiated their own programs for developing or selecting a suitable lead-free alloy composition.

### 5.11.4 Solder alloy selection—general criteria

Generally, the alloy selection is based on the following criteria:

- Alloy melting range in relation to service temperature
- Mechanical properties of the alloy in relation to service conditions
- Metallurgical compatibility, consideration of leaching phenomenon, and the potential formation of intermetallic compounds
- Rate of intermetallic formation in relation to service temperature
- Other service compatibility (considerations such as silver migration)
- Wettability on specified substrate
- Eutectic versus noneutectic compositions
- Ambient environment stability

### 5.11.5 Selection menu—Pb-free solder<sup>30</sup>

From the simplest alloy (a binary system) to incrementally complex systems containing more than two elements, lead-free materials have been thoroughly

explored, designed and studied.<sup>30,32–34</sup> Six systems and their corresponding compositions stand out in terms of their performance merits. Their strengths in comparison with the established alloy compositions are summarized below. These six systems are

1. Sn/Ag/Bi
2. Sn/Ag/Cu
3. Sn/Ag/Cu/Bi
4. Sn/Ag/Bi/In
5. Sn/Ag/Cu/In
6. Sn/Cu/In/Ga

A detailed discussion of each of these systems is omitted in this text. Readers can obtain detailed illustrations and data for each of these systems in a newly released textbook.<sup>30</sup> Some compositions are covered by patents.<sup>32–42</sup> The selected compositions from each of the systems are also compared with the pertinent known lead-free alloys as well as with 63Sn/37Pb. Figures 5.57 through 5.66 summarize the relative performance of these selected compositions with the established solder alloys. An overall comparison is provided among these six systems, leading to the ranking by melting temperature (Table 5.16) and fatigue life (Table 5.17), respectively, and to a final slate of selections.

**TABLE 5.16 Ranking of Viable Alloy Compositions by Melting Temperature**

Alloy	Melting T°C	N <sub>f</sub>
8.52Sn/4.1Ag/2.2Bi/0.5Cu/8.0In	193–199	10,000–12,000
88.5Sn/3.0Ag/0.5Cu/8.0In	195–201	>19,000
93.3Sn/3.1Ag/3.1Bi/0.5Cu	209–212	6,000–9,000
91.5Sn/3.5Ag/1.0Bi/4.0In	208–213	10,000–12,000
92.8Sn/0.7Cu/0.5Ga/6.0In	210–215	10,000–12,000
95.4Sn/3.1Ag/1.5Cu	216–217	6,000–9,000
96.2Sn/2.5Ag/0.8Cu/0.5Sb	216–219	6,000–9,000
96.5Sn/3.5Ag	221	4,186
99.3Sn/0.7Cu	227	1,125
Reference 63Sn/37Pb	183	3,656

The alloy also has impressively higher strength than any of the binary alloys—63Sn/37Pb or 96.5Sn/3.5Ag or 99.3Sn/0.7Cu.

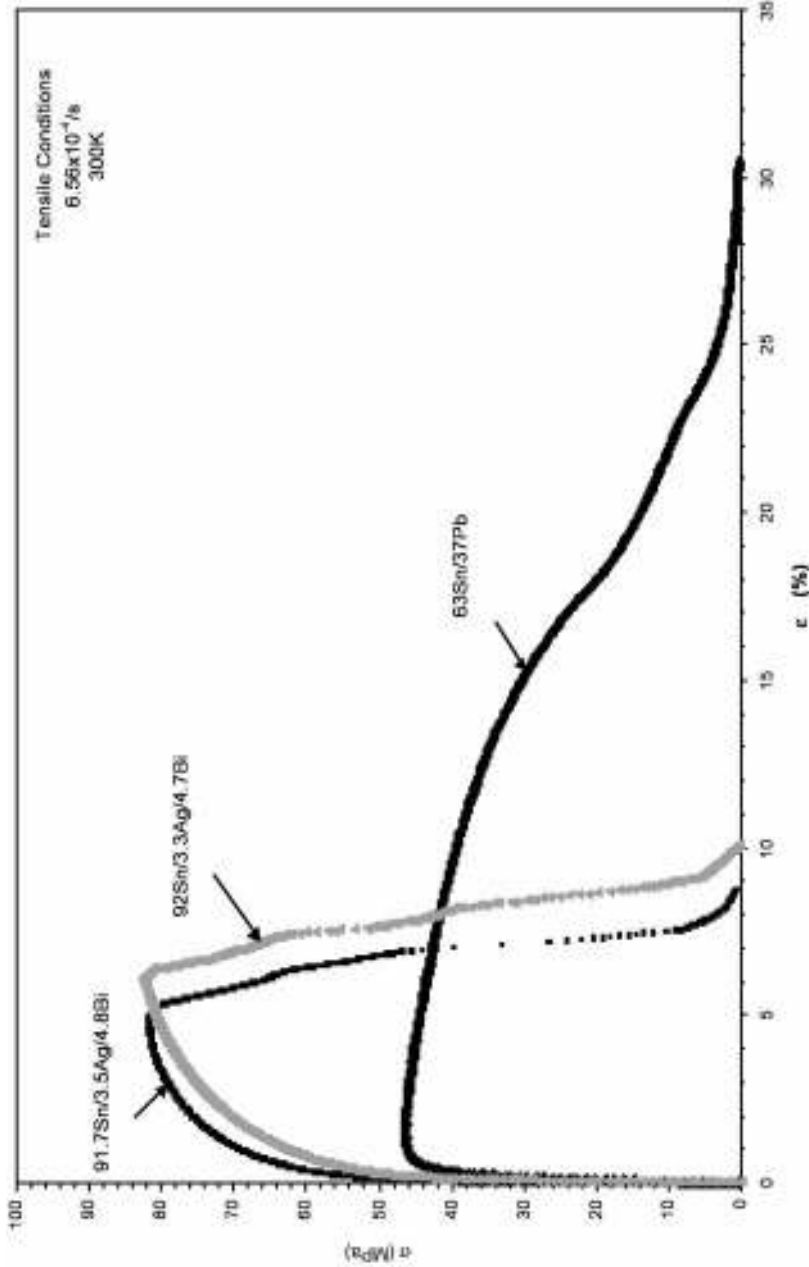


Figure 5.57 Tensile stress ( $\sigma$ ) vs. strain ( $\epsilon$ ) at 300K and  $6.56 \times 10^{-4}$  /second for Sn/Ag/Bi alloys and 63Sn/37Pb.

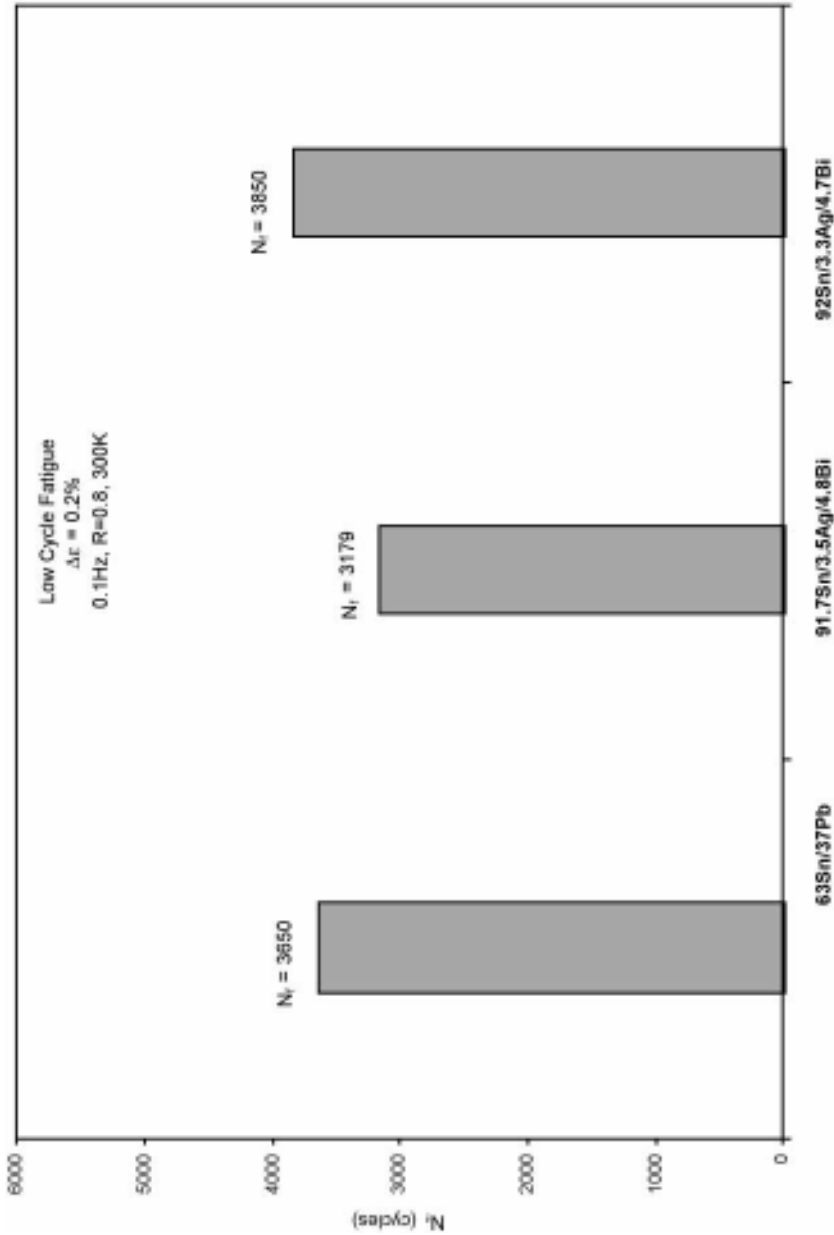
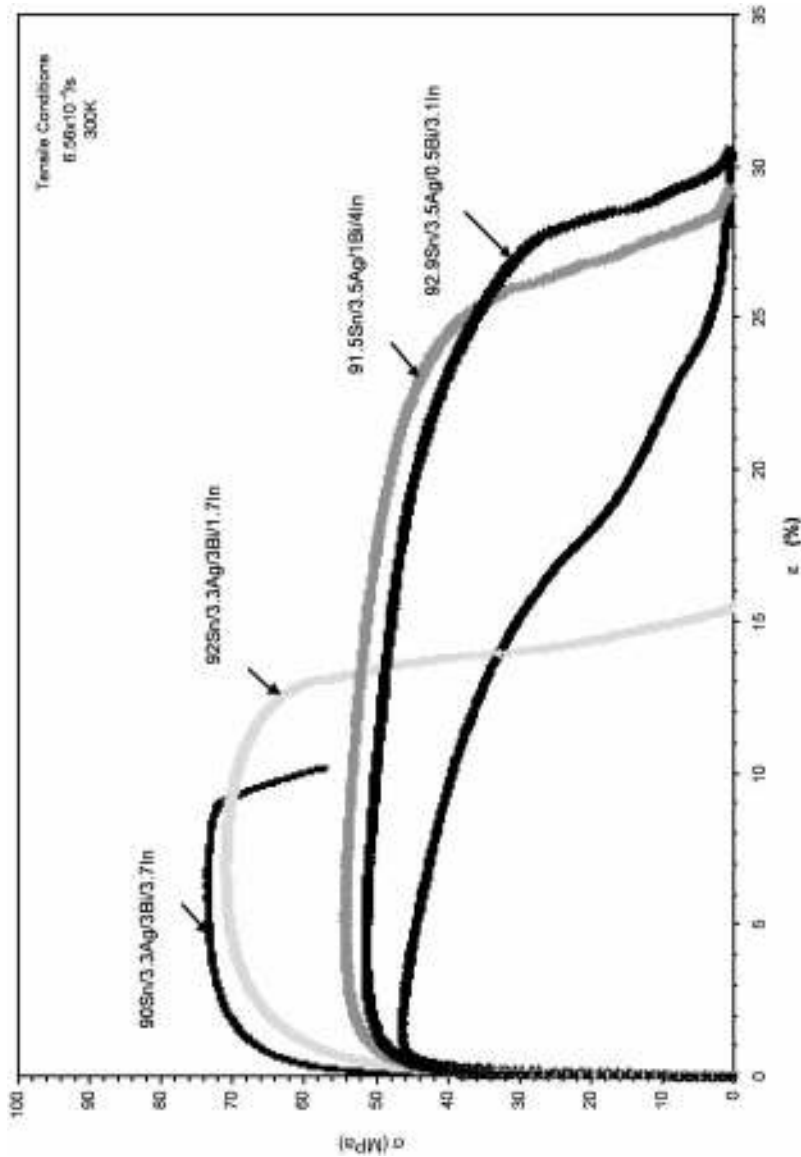


Figure 5.58 Comparison of fatigue life of Sn/Ag/Bi alloys with 63Sn/37Pb.



**Figure 5.59** Tensile stress ( $\sigma$ ) vs. strain ( $\epsilon$ ) at 300K and  $6.56 \times 10^{-4}$  /second for Sn/Ag/Bi/In alloys and 63Sn/37Pb.

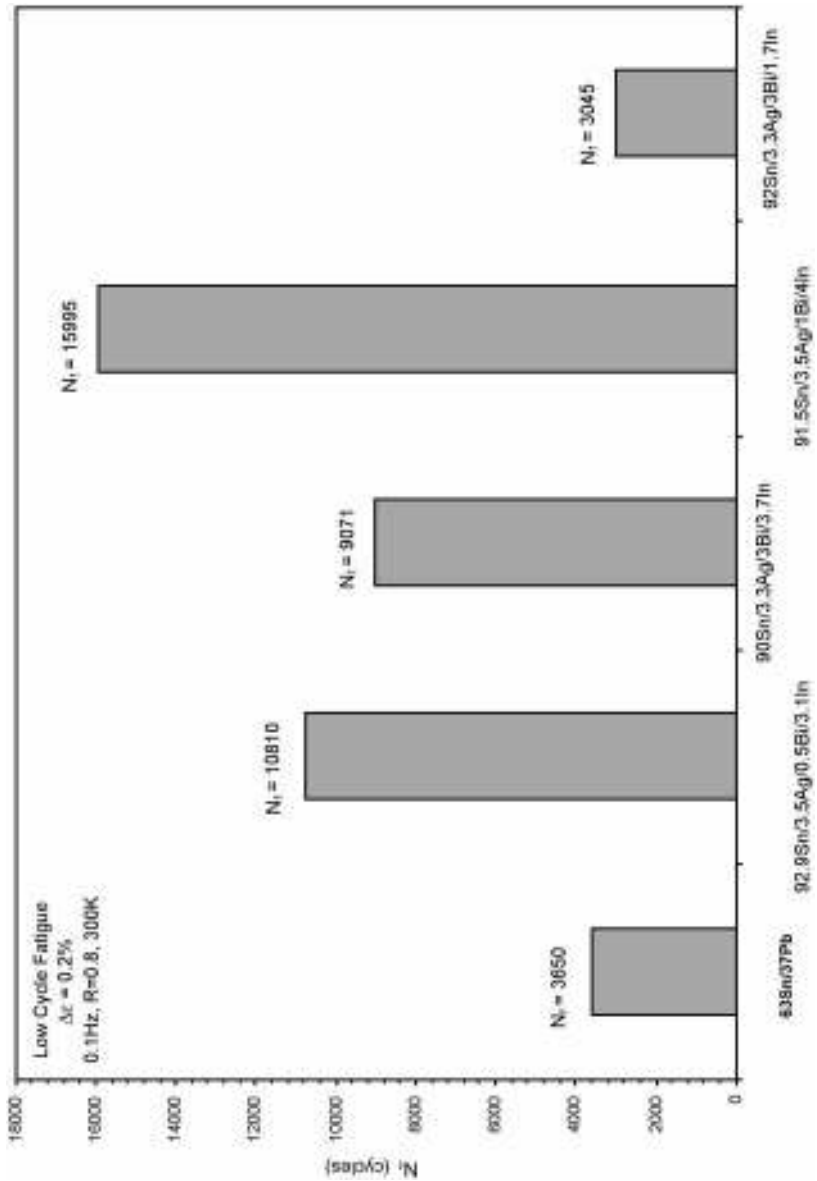
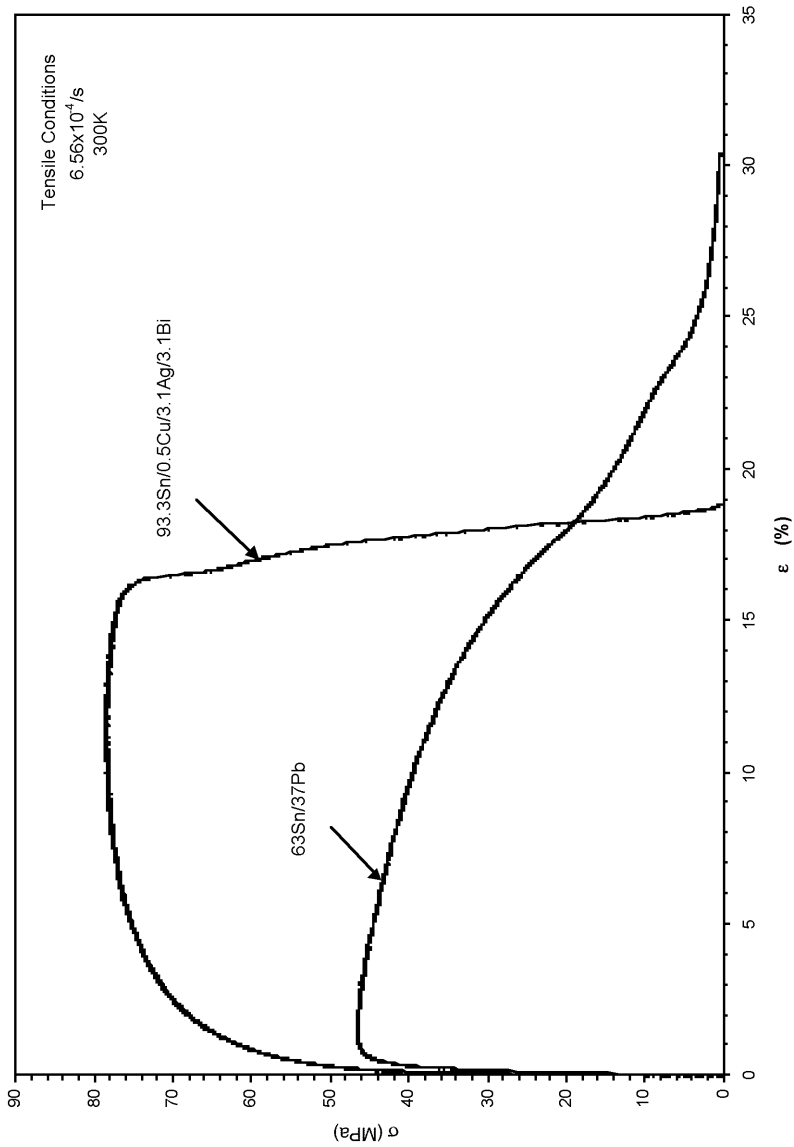


Figure 5.60 Comparison of fatigue life of Sn/Ag/Bi/In alloys with 63Sn/37Pb.



**Figure 5.61** Tensile stress ( $\sigma$ ) vs. strain ( $\epsilon$ ) at 300K and  $6.56 \times 10^{-4}$  /second for Sn/Ag/Cu/Bi alloys and 63Sn/37Pb.



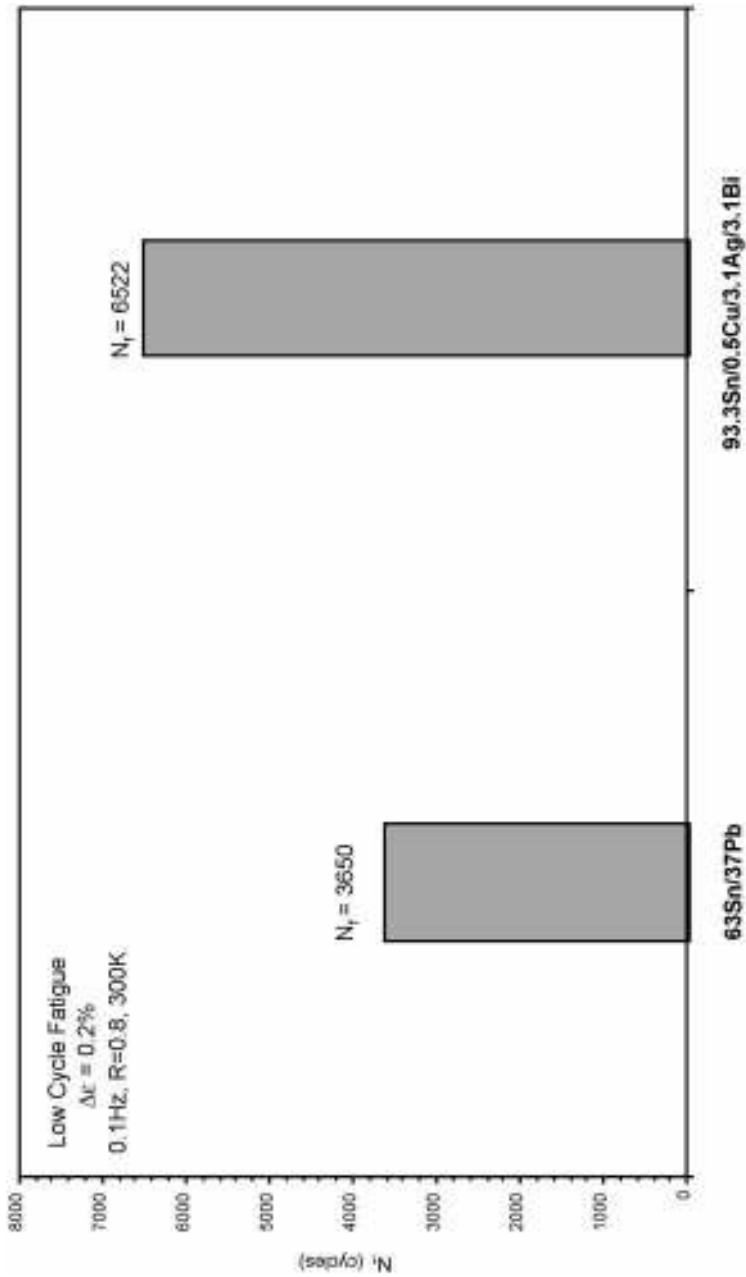
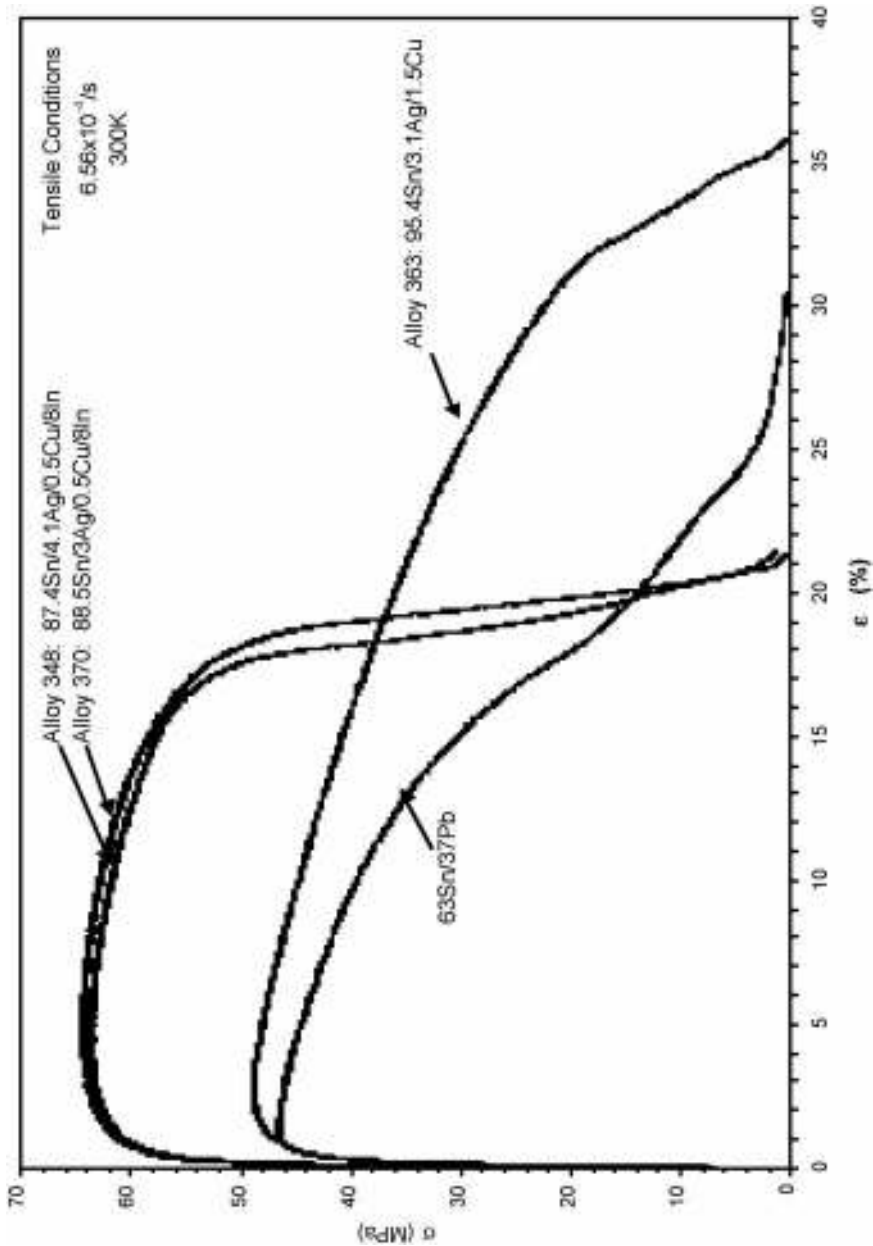
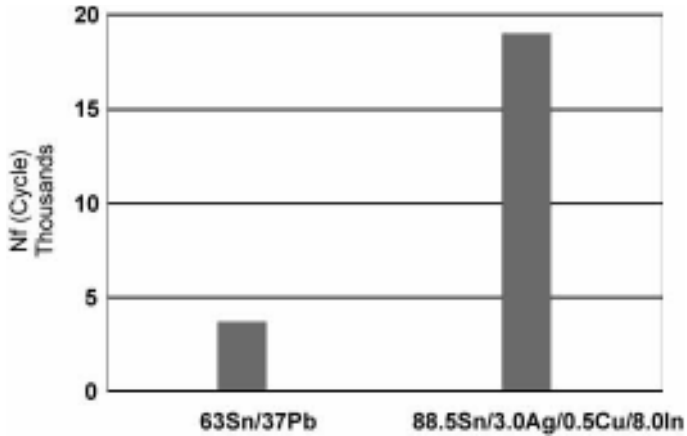


Figure 5.62 Comparison of fatigue life of Sn/Ag/Cu/Bi alloys with 63Sn/37Pb.



**Figure 5.63** Tensile stress ( $\sigma$ ) vs. strain ( $\epsilon$ ) at 300K and  $6.56 \times 10^{-4}$  /second for Sn/Ag/Cu/In alloys and 63Sn/37Pb.



**Figure 5.64** Comparison of fatigue life of Sn/Ag/Cu/In alloys with 63Sn/37Pb.

**TABLE 5.17** Ranking of Viable Alloy Compositions by Fatigue Resistance

Alloy	Melting T°C	N <sub>f</sub>
88.5Sn/3.0Ag/0.5Cu/8In	195–201	>19,000
91.5Sn/3.5Ag/1.0Bi/4.0In	208–213	10,000–12,000
92.8Sn/0.7Cu/0.5Ga/6.0In	210–215	10,000–12,000
85.2Sn/4.1Ag/2.2Bi/0.5Cu/8.0In	193–199	10,000–12,000
93.3Sn/3.1Ag/3.1Bi/0.5Cu	209–212	6,000–9,000
96.2Sn/2.5Ag/0.8Cu/0.5Sb	216–217	6,000–9,000
95.4Sn/3.1Ag/1.5Cu	216–217	6,000–9,000
96.5Sn/3.5Ag	221	4,186
92Sn/3.3Ag/4.7Bi	210–215	3,850
99.3Sn/0.7Cu	227	1,125
Reference 63Sn/37Pb	183	3,650

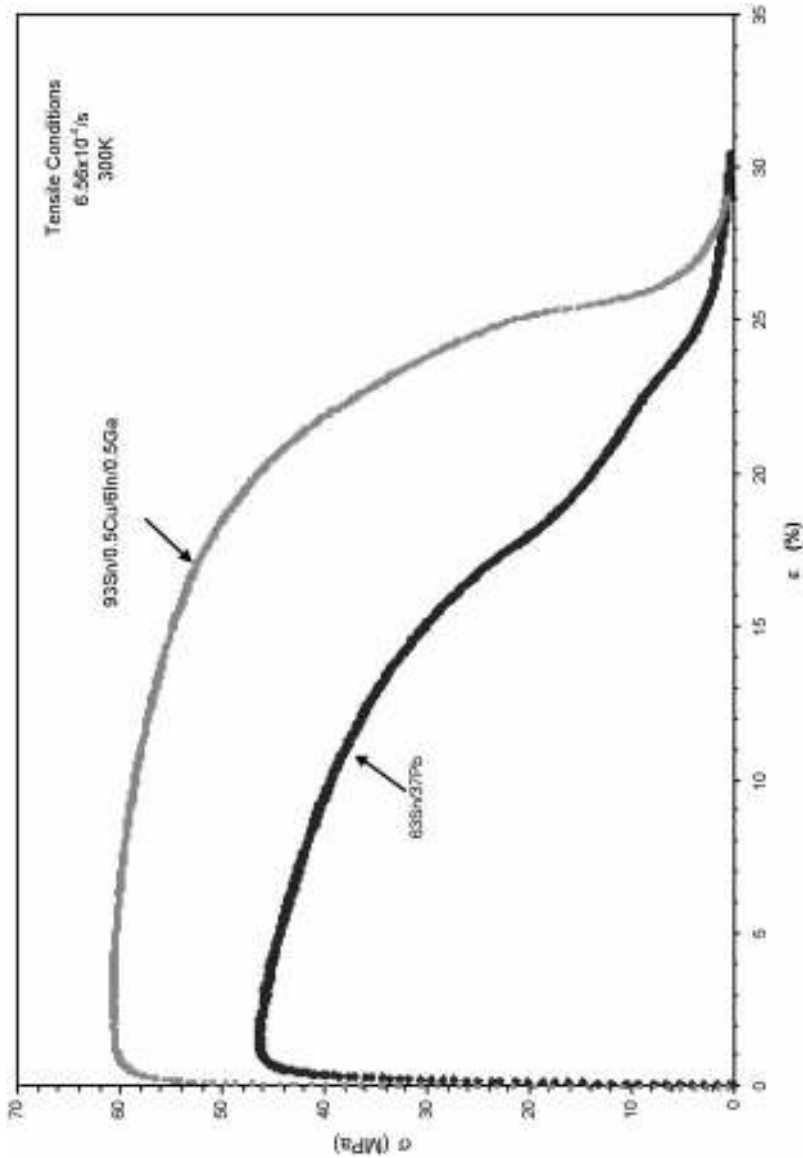
### 5.11.6 Pb-free recommendations

- An optimal composition should be determined based on the required performance level for a specific application. Tables 5.16 and 5.17 provide the relative performance of the selected alloys that show the most promise.
- A slate of compositions as listed below can be considered:

Sn/3.0–3.5Ag/0.5–0.5Cu/4.0–8.0In

Sn/3.0–3.5Ag/3.0–3.5Bi/0.5–0.7Cu

Sn/3.3–3.5Ag/1.0–3.0Bi/1.7–4.0In



**Figure 5.65** Tensile stress ( $\sigma$ ) vs. strain ( $\epsilon$ ) at 300K and  $6.56 \times 10^{-4}$  /second for Sn/Cu/In/Ga alloys and 63Sn/37Pb.

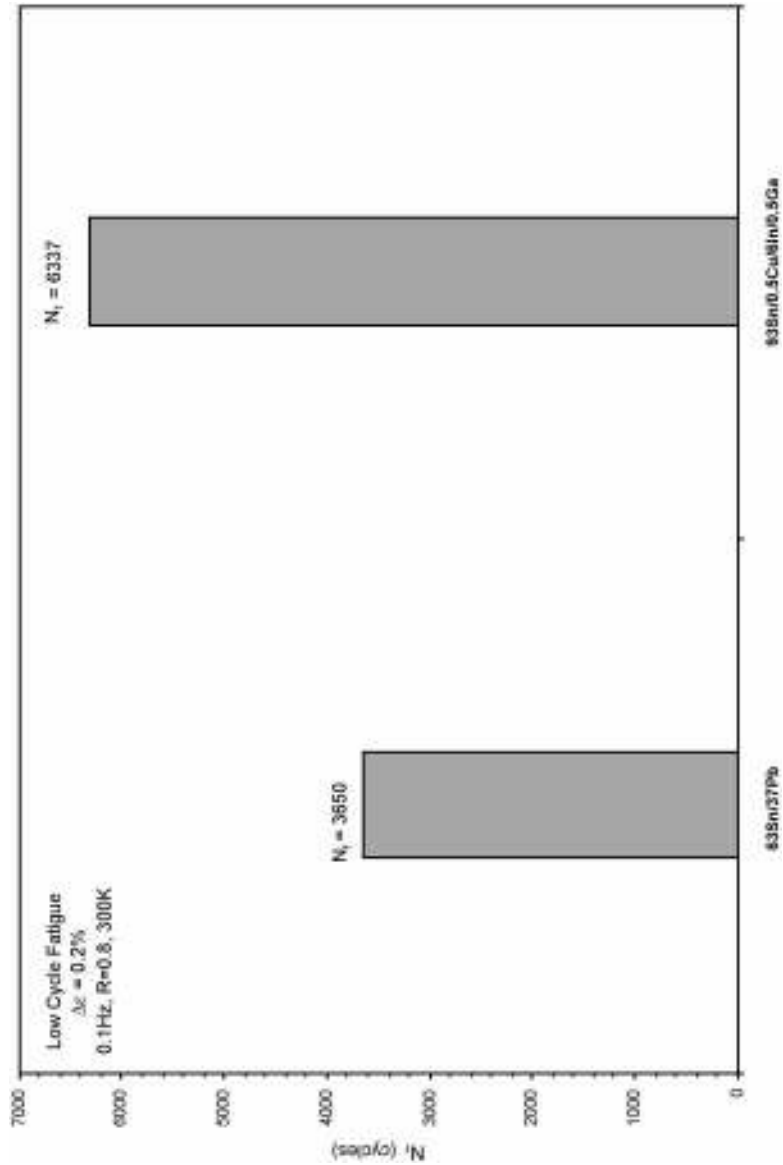


Figure 5.66 Comparison of fatigue life of Sn/Cu/In/Ga alloys with 63Sn/37Pb.

Sn/0.5-0.7Cu/5.0-6.0In/0.4-0.6Ga

Sn/3.0-3.5Ag/0.5-1.5Cu

Sn/3.0-3.5Ag/1.0-4.8Bi

99.3Sn/0.7Cu

96.5Sn/3.5Ag

- Melting temperature (liquidus temperature) is an important selection criterion.
- A proper reflow profile is able to compensate, to some extent, for the higher melting temperature (higher than 183°C) associated with lead-free alloys.
- For surface mount PCB assembly, the melting temperature of solder alloys below 215°C provides the necessary process window.
- For a reflow process, the peak temperature should be kept below 240°C, preferably 235°C; for wave soldering, the temperature should be below 245°C.
- Alloy intrinsic wetting ability is crucial to the quality and integrity of solder joints and the production yield.
- Overall, technological advancement has been made in enhancing creep and fatigue resistance by lead-free research and the viable alloys are identified for highly fatigue-resistant applications.

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# Electroplating and Deposited Metallic Coatings

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## 6.1 Electroplating for Electronic Applications

The electroplating industry is essential to many manufacturing operations. Electroplated coatings and related finishes are classified into three categories according to their main function, although these categories do overlap. Plated finishes may be used to

1. Improve the appearance of the part
2. Impart a protective surface on the part
3. Modify the chemical or physical properties of the part's surface

Without electroplating and surface finishing, our modern standard of living would be difficult to maintain.<sup>1</sup> Surface finishing plays a primary role in the electronics, communications, and aviation/aerospace industries. These industries drive product miniaturization and demand increased product reliability. Present-day surface coatings are applied to parts in a manner that meets the designers' requirements while using chemical solutions that are environmentally friendly in both production processes and waste treatment.

Of the numerous elements in the periodic system, only about 16 are available as electroplated finishes. Of course, the number of coating processes increases when you include all of the alloy formulations.

Electroplating is adaptable, because it is used on tiny semiconductor parts as well as large industrial components. When to use a single-layer coating or a

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multilayer composite is based on expert opinion and experience with the coatings and how they perform. Electroplate coatings are not adaptable to all substrates, although most materials can be electroplated if proper preplating procedures are used. If a part is to be electroplated, some restraints on the design of the product may be imposed so that a satisfactory coating will result. Electroplated coatings are subject to rigid specifications. Control documents are provided by ASTM International as well as other associations, government bodies, and by the internationally recognized International Organization for Standardization (ISO).<sup>2</sup>

### 6.2 The Plating Cell

The purpose of this document is not to provide detailed directions for application of metallic coatings, as that is the expertise of the plater. The purchaser or engineer will find material informative in providing an elementary background in surface finishing. He will then know what can be expected of the coating and what is impractical.

All the coatings we discuss are plated out of a water-based chemical solution. The electroplating cycle includes a series of stations or tanks that will vary according to the type of part and the complexities of the plating process. Rinsing stations are provided between each processing station and after the final plating station to remove electroplating solution from the parts. The final rinse is critical to ensure that chemical salts do not remain and dry on the parts or cause the coating to corrode.

The plating cell consists of these components:

1. The rectifier or power supply. In the external circuit, it moves or pumps the electrons from the anode to the cathode.
2. Charged atoms, called *ions*, that carry the current in solution.
3. The electrode that is the source of the metal ions for the solution, and that provides the electrons for the circuit, is called the *anode* and is connected to the positive side of the rectifier.
4. The other electrode (the workpiece) is called the *cathode*. It is connected to the negative side of the rectifier and completes the circuit.

#### 6.2.1 Cathode reactions

The cathode is the negative electrode, and it represents the part being plated. The electrons on the surface of the part neutralize the positive charges on the metallic nickel ions in solution (Fig. 6.1). The net result is that metallic nickel is deposited on the surface of the part. At the same time, some of these electrons also neutralize the positive charges on hydrogen ions in the water solution. This forms hydrogen gas that is liberated at the surface of the part. This loss of hydrogen ions results in a higher concentration of hydroxide molecules and an increase in the pH of the solution at the workpiece–solution interface.<sup>3</sup> The more efficient the plating bath, the less hydrogen gas is formed. If the

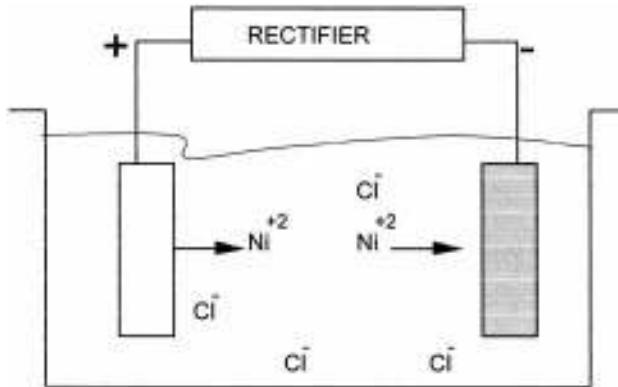


Figure 6.1 A galvanic (plating) cell.

concentration of metal ions in solution is low, or their movement to the cathode is impeded, the excess current can liberate additional hydrogen gas by splitting a water molecule.

### 6.2.2 Anode reactions

At the anode, electrons are removed from the metal electrode, and metallic ions are formed and released into the solution. This is the primary reaction with a soluble anode. Secondary reactions can also take place. One such reaction involves the generation and liberation of oxygen gas. This reaction also occurs when an insoluble anode is used as in precious metal plating. In this case, hydroxide ions in the aqueous solution supply electrons to the external circuit and produce water and oxygen gas.<sup>4</sup> It is important to avoid excessive anode current on soluble anodes, because the oxygen formed will react with the metal surface, forming oxides. These oxides interfere with proper anode dissolution. Like the cathode reaction, high current densities can split water but, in this case, it results in the release of oxygen gas and the production of hydrogen ions, which lowers the pH.

### 6.2.3 Cleaning

A typical processing cycle contains the steps of cleaning, rinsing, and activating the surface of the part prior to plating.<sup>8</sup> All the steps are important. Trying to take a shortcut in any of the processes can compromise the success of the operation.

The quality of the chemicals used in the various baths and the purity of the rinse water all work together to determine the overall quality of the product. Most mechanical processes, such as forming, machining and die casting, leave the substrate surface contaminated in some way.

Pretreatment cleaning is important to ensure good adhesion of the plating to the base metal. To remove contaminants from the surface of a part, in addition to chemical cleaners, physical work may also be incorporated. Grit or

bead blasting, scrubbing, media tumbling, and sanding are some examples. Solvent cleaning or degreasing involves a liquid and/or vapor immersion to remove solvent-soluble oil, waxes, and greases. (*Note:* environmental concerns may limit availability of some solvents.) Following the degreasing step is alkaline cleaning in the form of either a soak or spray operation. In many cases, the alkaline cleaning process is substituted for the solvent cleaning.

All alkaline cleaners contain chemical compounds that promote solution “wetting” of the surface. This allows the chemical formulations to attack and remove the surface soil and hold it in suspension.

More than 80 percent of plating “problems” can be traced back to improper surface cleaning and preparation. In the cleaning process, several energy forms may be used individually or combined to assist in soil removal. The most common of these forms are mechanical, thermal, electrical, and chemical. An example of the mechanical assistance is ultrasonic cleaning, which often is the only way to loosen a contaminant. Most cleaning processes do not make the contaminant disappear. Solution filtration is necessary to extend the life of most cleaners.<sup>5</sup>

Typical alkaline cleaner ingredients are sodium hydroxide, sodium metasilicate, sodium carbonates, and sodium phosphates. Sodium hydroxide (caustic soda) provides alkalinity, conductivity, and saponification (converting animal fats to water-soluble soaps).<sup>6</sup>

After the soil is removed from the surface of the part, the cleaner must keep it from redepositing. Other chemical components in the cleaners are the sequestering agents, chelating agents, deflocculating agents, and peptizing agents that aid in solution soil retention.

The sodium metasilicate provides soil dispersion and prevents redeposition. It also acts as an inhibitor to reduce alkaline cleaner attack on the active metal surfaces. Surfactants are surface-active agents that promote solution wetting of the surface by lowering the surface tension of the aqueous solution. These may be ionic or nonionic in structure.

Sodium carbonate in the cleaner acts as a buffer to stabilize the pH of the solution.

Phosphates improve rinsing quality and provide water conditioning.<sup>7</sup> (Some localities prohibit phosphate use, because they promote algae growth in lakes and rivers.)

Electrocleaning is usually the last (but a very important) step in most cleaning cycles.<sup>9</sup> There are three common types of electrocleaning. The first is *forward (direct)* or *cathodic*. In this process, the part is made to be the cathode, as is typical in plating. The second is *reverse* or *anodic*, in which the part is made to be the anode. The third is *periodic reverse*, wherein the advantages of both types are employed. Some processes may avoid the use of electrocleaning for various reasons, e.g., attack on active or light metals such as aluminum, magnesium, or zinc.

The cathodic reaction releases hydrogen and has the greatest gas evolution, hence the greatest amount of cleaning through the scrubbing action of the liberated gas. It also reduces oxide films on the surface, which promotes adhesion of the plating. The drawback is that it deposits smut. Smut is a metallic

contaminant from the solution that forms on the surface of the part as finely divided particles. The anodic reaction releases oxygen gas and does not produce this smut, but it will help remove any that has deposited on the surface. Thus, the anodic direction is more tolerant to metal contaminants that have accumulated in the cleaner. The downside of anodic cleaning is the generation of an oxide film on the part, which can passivate the surface (i.e., interfere with deposit adhesion).

Periodic reversal combines best features of both reactions.

All cleaners become contaminated with use. If you experience poor bonding between the plating and base metal, the cleaning step is suspect. Residual alkaline films remaining on the surface of the part after cleaning are difficult to remove by rinse alone. For this reason, an acid dip or *pickle* is used to neutralize this film.

The acid chosen will also remove any residual light surface oxides and microetch (lightly attack) the surface to improve bonding. Heat-treat scales or heavy oxides present on the surface are best removed in more concentrated or heated acids, away from normal production processes. All metals above hydrogen in the electromotive force (EMF) series (Table 6.1) react with the acid to form hydrogen gas. Caution should be observed when pickling high-strength alloy steels, because they are susceptible to absorption of hydrogen that can lead to hydrogen embrittlement of the steel.

**TABLE 6.1 EMF Series**

Anodic end	Standard potential volts at 25°C
Aluminum	-1.66
Zinc	-0.76
Iron +2	-0.45
Cadmium	-0.40
Nickel	-0.25
Tin	-0.137
<i>Hydrogen</i>	0.00
Copper +2	+0.34
Copper +1	+0.52
Silver	+0.80
Gold +1	+1.68
Cathodic end	

#### 6.2.4 Current distribution

Figure 6.2 illustrates an important aspect of electroplating—the current distribution on the surface of a part.<sup>1</sup> In plating, you are concerned with the vari-

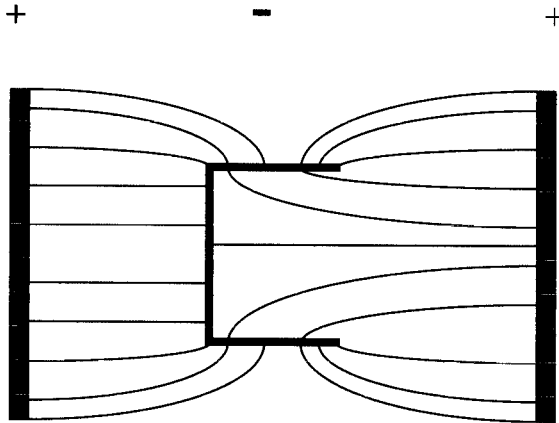


Figure 6.2 Current distribution box.

ations in thickness of the plated metal on a part. In almost all rack plating, some areas of the articles will be nearer to the anodes than others, and, with most plating solutions, these areas will receive a heavier deposit than those farther from the anodes.

The current flow lines depicted in the diagram flow from the anode (+) to the cathode (-) and are close together near the edges and on the outside corners of the part. Notice in the diagram that the current flow lines are farther apart in the bottom and at the inside corners of the part. These lines represent the current density or current concentration. Obtaining a uniform current distribution over the entire cathode surface is extremely difficult and seldom achieved in practical plating practices. The outside corners of the box may have as much as ten times the current density as the inside corners.

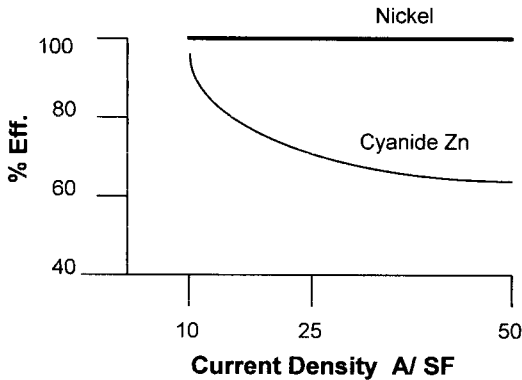
In many common plating baths, the metal deposit thickness can vary by this tenfold factor. Blind holes should be avoided on parts to be plated, as it is difficult to get any plating or coverage in these holes. The ability of a plating solution to produce deposits that are more uniform in thickness over a shaped cathode is known as the *throwing power* of the solution. An important factor influencing thickness distribution in some plating solutions is the decrease in plating efficiency with an increase in current density.

Current density is expressed in amperes per square foot ( $A/ft^2$ ). Figure 6.3 depicts the relationship between current density and plating bath efficiency for an acid nickel bath and a cyanide zinc bath.

Nickel deposition (efficiency) is seen as relatively constant over the range of 10 to 50  $A/ft^2$ . This means that nickel will plate about five times faster at 50  $A/ft^2$  than it will at 10  $A/ft^2$ . This gives a thicker deposit at the higher-current-density areas of a part.<sup>3</sup>

The behavior of the cyanide zinc bath is quite different. As the current density increases, the plating efficiency drops. Increasing amounts of hydrogen gas are produced at the cathode. As a result, the zinc deposits thickness variation will be about 2.5 to 1, not 5 to 1 as in the nickel plating. In the cyanide





**Figure 6.3** Plating efficiency vs. current density, nickel bath compared with a cyanide-zinc bath.

zinc bath, the metal distribution will be more uniform in thickness. Again, the term *throwing power* is used to describe this characteristic of deposit thickness uniformity. Because uniform deposit thickness over the surface of a part usually cannot be expected, it is important to specify those surfaces considered to be significant for proper operation or appearance of the part. These areas should then be specified as critical and an agreement reached beforehand between the purchaser and the plater as to ensure the minimum or maximum plating thickness required.<sup>11</sup>

Plating time is also a factor in controlling the deposit thickness, as is the total surface area of the part. The amount of metal deposited is controlled by the amount of current that flows in the circuit and the length of time the part spends in the plating bath. Although this is a very simplistic explanation, all plating processes follow this principle.

### 6.2.5 Deposit quality

Pinholes or porosity are common in all plated deposits. These openings through the plating will allow the underlying material to be attacked. Increasing the thickness of the coating reduces the amount of porosity at the expense of time and materials. In most cases, coatings of 1.5 to 2.0 mils in thickness have no pinholes. There are other ways of reducing the deposit porosity, such as pulse plating or the use of chemical additives in the plating bath. By using multiple plating layers, you minimize the effect of porosity and in effect improve substrate corrosion resistance. A deposit that is uniform in thickness, with no thin spots or skipped plating, provides good protection for the base metal.<sup>12</sup>

### 6.2.6 Brush plating

In the brush plating technique, the plating solution is carried to the part instead of the part being immersed in a plating bath. Most metals can be brush plated, and aluminum parts can also be anodized. This process can be used

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both in production and as a repair tool. The handle, called a *stylus*, has absorbent material wrapped around a carbon rod, which is connected to the positive side of the power supply. The negative pole of the power supply is connected to the part. The absorbent material is dipped into the plating solution and then swabbed or brushed along the area on the part that requires plating. Areas that are not intended to be plated are masked to protect them from the chemicals. Figure 6.4 details a typical brush-plating setup.<sup>20</sup>

## 6.2.7 Copper

Copper can be electroplated from acid, alkaline, and neutral bath formulations.<sup>2</sup> Each of these plating solutions has unique features to provide a very economical electrodeposition of copper on complex shapes. There are safety and environmental concerns associated with any plating process, and one always needs to address the chemical treatment and safe disposal of wastes to prevent pollution. Federal, state, and local regulations include restrictions for copper discharge. Copper is rarely used as the final finish, because its brightness is quickly lost in most atmospheres as a result of oxidation and surface corrosion. However, it performs a supportive role as an underplate for nickel, gold, tin, and other top coatings.

## 6.3 Acid Copper Plating

Copper coatings are popular because of copper's high electrical and thermal conductivity as well as its high melting point.<sup>21</sup> The electronics industry requires copper for properties such as solderability, corrosion resistance, high ductility, and low cost.

The acid copper sulfate baths are economical to prepare, operate, and waste treat. They are used in printed circuits, electronics, semiconductors, rotogravure, electroforming, and decorative and plating-on-plastics applications. In addition, the fine-grained structure of the deposit makes it ideal for producing sharp and well defined boundaries after machining or etching.<sup>23</sup>

The physical properties of the deposit, such as brightness, ductility, leveling, freedom from stress, and fine-grained deposits, are controlled through the

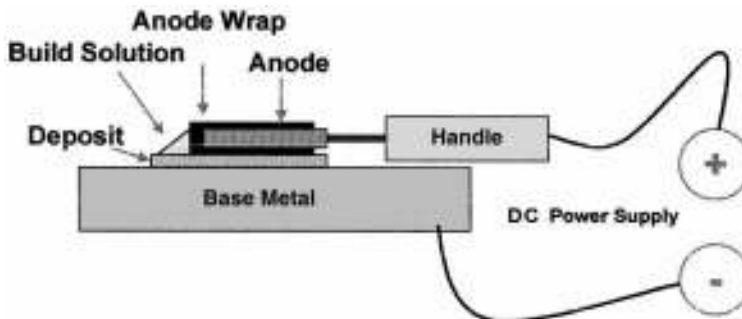
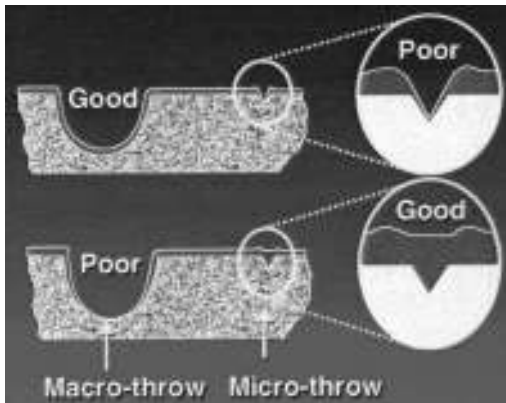


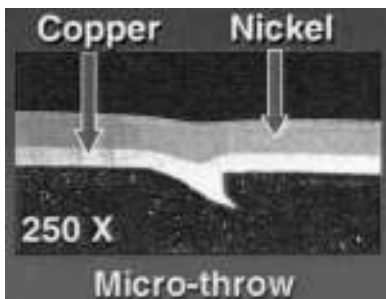
Figure 6.4 Typical brush-plating setup.

use of chemical addition agents.<sup>22</sup> Acid copper is desirable as an undercoat to nickel and chromium on zinc-based die castings because of its very good *micro-throw* and excellent ductility (Fig. 6.5). Elongation of 15 to 25 percent is common. Micro-throw is the ability to fill surface defects such as microporosity and other basis metal flaws. Fine-grained crystal structure and low stress are inherent in the deposits while plating at very high speeds. The use of proprietary addition agents, along with various DC wave forms such as pulse, square wave, or periodic reverse, combine to produce copper surface smoothness that is better than that of the substrate over which it is plated. It also provides an ideal metallic undercoat for plating on plastics. Leveling is the ability of the deposit to fill in minor surface defects and present a smooth surface finish (Fig. 6.6). Acid copper levels well, and its ductility and freedom from stress assist in overcoming differences in coefficients of expansion and contraction between subsequent plates and the plastic base material. This provides a thermal cushion when the workpiece is subjected to acceptability tests such as thermal cycling or solder float testing.

The acid copper electrolyte is prepared by dissolving copper sulfate in water and adding sulfuric acid, a small amount of chloride, and the specified amount of addition agents. The ability of addition agents to provide brightness and



**Figure 6.5** Depiction of macro-throwing and micro-throwing power. (Optical photo courtesy of F. Alt-mayer, Scientific Control Laboratories.)



**Figure 6.6** Leveling of acid copper over defect in zinc diecast.

leveling is influenced adversely by elevations in operating temperature. Therefore the bath operates slightly above room temperature up to 90°F (32°C). Operation above this temperature consumes extra amounts of brighteners; while not a drawback, this does increase the cost of operation. Because the bath does contain sulfuric acid, it is corrosive (Fig. 6.7).

The acid sulfate plating solution can tolerate large quantities of zinc and iron contaminants with the plating speed being affected only slightly. Chromium contamination affects the deposit quality at concentrations above 100 parts per million (ppm). One part per million is equal to 1 mg of contaminant per liter of solution. Organics will cause the deposit to become pitted, dull, and/or coarse-grained, with some burning of the deposit in high-current-density areas. In addition, the deposit can also become striated and experience a loss of leveling. Both air agitation and constant bath filtration are required to produce good deposits. Air supplied for agitation must be from a low-pressure blower, not “shop air” from a compressor. Compressed air can introduce organics in the form of lubrication oil. The chloride ion concentration is carefully maintained at specified levels to enable the addition agent to perform its function of providing all the desirable physical properties previously discussed. The very low levels of chlorides present in the bath require that anodes containing small amounts of phosphorus are used for good anode corrosion and to produce optimal deposits. These anodes must be bagged to prevent particulate material from the anode getting into the bath and causing rough deposits.

When plating copper on steel or zinc die castings, they must first have an appropriate strike of copper from a copper-cyanide bath.<sup>22</sup> This is to prevent immersion copper deposition from the acid bath from forming on the substrate. Typically, immersion coatings are nonadherent and undesirable. The cyanide copper strike will also prevent attack on the zinc metal from the acid in the acid copper bath.

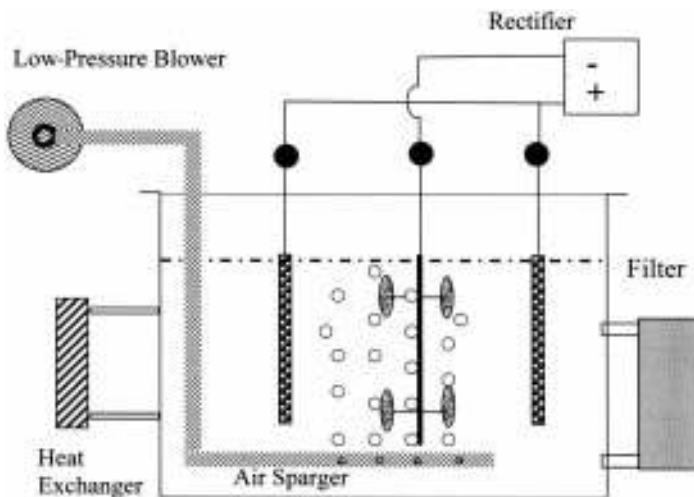


Figure 6.7 Example of an acid copper plating tank.

## 6.4 Cyanide Copper Plating

Electroplated copper from cyanide-based plating solutions has long been used both as an engineering or decorative finish and as an undercoat for other plated metals. Cyanide copper solutions are used on a wide variety of base materials. An important property of copper deposited from cyanide-based systems is its ability to form strong adherent bonds to most base metal and alloy substrates. Because acid copper plating solutions attack most basis metals and/or produce immersion deposits with poor adhesion, cyanide copper plating is used as a thin undercoating or strike to produce good adhesion.<sup>3</sup> Following the strike, a high-speed acid copper plating formulation can be used to produce the desired film thickness.

Cyanide plating solutions are highly poisonous, and the rinses and spent bath solutions must undergo complete destruction before disposal. Allowable cyanide in wastewaters is very small, and waste treatment is required in all areas. However, it should be recognized that cyanide destruction technology is well established and proven effective.<sup>16</sup>

Because deposits from cyanide plating solutions exhibit good throwing power, more complicated shapes can be completely covered, with a uniform film thickness. This is a result of the relationship of efficiency and current density. As the current density increases, the bath efficiency decreases. There is a drawback that must be addressed. The drop in plating efficiency yields an increase in the formation of hydrogen gas. This evolved gas can be absorbed by the base metal. The result can be a reduction of the metal's fatigue strength by hydrogen embrittlement. To relieve hydrogen embrittlement when plating on hardened steel (Rockwell C35 or higher), the parts are baked within 4 hr after the final plating operation at  $325 \pm 25^\circ\text{F}$  ( $162 \pm 14^\circ\text{C}$ ) for up to 24 hr.<sup>22,26,31</sup> Periodic reverse plating cycles in cyanide copper baths have been used with some success in producing fine-grain deposits with good leveling.

Plating of parts with cyanide copper will continue with little change in total volume until a suitable and environmentally acceptable system can replace it. The ability to plate an initial coating with good adhesion to light metal base materials with good throwing power and coverage are the key features of cyanide copper systems. The associated cyanide destruction, disposal costs, and safety measures required in cyanide handling can be accomplished with proper education and training.<sup>22</sup>

## 6.5 Pyrophosphate Copper

Copper pyrophosphate plating baths require more control and maintenance than cyanide or acid copper baths. They are relatively nontoxic and primarily used in electroforming operations and on printed circuits.<sup>23</sup> The operational temperature range of 110 to 140°F (43 to 60°C) should not be exceeded; above these temperatures, the pyrophosphate complex is hydrolyzed to orthophosphate. The orthophosphate formed will degrade the solution. Copper pyrophosphate baths are sensitive to organic contamination, addition agent breakdown products, and lead, all of which can cause dull, nonuniform depos-

**6.12 Chapter 6**

its with a narrowing of the plating range. The bath produces deposits that exhibit high purity and ductility along with nearly 40 percent elongation.<sup>25</sup> This was especially useful in the printed circuit industry for plated-through holes on thick multilayer boards, which require strong deposits to withstand the z-axis expansion during soldering and thermal cycling operations. The deposit also has high tensile strength of  $40,000 \pm 2000$  psi and low internal stress.<sup>22</sup> Improvements in substrate material and product design changes have reduced z-axis expansion, allowing the use of lower-cost nonpyrophosphate baths. The biggest drawback to the system, besides bath control, for the printed circuit industry was that the photoresists used in the pattern plating operation were dissolved by the bath's alkalinity. The bath is less corrosive to equipment than the acid copper and less toxic than the cyanide processes.<sup>22</sup> This bath can be used to deposit copper directly on zinc die-cast parts, steel, and zincate prepared aluminum.

**6.5.1 Other copper plating processes**

There is continuing development of a noncyanide alkaline copper bath. This type of bath would replace the cyanide bath for plating directly on zinc die-cast and steel. Presently, these formulations have found limited use in industry.

The fluoborate copper bath formulation allows very high current densities and increased plating speed. This is because the copper salt is highly soluble, and large amounts of it can be dissolved in water. The biggest drawback to fluoborate copper is the extreme corrosivity of the solution. Everything associated with the plating operation must be constructed of noncorrosive materials.<sup>22</sup> The bath operation is similar to the acid sulfate copper bath. Organic contaminants affect the deposit appearance and ductility. The other mechanical properties are only slightly affected by organics. Lead is the only metallic contaminant that is a problem in this bath.

**6.6 Nickel Plating**

The nickel plating processes are used extensively throughout the world for decorative, engineering, and electroforming purposes. Decorative electroplated nickel coatings are lustrous, smooth, and mirror bright. Engineering nickel coatings are smooth and matte in appearance and are most often applied to improve corrosion performance of industrial equipment. These pure nickel deposits can provide hardness and also can be used to control wear, surface erosion, and lubricity. Nickel is valued for its magnetic and electromagnetic characteristics and for optical properties such as reflectivity, emissivity, and absorptivity.<sup>1</sup> In electronics applications, nickel coatings are widely used as underlayers beneath precious metal deposits wherein the nickel acts as a barrier to prevent interdiffusion of substrate and coating. Additionally, this nickel barrier improves the reliability of electronic components. Nickel coatings thus enhance the value and expand the operating range and usefulness of industrial equipment and electronic components.<sup>6</sup>

Nickel coatings are most widely applied by electro-deposition from aqueous solutions. They can also be applied by electroless (autocatalytic) techniques,

by chemical and physical vapor deposition processes, and by thermal spray methods.

The solutions for decorative nickel plating differ from those for engineering applications in that they contain multiple addition agents. Fully bright deposits, for example, contain significant amounts of codeposited sulfur. The most common nickel solution used is the Watts nickel bath, which is based on nickel sulfate as the source of nickel (Mil-Spec QQ-N-290).

Soluble nickel salts can be irritating to skin and eyes and, in some cases, physical contact with nickel or certain nickel compounds may cause allergic dermatitis. Engineering coatings using sulfamate nickel plating are controlled by MIL-P-27418. This is a pure nickel that is generally used for functional or engineering purposes rather than for decorative purposes, because it provides good corrosion resistance and high-temperature stability. For electroforming and most electronic applications, a bath using nickel sulfamate as the metallic salt is preferred, as this coating can be produced with compressive or low-tensile stress.<sup>1</sup>

The sulfamate bath uses soluble sulfur depolarized nickel anodes, whereas the Watts bath anodes do not contain sulfur. The anodes for both baths are bagged because, as the anodes corrode, they can release small nickel particles called *fin*s. The bag helps to trap these fines and keeps them from coming in contact with the part; thus, it helps to prevent rough deposits. Continuous filtration of the bath is recommended with filter sizes ranging from 5 to 20  $\mu\text{m}$ .

Good agitation and solution circulation are recommended to produce the best deposits. Keeping contaminants low is an important factor in maintaining low stress and good quality deposits from both Watts and sulfamate plating solutions. In addition to affecting deposit appearances, contaminants can cause other problems such as lower cathode efficiencies, reduced throwing power and covering power, excess pitting, and poor adhesion.<sup>26</sup> It should be noted that the effect of these impurities could be additive, and many impurity effects are more pronounced at certain current densities. For this reason, regular purification of the solution is necessary to control contaminants and minimize their effects.

Metallic contaminants such as copper, lead, and zinc can be removed from both nickel solutions by *dummy* (i.e., low-current) electrolysis using corrugated cathodes at a current density of 2 to 5  $\text{A/ft}^2$ .<sup>27</sup>

Organic contamination may be removed from the nickel solution by treatment with activated carbon. Iron and chromium can be removed from the solution by precipitation. Their hydroxides become insoluble when you raise the pH of the bath to 5.0.

Generally, electrodeposits from a sulfamate nickel bath are used on electronic components as a barrier coating. Ultra-high-purity formulations are available that allow plated parts to be formed, bent, and crimped without damage to the deposit.<sup>28</sup> Most sulfamate bath formulations produce deposits that have good tensile strength and low deposit tensile stress. The baths can also produce compressively stressed deposits. This is useful in high-speed strip line or reel-to-reel plating (see Table 6.2).

TABLE 6.2 Mechanical Properties of Electrodeposited Nickel\*

Bath	Hardness, HV	Tensile strength, psi	Elongation, % in 2 in (51 mm)	Internal stress, psi
Watts	130–200	50–70 ( $\times 10^{-3}$ )	20–30	+25 to +65 ( $\times 10^{-3}$ )
Sulfamate	170–230	60–110 ( $\times 10^{-3}$ )	5–30	–5 to +15 ( $\times 10^{-3}$ )

\*Without addition agents

Deposit characteristics can be varied as desired over a wide range. Chemical additives such as organic sulfonic acid salts and other sulfur-bearing compounds have been used as hardening agents and stress-reducing agents. These additives can reduce tensile stress or increase compressive stresses as well as increase deposit hardness, brittleness, and tensile strength. It is important to note that certain additives will incorporate sulfur compounds in the deposit. Removal of these compounds from the bath, once added, is difficult.<sup>28</sup>

Barrel plating with sulfamate nickel can lead to some problems if care is not taken in the process. Very pure nickel deposits passivate easily when current is interrupted, as happens in barrel plating. This results in a deposit that, when viewed under the microscope in cross section, appears as laminated layers.

The plating layers can separate at the laminations when stressed. A simple troubleshooting procedure to use when you have a plating defect wherein the gold plating over the nickel plate is peeling is to look at the bottom side of the gold blister for the appearance of nickel. If you see nickel, then the layers of nickel plating are separated because passivation of the nickel layer occurred during the plating. If nickel is not present on the bottom side of the peeled gold, then there was passivation of the surface between the nickel and gold plating steps that resulted in poor adhesion. If the substrate material is visible under the peeled layers, then the part was not properly cleaned and activated prior to plating.

## 6.7 Precious Metals

The precious metal group is also referred to as the *noble metals*. Both names are appropriate. They have high monetary value and show marked resistance to chemical reaction with inorganic acids. The plating application for these metals is determined by the metal's particular properties and characteristics.

Eight metals compose the precious metal group, as indicated in the bottom two rows of Table 6.3.

The following are some of the factors to consider in the selection of a precious metal for a particular application:<sup>21</sup>

- Contact characteristics
- Reflectivity
- Corrosion resistance



TABLE 6.3 Position of the Precious Metals in the Periodic Table

	26	27	28	29	←	Atomic number
	Fe	Co	Ni	Cu	←	Chemical symbol
Light group	44	45	46	47		
	Ru	Rh	Pd	Ag		
Heavy group	76	77	78	79		
	Os	Ir	Pt	Au		

- Solderability
- Heat resistance
- Wear resistance
- Color
- Cost

Each of the precious metals has both advantages and disadvantages. The following information highlights this. Silver provides low cost, but it does tarnish when exposed to sulfur. Gold provides low electrical resistivity but, at 24-karat purity, it is a soft, easily smeared coating. Palladium does not cold weld, but material costs are high.

Although the cost must be considered, it is secondary to the required properties. As an example, the plated finish on a PWB tab or separable electronic connector should display certain characteristics. These could include high corrosion and oxidation resistance, low contact resistance, low stress or high ductility, and low porosity. A uniform appearance and smooth surface topography are aids in functionality for this type of part.

### 6.7.1 Silver

Silver is a low-cost metal, has excellent thermal properties, and is the best conductor of electricity. The penalty for silver is that a black, brown, or yellow tarnish forms on the surface when it is exposed to sulfur. The tarnish formed raises the surface contact resistance. The poor resistance of silver to corrosion, tarnishing, and ion migration must be considered if you are specifying a silver coating. As with copper, postplating surface treatments of silver can reduce or prevent the formation of tarnish.<sup>4</sup> Commonly used surface treatments include protective lacquers and acrylic or epoxy films. There are also chromate conversion coatings per MIL-S-365 and organic preservatives that protect and still allow for a solder joint to be formed with the silver.<sup>30</sup> The last and most expensive treatment is to overplate the silver with 0.1 to 0.3  $\mu\text{m}$  of rhodium. This is generally not cost effective but works quite well. Typical silver thickness requirements for electronic contacts are 50 to 250  $\mu\text{in}$ ; this is generally applied over 150–300  $\mu\text{in}$  of nickel.

Of major concern when specifying silver plating is ion migration.<sup>2</sup> Silver ions under the influence of a high DC potential can move across insulated surfaces. This is prevalent in areas of high humidity. The ions can be reduced

back to silver metal atoms, and the tracks formed by this metal migration between two conductors can lead to electrical shorts. The methods employed to prevent this migration include wide spacing of adjacent tracks, the use of conformal coatings to prevent moisture intrusions, and overplating the silver surface with gold, rhodium, or platinum. Any discontinuities in the protective coating can expose the base silver, and ion migration can still occur.

A silver strike is always used before plating silver to avoid immersion deposition.<sup>4</sup> An immersion deposition, in many cases, is a nonadherent thin layer of the metal. This low- or nonadherent film would allow the functional plating to flake off under stress. With iron base material, a double strike is sometimes used. The first is a silver-copper cyanide alloy followed by silver. Always enter the silver strike bath “HOT,” i.e., current on with the part as the cathode.<sup>1</sup>

The common practice for plating silver on nickel alloys is to use a Woods nickel strike, which precedes the silver strike for improved adhesion of the final plating. Compounds that contain sulfur, selenium, or tellurium are the most common chemical brighteners for silver baths and are called *addition agents*. They are used to improve the surface characteristics of the deposit.

The most widely used agents perform multifunctional duties that include brightening, hardening, and grain refinement. Most organic brighteners used for silver are unsaturated alcohols and long-chain polar molecules. They are essentially surface-active agents (surfactants).

Antimony is the most powerful brightener and is used at 2 to 3 percent by weight. It produces beautiful silver deposits that are quite hard.<sup>4</sup> A major problem using antimony as an addition agent is that the deposit produced has only 10 percent of the conductivity of pure silver; therefore, the antimony brightened bath should not be used when plating electrical contacts.

Silver anode purity is generally expressed in parts per thousand. The manufacturer processes it to have a fine grain structure. Some suppliers recommend bagging the anodes for silver plating. Sloughing of anode particles into the plating bath can cause grainy or nodular plating, because these particles find their way to the cathode. Another costly anode problem is an accelerated state of stress-assisted corrosion that occurs when a small piece of anode breaks off, loses electrical contact, and is of no further use as anode material. Continuous bath filtration is recommended, which will remove most of the sloughed anode particulate from the bath along with any other suspended contaminant.

### 6.7.2 Rhodium

Rhodium has been used extensively for electronic applications that require wear resistance and stability at high temperatures. The high metal costs have minimized the application of heavy deposits. Rhodium is plated from very strong acid solutions, and these baths operate at low current efficiencies, generating considerable amounts of hydrogen gas.<sup>4</sup> Thicker deposits from proprietary systems contain additives for stress control and are almost always applied over an underplate of gold, silver, or nickel to avoid immersion deposition and solution contamination.<sup>16</sup> Rhodium has high and stable reflectivity in

the visible range, hence its appeal as a top coating in jewelry. The metallic color of rhodium is similar to that of stainless steel. This metal has excellent corrosion resistance and is almost as hard as chromium. In most cases, rhodium is plated directly over nickel, with the use of a nickel strike on most base metals to prevent immersion deposits. When plating rhodium on steel parts that exceed Rockwell C40 hardness, the parts must be baked within four hours of plating to reduce hydrogen embrittlement.<sup>31</sup>

### 6.7.3 Palladium

Palladium has been suggested as a replacement for gold, because it is harder than gold and does not cold weld. It has a low melting point and a density of  $12.02 \text{ g/cm}^3$ . When compared to gold of equal thickness, the palladium deposit weighs about half as much as gold. Because you buy precious metal plating salts in troy ounces but sell the deposit by thickness, this cost difference once was attractive. However, the increased cost of palladium salts in recent years has diminished the dollar savings. In the past, there were drawbacks to using palladium because of difficulty in obtaining low-stressed noncracked deposits. The baths presently in use are of the ammoniacal, chelated, or acid formulations. New palladium bath formulations are proprietary but allow for simplified chemical control and produce thicker deposits without cracking. They differ from the older-generation baths mainly in the use of additives for brightening and stress relief.<sup>4</sup> Palladium plated from these baths provides a deposit that is very low in surface porosity.

### 6.7.4 Gold

Gold is a relatively expensive coating, has low electrical resistivity, and provides low surface contact resistance, because it does not form surface oxides. Gold deposits of 99.99 percent purity (24 karat) smear under load and will easily bond (cold weld) to another gold surface, because it is such a soft metal. In separable connectors or contacts, the gold is alloyed with small amounts of other metals such as nickel, copper, or cobalt, to increase the deposit hardness.

For many years, the standard for electrical contacts has been an electro-deposited layering of nickel, at least  $50 \mu\text{in}$  thick, followed by at least  $30 \mu\text{in}$  of hard gold, then a 5- to  $10\text{-}\mu\text{in}$  thick layer of soft gold. This combination is usually accepted as the nearly ideal surface.<sup>30</sup>

The double gold layer serves to reduce surface porosity, which improves corrosion resistance, and the soft gold topcoat provides lubrication to the mating surface. This plating combination can also be easily soldered and, in some applications, wire bonded. Table 6.4 indicates different applications and the preferred plated gold thickness.

The precious metals also have some special properties that make them attractive. Platinum resists corrosion and serves as an anode in plating paths that contain chlorides. Gold has high reflectivity in the infrared region.

**TABLE 6.4 Deposit Thickness Requirements for Gold Plating**

Thickness, $\mu\text{in}$	Purpose
1–7	Flash color decorative coating
10–30	Minimum for solderability on contacts
30–50	Minimum for weldability on contacts
50–100	Etch resist and solderability
100–200	Engineering for abrasion resistance
200–300	Exceptional corrosion resistance
500–1500	Electron emission characteristics
$\geq 1500$	Electroforming applications

In the early and mid 1990s, a great deal of attention was paid to using palladium as a substitute for gold. Since that time, increases in the palladium metal cost have tipped the scales back toward favoring gold.

Iridium is ideal for protection of refractory metals at very high temperatures.

Thickness requirements for precious metal deposits are determined by the end use. Prime consideration in the choice of finish should be given to the physical properties of the deposit and the service requirements of the part.<sup>21</sup>

Generally, most gold electroplating baths are proprietary and covered by patents. The choice of which bath to use will depend on the functional requirements of the gold coating and the substrate upon which it is plated. Three types of cyanide gold plating baths are available for use today.<sup>4</sup> One is alkaline, at a pH of 9.0 to 13. The neutral-type baths operate at pH 6.0 to 8.0, and the acid type at pH 3.0 to 6.0. Potassium gold cyanide salts supply the metal necessary for deposition and will also increase the solution conductivity and improve the throwing power of the bath. In addition to forming the gold cyanide complex, the cyanide reduces the free gold ion concentration in solution, which retards the deposition of base metals and minimizes the formation of immersion deposits.

The bond between gold and cyanide is very strong, which accounts for the high stability of the gold cyanide complex even under acidic conditions. The alkaline bath provides good throwing power, and the deposit has reduced amounts of codeposited base metals. The neutral and acid baths do permit alloy formation through base metal codeposition but will cause little or no attack on delicate substrates. The acid bath solution does produce the purest commercial gold deposits. Along with conducting salts and pH buffers, baths producing bright deposits will contain brighteners that promote grain refinement. Many of these brighteners are metallic in nature and usually codeposit with the gold. The amount of codeposition depends on the type of brightener used. The metallic brighteners not only affect the appearance of the deposit, they also increase the hardness. Organic brighteners change the appearance of the deposit but do not necessarily alter the hardness. All brighteners tend to reduce the density and electrical conductivity of the gold electrodeposits.

The gold concentration in the plating solution is kept relatively low with respect to other plating bath formulations to minimize gold metal loss due to chemical drag-out following plating. The neutral and acid baths do not contain any “free cyanide” like the alkaline baths, because the cyanide molecule would be unstable in the lower pH range. This absence of free cyanide in these baths allows for alloy deposits. Chelating agents are used in these baths to retard the deposition of metallic impurities that may be present. All nonadditive baths produce deposits that are matte in appearance but, if alloyed, the deposits are semibright to bright. The acid baths, when alloyed with various metals, can produce deposits with a wide range of colors from pale yellow to deep orange. Pure unalloyed matte-finish gold electrodeposits produced from the acid bath have been measured at 99.999+ percent purity.<sup>30</sup> A bright acid gold solution that does not use phosphates as pH buffers may contain small amounts of nickel or cobalt complexes as brighteners. The formation of an organic-cyanide polymer (Munier polymer) as an inclusion in the deposit appears to contribute to the good wear resistance of these coatings.<sup>30</sup> Other brightening additives such as arsenic or thallium may also be used. These refine the grain structure and increase the deposit hardness. Typical gold deposit requirements for semiconductor components and wire bonding are 99.99 percent purity with a 90 Knoop maximum hardness. For wirewrap connections, the deposit requirement is 99.7 percent minimum purity.

For solderability, the gold deposit should be 99.7 percent minimum purity, and the thickness should not exceed 50  $\mu\text{m}$ . A minimum of codeposited metals is desirable to maintain good solderability.<sup>28</sup> If you are plating finger tabs for printed wiring boards, a deposit purity of 99.0 percent is acceptable with a hardness value of 91 Knoop and up. The deposit thickness should not be more than 100  $\mu\text{m}$ . For plated separable connectors, many combinations of purity and hardness are acceptable, depending on the specific requirements for the part.

The military specification MIL-G-45204 is a good reference for gold plating. After proper cleaning and activation of the substrate, a gold strike is desirable. The strike bath prevents chemical contamination of the pure gold plating bath by drag-in from previous plating baths, and it promotes adhesion of the deposit by activating the surface. The gold strike also prevents immersion gold deposits from forming on most substrates. Poor adhesion of immersion deposits can jeopardize subsequent deposit adhesion.

Following the gold plating bath, recovery rinses are used to minimize gold plating bath loss through solution drag-out. The final rinse should be with high-quality deionized water. This is to eliminate any water residue drying on the gold surface. The final process step is drying the plated parts to leave the gold as clean as possible.

Gold deposit hardness should be specified for all plated parts. The hardness of the deposit affects the wearability of the deposit.<sup>26</sup> The wear resistance of the deposit increases with increased hardness. The most commonly used hardening agents are cobalt, nickel, and iron. Small amounts of these materials can have dramatic effects on the hardness of the deposit. A high-speed plating process for pure gold can give you a deposit that exceeds 90 Knoop hardness without using metallic alloying agents. This increase in hardness results from

## 6.20 Chapter 6

the plating process. Pulse plating and periodic reverse plating will also affect the deposit characteristics of gold. Depending on the selection of the duty cycle used in pulse plating, a gold deposit can be produced that will have a density equal to that of pure wrought gold at 19.3 g/cc.

## 6.7.5 Deposit hardness

Table 6.5 lists the typical hardness ranges encountered for electrodeposits employed as finishes in electronic applications.

**TABLE 6.5 Comparisons of Metallurgical Properties of Deposits**

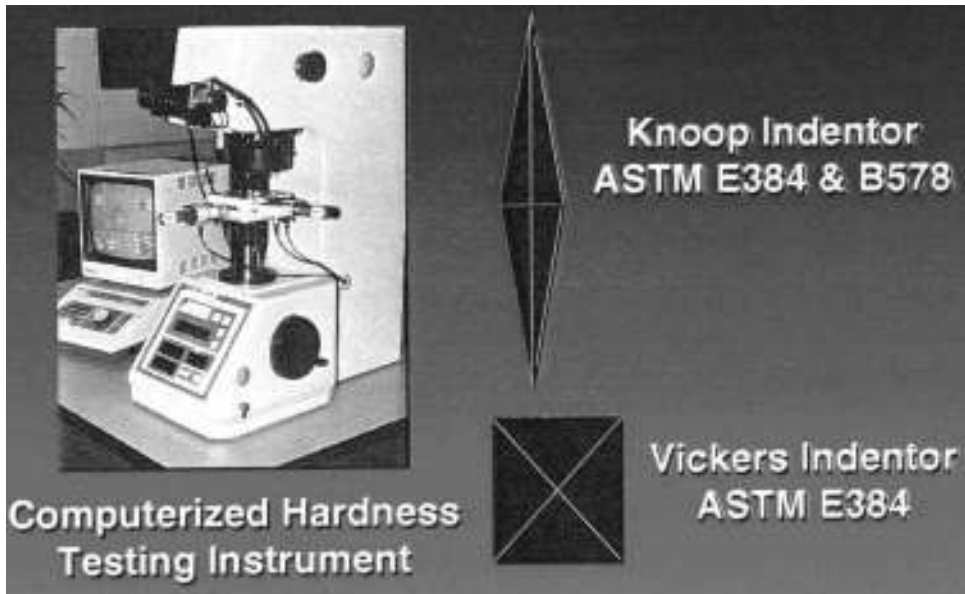
	Hardness, Knoop, 25 g load	Tensile stress, psi
Raw acid copper	100–120	1400
Bright acid copper	145–160	2000–4000
Cyanide copper		5000
Semibright nickel	250–350	
Bright nickel	500–700	
Chromium	700–1000	

To measure the hardness of a coating, a carefully prepared cross section of the part is marked with an indenter. The impression made in the coating is then examined under a microscope using a calibrated eyepiece. Knoop and Vickers are the most common hardness types. The Vickers indenter is a symmetric diamond, and measurements are the average length of the two diagonals. In contrast, the Knoop indenter is nonsymmetrical, and measurements are made of the long diagonal (see Fig. 6.8). Both types use a fixed load whose value should be identified with the presented data. The measuring instrument must be vibration free with no relative horizontal movement between indenter and deposit. The Knoop indenter has included angles of 130 and 172.5°, whereas the Vickers included angle is 136°. <sup>26</sup>

The best results are obtained with a metallurgical mount on a polished cross section. If you try to measure directly on a plated surface, you run the risk of a false value because of the anvil effect. The deposit tested directly on the plated surface must be sufficiently thick to prevent the substrate or underplate from compromising the reading. Be aware that work hardening of the deposit from the grinding and polishing operations is possible while producing the mount.

## 6.8 Deposit Performance

Temperatures exceeding 257°F (125°C) can degrade many types of electroplated finishes. Diffusion through the deposit grain boundaries and deposit po-



**Figure 6.8** Knoop and Vickers impressions for deposit hardness testing.

rosity will allow the movement of base metal atoms to the surface of the deposit.<sup>31</sup> These diffused metals are now exposed and can oxidize. The oxidized metals will increase the contact resistance of the deposit, which can lead to device failure.

Occluded polymers in the hard gold plating can also contribute to increased contact resistance. Hard gold samples exhibit significant increases in contact resistance after exposure to 200°C for 2000 hr.<sup>26</sup> Variation in solution composition, current density, and temperature can also affect the concentration of impurities in a deposit.

It is very important to analyze the deposit as well as the plating solution. Plating solution analysis is necessary for proper bath maintenance and can warn of accumulating metallic impurities. Specific analysis for hardeners and alloy constituents is also done on the plating solutions to control the bath composition and make sure the bath is operating within the manufacturer's specifications.

In general, gold deposits require an underplate. In most cases, a gold strike is used on top of the underplate. Typical underplates are nickel deposits, which provide a diffusion barrier to copper and copper-based alloys at high temperatures.<sup>31</sup>

For low-temperature applications, you can use copper as a diffusion barrier over brass alloys to retard the movement of zinc to the surface of the gold. A tin-nickel alloy is also a good corrosion-resistant deposit that promotes solderability, but the deposit is brittle.

Silver has severe drawbacks for high-reliability applications. It has excessive ion migration and cannot be used as underplate on military hardware.

Palladium-nickel alloys have bright, hard deposits that show little tendency to microcrack. The typical alloy composition range is 40 to 99 percent Pd. The various alloy compositions exhibit good chemical stability and are fairly wear-resistant. A typical hardness range for them is 450 to 600 Knoop. The alloys have a slight material cost savings over pure palladium. Table 6.6 provides a comparison of hard gold, palladium, and palladium-nickel films.

**TABLE 6.6 Comparison of Film Properties of Hard Gold, Palladium, and Palladium-Nickel<sup>4</sup>**

	Gold	Palladium	Palladium-nickel
Hardness (KHN 25)	140–200	450–600	450–550
Hardening agents	Co	Additives	Ni + additives
Grain size, Å	200–250	50–200	50–220
Density, g/cc	17.3	11.75	10.73
Ductility, % elongation	2.3–3.5	>9	>9
Volatile impurities, wt%	<1.5	<0.5	<0.1
Bulk thermal			
Stability, °C	150	>450	380
Porosity, pores/cm			
0.5 μm thick	60	80	20
1.0 μm thick	20	20	<10

## 6.9 Pulse Plating

In pulse plating, the metallic coating is deposited by pulsed electrolysis. Pulse plating can be defined as *current-interrupted electroplating*. Interrupted current consists of a direct current applied for a specific time period and then returned to ground (0 V) for another specific time period.

Pulse plating is useful in certain cases in which improved characteristics of electrodeposits are desired. It benefits the electronics industry by producing deposits with low porosity resulting from the higher deposit density. Pulse plating can produce a gold deposit with high purity and good ductility; it can control the deposit grain size and structure and produce a surface with low electrical resistance.<sup>29</sup>

For many years, the plating industry used current interruption (CI) to improve the performance of the deposit. The main difference between CI and pulse plating is length of time. The CI cycle is generally a matter of seconds, whereas pulse cycle is in milliseconds. The frequency of the pulse, the duty cycle used, and the waveform selected will determine the rate of electroplating within the parameters of any given electrolyte system. The duty cycle is de-



defined as the current time on ( $T_{on}$ ) divided by the current time on plus the current time off ( $T_{on} + T_{off}$ ).<sup>29</sup> Because the duty cycle is expressed as a percentage, you need to multiply your answer by 100. Therefore, a sequence of 2 ms on followed by 8 ms off would be a 20 percent duty cycle. Because the peak current in pulse plating could be five times greater than that used in straight DC, the plating time would not necessarily be longer.

The square and periodic reverse square are generally accepted as the standard pulse waveforms. Figure 6.9 shows an example of these waveforms. Many other waveforms can be used to produce unique deposit characteristics.

### 6.9.1 Electroless plating

Electroless plating is a controlled electrochemical reduction of aqueous metal ions onto a catalytic surface. Electroless plating baths do not utilize anodes or power supplies. A chemical identified as a reducing agent, with the help of the catalytic surface, converts the metallic ions into deposited metal at the surface of the part. This chemical process requires close control of the plating solution composition and conditions. In the electroless nickel process, the nickel alloy deposited is the catalyst, and the electrochemical reduction reaction to produce additional nickel metal is sustained by that deposit.<sup>14</sup> The process is referred to as *autocatalytic*. In all electroless baths, the metal ions are complexed to provide solution stability in the presence of the reducing agents used. All baths contain the following components:

1. A source of metallic ions
2. A reducing agent
3. Complexing agents
4. Reaction inhibitors and stabilizers

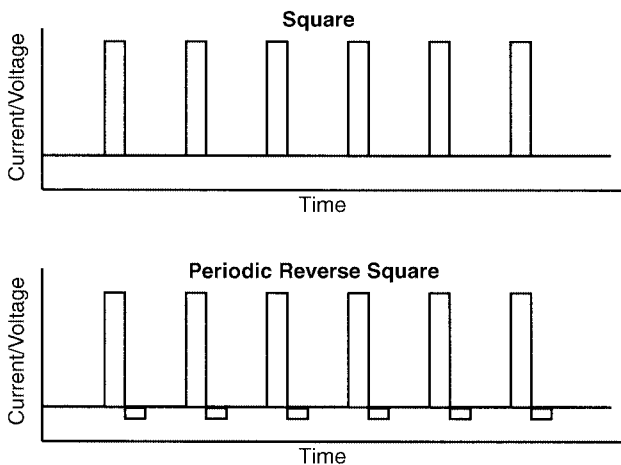


Figure 6.9 Pulse plating waveforms.

Energy in the form of heat generally drives the reaction and, of course, the solution becomes contaminated with reaction by-products. Electroless nickel is the most familiar of the autocatalytic plating solutions. Nickel sulfate or nickel chloride salts are commonly used in the EN bath formulation as a source of nickel ions. There are four reducing agents used with electroless nickel. They are sodium borohydride, dimethylamine borane (DMAB), hydrazine, and the most common sodium hypophosphite. When sodium hypophosphite is used as a reducing agent the metallic deposit produced is an alloy of nickel and phosphorous. Only the hydrazine produces an almost pure nickel deposit. Several theories have been proposed for the mechanism of the electroless deposition process. All of them account for the reduction of metallic nickel at the catalytic surface and the release of hydrogen gas.

One theory is that the hypophosphite ion is catalytically oxidized (dehydrogenated) on the surface to be plated. This releases hydride ions ( $H^-$ ) that are very reactive but are stabilized by the catalyst. The stable hydride ions are now available for the reduction of nickel ions at the surface of the part. The products of these multiple reactions are nickel, phosphorus, phosphite ions, hydrogen ions, and hydrogen gas. The phosphorus ion can also be reduced to a phosphorus atom. This phosphorus atom is codeposited with the nickel at 1 to 15 percent by weight. In reality, you have a nickel-phosphorus alloy deposit. If other reducing agents, such as borohydride or amineborane, are used in place of the hypophosphite, 0.2 to 6 percent by weight of boron is codeposited with the nickel. The selection of the reducing agent determines the metal alloy produced and influences the physical and chemical properties of the coating.

The primary function of the complexing agents is to control the activity of the “free” nickel ion concentration in the solution. The stabilizers control the reduction reaction so that deposition occurs only on the catalytic substrate. Good solution stability also affects the rate of deposition and may affect the character of the deposit.

Uncontrolled reactions or bath decomposition is usually preceded by the increased evolution of hydrogen gas and the appearance of finely divided black particles in the solution. If the stabilizing chemical is in excess in the bath, incomplete deposit coverage, skipped or missed plating, and deposit porosity are the most likely results.

The reaction during nickel deposition produces by-products that accumulate in the bath and have an effect on the process. The temperature control has a very important effect on the deposition reaction. In all electroless nickel systems, the plating rate increases with the increase in temperature. Below 150°F (66°C), the reaction rate is very slow. The typical bath operates in the temperature range from 190 to 200°F (88 to 93°C). Localized overheating of the solution must be avoided, or bath decomposition could result.

Some precious metals can also be deposited from electroless formulations. The common ones are silver, gold, palladium, and platinum. Gold and silver electroless formulations use a boron-type reducing agent.<sup>17</sup> Gold can also be deposited from a hypophosphite bath. All these solutions produce alloying deposits containing small amounts of either phosphorus or boron from the reducing agent. Electroless copper deposition is usually accomplished from

alkaline solutions utilizing formaldehyde as the reducing agent. *Note that formaldehyde is considered a potential cancer-causing agent, and the exposure of production operators to this material must be limited.* Typical solutions contain copper sulfate as the source of copper, sodium hydroxide for alkalinity, and Rochelle salts as a complexing agent to keep the copper ions in solution. Additional chemical compounds are added in trace quantities to prevent spontaneous formation of finely divided copper particles and consequent solution decomposition. For each atom of copper deposited, at least two molecules of formaldehyde and four molecules of hydroxide ion are consumed, and one molecule of hydrogen gas is evolved. In practice, there is always additional consumption of formaldehyde and hydroxide by a disproportionate reaction.

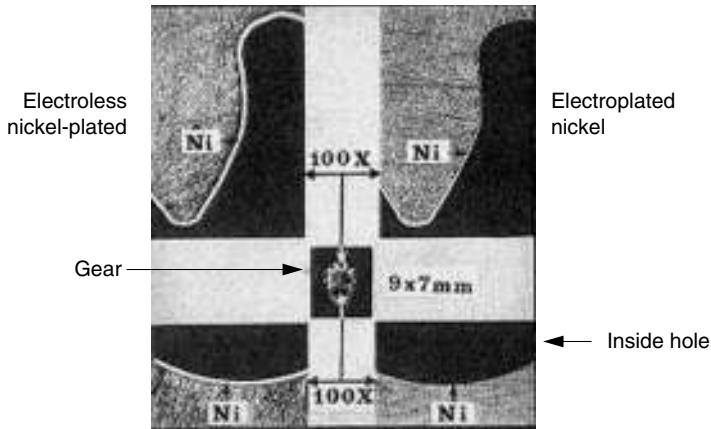
Electroless palladium and platinum deposits exhibit microcracking as a result of the hydrogen produced in the reaction. This hydrogen is absorbed in the deposits, making thick deposits brittle. Electroless silver processes are rare; however, an alkaline dimethylamine borane is referenced.<sup>47</sup> Immersion silver coatings have been used as a substitute for nickel/gold on copper for wire bonding and soldering operations.<sup>2</sup>

Immersion-type gold plating has been around for years and is very successful in some applications. Because immersion deposition relies on a replacement reaction between the substrate metal and the metal ions in solution, the deposit thickness is limited. In summary, when selecting an electroless deposit, one must also identify the reducing agent utilized, because the properties of the deposit are affected by the alloying element incorporated in the coating.<sup>18</sup> Substrates are generally prepared for electroless plating in the same manner as for electroplating. However, special activation procedures are necessary to provide deposit initiation on noncatalytic metals or on nonconductors. Electroless plating is utilized where advantage can be taken of one or more of the unique characteristics provided by the deposit. These include exceptional deposit thickness uniformity; low porosity; solderability; the ability to deposit directly on nonconductors; and specific chemical, mechanical, or magnetic properties of the deposit (see Fig. 6.10).

## 6.10 Tin and Tin Alloy Plating

The most common nonprecious metal finishes on electronic components are pure tin and tin alloys. MIL-T-10727 and ASTM B22 provide useful information on the tin-lead alloys. The use of tin and tin alloy plating has increased largely because of applications in the electronics industry.<sup>32</sup> The deposited metal is inexpensive and has properties of solderability and performance that are well understood.

For improvement of base metal solderability, the part can be either tin or tin-lead plated or dipped in a molten solder that is an alloy of tin and lead in various compositions. There are also commercially available immersion tin coatings. These coatings work on copper and other “noble metal” substrates by the replacement reaction. When the tin has replaced all the available surface



**Figure 6.10** Uniformity of electroless nickel. (Optical photo courtesy of Don Baudrand, Witco Corp.)

ions of the substrate, the reaction stops. MIL-T-81955 covers thin immersion tin on copper and copper alloys. The solder mask over bare copper (SMOBC) process may use immersion tin to preserve solderability on printed wiring boards, although the process is more expensive than tin plating and reflow or hot air solder leveling (HASL). The immersion coatings are thin and porous, so they offer minimal protection in high-temperature or high-humidity environments.<sup>2</sup>

The solderability of a surface comprises the physical, metallurgical and chemical history of the finish before, during, and after manufacture. The solderability of assemblies with tin-based solder is directly dependent on a thin bonding layer between the surface metallization and the tin in the solder. Impurities such as sulfides, carbonates, and oxides degrade the quality of this bonding layer.

Similarly, solderability can be degraded if reactions result in an increase or segregation of impurities to the solderable surface.<sup>33</sup>

Solderability of a surface permits molten solder to readily wet that surface under the correct conditions of flux, time, and temperature. Proper wetting occurs when a metallurgical bond or intermetallic compound (IMC) is established between the tin and base metal surface. A definition of intermetallic compound (IMC) is the alloy formed between the solder and the metallization.<sup>20</sup>

Nonwetting of a surface by solder is defined as no metallurgical bond formation and the solder pulling back, exposing the base metal as it solidifies. Oxides, organic films, and/or nonmetallic occlusion on the substrate surface can cause nonwetting.

Dewetting is the result of less severe surface contamination, but it still is an interruption of the IMC growth near the surface. This is most likely caused by the presence of nonreacting material on or near the surface. In dewetting, the base metal is covered with a thin intermetallic solder layer while the bulk of the solder has pulled back away from the area.<sup>35</sup>

There are three types of solderable coatings: fusible, soluble, and nonsoluble. Examples of each of them are as follows:

- *Fusible*—tin and tin-lead deposits melt into the solder, and the bond is formed with the base material.
- *Soluble*—examples of which are gold, silver, and to some extent copper.<sup>33</sup> The solder bond is to the substrate or underplating, because the top plating layer is dissolved into the molten solder.
- *Nonsoluble*—such as nickel, iron, iron-nickel alloys, and tin-nickel. The solder wetting occurs directly at the surface of the coating; i.e., the intermetallic compound forms with the coating.<sup>35</sup>

There are many sources of solderability problems in fusible coatings. Listed below are some of the most common:<sup>23</sup>

- Base metal contamination
- Base metal preparation
- Plating process
- Post-plate thermal excursions
- Environmental storage factors
- Component soldering (PWB)
- Intermetallic compounds

Base metals can gather heavy oxides during die or wire bonding, mold curing, or stabilization bakes. Copper and silver base materials can form intermetallic compounds that result in brittle unreliable solder joints. Too often, the blame is placed on the plating process as the only source of the problem.

IMC formation occurs by diffusion; thus, the IMC surface, along with any transferred contaminants, becomes the new metallization to which tin must bond during soldering.<sup>35</sup>

The segregation of lead adjacent to the IMC can retard the melting rate as a result of the relatively high melting point of the lead-rich layer. The IMC layer grows in a coherent manner sweeping impurities to the IMC–plating interface.<sup>34</sup>

Organic vapors from curing ovens can contaminate the plated surface during bake-out procedures.

If a barrier plating is used on the substrate, choose a plating process that contains a minimum of codeposited materials such as organics or sulfur.<sup>3,27</sup> These contaminants can oxidize at the tin–barrier interface and interfere with solderability.

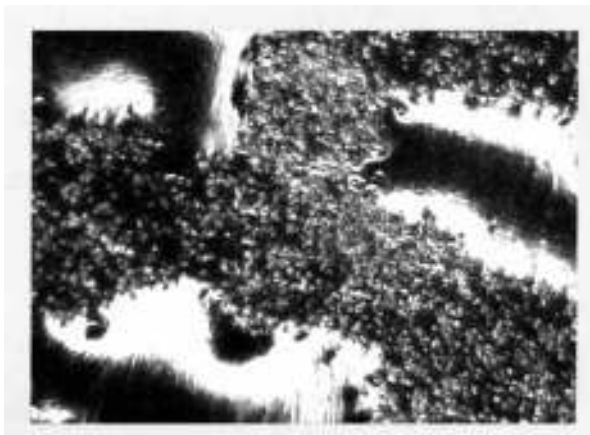
Passive or contaminated base metal surfaces are a problem in plating as well as soldering. Tin or solder plating over passivated (surface oxides) or contaminated surfaces constitutes a fabrication problem. During soldering, the plating would melt, and the surface would have too low a surface energy to

bond to the tin in the solder. Improper cleaning or surface preparation can furnish a surface that is good enough for mechanical bonding but not clean enough for soldering a fusible coating. The intermetallic bond cannot be established, and wetting will *not* occur.<sup>36</sup> There is also an incompatibility problem wherein migration of zinc atoms from brass moves toward the surface and into the solder. In the case of brass, you must remove the intermetallic and also prevent further migration of zinc into the tin or tin-lead coating. Copper and nickel are commonly used on substrates as the barrier plate.<sup>40</sup> If a plating process based on acid tin is used, then choose grain refiners that codeposit a minimum amount of organics. The trapped organics can outgas during reflow or soldering as shown in Fig. 6.11. Also occurring during the “burn-in” procedure are thermal excursions that may allow organics to degrade the solder–substrate interface resulting in dewetting or simply decreasing the final solder joint strength. A safe upper limit is for a deposit to contain no more than 0.05 wt% organic inclusions measured and recorded as carbon.

Some organics in a plating bath do not codeposit, but their breakdown products do. Routine carbon treatment of the plating bath is necessary to remove the breakdown products. The breakdown of the organic additives can be the result of elevated bath temperature, excessive agitation that brings oxygen into the bath, or electrochemical activity.

The most common inorganic found in tin and tin-lead systems is copper. The most likely source of this copper is drag-in from copper plating baths. A second source is copper-plated parts that drop into the plating tank and dissolve. A level of 20 ppm copper will darken deposits, and 140 ppm will cause a grainy appearance at reflow and promote dewetting due to excessive intermetallic formation.<sup>33,34</sup>

Poor rinsing can leave chemical films or plating salts on the deposit surface that can also cause dewetting.



**Figure 6.11** Blisters caused by organic contamination of solder bath. (Optical photo courtesy of EC&S Analytical Solutions.)

Thin coatings resulting from poor solution throwing power will allow oxygen penetration to the substrate, or the total metal in a thin deposit can be consumed by intermetallic formation. High lead content can raise liquidus temperatures, which could result in microcracks at the solder joints. Flux reacts more slowly with surface oxide films, thus compromising the solder joint integrity.

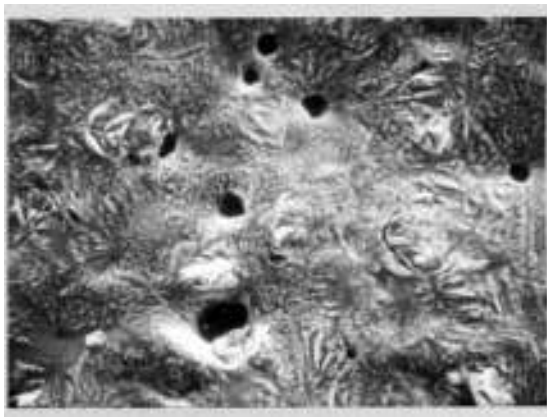
Post-plate burn-in of components is the single largest contributor to solderability failures in the assembly process. When the coating is tin-lead, and a majority of the tin is consumed to form the intermetallic, this increases the lead concentration in the unreacted coating. The intermetallic compound formed, as well as the lead, will oxidize and interfere with the soldering operation.<sup>35</sup>

Organics can migrate to the surface during time-temperature excursions. During soldering, these organics can cause dewetting, or outgassing can occur that produces porosity in the coating or at the joint (Fig. 6.12).

### 6.11 Environmental Storage Factors

Surface oxidation and oxygen penetration to the substrate can interfere with the intermetallic formation. Contamination such as ink or fingerprints on the surface or plastizers from packaging can form on parts in storage and disrupt solderability. All halogens except fluorine react readily with tin at room temperatures. Lead will react with organic vapors. Oxygen penetration along grain boundaries is greater in humid conditions. This penetration will cause more rapid oxidation of any impurities that are present. Tin forms intermetallics with all base metals. Intermetallic growth rate at room temperature for tin plated copper is 1 to 1.5  $\mu\text{m}$  per year as  $\text{Cu}_6\text{Sn}_5$ . Make sure that the solder problems are not the result of solder pot contamination.<sup>35,36</sup>

To increase the resistance of the coating to oxidation or to improve the chemical resistance of the deposit, tin can be reflowed or fused, which melts the coating and closes the pores in the deposit.



**Figure 6.12** Pitting as a result of organic inclusions in tin-lead plating after fusing. (SEM photo courtesy of EC&S Analytical Solutions.)

## 6.11.1 Tin whiskers

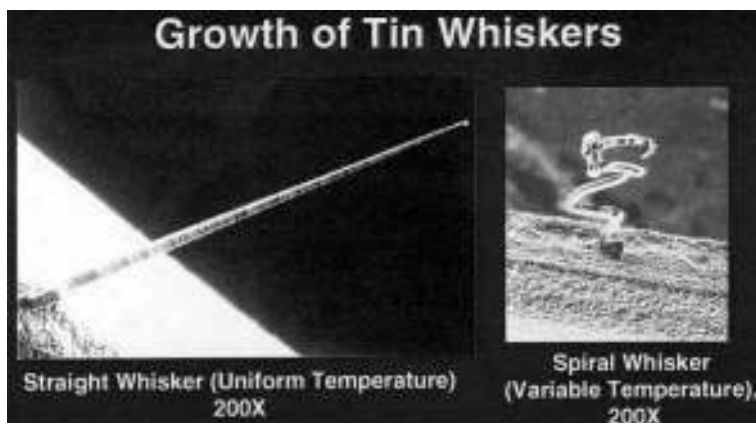
Tin whiskers are hair-like crystals that appear to grow spontaneously from a solid tin-plated surface. They can grow up to 1  $\mu\text{m}$  in diameter and 5 mm long (Fig. 6.13).

Some studies have shown that a nickel base layer prevents whisker growth. As an additional precaution, an added stress relief heat treatment (i.e., fusing the tin coating) can be performed. Reflow or fusing reduces the risk of tin whisker growth.<sup>37</sup> The electroplated pure tin layer now has the same properties as a hot-dip coating of tin on nickel. This combination does not form whiskers. The whiskering reduction may be a result of alloying to the base metal or stress relief of the deposit.

Thin tin or tin-lead alloy plating provides a short diffusion path for metallic contaminants. Oxygen would have to travel only a short distance through the thin coating to oxidize the metallization. Metallic elements can migrate to the surface of the plating and oxidize. If oxidation of the metallization occurs, a compressive stress can form under the deposit, because the corrosion products produced occupy more volume than the metal they replace. The oxide layer formed on the metallization could impair the solderability, thereby resulting in a dewetting or nonwetting condition. Another method of minimizing the formation of tin whiskers in tin plating is to alloy the tin with 1 to 2 percent lead or bismuth.<sup>38</sup>

**6.11.1.1 Solderability.** The *finish* describes the metallization in addition to any coating such as tin or tin-lead plating that may be present. Analysis of a solder/copper base metal interface shows the formation of copper/tin intermetallics. Typically,  $\text{Cu}_3\text{Sn}$  and  $\text{Cu}_6\text{Sn}_5$  are the primary alloys.

Tin reacts most readily with pure metal, less readily with either tarnished metal or pure IMC, and least of all with contaminated IMC.



**Figure 6.13** Tin whiskers. (Photo courtesy of American Electroplaters & Surface Finishers Society, Inc.)



The following is a list of plating bath factors that affect solderability:

- High current density
- Organic contamination
- Suspended particulates
- Low metal concentration
- Thin deposits

The plater must be sure to keep the current density within the manufacturer's specified range, because high current density can result in burned coatings or improper alloy composition in some bath formulations.

A 0.05 percent epoxy contamination in sulfate-type electrolyte is enough to cause organic contamination of the tin coating. Suspended particles can be occluded in the deposit, causing localized stress. Low metal content in the bath can result in poor grain formation or incorrect alloy composition. If the plating is below 2  $\mu\text{m}$  in thickness, the deposit is unable to distribute the stress that could result in whisker growth.<sup>39</sup>

Newer production processes, however, call for more aggressive manufacturing cycles, including higher soldering or molding temperatures, longer cure times, and several passes through a range of temperature profiles. The manufacturing processes and the storage practices of the manufacturer can affect components solderability.

Information regarding the degree of solderability degradation present in each phase of production can be combined with the knowledge of the original finish solderability to determine the primary influences on the product's overall solderability.<sup>35</sup>

Most base metals will have a nickel diffusion barrier layer that serves as the solderable metallization layer. This nickel layer generally has a protective coating of tin plating or gold plating.<sup>31</sup> If gold is used, the gold quickly dissolves into the molten solder during soldering, and the solder bonds to the nickel metallization. This bonding can be impeded if the solderable finish is contaminated. Gold must be sufficiently thick to be nonporous, and the nickel must be oxide free prior to the gold plating process.

Tin wets the nickel underplating and not the oxide film, because tin has a greater affinity for nickel than for nickel-oxide. To maintain good solderability, the nickel must remain oxide-free during the interval between plating and soldering.

Tin plated directly on nickel in a single operation has better solderability shelf life than tin plated on an activated nickel as would occur in an interrupted process.<sup>33</sup> Diffusion of impurities to the nickel layer increases when the time interval grows and includes the fabrication processes and thermal excursions. Examples of thermal cycles are when the connector leads undergo high-temperature exposure during the molding of component bodies, the de-flashing operation, package sealing, epoxy curing, heat-shrink coating, stabilization bake, burn-in, and component marking.

Diffusion is the key mechanism for solderability degradation.<sup>31</sup> Atoms in the solid state diffuse, i.e., move toward one another and then react to form

compounds. *Note: this solid state diffusion occurs below the melting point of the solder.* Nickel is superior as a diffusion barrier material in most environments. It is not sufficient to just specify “nickel” for optimal use. The nickel layer must be a fine-grain, high-purity (sulfur-free) deposit.

*Proper design is not a guarantee of solderability. The entire fabrication history is critical in achieving this goal.*<sup>33</sup>

The following are known good plating practices to achieve defect free surfaces:

1. Plate with sufficient thickness to provide a good diffusion barrier.
2. Maintain clean plating solutions and provide filtration to remove all particles from the bath.
3. Use good cleaning and activation preplate steps.
4. Monitor all plating solution constituents and operating conditions to produce a high-quality deposit.

These known good practices will minimize or help to eliminate plating problems in the majority of electronic devices. Why won't these good practices solve all the problems?

Some devices operate at elevated temperatures. The diffusion rate of metallic atoms is increased by the heat. Thicker plated deposits may be required to retard base metal diffusion to the surface. Pure nickel electroplate may not be the best diffusion barrier in some applications. Electroless nickel provides a somewhat better diffusion barrier, but at a little higher electrical resistance, and the plating cost may double. Diffusion of metals, and in some cases non-metals, can lead to changes in surface resistivity.<sup>31</sup>

One of the requirements for tin and tin-lead coatings is that they have “long term” solderability and be reflowed or fused without dewetting. The organic film that has been used to preserve the solderability of copper is a solution of benzotriazole in IPA and/or water. Imidazole, the active agent in flux, will remove this film during the soldering operation.<sup>35</sup>

The organic inclusions, surface oxides, and intermetallic compounds all affect solderability and fusing of the electroplated tin and tin-lead electrodeposits. Organic inclusions are particularly significant, because most electroplating processes utilize “organic addition agents” to impart brightness to the deposits.

The organic content of a deposit can be assessed by a number of methods. Elemental gas fusion analysis for carbon remains the most direct and accurate and provides quantitative results. However it requires sophisticated analytical instrumentation.

An in-service problem with tin or tin-lead plating of connectors is fretting corrosion. *Fretting* refers to the repetitive sliding movements between mated surfaces that can result in open circuits.

Applications to be avoided are those involving low-frequency vibrations, a long wipe distance/cycle, and low contact force. Fretting corrosion is characterized by the presence of black spots at the point of motion. The spots indi-

cate a buildup of tin-oxide debris that acts as an insulator in low-contact-force applications.<sup>33</sup> To circumvent the problem, a high contact force will reduce sliding and provide contact resistance stability, but be aware that the increase in contact force may accelerate wear.

Contact lubrication reduces wear by decreasing the coefficient of friction, floating debris away from the contact area, and preventing oxidation of the exposed metallurgy. A downside of lubrication, however, is attraction of dust and lint to the contact surfaces.

The electronics industry uses alloys with tin contents in the range of 30 to 98 wt% tin as well as pre-tin plating. In general, the higher the tin content of the alloy, the greater the ease of soldering.

There are electroless tin deposits that use titanium chloride as the reducing agent,<sup>46</sup> and electroless solder from fluoborate and sodium hypophosphite are cited in the literature.<sup>47</sup>

**6.11.1.2 Get the lead out.** For decades, the electronics industry has been utilizing tin-lead as both an electrodeposited finish and a solder joint material. There are environmental concerns about the amount of lead in electronic components. Pressure in the U.S. and foreign markets has forced manufacturers to turn to lead-free alternatives in both plating and solder material. Legislation has been adopted to require the elimination of lead by 2002 in Japan and by 2008 in Europe.<sup>41</sup> Lead is very toxic and can enter the groundwater through leaching. Investigations continue into finding nontoxic replacements for lead-containing finishes.

Listed below are the eutectic melting points of some tin alloy solders that do not use lead.

High-melting <sup>33</sup>	
221°C	SnAg 96.5/3.5
227°C	SnCu 99/1
236–240°C	SnSb 95/5
280°C	AuSn 80/20
Low-melting	
139°C	BiSn 57/43
117°C	InSn 52/48

In high- and low-melting point solder joints, half the metal comes from the solder used and the other half from the pretinning of the components. The lead alloy can dramatically change the melting point of the joint.

An example of this is a PbSnAg (88/10/2) solder with a melt temperature of 290°C. The melting point of this solder can be lowered to 179 to 200°C when

soldered to a 60/40 SnPb coated component, resulting in a finished composition of SnPbAg of (53.2/45.1/1.7).<sup>33</sup>

Lead is a headache for the plater because of the need for environmentally safe disposal. Many shops are eliminating solder plating entirely so they do not have to deal with treatment of lead containing wastes. Other shops address the problem by segregation of the lead-containing waste stream and through waste treatment of the lead before it hits the sewer system.

### 6.11.2 Lead-free electrodeposits

The electronics industry is rapidly moving toward lead-free solders.<sup>41</sup> By alloying tin with lead, you produce many desirable deposit characteristics. Among them are a lower melting point, retarded whisker growth, and excellent solderability. There are many tin alloy deposits other than tin-lead for component finishes. The reported finishes are tin-zinc, tin-nickel, tin-cadmium, tin-cobalt, tin-bismuth, and tin-copper.<sup>41</sup> Electroplated pure tin may be the simplest process replacement for tin-lead. Tin is a nontoxic metal, and recycle-recovery procedures are well established. Precious metals are not a cost-effective replacement, and solder joint embrittlement can be a nagging problem.

Lead-free deposits such as tin-copper and tin-bismuth are two of the viable replacements for tin-lead. In any alloy plating system, the final composition of the deposit can be difficult to control. Special applications may warrant the use of tin-bismuth alloy coatings, but in general they have not been accepted for printed wiring board manufacturing. The tin-bismuth and other environmentally friendly alloys are being evaluated by the National Center for Sciences. They completed a study of more than 75 different alloys without finding an exact drop-in replacement.<sup>41</sup> Tests were designed to measure the solderability of these deposits and compare them to tin-lead and tin-silver-copper. The use of the wetting balance allowed for accurate measurements to be taken. The wetting balance measures and reports the wetting force versus time for a solder meniscus to wick up the surface of a test sample.

In "Factors Influencing the Solderability of Lead-Free Electrodeposits,"<sup>42</sup> the authors determined that the solderability performance of the pure tin, tin-copper, and tin-bismuth electrodeposits compared favorably with tin-lead when using tin-silver-copper or tin-lead solders. Aging of the deposits for 16 hr at 155°C followed by steam exposure for 4 hr had the biggest effect on solderability. An RMA or no-clean flux was needed to achieve maximum wetting force. When the deposits were tested after the 16-hr bake, the pure tin or tin-bismuth performed well. The authors concluded that, by choosing the correct soldering parameters, many of the lead-free deposits might be suitable replacements for tin-lead finishes.

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# Printed Circuit Board Fabrication

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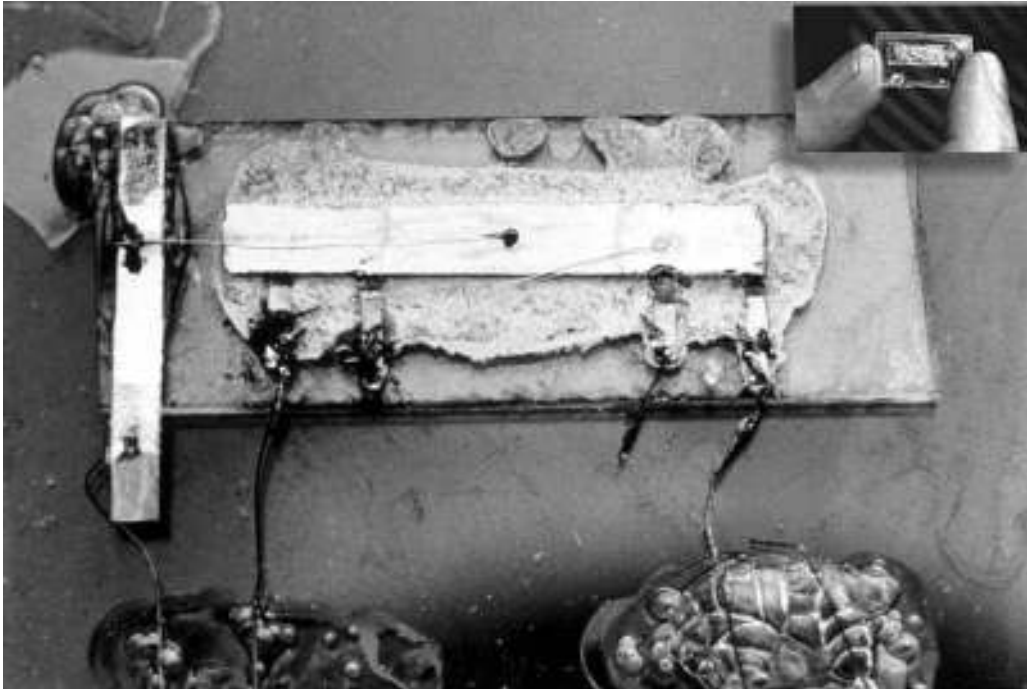
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## 7.1 Introduction

Of all of the elements of an electronic system, perhaps none is more essential than the printed circuit board. At the same time, however, no other element seems to be so underappreciated. Prior to the advent of the printed circuit, electrical interconnections between components were made in a point-to-point fashion. This was both very time consuming and highly error prone. The printed circuit offered a way to make ordered interconnections between components while radically reducing the potential for error by allowing faithful reproduction of the circuit using a combination of lithographic and etching methods. It has been that way virtually ever since.

Today, it can be easily argued that the printed circuit is the foundation of almost all electronic products and systems and a technological marvel of immense dimensions, but it is commonly overshadowed by the more glamorous integrated circuit. Interestingly, the printed circuit is likely to have served as the inspiration for the inventors of the IC, given that the concepts described by both Jack Kilby and Robert Noyce appear to have borrowed from printed circuit manufacturing methods. Kilby had, in fact, joined pioneering printed circuit company, Centralab, in Milwaukee, WI, in 1947 after leaving college. Figure 7.1 shows first Kilby's IC. Regardless, the printed circuit will assuredly remain an indispensable element of electronics for many years to come.



**Figure 7.1** Jack Kilby's original integrated circuit. (Photo courtesy of Texas Instruments.)

The purpose of this chapter is to give the reader an overview of this important electronic interconnection technology. Attention will be given to the materials and processes used in their construction and, in addition, most of the many forms of printed circuits will be reviewed and described. Rigid, flexible, multilayer, metal core, and molded boards are among the types that will be covered. However, no attempt will be made to provide an exhaustive look at printed circuit technology. Rather, it is intended and hoped that the reader will be provided with a sufficient level of understanding of the printed circuit technology to feel confident and comfortable moving through the technological forest of electronic interconnection substrates. The reader will be shown many different constructions and be provided with enough information on process to have, hopefully, a good understanding of how PCBs are made, from the very simple to the very complex. Finally, it is hoped that the reader will be able to use this information to make informed choices relative to future interconnection needs.

### 7.1.1 Background and history

The origins of the printed circuit have been variously traced to either the late nineteenth century or the early twentieth century. That period marked the rise of useful inventions predicated on the use of electrons and wire. The telegraph, the telephone, and the radio are the hallmark inventions of the period.



A point of entry from the wiring perspective came in 1903 from the inventor, a German by the name of Albert Hanson. Hanson conceived of a method of producing conductive metal patterns on a dielectric by cutting or stamping copper or brass foil patterns and laminating or bonding them in paraffin paper. Although only two metal layers were described, it is easy to envisage that multiple layers could be produced using his concept.

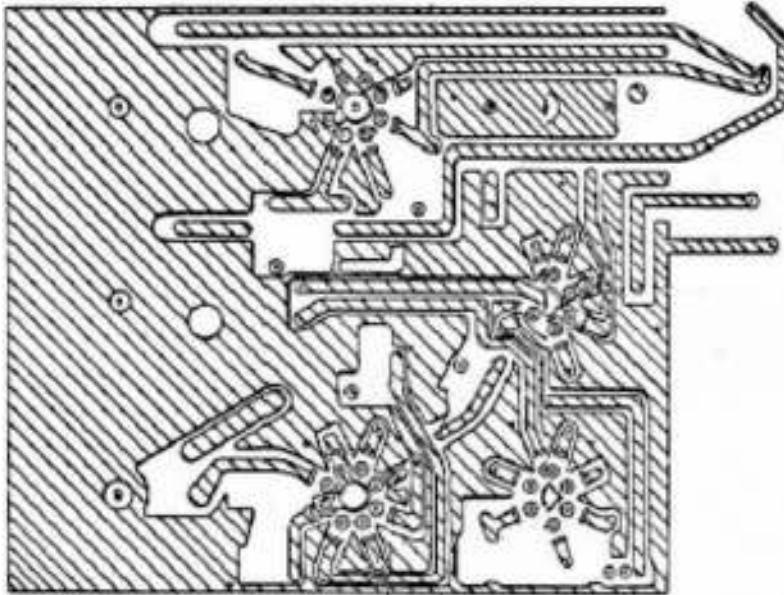
The American patron saint of inventors, Thomas Edison, also took a turn at circuit processing invention at the prodding of this then assistant, Frank Sprague, later of Sprague Electric Company fame. Sprague had challenged Edison in 1904 with finding ways to pattern conductors on linen paper. Edison responded with a number of different ideas, including two that are, at least in spirit, in use today. These methods include a crude version of today's polymer thin film technology and patterning of silver salts to be reduced in situ, which, in concept, resembles today's additive processing.

Print-and-etch methods commonly used today in circuit production can trace their roots to methods described by inventor Arthur Berry in 1913, wherein he used the method to create resistive heaters (British patent 14,699). Another method of note was conceived of by Max Schoop, who developed a method of flame spraying of metal through a mask to create circuit patterns on a dielectric base (U.S. patent 1,256,599). Electroplating of the circuit pattern appears to have been the invention of Charles Ducas, in 1927 (British patent 1,563,731). The method had the added advantage of allowing release and transfer of the circuits from the base onto which they were plated. The basic concept of transferring circuit patterns has merit and has been visited since that time by others who made improvements to the concept.

Paul Eisler is the next inventor of note in the pantheon of printed circuit technology pioneers. The self-proclaimed "father of the printed circuit," Eisler made significant contributions to printed circuit technology. Eisler's innovations spearheaded the allies' effort to make more reliable proximity fuses for munitions. The advantages offered by the PCB are credited with causing the destruction of large numbers of V2 rockets and thus ending the terror bombing of England. Examples of one of his circuit concepts are illustrated in the patent drawing shown in Fig. 7.2.

After World War II, printed circuit technology began to unfold in earnest as investigation into defining and refining their manufacturing methods began to grow and expand. The following paragraph gives an indication of how diverse the approaches were.

...circuits are defined as being printed when they are produced on an insulated surface by any process. The methods of printing circuits fall in six main classifications: *Painting*—Conductor and resistor paints are applied separately by means of a brush or a stencil bearing the electronic pattern. After drying, tiny capacitors and subminiature tubes are added to complete the unit. *Spraying*—Molten metal or paint is sprayed on to form the circuit conductors. Resistance paints may also be sprayed. Included in this classification are an abrasive spraying process and a die casting method. *Chemical deposition*—Chemical solutions are poured on the surface originally covered with a stencil. A thin metallic film is precipitated on the surface in the form of the desired electronic circuit. For conductors the film is elec-

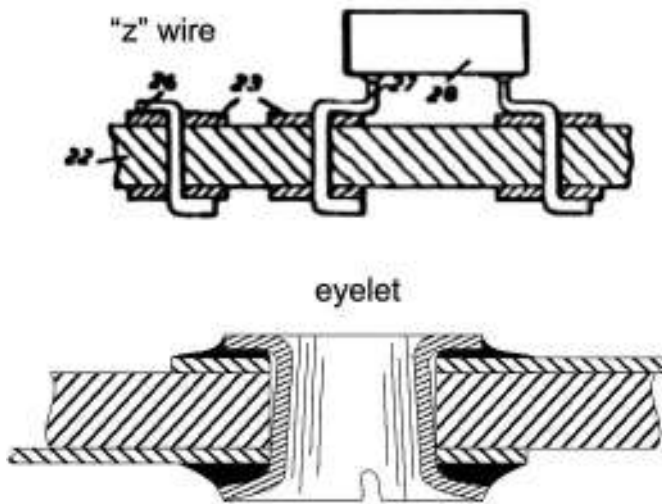


**Figure 7.2** Example of an early printed circuit design layout. Note that components mainly had leads in a circular pattern consistent with vacuum tubes and the early TO packages.

troplated to increase conductance. *Vacuum processes*—Metallic conductors and resistors are distilled onto the surface through a suitable stencil. *Die stamping*—Conductors are punched out of a metal foil by either hot or cold dies and attached to an insulated panel. Resistors may also be stamped out of a specially coated plastic film. *Dusting*—Conducting powders are dusted on, either with a binder or by an electrostatic method.... Principal advantages of printed circuits are uniformity of production and the reduction of size, assembly and inspection time and cost, line rejects and purchasing and stocking problems....

The forgoing paragraph was from a publication titled *Printed Circuit Techniques*, written by Cleo Brunetti and Roger W. Curtis and published 1947 by the U.S. government. Clearly, those involved in the early manufacture of printed circuits were very clever. Few stones, it seems, were left unturned in their efforts to find cost-effective ways of delivering patterned circuits to the nascent electronics industry.

Up to this point in this review, most of the circuit concepts described have been single sided; however, the drive for more functionality in an electronic assembly translated naturally to greater complexity and more wiring. Two metal layers became the next requirement. Interconnection between the two sides was accomplished initially by simple but slow methods. The z-wire interconnection served the purpose originally (see Fig. 7.3) but was supplanted by the use of eyelets (the same method as is used to reinforce lace holes in shoes), which were easier to use. However, as hole counts rose, there was a need to improve productivity in making side-to-side interconnection, and the plated-through hole concept was brought into practice.



**Figure 7.3** Before plated-through hole technology was developed, through-hole connections were made by wires soldered to lands on both sides of the PCB as indicated by the drawing from an early patent (top).

The multilayer board was the next important milestone on the path of printed circuit innovation. Original concepts such as the one illustrated in Fig. 7.4 had layers of circuitry being laminated to prefabricated double-sided circuits, with access being provided by larger holes in the outer layers. The plated-through hole multilayer circuit followed as a natural extension, and the multilayer circuit was later married to the flexible circuit to create the rigid flex circuit. In the time since the early days of printed circuit technology, there has been a steady stream of improvements to the fundamental technology, and it is safe to say that there will be many more improvements in the years ahead. Some potential directions are discussed at the end of this chapter.

## 7.2 Materials of Construction for Printed Circuit Laminates

Rigid printed circuit laminates normally consist of three fundamental elements,

1. A reinforcement, such as glass cloth, paper, or other material
2. A resin
3. A conductive or catalytic layer

Each of these element serves a specific purpose. Generally, as laminate thickness increases, heavier glass cloths or reinforcements are commonly used, and the resin content in the laminate decreases. Because laminates are commonly exposed to high temperatures both in assembly and use, many laminate mate-

June 27, 1961

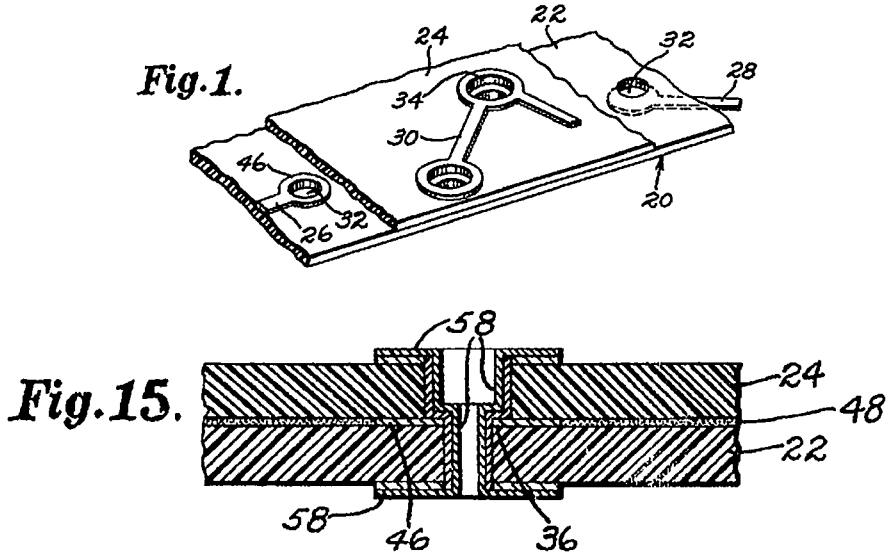
R. CHAN

2,990,310

LAMINATED PRINTED CIRCUIT BOARD

Filed May 11, 1960

2 Sheets-Sheet 1



**Figure 7.4** This early multilayer circuit patent used holes of different sizes to facilitate making plated-through hole connections.

rials have been engineered to roughly match the thermal expansion rate of copper. This minimizes any potential for warping in plane, which can cause problems in assembly and possibly result in reduced reliability of the plated-through hole or solder joints on the PCB.

Laminates can be made with varying resin-to-glass ratios, depending on the performance needs of the finished product. Specifically, the glass-to-resin ratio of a laminate has a direct effect on dielectric constant, with higher resin contents resulting in lower dielectric constant being obtained. However, laminates with higher resin content tend to have higher coefficients of thermal expansion (CTEs) in the z-axis and lower dimensional stability. On the other hand, if resin content is too low, weave exposure and a phenomenon called *measling* may result. In the past, this condition has been proven to be a largely cosmetic defect, but it is a concern, because it is an indication that either the resin coating or the lamination process is not in full control. Moreover, as the electronics industry moves to higher frequencies, the need for higher consistency in the laminate product is of great importance to both design and performance.

### 7.2.1 Reinforcements

Reinforcements are the conceptual and literal foundation of a laminate, and they provide important mechanical properties. These are the materials that,

when coated with resin, become the individual laminae or “building blocks” of the finished laminate. Although it is possible to employ a wide variety of different materials as reinforcements, only a very limited number of choices are commonly used in printed circuit laminates.

The reinforcement serves several different functions. For example, it imparts important mechanical properties such as strength and rigidity. The reinforcement also provides the important attribute of the dimensional stability required for accurate manufacture and assembly. Electrical properties of the laminate are also affected by the reinforcement choice. The effect is not only in terms of the electrical properties of reinforcement itself; it also changes as the ratio of resin to reinforcement is altered. Finally, because they are normally less expensive than the resins with which they are combined, reinforcements also help keep cost of the laminate in line with customer expectations or demands.

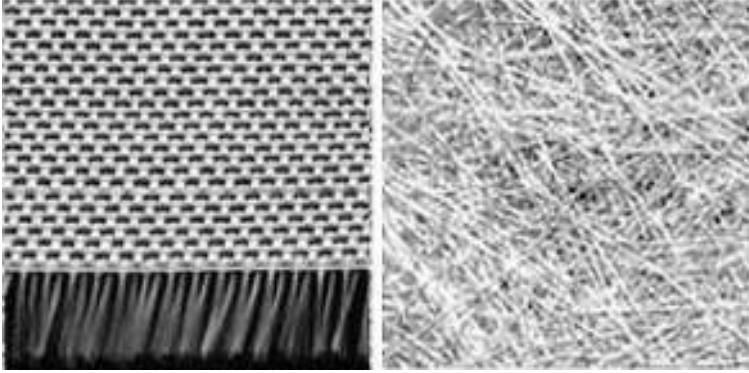
The following is a review of some of the more common reinforcements used in the construction of printed circuit laminates.

**7.2.1.1 Paper.** Paper-based reinforcements have been used in the construction of laminates for a wide variety of products for many years and have proven to be a valuable material for use in the manufacture of printed circuit laminates. Paper is easily mass produced, and thus it is not surprisingly one of the lowest-cost options among reinforcements. One clear disadvantage of paper-based laminates is that they are much more difficult to make fireproof.

**7.2.1.2 Glass fiber.** Glass fibers are one of the most universally employed reinforcements for resin-based laminates. Glass fibers are an excellent choice because of the good mix of electrical and mechanical properties they exhibit. Glass fibers, for example, are not only excellent insulators, they also have the kind of physical and mechanical properties that are required to supply the strength and dimensional stability required for manufacture, assembly, and component support in use. A number of different types of glass formulations can be used to create the glass fibers. These are given letter designators. E-type glass is the most commonly used in laminates for printed circuits; however, D-type glass is used in some applications for its lower dielectric constant, and S-type glass is used in applications demanding higher strength.

Glass fibers can be employed in one of two fashions, either as a woven cloth or as a chopped glass fiber based paper (see Fig. 7.5). Both forms of glass reinforcement are used, but, of the two, woven glass cloths are by far the most common. While the potential number of choices of glass cloth is quite substantial in terms of the different fiber diameters, yarn construction, and weave, the number actually used in laminate manufacture is, fortunately, rather small. Only a few different types of glass cloth see any significant use; these are characterized in Table 7.1.

**7.2.1.3 Others.** Many other specialty materials have been used to reinforce printed circuit laminates, including such exotic materials as quartz cloth and



**Figure 7.5** Glass cloths for reinforcing laminates can be either woven or a mat of chopped fibers as shown above.

**TABLE 7.1** Characteristics of Selected Electronic-Grade Glass Cloths

Glass fabric style	Yarns per cm	Weight, g/m <sup>2</sup>	Thickness, μm
104	~24 × 20	19.7	30
108	~24 × 19	48.5	51
112	~16 × 15	71.2	81
116	~24 × 23	107	102
2112	~16 × 15	71.6	76
2116	~24 × 23	107	102
7628	~18 × 13	203	173
7642	~18 × 8	232	279

aramid fibers. Aramid fibers have proven especially useful in applications wherein a low in-plane expansion rate is desired. These materials actually have a negative in-plane expansion rate, which helps offset the normally high expansion rate of the resin; however, this benefit is offset by the material's high z-axis expansion.

Other unusual reinforcements can and have been used. Graphite is an example of a nontraditional reinforcement. However, it requires special care in design and use, because it is conductive.

### 7.2.2 Organic resins

Organic resins are the second key element of a laminate. The resin serves as a binder to hold the reinforcements together and impart important electrical properties to the laminate. Resins used for electronic-grade laminates are gen-

erally relatively low in their dielectric constant and loss tangent, which are key properties in electronic design, especially in high-performance applications. The resin system also establishes the thermal performance limits of the laminate. This is a matter of increasing importance as some companies prepare to convert to lead-free solders, which have melting temperatures up to 40°C higher than traditional solders. Flame retardants are commonly added to the resins to assure that the laminates will not support combustion and will meet Underwriter's Laboratories specification 94-V0.

**7.2.2.1 Phenolics.** Phenolics are among the longest used and best known of general-purpose thermosetting resins. Although their performance is limited, they have proven quite suitable for electronic-grade laminates. Phenolics are the lowest-cost resin used for laminates, and many consumer electronics are fabricated using these materials.

**7.2.2.2 Epoxies.** Epoxies are the most common resin materials, and they are combined with glass cloth to produce laminates. As compared to other laminate materials, epoxies offer advantages in availability and relative ease in processing. The many different types and blends of epoxies provide a wide range of selection in terms of applications and soldering processes; epoxies with a  $T_g$  (glass transition temperature) from 110 to 120°C up to 180 to 190°C are available from most laminate suppliers. However, the most commonly used are in the range of 135 to 145°C. There are also some low-loss, low-dielectric-constant epoxy materials in development that are expected to have a  $T_g$  in the range of 210°C.

**7.2.2.3 Polyimides.** Polyimides are among the highest-performance resins used in the manufacture of printed circuit laminates. These materials, with glass transitions in the range of 260°C, can withstand very high temperatures for extended periods, making them a good choice for applications wherein high temperatures are experienced or the components used are high-wattage devices. The military also has special interest in high-temperature materials, as they make any required work and repair easier.

**7.2.2.4 Others.** A number of other resins are useful for creating laminates, such as cyanate esters and bismalamide triazine (BT). These products are seeing application in unique and special applications. For example, BT resins are proving very popular for the manufacture of organic laminate-based packages for integrated circuits. Liquid crystal polymers are also seeing greater levels of interest for certain types of applications because of their good combination of electrical and mechanical properties coupled with their very good dimensional stability.

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### 7.2.3 Flexible (unreinforced) laminates

Flexible circuits are a special subset of printed circuit manufacture and require their own special laminates. These materials normally consist of a base film, adhesive, and copper foil; however, there is increasing interest in adhesiveless laminates. The materials for these laminates tend to be thermoplastic in nature, which makes them better suited to flexing without fracture and failure. The adhesives, when used to create flex circuit laminates, are generally formulated to be more flexible than traditional thermoset resins. There are two basic resin systems employed in flex circuit manufacture: polyester and polyimide; however, a number of materials of intermediate performance and price have seen use. One example of note is polyethylene naphthalate (PEN).

**7.2.3.1 Polyester.** Polyester is a low-cost resin that is used in a substantial number of electronic products. Common examples are keyboards and printer cables. Polyester is used with both copper and polymer thick film circuits. The major limitation for polyester is related to its thermal performance. Because of its low melting temperature, it is generally considered unsuitable for soldering; however, this can be addressed by careful engineering. Major OEMs such as TI and Kodak have developed methods for special applications that require soldering to polyester, and some manufacturers have specially developed tools to address the problem.

**7.2.3.2 Polyimide.** Polyimide is the choice for most flex circuit applications because of its excellent thermal performance and its good electrical and mechanical properties. It also exhibits reasonable dimensional stability, which facilitates circuit manufacture and assembly. This material is also being used extensively in the creation of IC packages. One limitation of polyimide is the fact that it tends to absorb moisture, which can be a concern when soldering.

**7.2.3.3 Special materials.** A wide range of niche substrate laminate products have been developed in support of special printed circuit manufacturing methods. An example of such a product is resin-coated copper (RCC). This material is used for high-density buildup technologies, which are discussed later in this chapter.

### 7.2.4 Foils

Metal foils are commonly laminated to resin composites to complete the raw material needed for printed circuit manufacture. Many different foils are potential candidates for the creation of a metal-clad laminate, but copper is the most common because of its excellent electrical properties and its general ease of processing and amenability to solder assembly. Thinner foils are generally



used by the printed board manufacturer for “fine-line” designs to reduce the amount of undercutting of circuit conductors that occurs during the etch operation and meet the requirements of high-density printed circuits for flip-chip and chip-scale packages.

Copper foils can be created in one of two ways: mechanical rolling and deposition. In the area of deposition, the potential methods include electrodeposition, electroless deposition, vapor deposition, and sputtering. The first of these methods is the one most commonly used to manufacture copper foil for printed circuit laminates. The other methods are generally used to deposit foil directly on the laminate without the aid of a lamination process. Electrodeposition and electroless deposition employ wet chemistry to deposit metals, whereas vapor deposition and sputtering are dry deposition methods for metal and are carried out in a vacuum. Table 7.2 lists the designations for the most common types of copper foil as called out by IPC-MF-150.

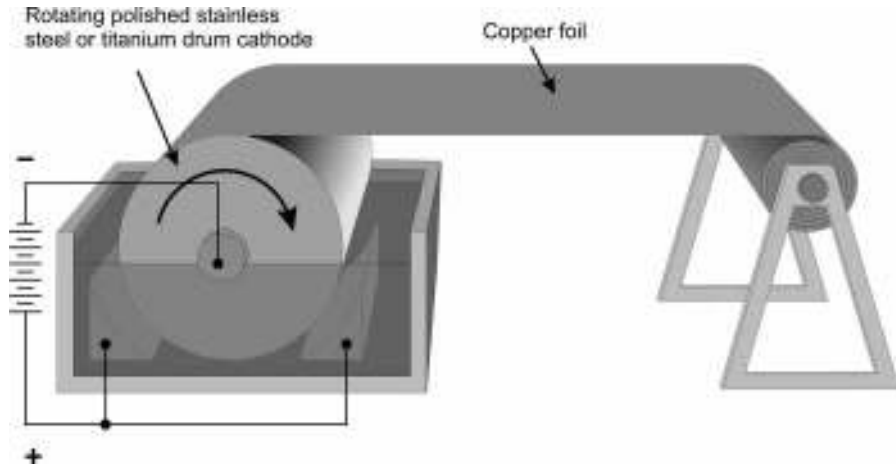
**TABLE 7.2 Copper Foil Designations\***

Copper foil type	Number	Designator	Description
Electrodeposited (E)	1	STD–Type E	Standard electrodeposited
	2	HD–Type E	High-ductility electrodeposited
	3	THE–Type E	High-temperature elongation electrodeposited
	4	ANN–Type E	Standard electrodeposited
Wrought (W)	5	AR–Type E	As rolled-wrought
	6	LCR–Type E	Light cold rolled-wrought
	7	ANN–Type E	Annealed rolled-wrought
	8	LTA–Type E	As rolled-wrought, low temp. annealable

\*Copper foil is available in both electrodeposited and wrought forms. The IPC standard for copper foils, IPC-MF-105, has broken out these foils into eight different types, as described above.

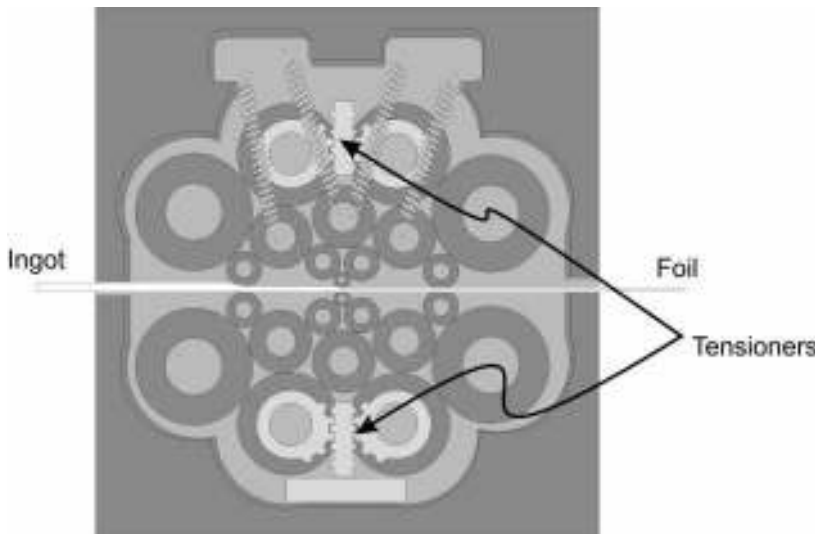
**7.2.4.1 Electrodeposited.** Electrodeposited foil is most commonly used for rigid printed circuit laminates. The foil is plated onto polished stainless steel or titanium drums that are negatively charged and rotated slowly through a plating bath. The thickness is controlled by the rate of rotation, the current density, or a combination of the two. Figure 7.5 illustrates the process.

The surface is commonly provided with a roughening treatment to increase the surface area and improve the foil’s peel strength. This can be important for surface mount components of large mass, lest they pull away from the surface as a result of shock and vibration. The thickness of the treatment can, however, influence processing and might limit the minimum feature sizes that can be reliably etched. This is discussed in more detail later in this chapter.



**Figure 7.6** Electrodeposited copper foil is the type most often used in circuit manufacture. The foil is produced by rotating a highly polished drum of passivated stainless steel or titanium in a copper plating solution with current applied. The rate of rotation controls the copper thickness.

**7.2.4.2 Rolled.** Rolled copper foil is most commonly used in the manufacture of flexible circuits. Wrought and annealed foils have proven excellent for use in situations wherein the foil must be bent or formed. Figure 7.7 shows the layout of the rollers for a foil rolling mill.



**Figure 7.7** Rolled copper foil is manufactured from ingots of copper successively rolled down to the desired thickness in specially designed rolling machines such as shown above.

**7.2.4.3 Conductive inks.** Conductive inks are among the oldest methods of creating printed circuits and are largely responsible for giving the technology its name. The technology is used for both high- and low-end products. For example, with ceramic substrates, it is used to create hybrid circuits and is fired in an oven to create circuits of high conductivity. For lower-end products, such as keyboards and some low-cost electronic devices, the curing is done at low temperatures and using low-cost materials for substrates such as polyester film. Other applications include migration protection for silver conductive ink, low-voltage circuits, shield areas, and heating elements.

The inks are generally combinations of resins and conductive fillers such as powdered silver. The conductivity can be modified to create resistors of varying values by the addition of more resistive fillers such as carbon or graphite powders.

Carbon-based conductive inks are easy to screen through properly designed screen fabrics. A coating thickness between 25 and 30  $\mu\text{m}$  will provide sheet resistance between 14 and 20  $\Omega/\square$ . The inks are one-part systems and are thermally cured. Newer versions are IR curable, which greatly reduces the processing cycles.

The inks must be resistant to hot-air leveling and other soldering processes. It is critical that the conductive properties of the ink not change appreciably after any thermal excursion.

## 7.3 Laminate Types for PCBs

Laminates used in PCB manufacture, whether rigid or flexible, are created in two primary forms: single-clad and double-clad laminates. They are also produced in a number of different thicknesses to facilitate the manufacture of PCBs with different thickness requirements and for the construction of multilayer PCBs. When used in the manufacture of multilayer circuits, the laminate is commonly referred to as a *core material*.

### 7.3.1 Single-clad laminates

Single-clad laminates have copper on one side only and are used either for the manufacture of single-sided circuits or for the manufacture of multilayer circuits as an inner layer or, more commonly, as a cap laminate.

### 7.3.2 Double-clad laminates

Double-clad laminates are essentially identical to single-clad laminates in description and use except that copper is laminated to both sides of the structure.

## 7.4 Laminate Selection

The selection of a laminate is based on the requirements of the product, both in assembly and use. Ideally, the laminate choice should be made from stan-

standard structures to avoid delays and potentially costly qualification of new constructions. When several laminates are potential candidates, the choice should be made in favor of the one that has the best balance of properties. Table 7.3 lists some of the different potential criteria for making a selection.

**TABLE 7.3 Laminate Selection Criteria**

• Coefficient of thermal expansion (CTE)	• Maximum continuous operating temperature
• Electrical properties	• Mechanical strength
• Flame resistance	• Overall thickness tolerances
• Flexural strength	• Reinforcing sheet material
• Glass transition temperature ( $T_g$ )	• Resin formula
• Machinability	• Thermal stability

As previously described, laminates come in many different resin and reinforcement combinations. The National Electronics Manufacturers Association (NEMA) and the U.S. military have both devised designators to describe the materials in a shorthand fashion. Table 7.4 provides a list of some of the most commonly used designators for different laminate types, and Table 7.5 provides examples of the applications for different constructions.

## 7.5 Laminate Material Preparation

The resin and reinforcement material are combined to create the raw material used for the creation of a laminate. The end product is commonly referred to as either *prepreg* or *B-stage*. *Prepreg* is short form for *reinforcement preimpregnated with resin*, and B-stage refers to the fact that the resin is dry to the touch but not fully cured.

This material is created by drawing the reinforcement material through a wet resin bath and then drying it and slightly advancing its state of cure—normally through the addition of heat. The basic manufacturing process is illustrated in Fig. 7.8.

### 7.5.1 Lamination methods

A lamination process is used to create laminates that can be used for manufacture of printed circuit boards. In lamination, the prepreg or B-stage material is layered, most often between sheets of treated copper foil. Following lay-up of the material, the material stack is subjected to heat and pressure, and this drives the resin to a fully cross-linked or cured condition wherein it has all of the desired properties. There are several different methods of creating laminate material.

### 7.5.2 Batch

Batch processing is the simplest and was thus one of the first methods developed for laminate manufacture. In their simplest form, lamination presses for

TABLE 7.4 Laminate Designators and Descriptions

NEMA designation	Military designation (MIL-P-13949)	Basic construction of laminate
XXXXP	–	Phenolic resin with paper reinforcement, heat required for punching
XXXXPC	–	Phenolic resin with paper reinforcement, room-temperature punching
CEM-1	–	Composite epoxy laminate, glass cloth outer with paper center
CEM-3	–	Composite epoxy laminate, glass cloth outer with mat glass center
FR-1	–	Similar to XXXP but flame retardant
FR-2	–	Similar to XXXPC but flame retardant
FR-3	PX	Similar to FR-2 but epoxy based and stronger
G-10	GE	Epoxy glass laminates without flame retardant
FR-4	GF	Epoxy glass laminate, flame retardant
FR-5	GH	High-temperature epoxy glass laminate, flame retardant
–	GI	Glass reinforced polyimide resin
–	GP GT, GX, GY	Fluoropolymer resins reinforced with various glass materials woven or mat fiber and having slightly different electrical properties
–	GC	Woven glass cloth with cyanate ester resin
–	GM	Woven glass cloth with bismalimide triazine resin
–	BF	Nonwoven aramid fiber with epoxy resin
–	BI	Nonwoven aramid fiber with polyimide resin
–	SC	Woven S type glass cloth with cyanate ester resin

batch processing consist of a hydraulic ramp and a heated platen, which is pressed against a parallel platen that resists the pressure of the hydraulic ram. It is obviously possible to have several openings and to have all of the platens heated. Heating can be done electrically, by steam, or by hot oil circulated through the platens. The choice is predicated on the temperature required for lamination. Figure 7.9 illustrates the basic process.

### 7.5.3 Continuous lamination

Continuous lamination is a somewhat self-descriptive method wherein the laminate is produced in a continuous web. The prepreg and foil are fed into a specially designed and manufactured lamination press. There are both economical and technical advantages to such methods; however, there are only a very limited number of suppliers of such products. A conceptual example of continuous lamination is provided in Fig. 7.10.

TABLE 7.5 Substrate Materials for Electronic Devices\*

Type	Composition	General properties	Applications
CEM-1	Epoxy/glass fabric surface, epoxy/cotton paper core	Punchable at room temperature, good electricals but less than polyester, good flex and impact strength	Consumer electronics
CEM-3	Epoxy/glass fabric surface, epoxy/cotton paper core	Punchable but harder than CEM-1, good electricals, suitable for PTH applications	Computers, peripherals, keyboards
FR-4	Epoxy/glass fabric	High flex and impact strength, excellent electrical properties, commonly used for PTH applications	Computers, telecom, military
G-10	Epoxy/glass fabric, non-flame-retardant	High flex and impact strength, excellent electrical properties, excellent dimensional stability	Structural
FR-5	Modified epoxy/glass fabric	Improved hot flex strength compared to FR-4, excellent electricals	Military products
High-performance	Bismalimide triazine (BT), polyimide PTFE (Teflon <sup>®</sup> ), cyanate ester epoxy/PPE (Getek <sup>®</sup> )	Excellent thermal properties, lower x-y-z CTE, high reliability, excellent electrical properties	Chip interposers, mainframes, telecom, military
Flex	Polyimide, polyester, FEP	High flexibility, high-ductility copper, excellent electrical and thermal properties	Automotive, computers, military, telecom

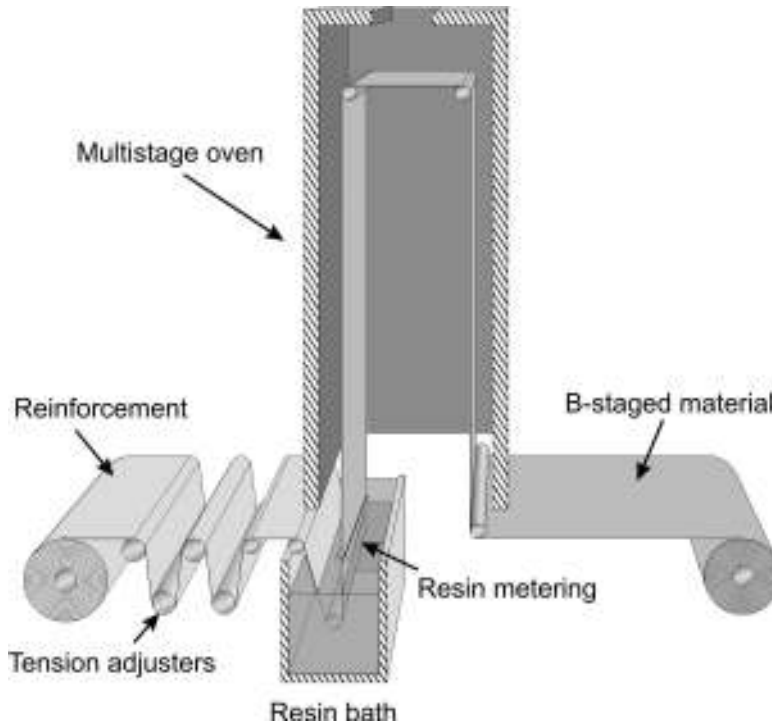
\*SOURCE: IPC.

#### 7.5.4 Vacuum-assisted lamination

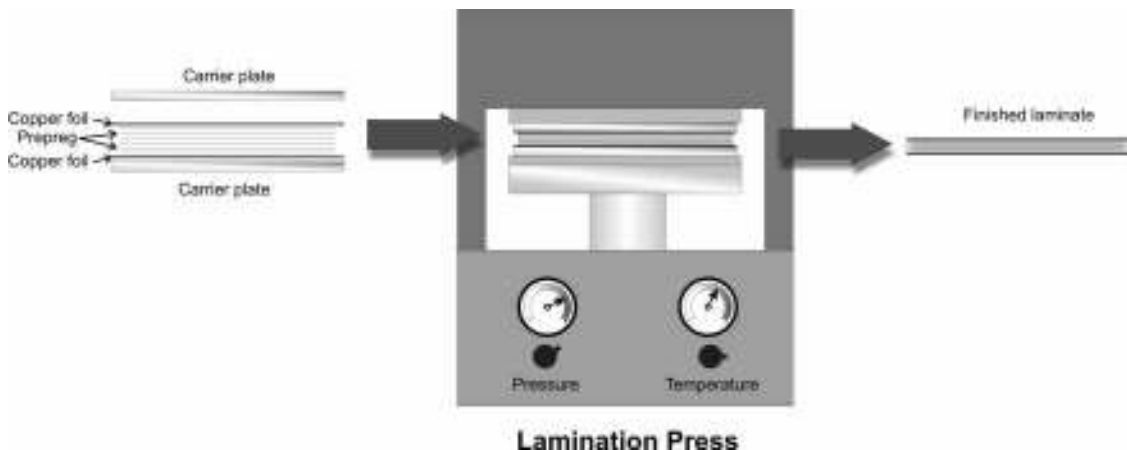
Traditional lamination methods can be improved by carrying out the process in a vacuum. The negative pressure facilitates the removal of entrapped air and can improve the quality of the laminate. The reduced pressure created by the vacuum allows for lower lamination pressures to be used with the hydraulic ram.

#### 7.5.5 Vacuum-assisted autoclave lamination

Vacuum-assisted autoclave lamination methods were originally developed for the lamination of complex shapes. The method takes advantage of normal atmospheric pressure by simple removal of air. The effect is the same as seen in vacuum-packaged foodstuffs, whereby the vacuum bag conforms to shape of the materials contained within. The negative pressure is augmented by gas pressure in a pressure vessel. This creates an isostatic or uniform pressure from all directions on the laminate stack and allows for lower lamination pressures to be used.

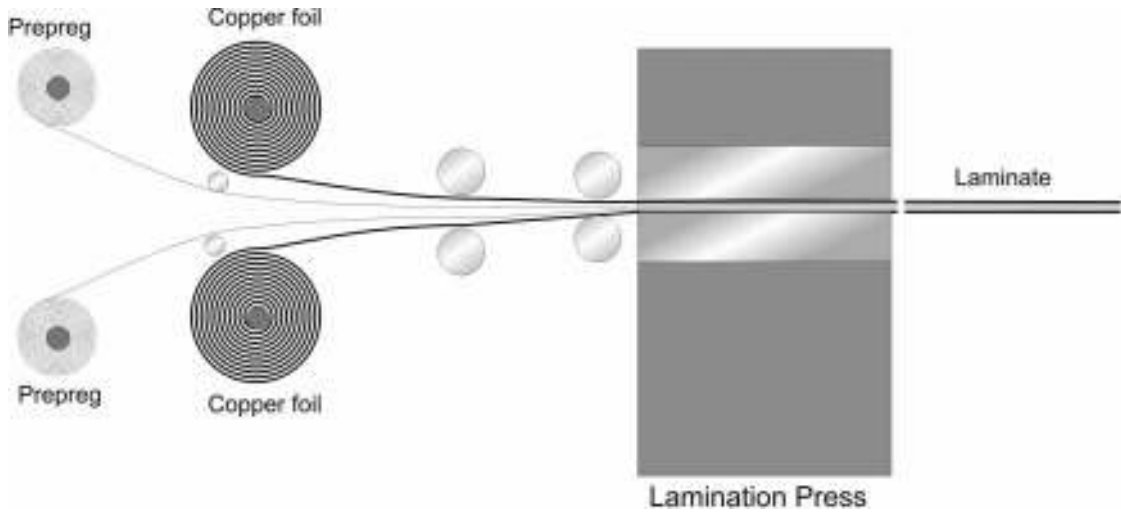


**Figure 7.8** Reinforcement materials such as glass cloth are converted into prepreg materials for laminate manufacture by coating them in special resin “treaters.” The material is coated with resin and then dried and partially cured in a special oven from which it emerges dry and tack free.



**Figure 7.9** Standard laminate manufacture is accomplished by placing plies of B-stage or prepreg between sheets of copper foil and applying heat and pressure.

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**Figure 7.10** Lamination methods have been developed that allow laminates to be manufactured in a continuous fashion. The basic concept is illustrated above.

## 7.6 Generic Process Overview for a Plated-through Hole Printed Circuit

The processing of printed circuits varies widely. As was indicated in the background section of this chapter, many different approaches to the manufacturing process have been tried and used since PCB technology was first developed. Still, some methods are more common than others. This is because materials, processes, and equipment for PCB manufacturing needed a focal point to create a viable infrastructure. The process description that follows is a somewhat “generic” process. The term “somewhat” is used, because many subtle differences can be employed at each of the process steps described.

This particular section will describe the manufacturing steps for making a plated-through hole printed circuit board using a pattern plating process. Most of the steps described are common for both double-sided and multilayer plated-through hole PCBs. Some alternatives to this process flow are described later in this chapter.

### 7.6.1 Stacking and pinning

Stacking and pinning is the term used to describe the act of cutting of sheets of copper clad laminate to a common size and the stacking them and pinning them all together to allow all the laminates to be drilled at one time. This is a common method for controlling the cost of drilling.

In the process, of creating the stack a backup material is always included on the bottom and an entry material may be used on top. The purpose of the backup material is to prevent the drill from drilling into the drill bed. The entry material can be one of a number of different materials. For example it can be a



sheet of 250- $\mu\text{m}$  aluminum foil or an unclad piece of a composite material of similar thickness. The purpose of the entry material is to reduce or eliminate the formation of drill burrs at the hole edge (see Fig. 7.11).

## 7.6.2 Drilling

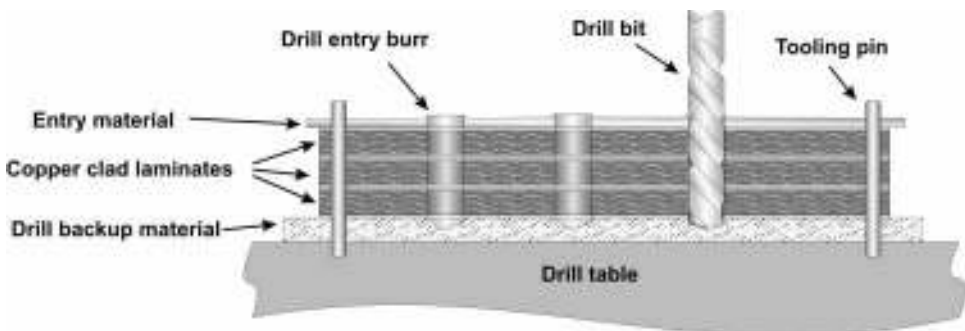
The drilling process is one of the more important steps in the manufacture of a printed circuit board. Today most if not all drilling is performed on numerically controlled drill machines. The stacked and pinned laminates are placed onto the drill bed and the pins, which extend beyond the surface of the drill stack, are placed in alignment holes located in the drill bed. The location of the holes serves as a datum for the drill program and all holes are drilled based on their location relative to these alignment pins.

Careful control of the drilling process is required to assure the quality of the final plated through hole. Hole quality is achieved by characterizing the materials in a drill study and by adjusting the in feed rate of the drill bit along with the speed of rotation of the drill bit. Excess time in the hole can cause resin smear, while too fast an in feed rate can break drills or result in rough holes.

## 7.6.3 Hole preparation and metallization

Hole preparation and metallization are also very important elements in the creation of a reliable plated-through hole PCB. A well plated through hole is highly reliable, but a poorly plated through hole may not be. The hole preparation steps vary from process to process and can be quite extensive. In addition, the metallization may be replaced with a coating of carbon or graphite film. The flow chart in Fig. 7.12 illustrates process flow for typical through hole preparation steps for electroplating. A general over view of hole wall preparation and metallization is provided below.

**7.6.3.1 Drill smear removal.** No matter how diligent one is in drilling the via, inevitably, the smear remaining on interconnect faces and the less-than-opti-



**Figure 7.11** Stack drilling greatly improves drill process productivity. The stack height can vary with the material, its thickness, and the drill diameter. Entry and backup materials play very important roles in the drill process.

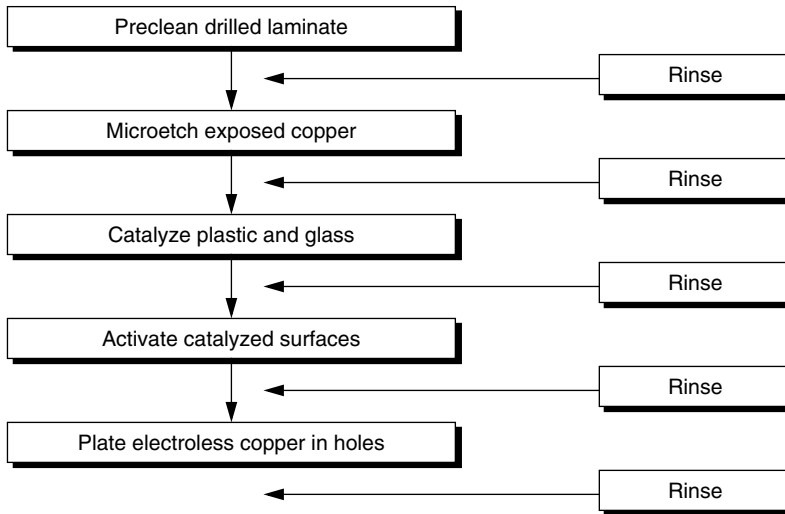


Figure 7.12 Basic electroless copper process flow.

mal topography of the hole wall present a significant challenge with respect to metallization. The goal of the metallization process to produce a continuous-void copper deposit that remains tightly adherent to the hole wall, resin, glass, and copper surfaces. While this sounds like a tall order, setting and controlling the desmear process will ensure that such a goal is met.

With respect to smear removal, several of wet-chemical, and one dry-chemical, methods can be utilized. These are sulfuric acid, chromic acid, alkaline permanganate, and plasma. Alkaline permanganate is by far the method of choice. Plasma, described as a dry chemical desmear process, is often employed when processing materials such as Kapton<sup>®</sup> or other very difficult-to-process materials such as polyphenylene oxide and epoxy resins. Otherwise, alkaline permanganate processes are very versatile for the majority of the fabricator's needs. The main issue with plasma is that it tends to leave the resin surface somewhat inert. This condition makes it difficult to achieve optimal adhesion of copper metal deposited during the metallization step. Common practice is to follow plasma with alkaline permanganate to impart a reasonable topography on the resin surface.

It is important to keep in mind that different resin types react differently to the alkaline permanganate process. Generally, the higher the degree of cross-linking, the less the degree of resin removal. For example, standard FR-4 ( $T_g$  of  $140^\circ\text{C}$ ) will experience a greater degree of resin removal (measured by weight loss) than a  $170\text{-}T_g$  material under the same conditions. Process engineers must adjust parameters of the alkaline permanganate process so as to achieve sufficient resin removal.

**7.6.3.2 Metallization.** The metallization of PWB substrates (in particular, the metallization that is necessary to render through holes and vias conductive

and reliable) is one of the critical success factors in PWB fabrication. Numerous experts in the field of plated-through via/blind via reliability have proven that long-term reliability is heavily dependent on the quality and uniformity of the copper deposit within the through hole and blind via.

The data largely support this fact. However, it is often not recognized that, to deposit a uniform copper layer in a blind via or through hole, the metallization process that precedes the application of the electrodeposited copper is the critical success factor. It is the process of making the via conductive that determines whether the subsequent electrodeposited copper will be continuous and adherent to the resin and any supporting structures such as glass or other fiber material. Today, several processes can be utilized to render vias conductive. These are as follows:

1. Electroless copper
2. Palladium-based direct metallization
3. Graphite
4. Carbon black
5. Conductive polymer

**Electroless copper.** Long considered the standard for metallization, electroless copper process consists of numerous steps. These steps are outlined in Fig. 7.12. The precleaning/conditioning step is required to remove oils, soils, and other contaminants. In addition, the resin surfaces and glass fiber bundles are conditioned to accept the tin-palladium catalyst. The microetch solution removes oxides from the copper surfaces and, in particular, the copper interconnects and the capture pads. This step is required to promote copper-to-copper adhesion to the critical interconnect interfaces such as the interlayer post or capture pad of a blind via. The predip is designed to minimize drag-in of copper to the tin-palladium activator. The palladium acts as a catalyst for the electroless copper plating process. Employing a complex chemistry (see Table 7.6), which normally utilizes formaldehyde as a reducing agent, a thin coating of copper is deposited on hole walls, interconnects, and, in the case of blind vias, the capture pad. However, a by-product of the electroless copper, hydrogen gas, is believed to interfere with the complete and uniform deposition of the copper. All chemical steps and rinses for the electroless copper process must be controlled. The process manual, detailing optimal operating conditions and chemical parameters, must be strictly followed.

The three most critical defects that manifest themselves at this stage are

1. Voids on the glass, resin, or both
2. Hole wall pull-away, whereby the plated copper fails to adhere to the hole wall
3. Interconnect defect, also known as *post separation*

**Direct plate.** Direct plating onto a palladium seed layer is a viable alternative to electroless copper. In the basic process, the palladium seed layer is of suffi-

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TABLE 7.6 Electroless Copper Bath Constituents

Bath constituent	Examples of sources	Purpose
Copper ions	CuSO <sub>4</sub> , Cu(NO <sub>3</sub> ) <sub>2</sub>	Metal source for reduction and deposition
Complexing agent	EDTA, quadrol	Prevents formation of Cu OH, acts as primary stabilizer
Formaldehyde	37% H <sub>2</sub> CO (13% methanol)	Reducing agent for electroless copper
Hydroxyl ions	NaOH, KOH	Raises pH to levels required for autoreduction reaction to occur
Stabilizers	Inorganic and organic sulfur compounds, oxygen, addition reagents for formaldehyde, metal salts, cyanides, and nitriles (additives typically present in the 0.001 to 200 ppm range)	Serve as secondary stabilizers moderating the rate of reaction and preventing spontaneous plate-out
Surfactants	Many different types of surface active agents explored, including cationic, anionic and nonionic types	Improve plating uniformity, effect mass transfer at metal surface, help to moderate evaporation

cient thickness to allow electrolytic plating of the through holes to be achieved.

**Graphite and carbon black.** Graphite and carbon are both sufficiently conductive to allow the circuit manufacturer to plate through holes with them, creating a carbon-based conductor. The plating rapidly coats the through hole in the process. Special processes are normally required, and care must be taken to ensure that the copper surfaces on the inner layers are cleaned before plating is applied.

## 7.6.4 Resist coating

Resist coating of drilled and metallized boards can be accomplished using any of several methods. Screen printing has been a mainstay process for many years; however, it is limited in terms of the features it can define. While it can be very cost effective, screen printing also has relatively long setup times as compared to other resist coating methods.

The other methods for resist coating are normally associated with photoimageable resists. These methods include, roll coating with dry film resist, flood printing with a liquid resist, and electrophoretic coating. The latter process is similar to electroplating except that a polymer film is plated rather than a metal one.

Roll coating of dry film is one of the most popular methods because of its relative ease and cleanliness. It also is capable of producing fine-line circuit images such as required by many of today's advanced products. In addition to variations in resist applications, there are two different forms of resist, based

on their exposure mechanisms and chemistry. The variations are called *positive working resists* and *negative working resists*. The former is less commonly used than the latter, although it is generally capable of resolving finer features. With positive working resists, the areas exposed to light are developed away; with negative working resists, the opposite is the case (i.e., where the light strikes the surface, the resist will remain after development). See Fig. 7.13 for examples of imaging processes.

### 7.6.5 Image patterning

An imaging step is required for all photoimagable plating resists. The process is self-descriptive; however, there are a number of potential variations on the exposure process. Perhaps the most common form of exposure is contact printing, wherein a film containing the desired circuit pattern is aligned with the drilled hole pattern, and the two items are brought into intimate contact by means of a vacuum frame. Exposure is done by means of a UV light source, and exposure length is determined by the type of resist and its thickness.

Other processing methods include off-contact printing and laser-direct writing. In the former case, exposure is accomplished by image projection over a short or long distance. In the latter case, a laser is used to scan the image onto the resist. These methods may see increased use in the future.

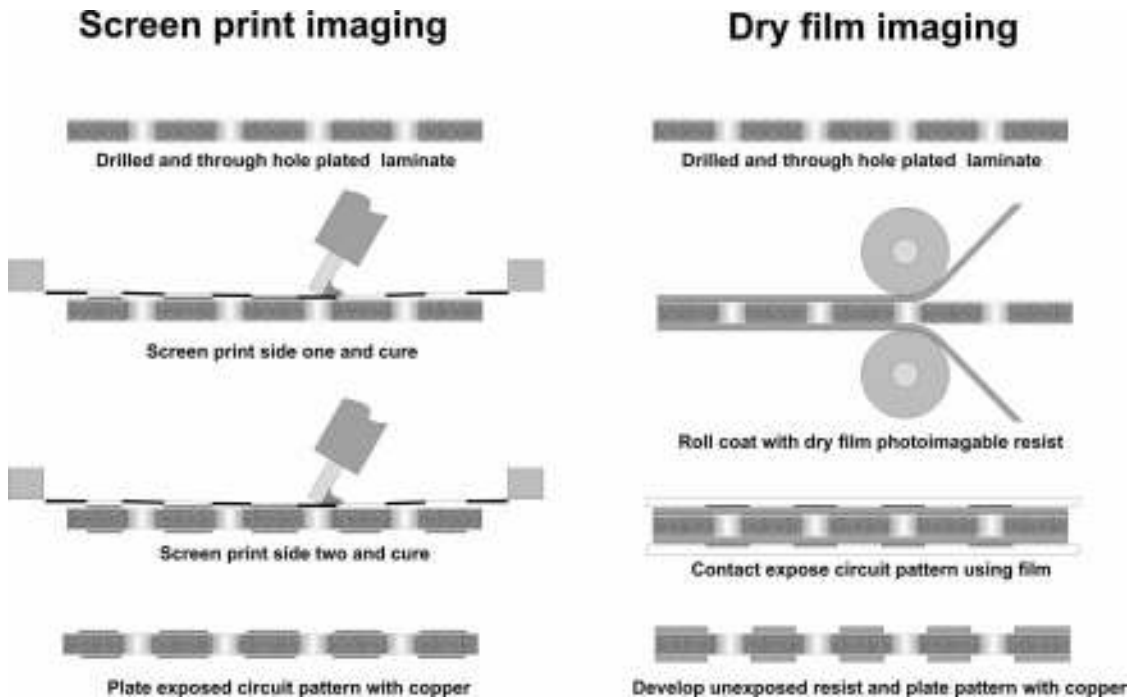


Figure 7.13 Imaging process comparison between screen printing and dry film lamination.

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### 7.6.6 Image development

Development is normally carried out using a conveyORIZED process whereby the exposed panels are passed between spray banks of a solution that is designed to dissolve the unexposed resist (or exposed resist, in the case of a positive working resist). Presently, the solutions used are relatively benign and consist of heated dilute (~1 percent) solutions of sodium or potassium carbonate. Care must be taken to avoid overexposure and underexposure and, similarly, to neither overdevelop nor underdevelop the resist. Failure to do so can lead to problems in later processing steps.

### 7.6.7 Electroplating of the circuit pattern

Electroplating processes are used to bulk metallize the circuit patterns on the surface and through the holes. Because a negative image of the circuit is most commonly patterned onto the drilled and metallized panel, this process is called *pattern plating*.

In the process, the panel is clamped in a plating rack of some sort so that an electric potential can be applied. Because the metal ions in solution are almost invariably positively charged, a negative potential is placed on the rack. The panel is called the *cathode* in this case. The thickness of the copper and other plated metals is controlled by a combination of time and current. Normally, copper is plated to a total thickness of approximately 25  $\mu\text{m}$  (0.001 in), but thicker callouts are common in military boards. Other metals are often plated over the top of the copper. These metals include, tin, tin-lead solder, nickel, gold, and others. The thickness of these metals is normally substantially less, as they serve as finishing metals only.

### 7.6.8 Resist stripping

After all the required metal plating layers are completed, the plating resist is no longer required, so it can be removed. This is accomplished by exposing the plating resist to a suitable chemistry. The chemistry will vary with the chemistry of the resist, but it is normally an alkaline solution with surfactants. A suitable resist stripping chemistry will safely remove the resist without damaging the metal finishes. Whereas resist stripping can be performed using a batch dipping process, conveyor-based processes, vertical and horizontal, are very common. Care must be taken to fully remove the resist and properly rinse the boards after stripping, or problems can arise during the etching process. The greatest concern is shorts or bridges between circuit traces caused by leftover resist.

### 7.6.9 Copper pattern etching

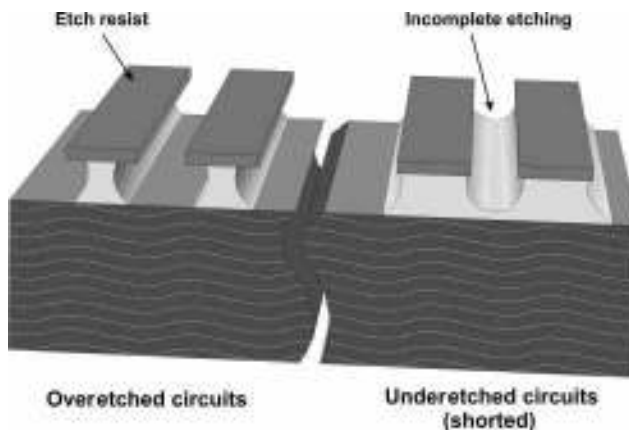
An etching step normally follows the stripping process. The etching step removes all of the copper that is not coated with either a suitable etch resistant metal or polymer etch resist. When metals are used as the etch resist, they obviously must be resistant to the etching chemistry. For example, when tin or

tin-lead is employed as the etch resistant metal, ammonia-ammonium chloride and sulfuric-hydrogen etchants can be used, but cupric chloride etchants cannot. Etching must be controlled so as not to neither overetch nor underetch the circuits. The effects of both are illustrated in Fig. 7.14. Etching can result in shorts. Close spacing of traces with thicker copper foils are often contributing factors.

### 7.6.10 Solder mask

Solder masks are used to prevent solder from being deposited or flowing onto circuit features other than the proper areas of interest, such as points of attachment. Solder masks were originally developed for PCBs that were to be assembled using wave soldering methods, and they were originally applied only to one side of the PCB—the side that was to be exposed to the solder wave. Without a solder mask, circuit traces on the bottom of the assembly were subject to shorting with solder bridges. Later, as line traces and spaces became finer, the application of solder mask to both sides of the board was implemented to protect the traces from physical damage and inadvertent shorting. Today, with double-sided assembly in widespread use, it is very common for solder mask to be applied to both sides of the PCB.

With the technology trending toward finer lines and tighter spaces, and with the proliferation of microvia technology, solder mask is assuming even greater responsibilities in bare-board fabrication. Liquid photoimagable solder masks (LPISMs) are clearly leading the market. Screen print masks, which dominated the industry for many years, are only marginally reliable for today's products, given their great difficulty in resolving lines and spaces smaller than 10 mils in width. Clearly, liquids have made significant inroads.



**Figure 7.14** Control of the etching process is vitally important to the successful manufacture of a printed circuit. Overetched circuits may not meet designed performance requirements, and underetching can result in shorts. Close spacing of traces is often a factor in both cases.

Presently, solder masks are available in several forms and chemistries. These are reviewed in the following sections.

**7.6.10.1 Solder mask, general types.** Solder masks are provided in several different formats, each having different curing mechanisms. There are three general types.

**Heat-curable resins.** Heat-curable resins are a common type of solder mask. They are commonly applied using screen printing methods. In application, the solder mask resin, normally an epoxy, is screen printed onto everything except the areas and through holes that will be used for assembly.

**UV-curable resins.** UV-curable resins are normally applied in the same fashion as described for heat-curable resins; however, they have the advantage that they can be quickly cured by exposure to UV light. The properties of these masks differ somewhat from the heat-cured types, but they are generally well suited to the task.

**Photoimageable resins.** Photoimageable resins are similar to UV-curable resins but with the added advantage that they can be easily photodefined or exposed and developed with an appropriate chemistry. These materials can be applied in wet form by spraying, dipping, curtain coating, or flood screening, or in dry form as a laminated film.

**7.6.10.2 Solder mask formulations.** Typically, the chemistry used in LPISMs falls into three general categories.

1. Epoxy
2. Acrylate
3. Epoxy-acrylate

It is generally accepted that the “epoxy-only” formulations offer superior adhesion and resistance to solvents than do the acrylate or epoxy acrylate blends. These facts, however, do not obviate the latter two from the market. The epoxy-only masks display a toughness and resistance to chemical degradation as a result of a high degree of cross-linking. Because these bonds occur in three dimensions, the epoxy presents an excellent barrier to moisture and other solvent penetration. Epoxy coatings are compatible with the epoxy of the substrate, thus promoting excellent adhesion.

Acrylates, the other major material category, are known for processing speed. UV curing, as opposed to thermal cycles required of epoxy-only masks, offer very fast curing times. Some suppliers market epoxy acrylate blends that offer properties that lie in between the epoxy- and acrylate-only systems.

Today, most all LPISMs contain some epoxy oligomers and polymers formulated with the acrylate-based chemistries. The acrylate groups are bound to the epoxy molecules to speed up exposure time. This type of mask is given a fi-



nal cure to complete the cross-linking reaction and advance the physical and electrical properties of the mask.

As one may surmise, LPISM formulations are much more complicated than described above. Listed below is one formulation gleaned from several patents and private conversations over the last few years. Each component listed has a specific purpose, and substitutes are probably available.

Ingredient	Purpose	Wt%
Butyl cellosolve	Solvent	8.5
Carbaset resin (Goodrich)	Cross-linking resin	30
Triethylene glycol diacrylate	Oligomer	18
N-methylol acrylamide	Monomer	5
Syloid (WR Grace)—silica	Filler	15.5
Kynar 301F (polyfluoride)	Filler	13
Irgacure 651 (photoinitiator)	Photoinitiator	4
Carboxybenzotriazole	Adhesion promoter	6
Antioxidant 2246	Oxidation inhibitor	0.1

A proper balance of resin, filler, photoinitiators, and acrylate materials will be critical for the success of the LPISM.

It should be noted that some LPISMs currently on the market contain solvents (as in Table 7.6), but others are aqueous based. Generally, if the mask requires a drying step before exposure, it most likely contains a solvent. Another caveat: is the exposed mask aqueous and solvent developable? Solvent-based processing brings its own issues to the board fabrication facility and must be dealt with on a case-by-case basis.

Another aspect of solder masks is whether the formulation is a single-part product or requires a mix on site. The single-part variety is preferred, because it eliminates the possibility of operator error in the form of adding too much or too little of a component. With single-pack materials, however, the shelf life is limited. It may be important for any company serving this market to offer both types of mask.

**7.6.10.3 Solder mask selection criteria.** A number of criteria are of the utmost importance to the fabricator, end user, and assembly house. Table 7.7 lists these criteria.

If a particular solder mask process has any chance of market penetration, the process must meet UL and IPC standards (IPC-SM-840C). Certainly, the mask must also have been qualified and approved by the end user. In addition, the 2000 IPC Technology Roadmap noted that, in the year ahead, LPISM

**TABLE 7.7 Important Solder Mask Selection Criteria**

Manufacturing area of concern	Selection criteria
PWB fabricator	UV cure needed Smallest hole size cleared Acts as plating resist (nickel-gold) Solvent content—low VOCs Tack dry process window Material costs Photo speed Fine pitch resolution
PWB assembler	Adhesion to metallic surfaces Hardness Glossiness Dam holding capability Flux compatibility Solder paste compatibility
Final product vendor	Surface insulation resistance Breakdown voltage Ionic retention Coverage thickness Performance UL approval Key OEM acceptance Conforms to IPC-SM 840 C

must be capable of holding 2-mil solder dams and have uncompromising compatibility with a variety of assembly materials and electroless plating processes.

**7.6.10.4 Solder mask application.** Solder mask coating operations vary with the type of mask being applied. For example, screen printing can be used to apply the solder mask everywhere except the areas where soldering is to take place. In contrast, dry film solder masks are roll laminated onto the circuit using heat and pressure. The coated circuit is exposed and developed in a fashion nearly identical to the process used for circuit patterning with dry film.

Several methods are available for applying the liquid photoimageable solder masks.

1. Curtain coating
2. Electrostatic spray
3. High-volume, low-pressure (HVLP) spray
4. Screen printing (either horizontal or vertical)

**Curtain coating.** With this method, a PCB is transported horizontally along a conveyor, and the solder mask is applied as a liquid stream or curtain. The curtain is formed as the ink falls through the coating head. Only one side of

the board can be coated at a time. Ink formulations for curtain coating are lower in solids content than standard screen coating inks. Thus, the mask will not plug holes in curtain coating applications. The speed of the conveyor transporting the board determines wet ink thickness, and subsequently, mask thickness.

The advantages of curtain coating are as follows:

- high productivity
- relatively uniform resist coating thickness
- good coverage over circuit traces in general
- relatively little waste of material

The disadvantages are

- Low resist viscosity may lead to resist falling off traces (excess solvent added).
- Low solids and high solvent content make it less economical than a screen coat.
- Some issues exist with air entrapment.
- Only one side of panel can be coated at a time.
- High solvent content may cause regulatory problems.

**Electrostatic spray coating.** From an academic point of view, electrostatic coating of a printed wiring board is not purely electrostatic. Because the PCB is mostly an insulator at the point of solder mask application, a pure electrostatic process is questionable. To make this coating process work, the solder mask material is conducted into a high-rotation spray bell under high voltage. The resist flow tears off at the bell edge to form microdroplets. These droplets become charged at the spray bell then deposit on the PCB and discharge electrically. The printed wiring board must be earthed so that the droplets of resist can discharge. An electric field develops between the first very thin resist coating on the board and the spray bell. Electrical lines of flux concentrate on circuit traces. This allows for the resist coating to build up, starting from the edge. One can achieve excellent coverage this way.

Electrostatic processing has the following advantages:

- High productivity
- Plated-through holes not filled with resist
- Resist thickness easily adjusted
- No entrapped air in the coating

The following disadvantages are involved with electrostatic coating:

- High resist consumption due to overspray
- Coating thickness fluctuations

- Relatively high capital investment
- Tenting very difficult

**High-volume, low-pressure spray.** There are two variations to spray coating: (1) horizontal and (2) vertical. In horizontal processing, only one side of the board is coated at a time. In most such systems, the panel is tack dried before the second side is coated. Some systems include a variation whereby, after coating one side, the panel is carried on a V belt. The panel is flipped and the second side coated before the tack dry is carried out. In this case, the panel is tack dried only once. However, it is difficult to process very thin panels in such a system.

Newer models transport the panels on a conveyor. The heated spray guns first coat the bottom side of the panel, which is followed by a coating of the panels on the top side prior to tack dry. With vertical HVLP spray applications, both sides of the PWB are coated simultaneously. Typical equipment utilizes four heated spray heads with overlapping spray patterns. Models are available to coat are 100, 200, and 300 panels per hour.

The advantages of HVLP spray processing are

- Excellent coverage of dense circuit traces
- High productivity
- Relatively low capital costs

The major disadvantages of HVLP include

- Overspray major issue/contamination of equipment
- Tenting/plugging of holes impossible
- Spray coatings exhibit a slight orange peel appearance

**Screen printing.** Screen printing is accomplished either horizontally or in a double-sided vertical mode. On a worldwide basis, screen coating of solder mask is the most popular means of application. Single-sided methods, primarily for hand screening, are easy to use and have a low entry cost.

In double-sided screen coating, the panels are fixed vertically, and the screens are fixed at an equal distance to the vertical panels. Squeegees on both sides of the panel are placed in exactly the same position on the opposite side of the panel while utilizing identical squeegee angle.

Double-sided vertical coaters made popular by Circuit Automation boast high productivity as a result of their ability to coat both sides of the board simultaneously. Other advantages of the double-sided method are

- Tack dry of both sides simultaneously
- No risk of over drying one side
- Consistent exposure and development

- High solids content; economical usage compared to other methods
- Lower wet ink weights; uniform edge coverage

The major disadvantages of the double-sided screen print method are

- Low productivity as compared to other methods
- Skipping possible on very dense circuitry
- Screen printing stencils require setup time and increased cost
- High squeegee velocities may cause skips and blisters

**7.6.10.5 Performance requirements.** Solder masks in general are facing much more stringent performance requirements. Liquid photoimageable solder masks in particular are viewed as being a key enabling type for future products and are thus being required to meet an ever more challenging set of performance criteria. Generally, solder mask performance is measured based on the following:

- Ability to hold 2-mil solder mask dams
- Sufficient coverage over traces without high thickness on laminate
- No bubbles or pinholes in the mask
- Shortest possible processing times
- Ink easily developed out of holes
- Nearly vertical sidewalls
- Ability to be processed in nickel-gold plating solutions

Liquid photoimageable solder masks must meet all the criteria set forth in

- IPC-SM 840C
- Siemens SN 57030
- UL 94 V-0
- Bellcore NWT-TR-000078
- Thermal shock testing according to IBM

Typically, all solder masks must be able to resist attack by solvents and other chemicals that may come in contact with the mask during plating and assembly operations. A critical feature desired of all solder masks presently is to serve as a low-level environmental protectant. That is, the mask must provide a minimum acceptable insulation resistance; must not exhibit evidence of electrical migration; and shall not exhibit blistering, delamination, or crazing when tested under TM 2.6.7.1 of the IPC-TM-650.

### 7.6.11 Solderable finishes

Surface finish is critical to the creation of reliable interconnections. Connection from the board to a device occurs at the surface. However a surface finish used for solderability purposes only is at best a compromise. In an ideal world, the assembly engineer would receive bare copper PWBs for assembly. There would be no issues with flatness, product density, cleanliness, and so on. Unfortunately, this is not an ideal world. The ability of the assembly process to deal with oxidized copper as the solderable surface, with the flux activity used in today's assembly industry, is not presently a possibility. Because of this, the assembly engineer/designer needs to choose a surface finish that will meet, to the maximum extent possible, the product's needs, also keeping in mind that in today's highly cost-sensitive environment, the choice of the surface finish may be influenced heavily by its per-unit cost.

**7.6.11.1 Tin-lead finish.** The original surface finishes were by-products of PWB manufacturing; tin-lead (SnPb) as an etch resist, subsequently reflowed and fused, became the surface finish of preference for many years. This was commonly accompanied by a mix of electrolytic nickel gold to plate the tabs for edge connectors, and the combination directly reflected the technology of the components and assembly techniques of the time.

The introduction of SMT technology forced a change from the simple reflow SnPb surface finish to one that would meet the demands of the assembly industry. New designs required innovative solutions. Ball grid arrays, wire bonding pads, press fit, and contact switches were all outside the traditional realm of HASL and electrolytic nickel gold.

In addition, supposedly environmental concerns are being focused on the elimination of lead. No data has ever been presented to show that lead in electronic solders causes harm; however, marketing pressures and legislation are driving many companies to provide lead-free solutions. As a result, it can be anticipated that HASL will be modified from a standard solder to a new lead-free HASL and a new series of surface finishes.

**7.6.11.2 Organic solderability preservatives.** Organic solderability preservatives (OSPs), as the name implies, are organic coatings that preserve the copper surface from oxidation until it is soldered. The two most widely used preservatives are nitrogen-bearing organic compounds. *Benzotriazoles* is one class, and *imidazoles* is the other. Both of these organic chemicals have the ability to complex with the exposed copper surface. In that respect, they are copper specific and do not adsorb to the laminate or the solder mask.

Benzotriazoles form a monomolecular layer and protect the copper until it is exposed to a single thermal excursion at assembly. The coating will readily volatilize under reflow thermal conditions. Imidazoles form a thicker coating and will survive multiple thermal excursions at assembly.

**Process.** The following is a representative process for coating copper circuits with an OSP:

Process step	Temp., °F	Temp., °C	Time, min*
Cleaner	95–140	35–60	4–6
Microetch	75–95	25–35	2–4
Conditioner	85–95	30–35	1–3
OSP	120–140	50–60	1–2

\*For conveyORIZED equipment, the dwell time must be reduced. Consult with equipment and chemical suppliers.

**OSP finish.** A thin layer of organic compound coats the copper surface. The coating is as low as 100 Å for benzotriazoles and as high as 4000 Å for imidazole-type preservatives. The coating is transparent and not easily discernible, making inspection difficult.

**Component assembly and joining using OSP.** During the assembly and joining (i.e., soldering) process, the organic coating is readily dissolved into the screened paste or into the acidic flux, in either case leaving a clean active copper surface for soldering. The solder then forms a copper/tin intermetallic joint. Imidazoles may require a more aggressive flux after the first and second thermal excursions. Assemblers who use OSP are very familiar with the fluxing requirements for this finish.

**Limitations of OSP.** Because the coating is transparent and colorless, it is difficult to inspect. The organic coating is nonconductive. Benzotriazole, being a very thin coating, does not interfere with electrical testing. Some imidazoles, on the other hand, are thick enough to interfere with electrical tests. Most shops that use these thicker coatings do their electrical testing prior to OSP applications.

**7.6.11.3 Electroless nickel immersion gold (ENIG).** In this finish, a layer of electroless nickel with a thickness of 120 to 240 μin (3 to 6 μm) is deposited on the copper surface. The electroless nickel plating is followed by deposition of a thin coating (2 to 4 μin) of immersion gold. The nickel is a diffusion barrier to copper and is the surface to which the soldering occurs. The function of the immersion gold is to protect the nickel from oxidation or passivation during storage.

**ENIG process.** The following is a representative process for coating a copper surface using ENIG:

Process step	Temp., °F	Temp., °C	Time, min.*
Cleaner	95–140	35–60	4–6
Microetch	75–95	25–35	2–4
Catalyst	RT	RT	1–3
E nickel	180–190	82–88	18–25
I gold	180–190	82–88	6–12

\*Note: The long dwell times needed for this process make horizontal conveyerization impractical.

**Applications for ENIG.** ENIG gives a flat coplanar surface. It is solderable, wire bondable, and ideal as a switch contacting surface. ENIG has excellent solder wettability characteristics. The gold readily dissolves in the molten solder, leaving a fresh nickel surface to form the solder joint. The amount of gold that dissolves in the solder is insignificant and will not cause solder joint embrittlement. The nickel forms a tin/nickel intermetallic joint.

**7.6.11.4 Electroless nickel/electroless palladium/immersion gold (ENEPIG).** This finish has proven useful to some circuit providers. In the process, an electroless nickel layer of 120 to 240  $\mu\text{m}$  (3 to 6  $\mu\text{m}$ ) is deposited on the copper surface. This is then coated with an electroless palladium layer of a thickness of 4 to 20  $\mu\text{m}$  (0.1 to 0.5  $\mu\text{m}$ ) and, finally, topped with immersion gold at 1 to 4  $\mu\text{m}$  (0.02 to 0.1  $\mu\text{m}$ ). The electroless palladium layer eliminates any probability of corrosion that may be caused by the immersion gold deposition reaction and creates an ideal surface for gold wire bonding. The gold layer caps the palladium and ensures that its catalytic activity is contained.

**Process steps.** The sample process steps for a process to produce circuits with electroless nickel with palladium finish are provided in the following table:

Process step	Temp., °F	Temp., °C	Time, min.
Cleaner	95–140	35–60	4–6
Microetch	75–95	25–35	2–4
Catalyst	RT	RT	1–3
E nickel	180–190	82–88	18–25
Catalyst	RT	RT	1–3
E palladium	120–140	50–60	8–20
I gold	180–190	82–88	6–12



**Applications for ENEPIG.** ENEPIG gives a flat coplanar surface. ENEPIG is the universal surface finish. It is capable of functioning as the ENIG finish. In addition, the electroless palladium at this thickness makes an ideal surface for gold wire bonding.

During soldering, the palladium and the gold both eventually dissolve in the solder, and the joint forms a nickel/tin intermetallic. During wire bonding, the aluminum and the gold wires bond to the palladium surface. Palladium is a hard surface and is suitable for contact switching.

**Limitations of ENEPIG.** The primary limitation for this finish is the additional cost of palladium as well as the added processing steps at the board shop.

**7.6.11.5 Immersion silver.** In principle, immersion silver deposits provide a thin (5 to 15  $\mu\text{m}$  or 0.1 to 0.4  $\mu\text{m}$ ) dense silver deposit incorporating an organic. The organic seals the surface and allows for extended shelf life. Silver offers a flat, extremely solderable surface that may be applied with high productivity in conveyORIZED equipment. The surface is also bondable for both aluminum and gold wire.

**Process steps.** The process steps are as shown in the following table:

Process step	Temp., °F	Temp., °C	Time, min.*
Cleaner	95–140	35–60	4–6
Microetch	75–95	25–35	2–4
Predip	RT	RT	0.5–1
I silver	95–115	35–45	1–2

\*For conveyORIZED equipment, the dwell time must be reduced. Consult with equipment and chemical suppliers.

**Application of immersion silver.** Immersion silver is an ideal surface for soldering. During assembly, the silver readily dissolves into the solder, allowing the formation of a copper/tin intermetallic solder joint, similar to HASL and OSP. It offers the coplanarity that HASL lacks, and it is also lead free. Unlike OSP, it offers ease of inspection with no compromise in performance after the third thermal excursion. Immersion silver lends itself well to electrical testing in the board shop. At this time, the application as a contact surface for extended use remains to be demonstrated.

**Limitations of immersion silver.** The concern with silver has always been silver migration in electronic environments. This is a result of the property of silver to form water-soluble salts when exposed to moisture and electrical bias. Using immersion silver with the incorporation of organics minimizes this phenomenon. In addition, the immersion silver as a surface does not survive the assembly process. After wire bonding, the exposed silver is encapsulated and hence is isolated from the environment.

**7.6.11.6 Immersion tin.** Immersion tin became viable as a surface finish when two problems, grain size and copper/tin intermetallics, were overcome. The deposit was engineered to be very fine grained and nonporous. A thick deposit of 40  $\mu\text{m}$  or 1.0  $\mu\text{m}$  was feasible, thus ensuring a copper-free tin surface. A new class of immersion tin processes provide exactly that.

**Process for immersion tin.** The following are representative processing steps for the immersion tin process:

Process step	Temp., °F	Temp., °C	Time, min.*
Cleaner	95–140	35–60	4–6
Microetch	75–95	25–35	2–4
Predip	75–90	25–30	1–2
I tin	140–160	60–70	6–12

\*For conveyorized equipment the dwell time must be reduced. Consult with equipment and chemical supplier.

**Application of immersion tin.** Immersion tin is a highly solderable surface and forms the standard copper/tin intermetallic solder joint. Tin provides a dense, uniform coating with superior hole wall lubricity. This characteristic makes it the choice for backplane panels that are assembled by *press fit* or *pin insertion*.

**Limitations of immersion tin.** The bath makeup entails the use of thiourea, which is banned in certain geographical locations for environmental reasons. During processing in the board shop, the primary by-product in the bath is copper thiourea. Waste treatment allowance must be made for the containment of the thiourea and its copper-salt by-product.

The shelf life of the surface is, to some extent, limited (less than one year). This is a result of the progression of the copper/tin intermetallic until it reaches the surface and renders the product nonsolderable. This could accelerate under excessive temperature and humidity conditions.

**7.6.11.7 Surface finish summary.** Each one of these surface finishes offers connectivity solutions in some areas. Only one ENEPIG is capable of meeting all the different assembly requirements. It is often referred to as the “universal finish.” The cost of such a process is very high. However, the ENEPIG surface finish offers both wire bondability and solderability.

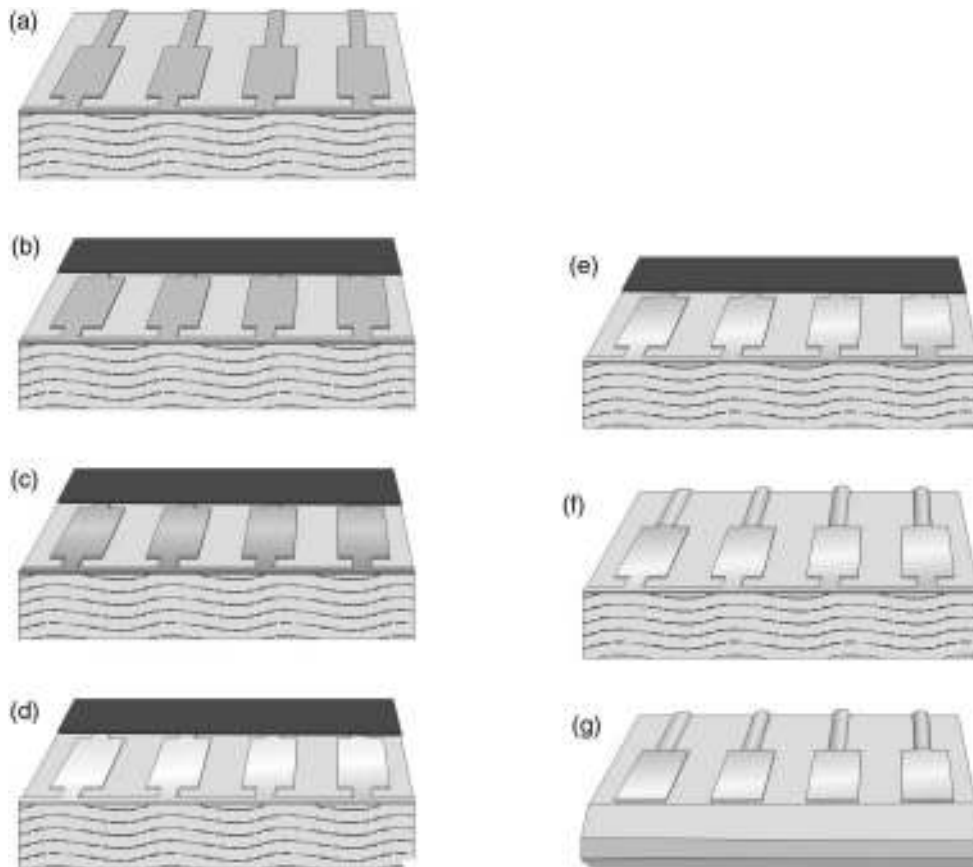
## 7.6.12 Edge card contact plating

Edge card contacts are a convenient way of interconnecting the circuit card to a next level or system board. The process of plating edge card circuits consists of a few modest steps. First, the area above the contacts is masked off using a

suitable “plater’s tape.” If a metal etch resist was used, this is removed using an appropriate chemistry (i.e., one that does not aggressively attack copper). The exposed copper is overplated first using nickel and then (normally) gold. The nickel acts as a barrier layer to prevent diffusion of copper into gold. It also serves as an anvil of sorts, because both copper and gold are relatively soft metals and can be easily galled. The process steps are illustrated in Fig. 7.15.

### 7.6.13 Depanelization processing

Once all major processing steps are completed, the panel can be separated into individual circuits. This process is called *depanelization*. The two primary methods for separating out the circuits are punching and profiling. Punching requires a tool and die set and tooling holes to ensure the parts are properly aligned for punching. Profiling is commonly done using a numerically controlled (NC) router. Again, tooling holes are required to ensure accuracy. Other numer-



**Figure 7.15** Edge card contact manufacturing steps: (a) etched contacts with bus, (b) apply chemical resistant tape, (c) etch solder (or other metal), (d) plate nickel barrier metal, (e) plate gold over nickel, (f) remove tape from circuit, and (g) shear bus and bevel edge.

ically controlled cutting methods are potential candidates for depanelization of circuits, including the use of lasers and high-pressure water jet cutters.

When small circuits are being designed, it is normally advantageous to assemble the circuits in panel form. In such cases, the circuits are commonly cut only part way out of the panel. Following assembly, the circuits can be separated into individual parts by cutting the tabs that hold the circuits in the panel. For rectangular circuits, one- or two-side scoring of the panel can be used instead. This allows the assembly to be easily snapped apart in chocolate bar fashion. A word of caution is offered, however. One must exercise care, as it is possible to crack solder joints and components when snapping apart such assemblies. Figure 7.16 illustrates the general concepts just described.

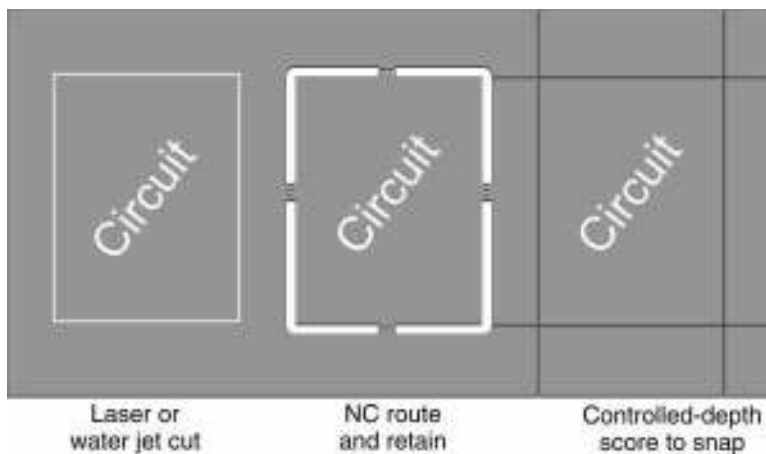
#### 7.6.14 Edge beveling

Following depanelization, it is common practice to bevel the edges having contacts to facilitate insertion. Special tools have been developed that make this process very simple. The last step in Fig. 7.15 illustrates a beveled edge.

#### 7.6.15 Additive and subtractive processing

There are two primary methods for creating metal circuit patterns on insulating base materials, additive and subtractive. There are also a number of potential variations on these two common themes; for example, there are processes that use combinations of these two, such as so-called *semiadditive* or *semisubtractive* processes. A brief examination of some of these themes will help to clarify the differences.

**7.6.15.1 Additive processes.** There are several approaches to making additive circuits, so there is potential for some confusion in the terms used for some of



**Figure 7.16** Methods for depanelizing finished circuits.

these manufacturing concepts, which are similar in intent but very different in process. Some of the first circuits manufactured in volume used what must be considered, in practical terms, additive processing methods. These circuits were produced by screen printing circuits directly onto insulators. The insulators could be either organic (such as epoxy or polyester resin) or inorganic (such as ceramic or glass) in nature. Other methods for creating additive circuits include electroless copper-plated circuits and transfer laminated circuits. Figure 7.17 illustrates the process steps for a simple two-sided additive board.

**7.6.15.2 Subtractive processes.** Subtractive processes were also used very early on in the development of circuit manufacturing methods. While the so-called “print-and-etch” process is the most common image of subtractive processing, there are a number of possible variations. These include punching of copper foil, embossing and milling, and various plate-and-etch processes. The panel plate subtractive process in Fig. 7.17 illustrates the process steps for manufacture of a two-sided subtractive PCB.

**7.6.15.3 Semiadditive processes.** There is a crossover point at which the line blurs, regardless of whether a process is additive or subtractive. Such processes are most often called *semiadditive*, but the term *semisubtractive* is also used occasionally. The term is most often used for describing processes wherein a very thin layer of copper foil is used on the other layers. The chief advantages are that it allows very fine line circuits to be produced and that a lesser amount of materials, such as etching solutions, are consumed in processing. Figure 7.17 provides a simple example of this process for manufacturing a two-sided PCB.

## 7.7 Single-Sided Circuit Process Examples

Having earlier described a general process for a double-sided PCB, it is now possible to describe fairly easily some common single-sided circuit processes. A number of potential methods and variations on their themes exist. The following are a few examples.

### 7.7.1 Print-and-etch

Print-and-etch processing is perhaps the least complex method for making a simple printed circuit. In processing, the metal foil clad laminate is coated with a circuit pattern using any of the previously describe processes, and the circuit is etched. Holes, if needed, can be drilled before or after etching. Figure 7.18 shows a cross section of the simple construction.

### 7.7.2 Foil routing

A novel method for producing single-sided (also double-sided, with special processing) circuits is to rout the metal-clad laminate to a controlled depth, re-

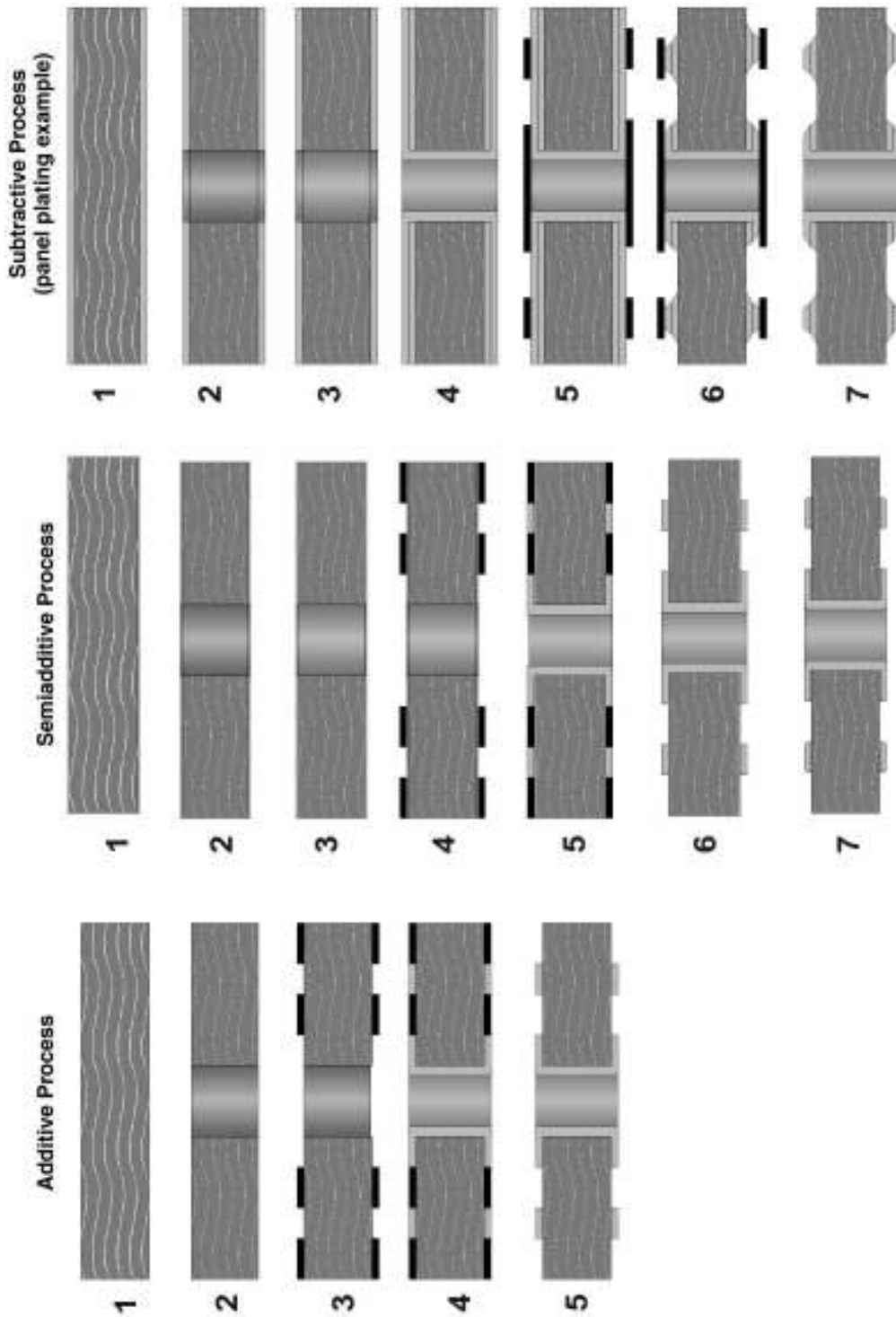
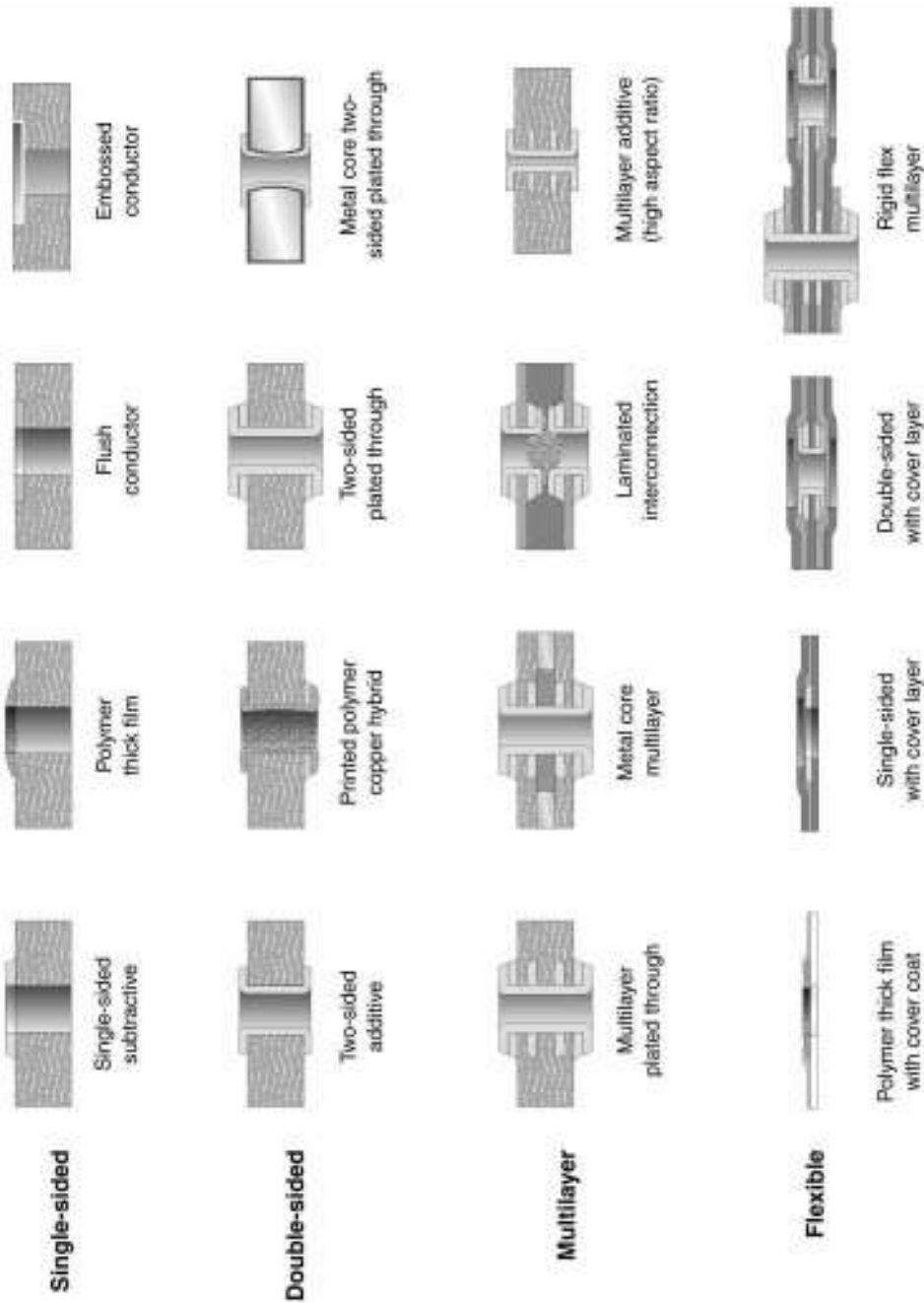


Figure 7.17 Comparison of three different PCB manufacturing methods.



**Figure 7-18** Numerous ways exist to fabricate PCBs, and there are also many different possible constructions. Shown above are samples of some of the constructions used. (Note: The cross sections are not all drawn to a common scale.)

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moving the copper that is not needed for the circuit. Thus, each circuit trace is individually defined by routing completely around its periphery. The process is obviously slower than etching and allows only one circuit to be manufactured at a time, but it is nonpolluting and can be done in a small space. Figure 7.19 provides examples of product produced in this fashion.

## 7.7.3 Direct printing with conductive ink

Direct printing of the circuit pattern with conductive ink is one of the oldest methods and was described briefly earlier in this chapter.

## 7.7.4 Flush grinding

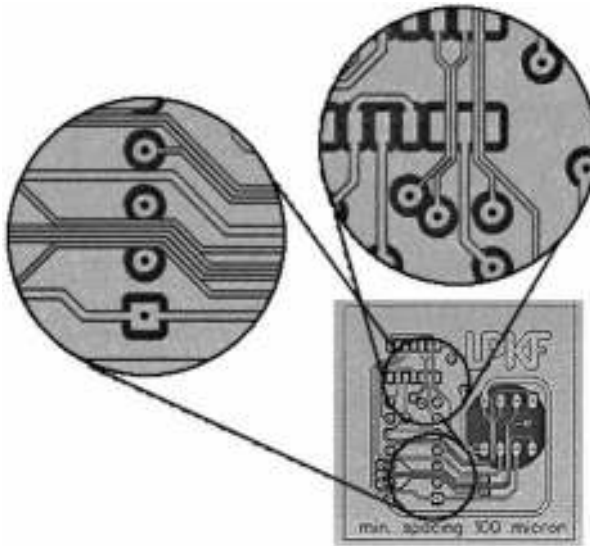
It is possible to emboss a plastic material with a circuit pattern and then metallize the result using one of several processes. The panel can then be ground flat to expose the raised portions of the polymer while the circuit pattern at the lower level remains.

## 7.8 Double-Sided Circuit Process Examples

As in single-sided processing, there are a number of different ways to create double-sided circuits. The following are brief looks at some of the more common processes.

## 7.8.1 Panel plate, tent, and etch

Panel plate, tent, and etch processing can be very reliable and economical, depending on the approach and materials chosen. Ideally, a very thin copper foil



**Figure 7.19** Example of foil routed PCB. (Courtesy of LPKF Laser & Electronics AG.)



should be used to start. This makes etching easier and more accurate. The method also obviates the need for an etch metal resist layer removal before solder mask coating. The process follows the steps outlined in Fig. 7.17 under the heading of “subtractive process.”

### 7.8.2 Panel plate, pattern plate

Panel plate, pattern plate processing is similar to the previous method except that, in place of tenting, a circuit pattern of an etch-resistant metal is plated, and the circuit is etched. This method obviates the concern for holes in the etch resist or breaks in the resist over holes, which can result in all the metal being etched out of the through hole. As in the case above, a very thin copper foil ideally should be used to start to make etching easier and more accurate.

### 7.8.3 Pattern plate

Pattern plating is a very common method used in circuit processing. Most often, it follows the process steps described in Sec. 7.9. When a thin copper foil is used to start, a semiadditive process can be used. This allows the processor to avoid having to plate and later remove an etch resist metal layer. The process steps for pattern plating using the semiadditive method are shown in Fig. 7.17.

### 7.8.4 Printed-through hole

An unusual method for making side-to-side connections on a PCB is to use conductive inks printed through the holes following a double-sided etch process. The ink is normally screened or stenciled on while the plane is placed on a vacuum table, which draws the ink down through the holes. The process is normally repeated from the other side to ensure full coating.

## 7.9 Standard Multilayer Circuit Process Example

There are many ways to produce a multilayer printed circuit, but only a few methods see any major use, and these are the products of many years of experiments and experience. The following are brief discussions of some of the key process steps in the creation of a multilayer printed circuit.

### 7.9.1 Inner layer image requirements

In the construction of a multilayer circuit, it is necessary to carefully control every step of the manufacturing process. Thus, the images that are to be generated for the circuit patterns should adequately address the needs of production. This is manifest in several ways (depending on the complexity of the design) but normally includes, as a minimum, the retention of copper around the circuit to improve dimensional stability and an adjustment of the circuit trace widths to compensate for the effects of the etching process. For contact exposure, a negative image is normally used (clear traces and opaque spaces), as negative-acting resists are most common.

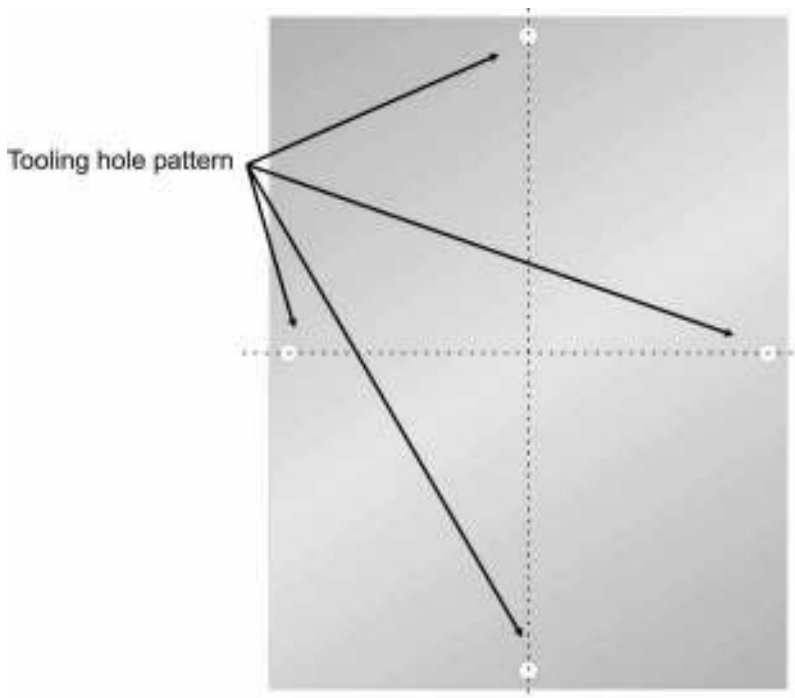
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**7.9.1.1 Inner layer material preparation.** Unless materials are purchased precut, the first step in the manufacture of a multilayer is to cut laminate sheets to the appropriate panel size. Normally, this is a size that is acceptable to all of the following processes. Depending on how the material is cut, the inner layer material (also commonly called *core material*) at this time may have the edges cleaned to minimize the potential for imaging defects caused by fragments or particles of glass or epoxy.

**7.9.1.2 Tooling hole generation.** Tooling holes are a vital part of multilayer manufacture. They are the key element of the registration system, which will be required to successfully produce the multilayer circuits. Highly accurate tooling hole punching systems have been developed that allow all the tooling holes to be punched at one time. Whereas the minimum number of tooling holes, in theory, is two, most tooling systems punch four holes. These holes are most often at the centers of the laminate sides near the edge (see Fig. 9.20). This approach has been developed with the intent of making the center of the panel the 0/0 point minimizing runout in any on direction.

## 7.9.2 Resist coating

The resist coating process is similar to that described earlier, except that, because of accuracy limitations, screen printing is rarely if ever used for such



**Figure 7.20** Illustration of typical tooling hole layout.

purposes. The panels must be clean and free of any foreign materials that might be impervious to or alter the etching rate. Roll coating of dry film resist is very common at present; however, other methods based on electrophoretic deposition of resists are proving popular for very fine-line circuits.

### 7.9.3 Exposure methods

There are several methods that can be used to expose the resist-coated laminate. Contact printing remains popular at present, wherein the coated core material is mated to the film containing the correct circuit pattern on top and bottom, using the tooling pin system, and then exposed to UV light. Although this method is still the most widely used, off-contact and laser-direct-write methods are showing some promise.

### 7.9.4 Development

Development methods are identical to those described earlier; however, because the laminates are very thin, special care in handling is required.

### 7.9.5 Etching

The etching process is a critical step in the processing of a printed circuit inner layer. This is especially true in the case of circuits being designed for controlled-impedance applications. The processes used are the same as those described earlier in this chapter.

### 7.9.6 Resist stripping

The resist stripping process step follows the etching step. The process is very simple, with the only major concern being that the stripping be complete and that the panels be adequately rinsed.

### 7.9.7 Copper circuit surface preparation

The surfaces of the copper circuits on the laminate are normally provided with an oxide treatment to improve the adhesion of the resin to the circuits. A number of different oxide treatments are available. Black oxide (cupric) was very common in the past, but newer methods have been developed that leave the exposed copper with a brown oxide (cuprous) finish that has some improved characteristics. The use of a so-called “double-treatment” copper foil can obviate the need for such a process and is favored by some manufacturers.

### 7.9.8 Lay-up for lamination

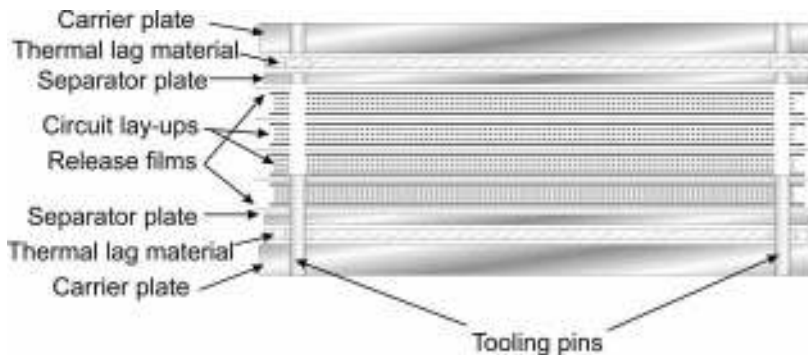
Circuit lay-up for lamination is accomplished by laying down circuit layers in an ordered fashion on a carrier plate of steel, which shares the same tooling hole layout as the punch. Plies of prepreg are placed between each of the inner layer cores until the stack is complete. The type of prepreg, in terms of cloth

type and resin formulation, is prescribed by the circuit design needs. Normally, two plies or sheets of the chosen prepreg are used between each of the layer pairs. A number of multilayer circuit panels can be laminated at one time. To facilitate handling of copper foil when cap foil lamination is desired, it is possible to purchase the thin copper foil preattached to a thicker metal carrier. This method obviates the need for separator plates between multilayer circuits in the stack. Figure 7.21 provides an example of a possible circuit lay-up.

### 7.9.9 Lamination methods

A number of different approaches to multilayer lamination have been developed over the years. Traditional lamination methods are still suitable for many products, but advanced high-density circuits often can be better served by other methods. One important method is to augment the process by the application of a vacuum during lamination. This approach helps to expel air from the laminate and prevents its entrapment during lamination. Entrapped air can cause problems in processing and weaken the laminate. To assist in air removal, methods have been developed wherein lamination takes place in a vacuum. Other nonstandard methods have also been developed such as vacuum autoclave lamination. In this process, the circuits are laminated by placing them in a high-temperature bagging material, drawing a vacuum on the bag to expel the air, and then placing the bagged circuits into a pressure vessel. Pressure is applied by adding CO<sub>2</sub> gas and heating the gas to lamination temperature by means of a convection oven inside the pressure vessel. This method is very popular with flex circuit manufacturers.

Beyond the lamination processes described earlier, there is one other that is quite unusual. In lay-up, a double sheet of copper foil is rolled back and forth between the individual circuit panels, forming a continuous dual-foil sheet. This assembly is then placed in a vacuum lamination chamber, and pressure is applied. Heat is generated by passing high-electric DC current through the



**Figure 7.21** Example of a possible lay-up for multilayer lamination. Variations are possible in terms of materials and stack-up heights, depending on the needs and preferences of both the product and the manufacturer.

copper foil, which causes it to heat up to temperatures at which the prepreg resin can flow, fill, and encapsulate circuit features and cure.

Following lamination, the panels are normally trimmed to remove resin flash at the edges of the panel. Again, it is advisable that the edges be dressed so that they do not cause problems in later steps such as imaging of the outer layers.

### 7.9.10 Drilling

Accurate drilling of a multilayer circuit is integrally linked to the tooling system. The tooling holes serve as a collective datum for the drilling machine. As such, the tooling holes must accurately link to the circuit patterns that were imaged, etched, and laminated to become internal elements of the PCB and invisible to the unaided eye.

The process of drilling must be very well controlled to ensure its quality. It is common to reduce the drill stack height for multilayer circuits to ensure drilled hole quality. This is especially true when very small holes are being drilled or when design features are especially small.

### 7.9.11 Hole cleaning and etchback

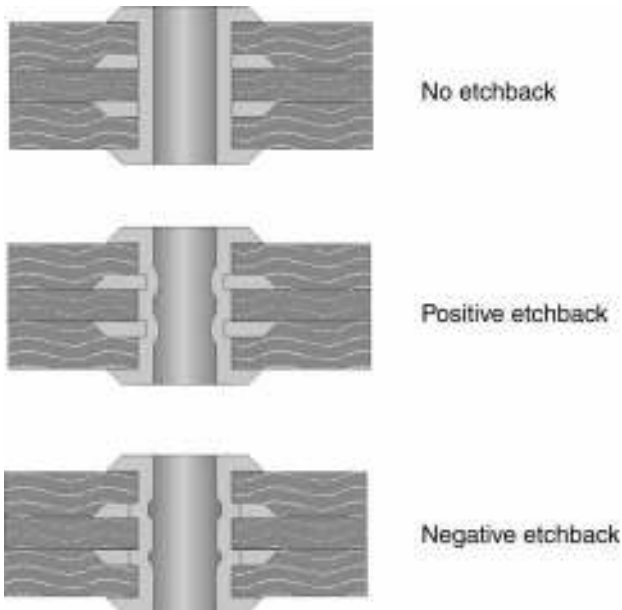
Following drilling, it is fairly common to perform some sort of cleaning process to remove any resin that might have smeared over the surface of the copper inner layers. Failure to remove such resin smear could degrade the reliability of the plated-through hole interconnection to the inner layer, or it could completely block the interconnection, depending on the severity of the smearing. Some customers request etchback of the resin from the inner layer lands. Doing so creates a so-called “three-point interconnection.” This is commonly referred to as *positive etchback* and is normally deemed to be a more reliable interconnection. In contrast, some board users suggest that negative etchback has advantages. Here, the copper is etched back slightly and provides easily verifiable evidence of resin removal, because it would otherwise interfere with the copper microetching process used as a part of the hole-plating process. Figure 7.22 illustrates the difference between the two methods.

### 7.9.12 Subsequent processes for multilayer PCB manufacture

The process steps following hole cleaning are essentially the same as those used for double-sided processing and can be used for reference as benchmark processes.

## 7.10 Mass Lamination

*Mass lamination* describes a technology wherein the laminate manufacturer fabricates multilayer panels in full sheet form, normally as a service to printed circuit manufacturers who either do not have lamination technology in house or whose lamination manufacturing capacity is limited.

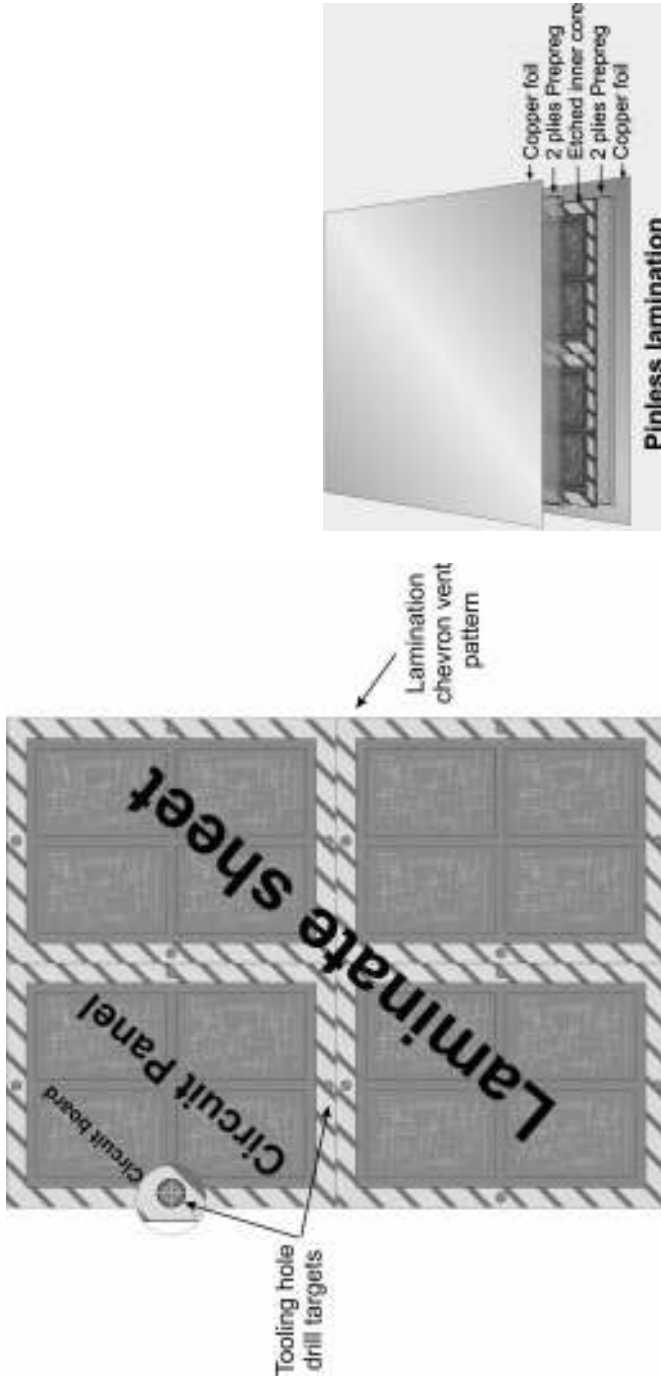


**Figure 7.22** Etchback can be either positive or negative, as illustrated above.

The method is generally limited to use with relatively simple multilayers and is most often used for four-layer multilayer circuits. However, higher layer counts have been achieved using modified approaches. Mass lamination differs from traditional lamination in that it is pinless. The inner layer cores are produced by accurately registering the top and bottom films of the inner core material (normally ground and power layers, which are not very complex) to the resist-coated panels and then exposing, developing, and etching them in the same fashion as is used for normal multilayer cores. Targets are etched into the copper foil in the locations where the tooling holes normally would have been punched and after lamination. The targets are accessed either by carefully milling through the copper and laminate above to expose them for accurate drilling or by means of an X-ray-assisted drill or punch. Once the tooling holes are drilled, the panels can be accurately registered with subsequent drilling of normal plated-through holes. The general process steps are illustrated in Fig. 7.23.

### 7.11 Metal-Core Printed Circuit Boards

Metal-core PCBs are a special subset of printed circuits. The name is adequately self-descriptive, and the purpose of these structures is normally to facilitate the rapid and efficient removal of heat from the board. These constructions are most desirable for use with products that will be generating large amounts of heat or that operate in conditions (e.g., aerospace) where convection cooling is of limited potential or value. There are a number of potential



**Figure 7.23** Mass lamination methods are used to laminate full sheets of circuit panels. After lamination, the sheet is cut into panels, and the tooling holes are drilled using the etched targets to ensure proper placement.

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constructions of these boards; however, if one is to keep true to the definition provided, there are only two general forms of metal core PCBs, double sided and multilayer. The following are descriptions of basic metal core structures.

**7.11.1 Double-sided metal-core**

Double-sided metal-core boards are the simplest form of the product. The fundamental structure consists of a piece of metal with holes, over which lies a coat of insulation topped with metal circuit patterns. The insulation material can vary. Porcelain, baked, enamel, and various organic coatings can be used. The choice is a function of the application and the amount of heat being generated and dissipated. Figure 7.18 provides an example of a simple structure.

**7.11.2 Multilayer metal core structures**

Multilayer metal core structures are also found in a variety of formats. The most common again follows the precepts of the basic definition of metal core, which consists of a multilayer circuit fabricated on either side of a central metal core. However, certain other constructions are included under the umbrella of metal core. These would include constructions where copper clad Invar is used to control the in-plane expansion of the board and where they might also serve as power and ground planes. An example of a basic metal-core board is illustrated in Fig. 7.18.

**7.12 Flexible Circuits**

Flexible circuits are a unique and very important form of printed circuit. The IPC standards document IPC-T-50, Terms and Definitions for Printed Boards, defines it as follows:

A patterned arrangement of printed wiring utilizing flexible base material with or without flexible coverlayers.

This is an accurate but somewhat limited definition, as it fails to consider fully how the technology can be applied. For example, flexible circuits can be used statically, in a “flex-to-fit” fashion, or they can be dynamically flexed either intermittently, such as when used in hinge applications, or nearly continuously when used in disk drive applications. Flexible circuits are most fundamentally a three-dimensional interconnection technology. Special design practices are required to create reliable flexible circuits, and potential users are advised to familiarize themselves with flex circuit design information before embarking on a flex circuit design to avoid potential problems. There are several different types of flexible circuits. These are described in the following sections.

**7.12.1 Single-sided**

Single-sided flex circuits are the most commonly produced members of the family. They are the lowest-cost variant and the type best suited to dynamic flexing applications. They can be produced using either etched metal or



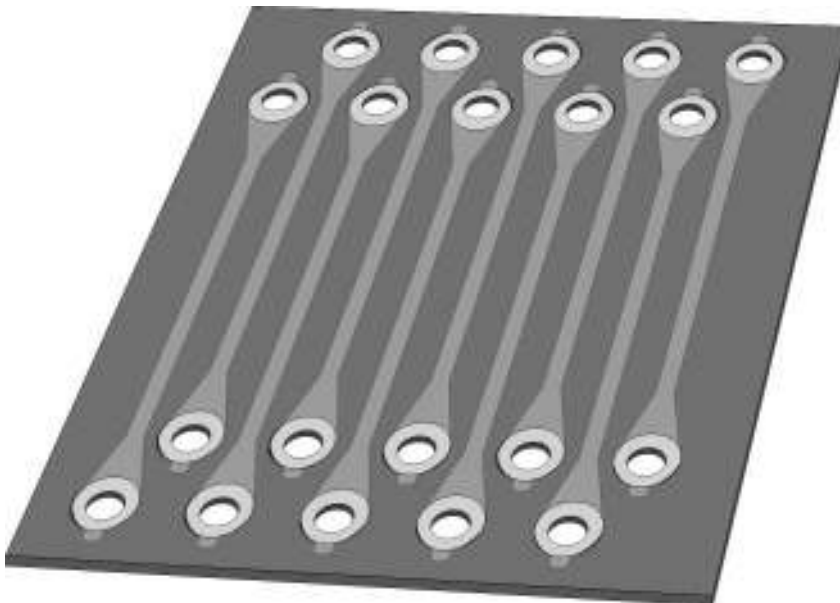
printed conductive inks to create the circuit patterns. The metal can be accessed from one or both sides if desired. In the latter case, the polymer base film is removed by a suitable means, such as a laser. A special-case variation involves selective etching of the copper to create a circuit that has copper of different thickness along the length of the circuit patterns—thin in areas to be flexed, and thicker in areas where interconnection is desired. A cover layer is commonly applied to protect the circuits and to improve their longevity in dynamic flexing applications. See Fig. 7.24 for an example.

### 7.12.2 Double-sided

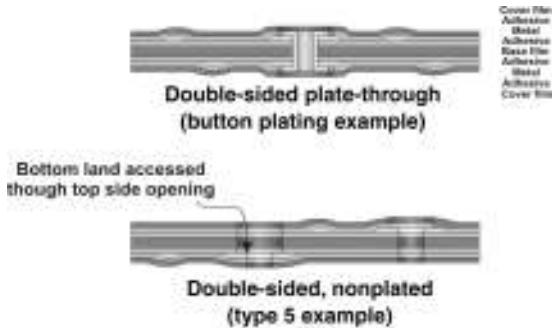
Double-sided flex circuits are the second most common form and are used where higher-density interconnection is required. These flex circuits obviously have two metal layers, and they are normally interconnected by means of a plated-through hole, although this is not always necessary. For example, the so-called “type 5” flex circuit is a nonplated-through hole flex wherein both metal layers are accessed from the same side. See Fig. 7.25 for examples.

### 7.12.3 Multilayer

Multilayer flex circuits are used in applications requiring higher-density interconnections. They are similar to their rigid counterparts but are often more complex and very engineering intensive. Very fanciful looking but highly practical multilayer flex circuits have been fabricated to solve complex electrical and electronic interconnection problems. It is possible to build multilayer flex



**Figure 7.24** Example of the construction of a simple single-metal-layer flex circuit.

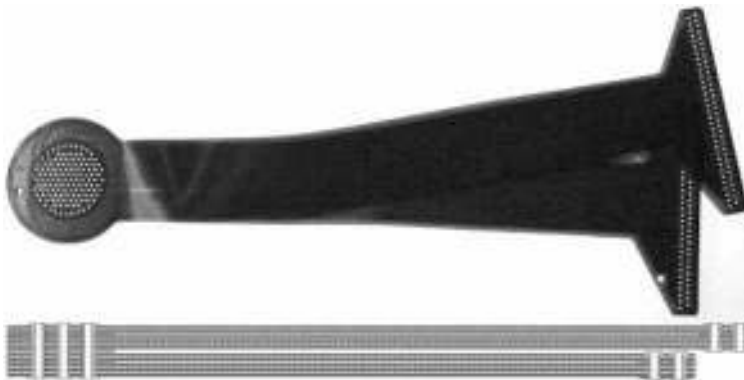


**Figure 7.25** Two-metal-layer flex circuits can be fabricated in one of the two basic ways shown above.

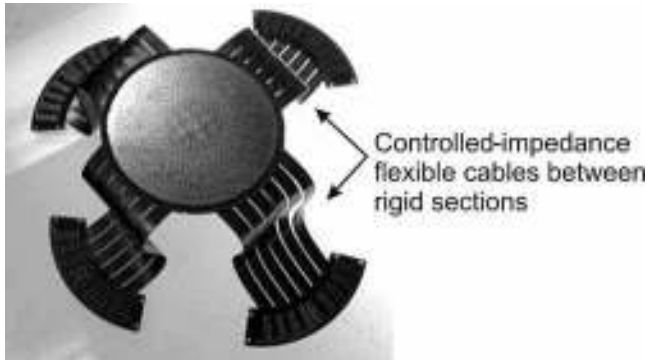
circuits with tentacles having varying numbers of layers broken out from a central section. See Fig. 7.26 for example.

#### 7.12.4 Rigid-flex

Rigid-flex circuits are the final variation of flex circuits. As the name suggests, they are a hybrid construction that brings together construction elements of both rigid and flexible circuits. Most often, the rigid portions of the rigid-flex circuit are used to support connectors and or components, and the flexible portions are used to interconnect the rigid sections. The technique won the favor of military product designers in the 1970s as a means of creating higher-reliability and lighter-weight interconnection structures than the wire harness alternatives that they often replaced. Like multilayer flex circuits, these circuits are frequently highly engineered and require a great deal of understanding of manufacturing process for them to be designed properly. Figure 7.27 provide an examples of a rigid-flex construction.



**Figure 7.26** A deceptively simple looking multilayer flex circuit with a complex construction as can be seen in cross section. Single and doubled sided flex circuits are pre fabricated, joined and plated through and the those structures are joined and plated through again to create the finished circuit.



**Figure 7.27** An example of a rigid-flex circuit with integral controlled impedance sections between rigid elements of the circuit.

### 7.13 High-Density Interconnection (HDI) Structures

Semiconductor manufacturing technology is the driving force behind the electronics industry. Semiconductor integrated circuit features continue to be reduced in size to meet the demand for more function in lesser amounts of space. This in turn has resulted in the creation of devices that operate at higher speeds and with greater efficiency with each new generation of product. However, as more recent generations of IC devices pressed the limits of older traditional IC packaging technologies, new technologies had to be developed. The early 1990s saw a number of different attempts to create substrates to meet this challenge and provide solutions. These products were generally referred to as *multichip modules* or *MCMs*. The substrates used for these structures were really the first of the HDI substrates, and they drew heavily from the technologies used to create ICs. They were, however, very expensive, and the final products were vexed by their inability to obtain reliable sources of known good die (KGD), without which their yields were low enough to be viewed as impractical.

About the same time, there was a surge of interest in a new IC packaging methods based on the used of printed circuit technology. The new approach, based on area array interconnections, was a response to the rising pin counts and the inability of industry to obtain good yields with the more traditional peripherally leaded packages. These devices are known now as *ball grid arrays* (BGAs). While the early structures were rather simple (beyond the need for relatively small holes) and presented little challenge to PCB manufacturers, as chip I/O counts increased, there was a need for additional layers of circuitry. The additional circuit layers were required to help redistribute the circuitry to a pitch more suitable to the needs of next-level PCB design, manufacture, and assembly. HDI concepts explored for MCMs were reexamined for use with these new packages but using advanced PCB technologies in place of the semiconductor technologies that were dominant in the earlier effort. This became a proving ground of sorts for a number of HDI manufacturing concepts.

### 7.13.1 HDI substrate construction types

Presently, a significant number of different processes have been proposed and/or developed for manufacturing high-density interconnection substrates. The IPC has attempted to bring some order to the matter by identifying and classifying, into general types, the various HDI PCBs that have been described in the literature. Thus far, six general types of HDI structures have been identified. These are described in the following sections.

**7.13.1.1 Type 1 construction.** The Type 1 HDI structure is typified by a circuit having a rigid core that could have multiple circuit layers on which microvia buildup layers and through holes can be plated simultaneously. Normally, the microvia layers can be plated up on either or both sides of the circuit core (see Fig. 7.28).

**7.13.1.2 Type 2 construction.** The Type 2 HDI structure is typified as a circuit having a rigid core that could have multiple circuit layers and that has holes plated through with copper. These holes are filled with resin before further processing and thus become blind vias (or possibly semiblind vias) on completion of the fabrication process. Completion is effected by plating microvia buildup layers on either or both sides of the circuit core (see Fig. 7.29).

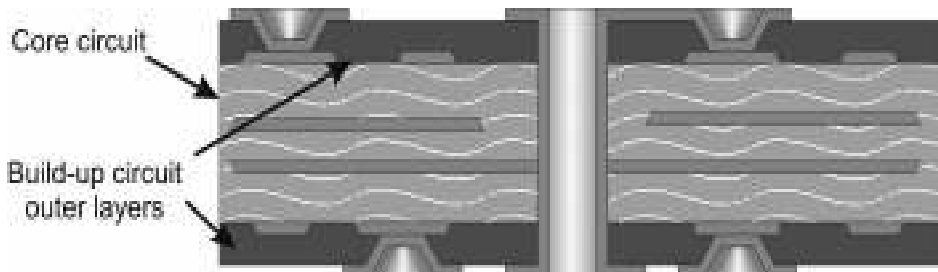


Figure 7.28 HDI construction Type 1, described in text.

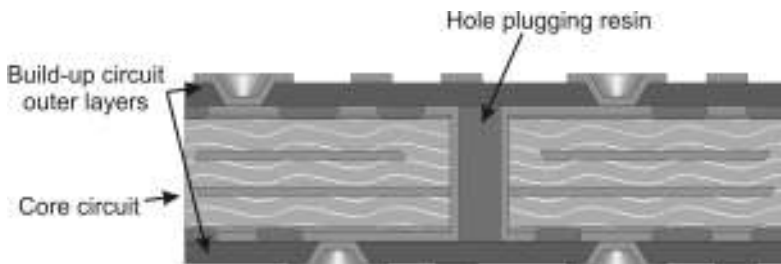
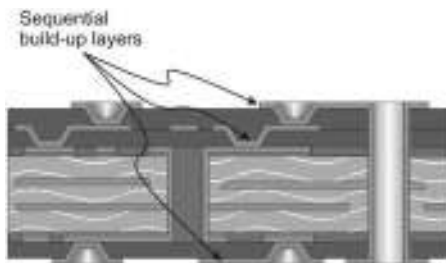


Figure 7.29 HDI construction Type 2, described in text.

**7.13.1.3 Type 3 construction.** The Type 3 HDI structure is typified by a circuit having a rigid core with buried vias (as in Type 2) and one or more microvia buildup layers on one side and two or more on the second side. These structures also have plated-through vias, which make direct connection from side to side (see Fig. 7.30). (Note: unbalanced structures are not recommended.)

**7.13.1.4 Type 4 construction.** The Type 4 HDI structure is typified by a circuit having rigid insulating or metal-core substrate with two or more buildup layers on each side. It also has plated-through vias connecting the two sides of the PCB (see Fig. 7.31).

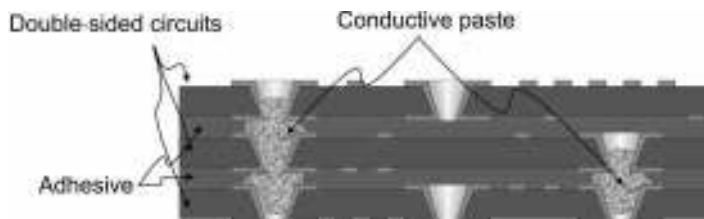
**7.13.1.5 Type 5 construction.** The Type 5 HDI structure is typified by co-laminated circuit structures with circuit layers interconnected during lamination to achieve vertical interconnection using conductive pastes or alloys. There are several variations on this basic theme (see Fig. 7.32).



**Figure 7.30** HDI construction Type 3, described in text.



**Figure 7.31** HDI construction Type 4, described in text.

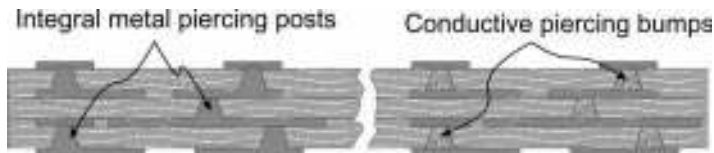


**Figure 7.32** HDI construction Type 5, described in text.

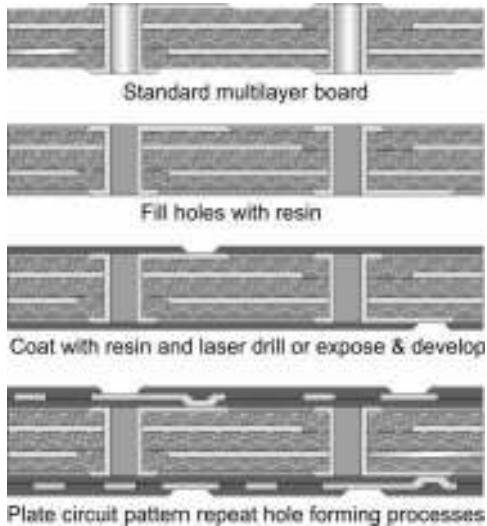
**7.13.1.6 Type 6 construction.** The Type 6 HDI structure is typified by circuits fabricated using insulation-piercing features of integral metal or stenciled conductive polymer, which make interconnection during a lamination process (see Fig. 7.33).

### 7.13.2 Build-up board example

The concept of the organic laminate build-up board was likely inspired by the technology used to fabricate hybrid circuits. Hybrid circuits are routinely fabricated by sequentially layering circuits and insulating materials to create the final product. However, hybrids generally employ inorganic materials in their construction and use a different set of manufacturing processes and equipment. The major attraction was hybrid circuit technology's small via structures that offered better routing space potential and improved electrical/electronic performance. As was illustrated in the foregoing discussion of HDI types, there are numerous variations on the basic HDI concept. Most of those are build-up type structures. The flow diagram in Fig. 7.34 provides a general illustration of the basic build-up board process.



**Figure 7.33** HDI construction Type 6, described in text.



**Figure 7.34** Simplified example of the basic process steps in the manufacture of a build-up board.

### 7.13.3 Co-laminated structure example

Co-laminated HDI circuits also are likely to have taken inspiration from hybrid circuit manufacture for many of the same reasons; however, there are some significant differences as well. Co-laminated HDI substrates offer a two important advantages: (1) they do not require the plating of high aspect ratio holes, and (2) the layers can be individually tested and yielded before lamination. IBM, Tessera, and CTS Corporation have all described such methods. An example of one such process is provided in Fig. 7.35.

### 7.13.4 Sequential laminated structure example

This approach to manufacture has been employed by at least two major Japanese companies, Matsushita and Toshiba. There are significant differences between the two approaches, but the final products are comparable. Toshiba uses an insulation-piercing conductive bump to make connection between layers of copper foil at predetermined points during lamination. In contrast, Matsushita prepunches or predrills the insulation layer and fills the holes with conductive paste before laminating on the copper foils. Packard-Hughes of Irvine, California, has described in a patent a concept similar to that used by Toshiba, but they use integrally plated copper bumps to pierce the insulating layer during lamination. Flow diagrams for these processes can be seen in Fig. 7.36.

## 7.14 Inspection, Evaluation, and Test of Printed Circuits

Regardless of the type of printed circuit that is designed, manufactured, and used, it is inevitable that, at the end of the manufacturing process, some man-

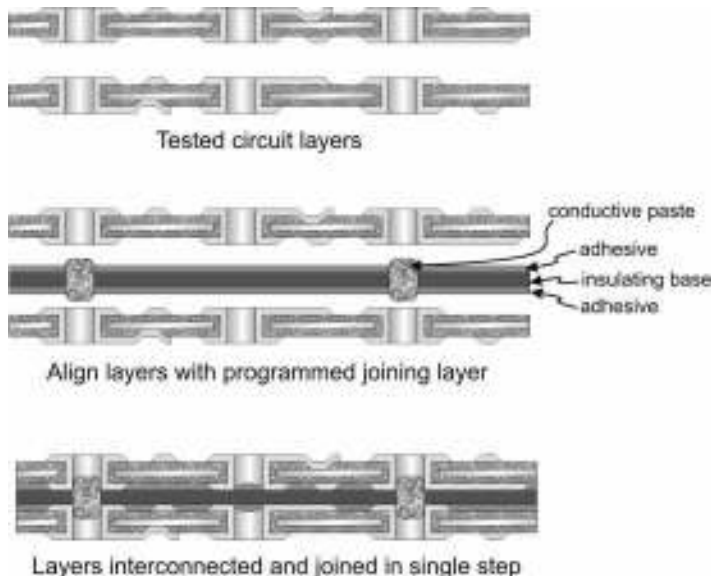


Figure 7.35 Simplified example of a co-laminated HDI structure.

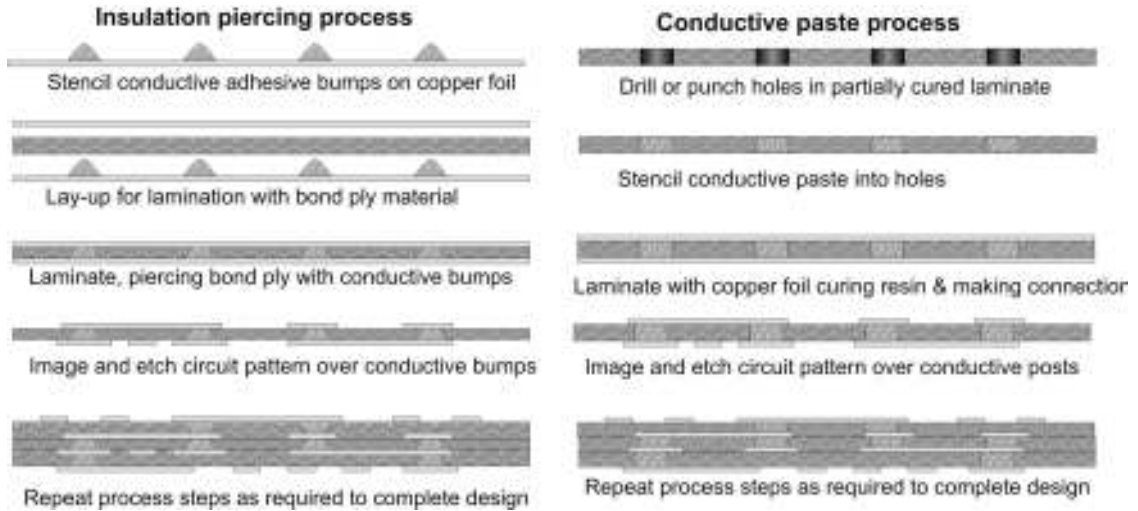


Figure 7.36 Several different methods exist for manufacturing sequentially co-laminated structures.

ner of inspection and test of the printed circuits will be performed. These processes are arguably the most important steps in the process. The reasons are quite simple, and one quick example will help to illustrate. The fact is that, although a printed circuit may be an expensive component in and of itself, the cost of the components that are to be mounted on the PCB are often much higher in total. This simple fact raises the importance of ensuring the integrity of the assembly function and quality to a high level. Thus, what to look for and what to test are important questions to be addressed.

#### 7.14.1 Inspection points for printed circuits

In evaluating the quality and functionality of PCBs, we duplicate many of the tests that were performed on the raw material by the laminate manufacturer to qualify their product. The logic of this redundant testing is that it provides a measure of assurance that the manufacturing processes used in creating the PCB have not in some way degraded the material beyond acceptable limits. As with the raw materials, testing requirements have been established in several key areas to ascertain that the product is acceptable for its intended purpose. Major categories for testing and evaluating PCBs include the following

- Visual criteria such as plating quality, solder mask coverage, and workmanship
- Dimensional measurements of the body of the circuit and its design features (e.g., circuit lines and minimum spacing and hole diameters)
- Construction integrity, including such matters as an examination of plated-through hole quality
- Electrical properties such as dielectric withstand voltage and characteristic impedance measurements, if specified.



- Cleanliness (usually measured in equivalent micrograms of NaCl per square centimeter), a measure that is generally indicative of the potential for latent failures caused by ionic conductive filament growth in moist environments
- Solderability, a measure of the wetting ability of the finish of the circuit
- Environmental properties

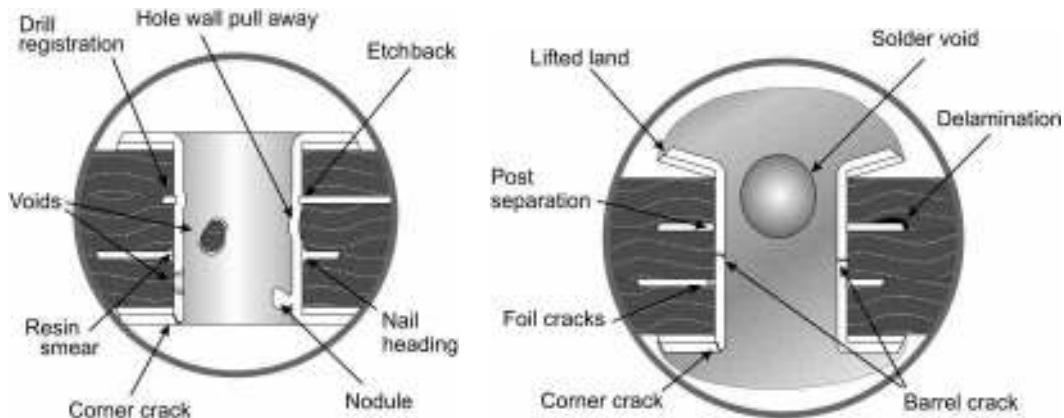
Testing requirements for each of the above-mentioned categories are reviewed here in a brief fashion. IPC specifications IPC-6011 and IPC-6012, which are qualification and performance specification for rigid printed boards (superseding the older IPC-RB-276 document), IPC-6013, “Specification for Single- and Double-Sided Flexible Printed Wiring” (superseding the IPC-FC-250A document), and IPC-A-600 are valuable documents that provide precise methods. These are available and are recommended if more detail is sought. Figure 7.37 provides examples of some of the types of defects that might be encountered.

#### 7.14.2 Cross-section evaluation

Inspection of a cross section of a finished plated-through hole on the PCB is normally desired to ensure that the applied metal platings are all within prescribed ranges. It is also possible to get a sense of the quality of the processing using this method. Figure 7.37 gives examples of the types of defects than might be encountered in examining a plated-through hole as received and post solder stress testing.

#### 7.14.3 Electrical testing

Electrical testing is thus recommended for highly complex boards and for boards that are designed to accept and interconnect large numbers of compo-



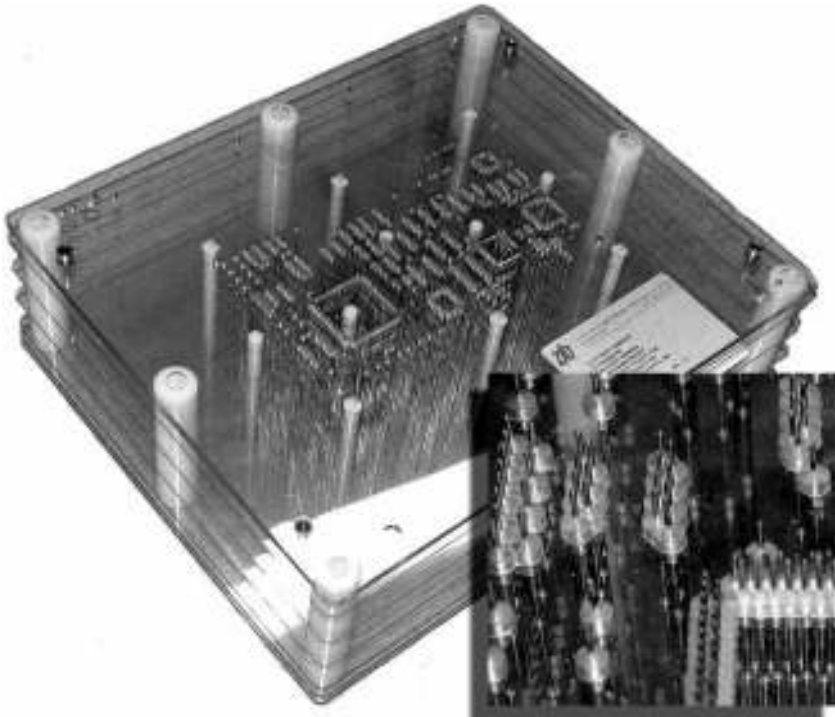
**Figure 7.37** Examples of potential copper plating defects that might be encountered in the examination of plated-through hole cross sections. On the left is a hole before solder stress testing, and on the right is an example of a through hole after solder stress testing. Not all defects are cause for rejection; some are simply cause for concern as indicators of possible process control problems.

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nents. Test fixtures (or test programs, in the case of flying-probe-type testers) are not free, but the savings they might be afforded by preventing bad boards from entering the component population assembly operation can be significant. The data for test can be relatively easily extracted from CAD data. Figure 7.38 shows an example of a test fixture.

## 7.15 Future Directions

The future of printed circuit manufacture is indefinite, except for the fact that one can state with reasonable confidence that there will always be a need for electronic interconnection substrates of some sort. New schemes for manufacturing printed circuits presently in development could radically alter the traditional approaches to manufacture. For example, one company in England (TDAO, Ltd.) is known to be working on a technology that would allow for the direct imaging and plating of flexible circuits in a continuous fashion. This concept would bring the industry closer to realizing the dream of making circuits directly from a computer without the need for film or resist. Another example is a concept for creating metal-core laminates with predrilled and metallized holes that can serve as the raw materials for structures such as represented by the circuits shown in Fig. 7.36.



**Figure 7.38** Example of a dedicated bed-of-nails test fixture. The insert shows a close-up view. (Photo courtesy of Zero Defects, Santa Clara, California.)

While no one can predict the future with absolute certainty, one thing that seems relatively certain in printed circuit manufacture is that the circuit traces and spaces, and the holes that connect them, will continue to get smaller with time. Of these two trends, the one that is likely to be most important is making smaller holes. Small holes are the key to improving circuit routing.

## 7.16 Summary

Printed circuits have had a long and colorful history, and they remain among the most important elements of electronic manufacture. There are numerous types of printed circuits and numerous approaches to their manufacture. With the ever expanding electronics market and the myriad of products that are being manufactured, there will likely be continuing increase in the number of different types of electronic interconnection substrates and printed circuits in the years to come.

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# Materials and Processes for Hybrid Microelectronics and Multichip Modules

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## 8.1 Introduction

Hybrid microelectronics technology is a distinct branch of electronics packaging technology and is primarily differentiated from other branches by the manner in which the interconnection patterns are generated. The foundation for the hybrid circuit is a substrate fabricated from one of the refractory ceramics. A metallization pattern is created on the substrate by one of the film technologies, forming the mounting pads and circuit traces to which we bond and interconnect additional active and passive devices as necessary. Another characteristic of hybrid technology is the ability to fabricate passive components. The thick and thin film technologies, for example, can be used to manufacture resistors with parameters superior to those of carbon resistors that are commonly used in conjunction with printed circuit boards.

The most commonly accepted definition of a hybrid circuit is a ceramic substrate metallized by one of the methods shown in Fig. 8.1, containing at least two components, one of which must be active. This definition is intended to exclude single-chip packages and circuits that contain only passive components such as resistor networks. By this definition, a hybrid circuit may range from a simple diode-resistor logic gate to a circuit containing in excess of 100 integrated circuits (ICs).

Multichip modules (MCMs) are close relatives of hybrid circuits. Although many of the assembly processes are common to those used to fabricate hybrid circuits, MCMs, as shown in Fig. 8.2, employ a wider range of substrate materials and metallization processes that provide a much higher packaging density.

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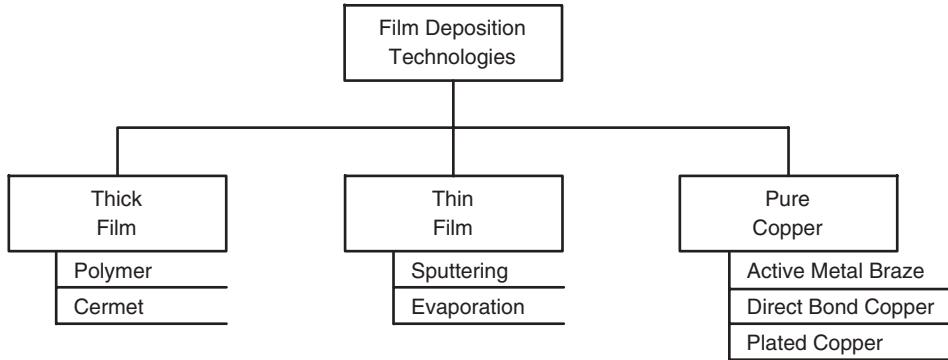


Figure 8.1 Film deposition technologies.

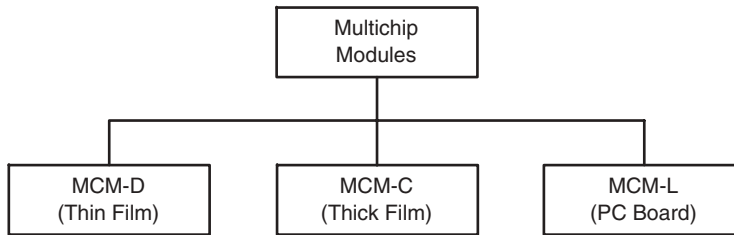


Figure 8.2 Multichip module technologies.

This chapter describes the methods and properties of the various materials, metallization processes, and assembly methods used to manufacture hybrid circuits and MCMs. Also included are design guidelines, a discussion of reliability considerations, and applications of hybrid circuits.

## 8.2 Ceramic Substrates for Hybrid Circuits

The substrate is the foundation of an electronic circuit and must perform many functions. It acts as the platform upon which to mount components and must be compatible with the processes intended to metallize the substrate and to attach the components to the metallized traces. The substrate may also be an integral part of the overall circuit package.

The desirable properties of a substrate for electronic applications include

- *High electrical resistivity.* A substrate must have high electrical resistivity to isolate adjacent circuitry.
- *High thermal conductivity.* High thermal conductivity assists in transporting the heat generated by electronic components during normal operation away from the components.
- *Resistance to temperature.* Many of the processes used to metallize substrates and assemble the components take place at elevated temperatures.

- *Inert to chemical corrosion.* Solvents, fluxes, and the like are harsh and must not attack the chemical structure of the substrate.
- *Cost.* The cost of the substrate material must be compatible with the cost of the end product.

The properties of ceramic substrates are advantageous for many microelectronic systems, ranging from simple, inexpensive circuits used in throwaway toys to elaborate multilayer structures used in space or medical applications. Only by understanding the properties of ceramic substrates can they be optimally utilized in this wide variety of applications.

Ceramics are crystalline in nature, with very few free electrons. They have high electrical resistivity, are chemically and thermally very stable, and have a high melting point. They are formed by the bonding of a metal and a non-metal and may exist as oxides, nitrides, carbides, or silicides. An exception is diamond, which consists of pure carbon subjected to high temperature and pressure. Diamond substrates meet the criteria for ceramics and may be considered as such in this context.

The primary bonding mechanism in ceramics is ionic bonding. An ionic bond is formed by the electrostatic attraction between positive and negative ions. Atoms are most stable when they have eight electrons in the outer shell. Metals have a surplus of electrons in the outer shell, which are loosely bound to the nucleus and readily become free, creating positive ions. Similarly, nonmetals have a deficit of electrons in the outer shell and readily accept free electrons, creating negative ions. Figure 8.3 illustrates an ionic bond between a magnesium ion with a charge of +2 and an oxygen ion with a charge of -2, forming magnesium oxide (MgO). Ionically bonded materials are crystalline in nature and have both a high electrical resistance and a high relative dielectric

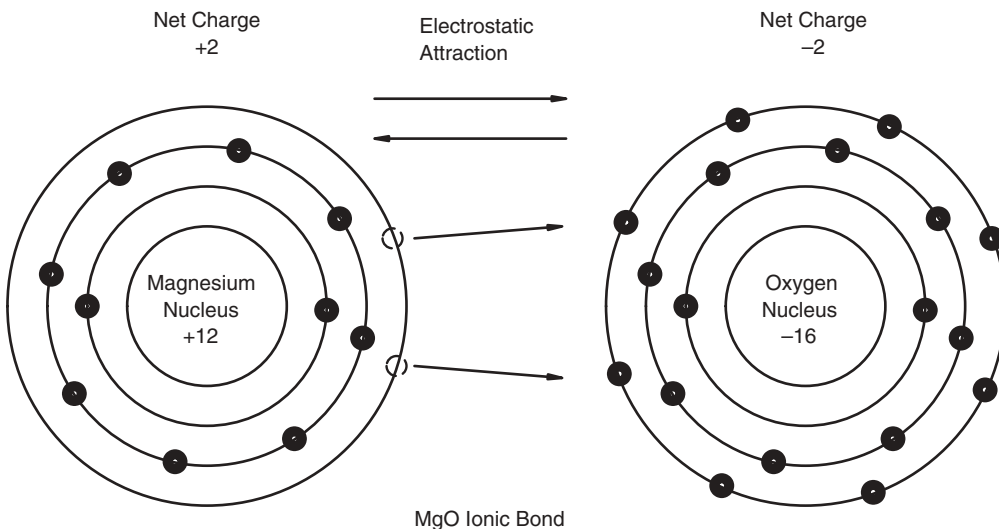


Figure 8.3 Magnesium oxide ionic bond.

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constant. As a result of the strong nature of the bond, they have a high melting point and do not readily break down at elevated temperatures. For the same reason, they are very stable chemically and are not attacked by ordinary solvents and most acids.

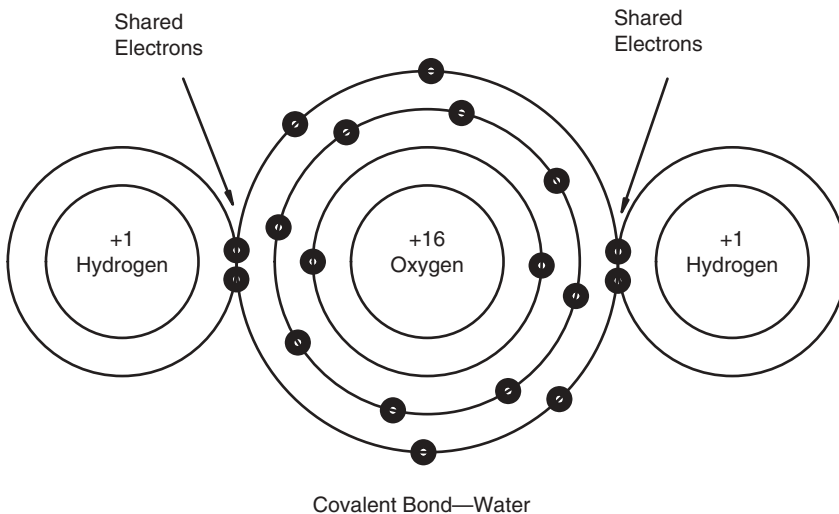
A degree of covalent bonding may also be present, particularly in some of the silicon and carbon-based ceramics. The sharing of electrons in the outer shell forms a covalent bond. A covalent bond is depicted in Fig. 8.4, illustrating the bond between oxygen and hydrogen to form water. A covalent bond is also a very strong bond, and may be present in liquids, solids, and gases.

A composite is a mixture of two or more materials that retain their original properties but, in concert, offer parameters that are superior to either. Composites in various forms have been used for centuries. Ancient peoples, for example, used straw and rocks to increase the strength of bricks. Modern day structures use steel rods to reinforce concrete. The resulting composite structure combines the strength of steel with the lower cost and weight of concrete.

Ceramics are commonly used in conjunction with metals to form composites for electronic applications, especially thermal management. Ceramic-metal (cermet) composites typically have a lower TCE and a higher thermal conductivity than ceramics, and they are more ductile and more resistant to stress. These properties combine to make cermet composites ideal for use in high-power applications in which thermal management is critical.

## 8.3 Surface Properties of Ceramics

The surface properties of interest, surface roughness and camber, are highly dependent on the particle size and method of processing. Surface roughness is a measure of the surface microstructure, and camber is a measure of the devi-



**Figure 8.4** Covalent bond between oxygen and hydrogen to form water.



ation from flatness. In general, the smaller the particle size, the smoother the surface.

Surface roughness may be measured by electrical or optical means. Electrically, surface roughness is measured by moving a fine-tipped stylus across the surface. The stylus may be attached to a piezoelectric crystal or to a small magnet that moves inside a coil, inducing a voltage that is proportional to the magnitude of the substrate variations. The stylus must have a resolution of 25.4 nm (1  $\mu$ in) to read accurately in the most common ranges. Optically, a coherent light beam from a laser diode or other source is directed onto the surface. The deviations in the substrate surface create interference patterns that are used to calculate the roughness. Optical profilometers have a higher resolution than the electrical versions and are used primarily for very smooth surfaces. For ordinary use, the electrical profilometer is adequate and is widely used to characterize substrates in both manufacturing and laboratory environments.

Camber and waviness are similar in form in that they are variations in flatness over the substrate surface. Referring to Fig. 8.5, camber can be considered to be an overall warpage of the substrate, whereas waviness is more periodic in nature. Both of these factors may occur as a result of uneven shrinkage during the organic removal/sintering process or as a result of non-uniform composition. Waviness may also occur because of a “flat spot” in the rollers used to form the green sheets.

Camber is measured in units of length/length, interpreted as the deviation from flatness per unit length, and is measured with reference to the longest dimension by placing the substrate through parallel plates set a specific distance apart. Thus, a rectangular substrate would be measured along the diagonal. A typical value of camber is 0.003 in/in (or 0.003 mm/mm), which for a 2-

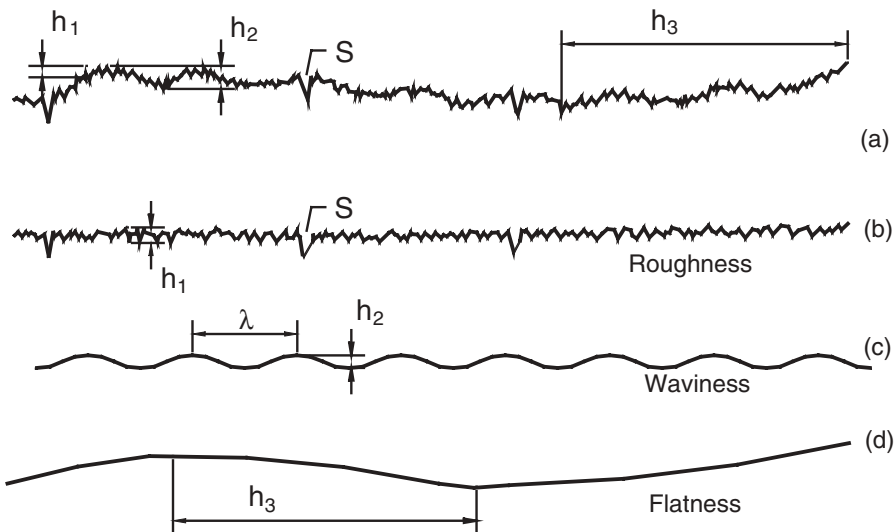


Figure 8.5 Surface characteristics.

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$\times 2$ -in substrate, represents a total deviation of  $0.003 \times 2 \times 1.414 = 0.0085$  in. For a substrate that is 0.025 in thick, a common value, the total deviation represents one-third of the overall thickness!

## 8.4 Thermal Properties of Ceramic Materials

### 8.4.1 Thermal conductivity

The thermal conductivity of a material is a measure of the ability to carry heat and is defined as

$$q = -k \frac{dT}{dx} \quad (8.1)$$

where  $k$  = thermal conductivity in  $\text{W/m}\cdot^\circ\text{C}$

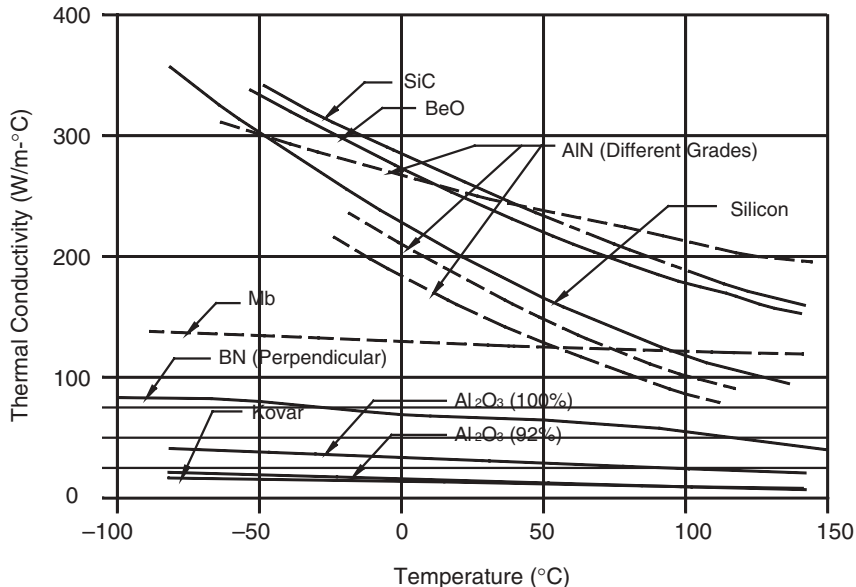
$q$  = heat flux in  $\text{w/m}^2$

$\frac{dT}{dx}$  = temperature gradient in  $^\circ\text{C/m}$  in steady state

The negative sign denotes that heat flows from areas of higher temperature to areas of lower temperature. A plot of thermal conductivity vs. temperature for selected materials is shown in Fig. 8.6.

### 8.4.2 Specific heat

The specific heat of a material is defined as



**Figure 8.6** Thermal conductivity vs. temperature for selected materials.

$$c = \frac{dQ}{dT} \quad (8.2)$$

where  $c$  = specific heat in W-sec/g-°C  
 $Q$  = energy in watt-sec  
 $T$  = temperature in kelvins (K)

The specific heat,  $c$ , is defined in a similar manner and is the amount of heat required to raise the temperature of one gram of material by one degree, with units of watt-sec/g-°C. The quantity “specific heat” in this context refers to the quantity,  $c_V$ , which is the specific heat measured with the volume constant, as opposed to  $c_P$ , which is measured with the pressure constant. At the temperatures of interest, these numbers are nearly the same for most solid materials. The specific heat is primarily the result of an increase in the vibrational energy of the atoms when heated, and the specific heat of most materials increases with temperature up to a temperature, called the Debye temperature, at which point it becomes essentially independent of temperature. The specific heat of several common ceramic materials as a function of temperature is shown in Fig. 8.7.

The heat capacity,  $C$ , is similar in form except that it is defined in terms of the amount of heat required to raise the temperature of a mole of material by one degree and has the units of watt-sec/mol-°C.

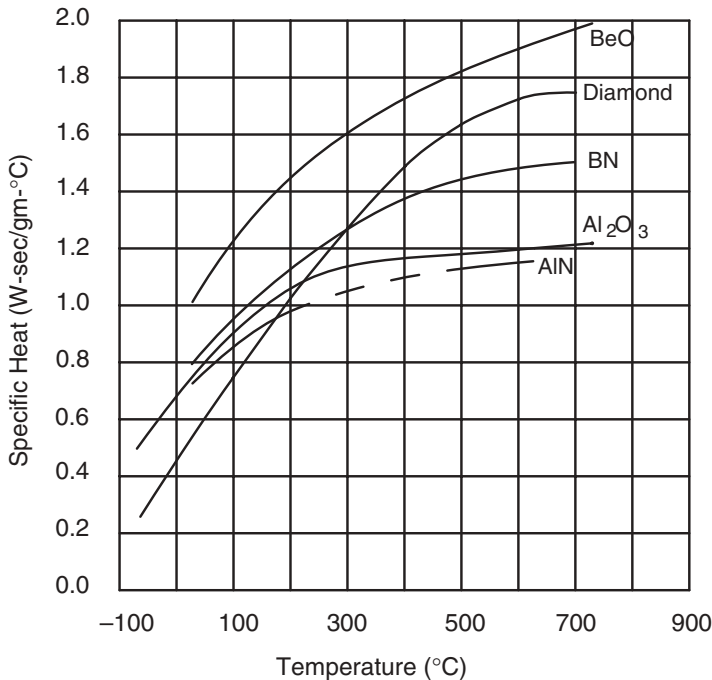


Figure 8.7 Specific heat vs. temperature for selected ceramic materials.

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## 8.4.3 Temperature coefficient of expansion

The temperature coefficient of expansion (TCE) arises from the asymmetrical increase in the interatomic spacing of atoms as a result of increased heat. Most metals and ceramics exhibit a linear, isotropic relationship in the temperature range of interest, whereas certain plastics may be anisotropic in nature. The TCE is defined as

$$\alpha = \frac{\ell(T_2) - \ell(T_1)}{\ell(T_1) - (T_2 - T_1)} \quad (8.3)$$

where  $\alpha$  = temperature coefficient of expansion in ppm/°C<sup>-1</sup>  
 $T_1$  = initial temperature  
 $T_2$  = final temperature  
 $\ell(T_1)$  = length at initial temperature  
 $\ell(T_2)$  = length at final temperature

The TCE of most ceramics is isotropic. For certain crystalline or single-crystal ceramics, the TCE may be anisotropic, and some may even contract in one direction and expand in the other. Ceramics used for substrates do not generally fall into this category, as most are mixed with glasses in the preparation stage and do not exhibit anisotropic properties as a result. The temperature coefficient of expansion of several ceramic materials is shown in Table 8.1.

**TABLE 8.1 Temperature Coefficient of Expansion of Selected Ceramic Substrate Materials**

Material	TCE (ppm/°C)
Alumina (96%)	6.5
Alumina (99%)	6.8
BeO (99.5%)	7.5
BN parallel	0.57
perpendicular	-0.46
Silicon carbide	3.7
Aluminum nitride	4.4
Diamond, Type 11A	1.02
AlSiC (70% SiC loading)	6.3

## 8.5 Mechanical Properties Of Ceramic Substrates

The mechanical properties of ceramic materials are strongly influenced by the strong interatomic bonds that prevail. Dislocation mechanisms, which create slip mechanisms in softer metals, are relatively scarce in ceramics, and failure may occur with very little plastic deformation (the small elongation that occurs

before failure). Ceramics also tend to fracture with little resistance. They have a very high melting point, as shown in Table 8.2.

**TABLE 8.2 Melting Points of Selected Ceramics**

Material	Melting point (°C)
SiC	2700
BN	2732
AlN	2232
BEO	2570
Al <sub>2</sub> O <sub>3</sub>	2000

### 8.5.1 Modulus of elasticity

The temperature coefficient of expansion (TCE) phenomenon has serious implications in the applications of ceramic substrates. When a sample of material has one end fixed, which may be considered to be a result of bonding to another material that has a much smaller TCE, the net elongation of the hotter end per unit length, or “strain” ( $E$ ), of the material is calculated by

$$E = TCE \times \Delta T \quad (8.4)$$

where  $E$  = strain in length/length

$\Delta T$  = temperature differential across the sample

Elongation develops a stress ( $S$ ) per unit length in the sample as given by Hooke’s law.

$$S = EY \quad (8.5)$$

where  $S$  = stress in psi/in ( $N/m^2/m$ )

$Y$  = modulus of elasticity in lb/in<sup>2</sup> ( $N/m^2$ )

When the total stress (as calculated by multiplying the stress/unit length by the maximum dimension of the sample) exceeds the strength of the material, mechanical cracks will form in the sample that may even propagate to the point of separation. This analysis is somewhat simplistic in nature, but it serves to provide a basic understanding of the mechanical considerations. The modulus of elasticity of selected ceramics is summarized in Table 8.3, along with other mechanical properties.

### 8.5.2 Modulus of rupture

Ordinary stress-strain testing is not generally used to test ceramic substrates, because they do not exhibit elastic behavior to a great degree. An alternative

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TABLE 8.3 Mechanical Properties of Selected Ceramics

Material	Modulus of elasticity (GPa)	Tensile strength (MPa)	Compressive strength	Modulus of rupture	Flexural strength	Density
Alumina (99%)	370	500	2600	386	352	3.98
Alumina (96%)	344	172	2260	341	331	3.92
Beryllia (99.5%)	345	138	1550	233	235	2.87
Boron nitride (normal)	43	2410	6525	800	53.1	1.92
Aluminum nitride	300	310	2000	300	269	3.27
Silicon carbide	407	197	4400	470	518	3.10
Diamond (Type 11A)	1000	1200	11000	940	1000	3.52

test, the modulus of rupture (bend strength) test, is preferred. A sample of ceramic, either circular or rectangular, is suspended between two points, a force is applied in the center, and the elongation of the sample is measured. The stress is calculated by

$$\sigma = \frac{Mx}{I} \quad (8.6)$$

where  $\sigma$  = stress in MPa

$M$  = maximum bending moment in N-m

$x$  = distance from center to outer surface in m

$I$  = moment of inertia in N-m<sup>2</sup>

The expressions for  $\sigma$ ,  $M$ ,  $x$ , and  $I$  are summarized in Table 8.4.

TABLE 8.4 Parameters of Stress in Modulus of Rupture Test<sup>1</sup>

Cross section	$M$	$c$	$I$
Rectangular	$\frac{FL}{4}$	$\frac{y}{2}$	$\frac{xy^3}{12}$
Circular	$\frac{FL}{4}$	R	$\frac{\pi R^2}{4}$

Referring to Fig. 8.8,<sup>1</sup> when these are inserted into Eq. (8.6), the result is

$$\sigma = \frac{3FL}{2xy^2} \quad (\text{Rectangular cross section}) \quad (8.7)$$

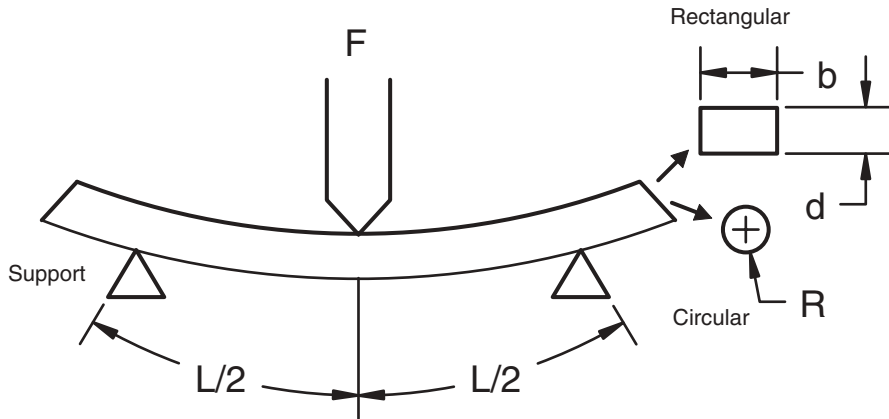


Figure 8.8 Modulus of rupture test.

$$\sigma = \frac{FL}{\pi R^3} \quad (\text{Circular cross section}) \quad (8.8)$$

where  $F$  = applied force in newtons  
 $x$  = long dimension of rectangular cross section in meters  
 $y$  = short dimension of rectangular cross section in meters  
 $L$  = length of sample in meters  
 $R$  = radius of circular cross section in meters

The modulus of rupture is the stress required to produce fracture and is given by

$$\sigma_r = \frac{3F_r L}{2xy^2} \quad (\text{Rectangular}) \quad (8.9)$$

$$\sigma_r = \frac{F_r L}{\pi R^3} \quad (\text{Circular}) \quad (8.10)$$

where  $\sigma_r$  = modulus of rupture in  $\text{n/m}^2$   
 $F_r$  = force at rupture

The modulus of rupture for selected ceramics is shown in Table 8.3.

### 8.5.3 Tensile and compressive strength

A force applied to a ceramic substrate in a tangential direction may produce tensile or compressive forces. If the force is tensile, in a direction such that the material is pulled apart, the stress produces plastic deformation as defined in Eq. (8.5). As the force increases past a value, referred to as the *tensile*

*strength*, breakage occurs. Conversely, a force applied in the opposite direction creates compressive forces until a value referred to as the *compressive strength* is reached, at which point breakage also occurs. The compressive strength of ceramic materials is, in general, much larger than the tensile strength. The tensile and compressive strengths of selected ceramic materials are shown in Table 8.3.

In practice, the force required to fracture a ceramic substrate is much lower than predicted by theory. The discrepancy is due to small flaws or cracks residing within these materials as a result of processing. For example, when a substrate is sawed, small edge cracks may be created. Similarly, when a substrate is fired, trapped organic material may outgas during firing, leaving a microscopic void in the bulk. The result is an amplification of the applied stress in the vicinity of the void that may exceed the tensile strength of the material and create a fracture. If the microcrack is assumed to be elliptical in shape with the major axis perpendicular to the applied stress, the maximum stress at the tip of the crack may be approximated by<sup>2</sup>

$$S_M = 2S_O \leq \left(\frac{a}{\rho_t}\right)^{1/2} \quad (8.11)$$

where  $S_M$  = maximum stress at the tip of the crack  
 $S_O$  = nominal applied stress  
 $a$  = length of the crack as defined in Fig. 8.9  
 $\rho_t$  = radius of the crack tip

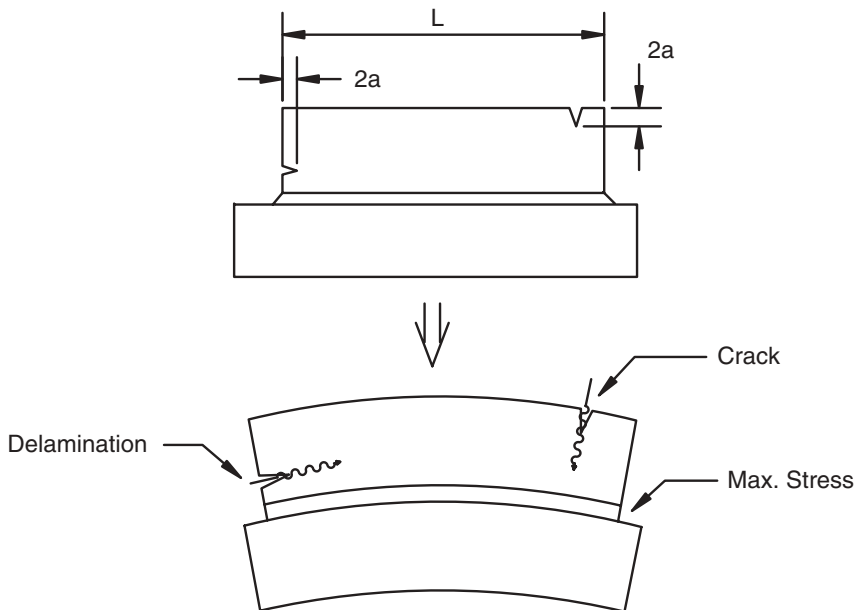


Figure 8.9 Cracks and chip-outs in substrate.<sup>5</sup>



The ratio of the maximum stress to the applied stress may be defined as

$$K_t = \frac{S_M}{S_O} = 2\left(\frac{a}{\rho_t}\right)^{1/2} \quad (8.12)$$

where  $K_t$  = stress concentration factor

For certain geometries, such as a long crack with a small tip radius,  $K_t$  may be much larger than 1, and the force at the tip may be substantially larger than the applied force.

Based on this analysis, a material parameter called the *plain strain fracture toughness*, a measure of the ability of the material to resist fracture, can be defined as

$$K_{IC} = ZS_C\sqrt{\pi a} \quad (8.13)$$

where  $K_{IC}$  = plain strain fracture toughness in psi-in<sup>1/2</sup> or MPa-m<sup>1/2</sup>

$Z$  = dimensionless constant, typically 1.2<sup>2</sup>

$S_C$  = critical force required to cause breakage

From Eq. (8.13), the expression for the critical force can be defined as

$$S_C = Z\frac{K_{IC}}{\sqrt{\pi a}} \quad (8.14)$$

When the applied force on the die caused by TCE or thermal differences exceeds this figure, fracture is likely. The plain strain fracture toughness for selected materials is presented in Table 8.5. It should be noted that Eq. (8.14) is a function of thickness up to a point but is approximately constant for the area-to-thickness ratio normally found in substrates.

**TABLE 8.5 Fracture Toughness for Selected Materials**

Material	Fracture toughness (MPa-m <sup>1/2</sup> )
Silicon	0.8
Alumina (96%)	3.7
Alumina (99%)	4.6
Silicon carbide	7.0
Molding compound	2.0

#### 8.5.4 Hardness

Ceramics are among the hardest substances known, and their hardness is correspondingly difficult to measure. Most methods rely on the ability of one ma-

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terial to scratch another, and the measurement is presented on a relative scale. Of the available methods, the Knoop method is the most frequently used. In this approach, the surface is highly polished, and a pointed diamond stylus under a light load is allowed to impact the material. The depth of the indentation formed by the stylus is measured and converted to a qualitative scale called the “Knoop” or “HK” scale. The Knoop hardness of selected ceramics is given in Table 8.6.

**TABLE 8.6 Knoop Hardness for Selected Ceramics**

Material	Knoop hardness (100 g)
Diamond	7000
Aluminum oxide	2100
Aluminum nitride	1200
Beryllium oxide	1200
Boron nitride	5000
Silicon carbide	2500

**8.5.5 Thermal shock**

Thermal shock occurs when a substrate is exposed to temperature extremes over a short period of time. Under these conditions, the substrate is not in thermal equilibrium, and internal stresses may be sufficient to cause fracture. Thermal shock can be liquid-to-liquid or air-to-air, with the most extreme exposure occurring when the substrate is transferred directly from one liquid bath to another. The heat is more rapidly absorbed or transmitted, depending on the relative temperature of the bath, because of the higher specific heat of the liquid as opposed to air.

The ability of a substrate to withstand thermal shock is a function of several variables, including the thermal conductivity, the coefficient of thermal expansion, and the specific heat. Winkleman and Schott<sup>3</sup> developed a parameter called the *coefficient of thermal endurance* that qualitatively measures the ability of a substrate to withstand thermal stress.

$$F = \frac{P}{\alpha Y} \sqrt{\frac{k}{\rho c}} \quad (8.15)$$

where  $F$  = coefficient of thermal endurance  
 $P$  = tensile strength in MPa  
 $\alpha$  = thermal coefficient of expansion in 1/K  
 $Y$  = modulus of elasticity in MPa  
 $k$  = thermal conductivity in W/m-K  
 $\rho$  = density in kg/m<sup>3</sup>  
 $c$  = specific heat in W-sec/kg-K

The coefficient of thermal endurance for selected materials is shown in Table 8.7. The phenomenally high coefficient of thermal endurance for BN is primarily a result of the high ratio of tensile strength to modulus of elasticity as compared to other materials. Diamond is also high, primarily because of the high tensile strength, the high thermal conductivity, and the low TCE.

**TABLE 8.7 Thermal Endurance Factor for Selected Materials at 25°C**

Material	Thermal endurance factor
Alumina (99%)	0.640
Alumina (96%)	0.234
Beryllia (99.5%)	0.225
Boron nitride ("a" axis)	648
Aluminum nitride	2.325
Silicon carbide	1.40
Diamond (Type 11A)	30.29

The thermal endurance factor is a function of temperature in that several of the variables, particularly the thermal conductivity and the specific heat, are functions of temperature. From Table 8.7, it is also noted that the thermal endurance factor may drop rapidly as the alumina-to-glass ratio drops. This is a result of the difference in the thermal conductivity and TCE of the alumina and glass constituents that increase the internal stresses. This is true of other materials as well.

## 8.6 Electrical Properties of Ceramics

The electrical properties of ceramic substrates perform an important task in the operation of electronic circuits. Depending on the applications, the electrical parameters may be advantageous or detrimental to circuit function. Of most interest are the resistivity, the breakdown voltage (or dielectric strength), and the dielectric properties, including the dielectric constant and loss tangent.

### 8.6.1 Resistivity

The electrical resistivity of a material is a measure of its ability to transport charge under the influence of an applied electric field. More often, this ability is presented in the form of the electrical conductivity, the reciprocal of the resistivity, as defined in Eq. (8.16).

$$\sigma = \frac{1}{\rho} \quad (8.16)$$

where  $\sigma$  = conductivity in siemens/unit length  
 $\rho$  = resistivity in ohm-unit length

The V-I relationship is governed primarily by injected carriers as opposed to thermal carriers (the opposite of the case with metals) and is given by

$$J = \mu\epsilon E^2 \quad (8.17)$$

The electrical conductivity of ceramic substrates is extremely low. In practice, it is primarily the result impurities and lattice defects and may vary widely from batch to batch. The conductivity is also a strong function of temperature. As the temperature increases, the ratio of thermal to injected carriers increases. As a result, the conductivity increases and the V-I relationship follows Ohm's law more closely. Typical values of the resistivity of selected ceramic materials are presented in Table 8.8.

**TABLE 8.8 Electrical Properties of Selected Ceramic Substrates**

Material	Property			
	Electrical resistivity ( $\Omega$ -cm)	Breakdown voltage (AC kV/mm)	Dielectric constant	Loss tangent (@ 1 MHz)
Alumina (95%)				
25°C	$>10^{14}$		9.0	
500°C	$4 \times 10^9$	8.3	10.8	0.0002
1000°C	$1 \times 10^6$			
Alumina (99.5%)				
25°C	$>10^{14}$			
500°C	$2 \times 10^{10}$	8.7	9.4	0.0001
1000°C	$2 \times 10^6$		10.1	
Beryllia				
25°C	$>10^{14}$	6.6	6.4	0.0001
500°C	$2 \times 10^{10}$		6.9	0.0004
Aluminum nitride	$>10^{13}$	14	8.9	0.0004
Boron nitride	$>10^{14}$	61	4.1	0.0003
Silicon carbide*	$>10^{13}$	0.7	40	0.05
Diamond (Type II)	$>10^{14}$	1000	5.7	0.0006

\*Depends on method of preparation. May be substantially lower.

### 8.6.2 Breakdown voltage

The term *breakdown voltage* is very descriptive. Although ceramics are normally very good insulators, the application of excessively high potentials can

dislodge electrons from orbit with sufficient energy to allow them to dislodge other electrons from orbit, creating an *avalanche effect*. The result is a breakdown of the insulation properties of the material, allowing current to flow. This phenomenon is accelerated by elevated temperature, particularly when mobile ionic impurities are present.

The breakdown voltage is a function of numerous variables, including the concentration of mobile ionic impurities, grain boundaries, and the degree of stoichiometry. In most applications, the breakdown voltage is sufficiently high that it is not an issue. However, there are two cases in which it must be a consideration.

1. At elevated temperatures created by localized power dissipation or high ambient temperature, the breakdown voltage may drop by orders of magnitude. Combined with a high potential gradient, this condition may be susceptible to breakdown.
2. The surface of most ceramics is highly “wettable,” in that moisture tends to spread rapidly. Under conditions of high humidity, coupled with surface contamination, the effective breakdown voltage is much lower than the intrinsic value.

### 8.6.3 Dielectric properties

Two conductors in proximity with a difference in potential have the ability to attract and store electric charge. Placing a material with dielectric properties between them enhances this effect. A dielectric material has the capability of forming electric dipoles, displacements of electric charge, internally. At the surface of the dielectric, the dipoles attract more electric charge, thus enhancing the charge storage capability, or capacitance, of the system. The relative ability of a material to attract electric charge in this manner is called the *relative dielectric constant*, or *relative permittivity*, and is usually given the symbol  $K$ . The relative permittivity of free space is 1.0 by definition and the absolute permittivity is

$\epsilon_0$  = permittivity of free space

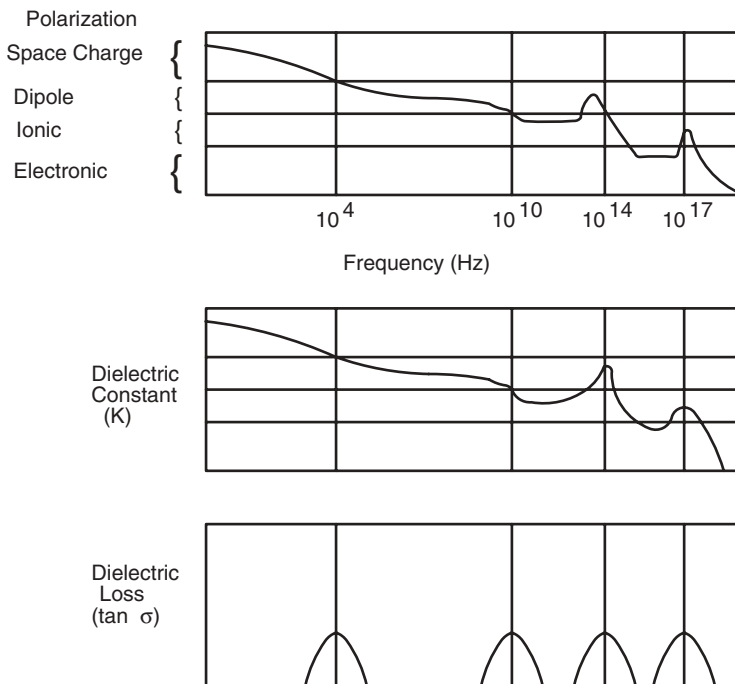
$$\epsilon_0 = \frac{1}{36\pi} \times 10^{-9} \frac{\text{farads}}{\text{meter}} \quad (8.18)$$

There are two common ways to categorize dielectric materials: as polar or nonpolar, and as paraelectric or ferroelectric. Polar materials include those that are primarily molecular in nature, such as water; nonpolar materials include both electronically and ionically polarized materials. Paraelectric materials are polarized only in the presence of an applied electric field and lose their polarization when the field is removed, whereas ferroelectric materials retain a degree of polarization after the field is removed. Materials used as ceramic substrates are usually nonpolar and paraelectric in nature. An exception is silicon carbide, which has a degree of molecular polarization.

In the presence of an electric field that is changing at a high frequency, the polarity of the dipoles must change at the same rate as the polarity of the signal to maintain the dielectric constant at the same level. Some materials are excellent dielectrics at low frequencies, but the dielectric qualities drop off rapidly as the frequency increases. Electronic polarization, which involves only displacement of free charge and not ions, responds more rapidly to the changes in the direction of the electric field and remains viable up to about  $10^{17}$  Hz. The polarization effect of ionic displacement begins to fall off at about  $10^{13}$  Hz, and molecular and space charge polarizations fall off at still lower frequencies. The frequency response of the different types is shown in Fig. 8.10, which also illustrates that the dielectric constant decreases with frequency.

Changing the polarity of the dipoles requires a finite amount of energy and time. The energy is dissipated as internal heat, quantified by a parameter called the *loss tangent* or *dissipation factor*. Furthermore, dielectric materials are not perfect insulators. These phenomena may be modeled as a resistor in parallel with a capacitor. The loss tangent, as expected, is a strong function of the applied frequency, increasing as the frequency increases.

In alternating current applications, the current and voltage across an ideal capacitor are exactly  $90^\circ$  out of phase, with the current leading the voltage. In actuality, the resistive component causes the current to lead the voltage by an angle less than  $90^\circ$ . The loss tangent is a measure of the real or resistive com-



**Figure 8.10** Frequency effects on dielectric materials.

ponent of the capacitor and is the tangent of the difference between  $90^\circ$  and the actual phase angle.

$$\text{Loss tangent} = \tan(90^\circ - \delta) \quad (8.19)$$

where  $\delta$  = phase angle between voltage and current

The loss tangent is also referred to as the *dissipation factor* (DF).

The loss tangent may also be considered as a measure of the time required for polarization. It requires a finite amount of time to change the polarity of the dipole after an alternating field is applied. The resulting phase retardation is equivalent to the time indicated by the difference in phase angles.

## 8.7 Properties of Substrate Materials

### 8.7.1 Aluminum oxide

Aluminum oxide,  $\text{Al}_2\text{O}_3$ , commonly referred to as alumina, is by far the most common substrate material used in the microelectronics industry, because it is superior to most other oxide ceramics in mechanical, thermal, and electrical properties. The raw materials are plentiful and low in cost and are amenable to fabrication by a wide variety of techniques into a wide variety of shapes.

Alumina is hexagonal close-packed with a corundum structure. Several metastable structures exist, but they all ultimately irreversibly transform to the hexagonal alpha phase. Alumina is stable in both oxidizing and reducing atmospheres up to  $1925^\circ\text{C}$ .

Weight loss in vacuum over the temperature range of  $1700^\circ\text{C}$  to  $2000^\circ\text{C}$  ranges from  $10^{-7}$  to  $10^{-6}$   $\text{g}/\text{cm}^2\text{-sec}$ . It is resistant to attack by all gases except wet fluorine to at least  $1700^\circ\text{C}$ . Alumina is attacked at elevated temperatures by alkali metal vapors and halogen acids, especially the lower-purity alumina compositions that may contain a percentage of glasses.

Alumina is used extensively in the microelectronics industry as a substrate material for thick and thin film circuits, for circuit packages, and as multilayer structures for multichip modules. Compositions exist for both high- and low-temperature processing. High-temperature cofired ceramics (HTCC) use a refractory metal, such as tungsten or molybdenum/manganese, as a conductor and fire at about  $1800^\circ\text{C}$ . The circuits are formed as separate layers, laminated together, and fired as a unit. Low-temperature cofired ceramics (LTCC) use conventional gold or palladium silver as conductors and fire as low as  $850^\circ\text{C}$ . Certain power MOSFETs and bipolar transistors are mounted on alumina substrates to act as electrical insulators and thermal conductors. The parameters of alumina are summarized in Table 8.9.

### 8.7.2 Beryllium oxide

Beryllium oxide ( $\text{BeO}$ , beryllia) is cubic close-packed and has a zinc blende structure. The alpha form of  $\text{BeO}$  is stable to above  $2050^\circ\text{C}$ .  $\text{BeO}$  is stable in dry atmospheres and is inert to most materials. It hydrolyzes at temperatures

TABLE 8.9 Typical Parameters of Aluminum Oxide

Parameter	Units	Test	Percentage (%)			
			85	90	96	99.5
Density	g/cm <sup>3</sup>	ASTM C20	3.40	3.60	3.92	3.98
Elastic modulus	GPa	ASTM C848	220	275	344	370
Poisson's ratio		ASTM C848	0.22	0.22	0.22	0.22
Compressive strength	MPa	ASTM C773	1930	2150	2260	2600
Fracture toughness	MPa-m <sup>0.5</sup>	Notched beam	3.1	3.3	3.7	4.6
Thermal conductivity	W/m-°C	ASTM C408	16	16.7	24.7	31.0
TCE	10 <sup>-6</sup> /°C	ASTM C372	5.9	6.2	6.5	6.8
Specific heat	W-sec/g-°C	ASTM E1269	920	920	880	880
Dielectric strength	AC kV/mm	ASTM D116	8.3	8.3	8.3	8.7
Loss tangent (1 MHz)		ASTM D2520	0.0009	0.0004	0.0002	0.0001
Volume resistivity	25°C	ASTM D1829	>10 <sup>14</sup>	>10 <sup>14</sup>	>10 <sup>14</sup>	>10 <sup>14</sup>
	500°C		4 × 10 <sup>9</sup>	4 × 10 <sup>8</sup>	4 × 10 <sup>9</sup>	2 × 10 <sup>10</sup>
	1000°C			5 × 10 <sup>5</sup>	1 × 10 <sup>6</sup>	2 × 10 <sup>6</sup>
	Ω-cm					

greater than 1100°C with the formation and volatilization of beryllium hydroxide. BeO reacts with graphite at high temperatures, forming beryllium carbide.

Beryllia has an extremely high thermal conductivity, higher than aluminum metal, and is widely used in applications where this parameter is critical. The thermal conductivity drops rapidly above 300°C but is suitable for most practical applications.

Beryllia is available in a wide variety of geometries formed using a variety of fabrication techniques. While beryllia in the pure form is perfectly safe, care must be taken when machining BeO, however, as the dust is toxic if inhaled.

Beryllia may be metallized with thick film, thin film, or by one of the copper processes. However, thick film pastes must be specially formulated to be compatible. Laser or abrasive trimming of BeO must be performed in the presence of a vacuum to remove the dust. The properties of 99.5 percent beryllia are summarized in Table 8.10.

### 8.7.3 Aluminum nitride

Aluminum nitride is covalently bonded with a wurtzite structure and decomposes at 2300°C under 1 atm of argon. In a nitrogen atmosphere of 1500 psi, melting may occur in excess of 2700°C. Oxidation of AlN in even a low concen-



**TABLE 8.10 Typical Parameters for 99.5 Percent Beryllium Oxide**

Parameter	Units	Value
Density	g/cm <sup>3</sup>	2.87
Hardness	Knoop 100 g	1200
Melting point	°C	2570
Modulus of elasticity	GPa	345
Compressive strength	MPa	1550
Poisson's ratio		0.26
Thermal conductivity	W/m·°C	
25°C		250
500°C		55
Specific heat	W-sec/g-K	
25°C		1.05
500°C		1.85
TCE	10 <sup>-6</sup> /K	7.5
Dielectric constant		6.5
1 MHz		6.6
10 GHz		
Loss tangent		
1 MHz		0.0004
10 GHz		0.0004
Volume resistivity	Ω-cm	
25°C		>10 <sup>14</sup>
500°C		2 × 10 <sup>10</sup>

tration of oxygen (<0.1 percent) occurs at temperatures above 700°C. A layer of aluminum oxide protects the nitride to a temperature of 1370°C, above which the protective layer cracks, allowing oxidation to continue. Aluminum nitride is not appreciably affected by hydrogen, steam, or oxides of carbon to 980°C. It dissolves slowly in mineral acids and decomposes slowly in water. It is compatible with aluminum to 1980°C, gallium to 1300°C, iron or nickel to 1400°C, and molybdenum to 1200°C.

Aluminum nitride substrates are fabricated by mixing AlN powder with compatible glass powders containing additives such as CaO and Y<sub>2</sub>O<sub>3</sub>, along with organic binders, and casting the mixture into the desired shape. Densification of the AlN requires very tight control of both atmosphere and temperature. The solvents used in the preparation of substrates must be anhydrous to minimize oxidation of the AlN powder and prevent the generation of ammonia during firing.<sup>4</sup> For maximum densification and maximum thermal conductivity, the substrates must be sintered in a dry reducing atmosphere to minimize oxidation.

Aluminum nitride is primarily noted for two very important properties: a high thermal conductivity and a TCE closely matching that of silicon. Several grades of aluminum nitride with different thermal conductivities are available. The prime reason for the difference is the oxygen content of the material. It is important to note that even a thin surface layer of oxidation on a fraction of the particles can adversely affect the thermal conductivity. Only with a high degree of material and process control can AlN substrates be made consistent.

The thermal conductivity of AlN does not vary as widely with temperature as does that of BeO. Considering the highest grade of AlN, the crossover temperature is about 20°C. Above this temperature, the thermal conductivity of AlN is higher; below, 20°C, BeO is higher.

The TCE of AlN closely matches that of silicon, which is an important consideration when mounting large power devices. The second level of packaging is also critical. If an aluminum nitride substrate is mounted directly to a package with a much higher TCE, such as copper, the result can be worse than if a substrate with an intermediate, although higher, TCE were used. The large difference in TCE builds up stresses during the mounting operation that can be sufficient to fracture the die and/or the substrate.

Thick film, thin film, and copper metallization processes are available for aluminum nitride. Certain of these processes, such as direct bond copper (DBC) require oxidation of the surface to promote adhesion. For maximal thermal conductivity, a metallization process should be selected that bonds directly to AlN to eliminate the relatively high thermal resistance of the oxide layer.

Thick film materials must be formulated to adhere to AlN. The lead oxides prevalent in thick film pastes that are designed for alumina and beryllia oxidize the surface of AlN rapidly, causing blistering and a loss of adhesion. Thick film resistor materials are primarily based on RuO<sub>2</sub> and MnO<sub>2</sub>.

Thin film processes available for AlN include NiCr/Ni/Au, Ti/Pt/Au, and Ti/Ni/Au.<sup>5</sup> Titanium in particular provides excellent adhesion by diffusing into the surface of the AlN. Platinum and nickel are transition layers to promote gold adhesion. Solders such as Sn60/Pb40 and Au80/Sn20 can also be evaporated onto the substrate to facilitate soldering.

Multilayer circuits can be fabricated with W or Mb/Mn conductors. The top layer is plated with nickel and gold to promote solderability and bondability. Ultrasonic milling may be used for cavities, blind vias, and through vias. Laser machining is suitable for through vias as well.

Direct bond copper may be attached to AlN by forming a layer of oxide over the substrate surface, which may require several hours at temperatures above 900°C. The DBC forms a eutectic with aluminum oxide at about 963°C. The layer of oxide, however, increases the thermal resistance by a significant amount, partially negating the high thermal conductivity of the aluminum nitride. Copper foil may also be brazed to AlN with one of the compatible braze compounds. Active metal brazing (AMB) does not generate an oxide layer. The copper may also be plated with nickel and gold. The properties of aluminum nitride are summarized in Table 8.11.

**TABLE 8.11 Typical Parameters for Aluminum Nitride (Highest Grade)**

Parameter	Units	Value
Density	g/cm <sup>3</sup>	3.27
Hardness	Knoop 100g	1200
Melting point	°C	2232
Modulus of elasticity	GPa	300
Compressive strength	MPa	2000
Poisson's ratio		0.23
Thermal conductivity	W/m-K	
25°C		270
150°C		195
Specific heat	W-sec/g-K	
25°C		0.76
150°C		0.94
TCE	10 <sup>-6</sup> /K	4.4
Dielectric constant		
1 MHz		8.9
10 GHz		9.0
Loss tangent		
1 MHz		0.0004
10 GHz		0.0004
Volume resistivity	Ω-cm	
25°C		>10 <sup>12</sup>
500°C		2 × 10 <sup>8</sup>

#### 8.7.4 Diamond

Diamond substrates are primarily grown by chemical vapor deposition (CVD). In this process, a carbon-based gas is passed over a solid surface and activated by a plasma, a heated filament, or a combustion flame. The surface must be maintained at a high temperature, above 700°C, to sustain the reaction. The gas is typically a mixture of methane (CH<sub>4</sub>) and hydrogen (H<sub>2</sub>) in a ratio of 1 to 2 percent CH<sub>4</sub> by volume.<sup>6</sup> The consistency of the film in terms of the ratio of diamond to graphite is inversely proportional to the growth rate of the film. Films produced by plasma have a growth rate of 0.1 to 10 μ/hr and are very high quality, while films produced by combustion methods have a growth rate of 100 to 1000 μ/hr and are of lesser quality.

The growth begins at nucleation sites and is columnar in nature, growing faster in the normal direction than in the lateral direction. Eventually, the columns grow together to form a polycrystalline structure with microcavities spread throughout the film. The resulting substrate is somewhat rough, with

a 2- to 5- $\mu$  surface. This feature is detrimental to the effective thermal conductivity, and the surface must be polished for optimal results. An alternative method is to use an organic filler<sup>7</sup> on the surface for planarization. This process has been shown to have a negligible effect on the overall thermal conductivity from the bulk, and it dramatically improves heat transfer. Diamond substrates as large as 10 cm<sup>2</sup> and as thick as 1000  $\mu$  have been fabricated.

Diamond can be deposited as a coating on refractory metals, oxides, nitrides, and carbides. For maximum adhesion, the surface should be a carbide-forming material with a low TCE.<sup>7</sup>

Diamond has an extremely high thermal conductivity, several times that of the next highest material. The primary application is, obviously, in packaging power devices. Diamond has a low specific heat, however, and works best as a heat spreader in conjunction with a heat sink. For maximum effectiveness,<sup>8</sup>

$$t_D = 0.5 \rightarrow 1 \times r_h$$

$$r_D = 3 \times r_h$$

where  $t_D$  = thickness of diamond substrate

$r_h$  = radius of heat source

$r_D$  = radius of diamond substrate

Applications of diamond substrates include heat sinks for laser diodes and laser diode arrays. The low dielectric constant of diamond, coupled with the high thermal conductivity, makes it attractive for microwave circuits as well. As improved methods of fabrication lower the cost, the use of diamond substrates is expected to expand rapidly. The properties of diamond are summarized in Table 8.12.

### 8.7.5 Boron nitride

There are two basic types of boron nitride (BN). Hexagonal (alpha) BN is soft and is structurally similar to graphite. It is white in color and is sometimes called *white graphite*. Cubic (beta) BN is formed by subjecting hexagonal BN to extreme heat and pressure, similar to the process used to fabricate synthetic industrial diamonds. Melting of either phase is possible only under nitrogen at high pressure.

Hot-pressed BN is very pure (>99 percent), with the major impurity being boric oxide (BO). Boric oxide tends to hydrolyze in water, degrading the dielectric and thermal shock properties. Calcium oxide (CaO) is frequently added to tie up the BO to minimize the water absorption. When exposed to temperatures above 1100°C, BO forms a thin coating on the surface, slowing further oxide growth.

Boron nitride in the hot-pressed state is easily machinable and may be formed into various shapes. The properties are highly anisotropic and vary considerable in the normal and tangential directions of the pressing force. The thermal conductivity in the normal direction is very high, and the TCE is very

TABLE 8.12 Typical Parameters for CVD Diamond

Parameter	Units	Value
Density	g/cm <sup>3</sup>	3.52
Hardness	Knoop 100 g	7000
Modulus of elasticity	GPa	1000
Compressive strength	MPa	11000
Poisson's ratio		0.148
Thermal conductivity	W/m-K	
Normal		2200
Tangential		1610
Specific heat	W-sec/g-K	
25°C		0.55
150°C		0.90
TCE	10 <sup>-6</sup> /K	1.02
Dielectric constant		
1 MHz		5.6
10 GHz		5.6
Loss tangent		
1 MHz		0.0001
10 GHz		0.0001
Volume resistivity	Ω-cm	
25°C		>10 <sup>13</sup>
500°C		2 × 10 <sup>11</sup>

low, making BN an attractive possibility for a substrate material. However, it has not yet been proven possible to metallize BN,<sup>9</sup> thereby limiting the range of applications. It can be used in contact with various metals, including copper, tin, and aluminum, and may be used as a thermally conductive electrical insulator. Applications of BN include microwave tubes and crucibles. The properties of boron nitride are summarized in Table 8.13.

### 8.7.6 Silicon carbide

Silicon carbide (SiC) has a tetrahedral structure and is the only known alloy of silicon and carbon. Both elements have four electrons in the outer shell, with an atom of one bonded to four atoms of the other. The result is a very stable structure that is not affected by hydrogen or nitrogen up to 1600°C. In air, SiC begins decomposing above 1000°C. As with other compounds, a protective oxide layer forms over the silicon, reducing the rate of decomposition. Silicon carbide is highly resistant to both acids and bases. Even the so-called *white etch* (hydrofluoric acid mixed with nitric and sulfuric acids) has no effect.

**TABLE 8.13 Typical Parameters for Boron Nitride**

Parameter	Units	Value
Density	g/cm <sup>3</sup>	1.92
Hardness	Knoop 100 g	5000
Modulus of elasticity	GPa	
Normal		43
Tangential		768
Compressive strength	MPa	
Normal		110
Tangential		793
Poisson's ratio		0.05
Thermal conductivity	W/m-K	
Normal		73
Tangential		161
Specific heat	W-sec/g-K	
25°C		0.84
150°C		1.08
TCE	10 <sup>-6</sup> /K	
Normal		0.57
Tangential		-0.46
Dielectric constant		
1 MHz		4.1
Loss tangent		
1 MHz		0.0003
Volume resistivity	Ω-cm	
25°C		1.6 × 10 <sup>12</sup>
500°C		2 × 10 <sup>10</sup>

Silicon carbide structures are formed by hot pressing, dry and isostatic pressing (preferred), CVD, or slip casting. Isostatic pressing using gas as the fluid provides optimal mechanical properties.

Silicon carbide in pure form is a semiconductor, and the resistivity depends on the impurity concentration. In the intrinsic form, the resistivity is less than 1000 W-cm, which is unsuitable for ordinary use. The addition of a small percentage (<1%) of BeO during the fabrication process<sup>10</sup> increases the resistivity to as high as 10<sup>13</sup> W-cm by creating carrier-depleted layers around the grain boundaries.

Both thick and thin films can be used to metallize SiC, although some machining of the surface to attain a higher degree of smoothness is necessary for optimal results. The two parameters that make SiC attractive as a substrate are the exceptionally high thermal conductivity, second only to diamond, and the low TCE, which matches that of silicon to a higher degree than any other ceramic. SiC is also less expensive than either BeO or AlN. A possible disad-

vantage is the high dielectric constant, 4 to 5 times higher than that of other substrate materials. This parameter can result in cross coupling of electronic signals or in excessive transmission delay. The parameters of SiC are summarized in Table 8.14.

**TABLE 8.14 Typical Parameters for Silicon Carbide**

Parameter	Units	Value
Density	g/cm <sup>3</sup>	3.10
Hardness	Knoop 100 g	500
Modulus of elasticity	GPa	407
Compressive strength	MPa	4400
Fracture toughness	MPa-m <sup>1/2</sup>	7.0
Poisson's ratio		0.14
Thermal conductivity	W/m-K	
25°C		290
150°C		160
Specific heat	W-sec/g-K	
25°C		0.64
150°C		0.92
TCE	10 <sup>-6</sup> /K	3.70
Dielectric constant		40
Loss tangent		0.05
Volume resistivity	Ω-cm	
25°C		>10 <sup>13</sup>
500°C		2 × 10 <sup>9</sup>

## 8.8 Composite Materials

Ceramics typically have a low thermal conductivity and a low TCE, whereas metals have a high thermal conductivity and a high TCE. It is a logical step to combine these properties to obtain a material with a high thermal conductivity and a low TCE. The ceramic in the form of particles or continuous fibers is mixed with the metal to combine the desirable properties of both. The resultant structure is referred to as a metal matrix composite (MMC).

The most common metals used in this application are aluminum and copper, with aluminum being more common due to lower cost. Fillers include SiC, AlN, BeO, graphite, and diamond. Compatibility of the materials is a prime consideration. Graphite, for example, has an electrolytic reaction with aluminum but not with copper.<sup>11</sup> Two materials will be described here: AlSiC,

a composite made up of aluminum and silicon carbide, and Dymalloy<sup>®</sup>, a combination of copper and diamond.

### 8.8.1 Aluminum silicon carbide

Aluminum silicon carbide (AlSiC) is produced by forcing liquid aluminum into a porous SiC preform. The preform is made by any of the common ceramic processing technologies, including dry pressing, slip molding, and tape casting. The size and shape of the preform is selected to provide the desired volume fraction of SiC. The resulting combination has a thermal conductivity almost as high as that of pure aluminum, with a TCE as low as 6.1 ppm/°C. AlSiC is also electrically conductive, prohibiting its use as a conventional substrate.

The mechanical properties of the composite are determined by the ratio of SiC to aluminum as shown in Fig. 8.11.<sup>10</sup> A ratio of 70 to 73 percent of SiC by volume provides the optimal properties for electronic packaging.<sup>10</sup> This ratio gives a TCE of about 6.5 ppm/°C, which closely matches that of alumina and beryllia. This allows AlSiC to be used as a base plate for ceramic substrates, using its high thermal conductivity to best advantage.

AlSiC, being electrically conductive, may be readily plated with aluminum to provide a surface for further processing. The aluminum coating may be plated with nickel and gold to permit soldering, or it may be anodized where an insulating surface is required.<sup>12</sup> An alternative approach is to flame spray the AlSiC with various silver alloys for solderability.

Two other advantages of AlSiC are strength and weight. The aluminum is somewhat softer than SiC and reduces the propagation of cracks. The density is only about 1/3 that of Kovar<sup>®</sup>, and the thermal conductivity is over 12 times greater.

AlSiC has been used to advantage in the fabrication of hermetic single-chip and multichip packages and as heat sinks for power devices and circuits. Although difficult to drill and machine, AlSiC can be formed into a variety of

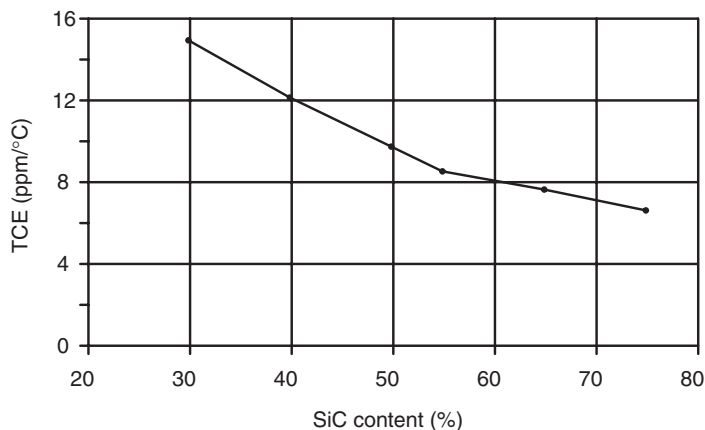


Figure 8.11 TCE vs. SiC content for AlSiC.



shapes in the powder state. It has been successfully integrated with patterned AlN to form a power module package.<sup>12</sup>

The TCE linearly increases with temperature up to about 350°C and then begins to decrease. At this temperature, the aluminum matrix softens, and the SiC matrix dominates. This factor is an important feature for power packaging. The parameters of AlSiC are summarized in Table 8.15.

**TABLE 8.15 Typical Parameters for AlSiC (70% SiC by Volume), SiC, and Aluminum**

Parameter	Units	AlSiC	SiC	Al
Density	g/cm <sup>3</sup>	3.02	3.10	2.70
Modulus of elasticity	GPa	224	407	69
Thermal conductivity (25°C)	W/m-K	192	*	55
TCE	10 <sup>-6</sup> /K	7.0	3.70	23
Volume resistivity (25°C)	μΩ-cm	34	>10 <sup>13</sup>	2.8

\*Depends on method of preparation and number/size of defects.

### 8.8.2 Dymalloy<sup>®</sup>

Dymalloy is a matrix of Type I diamond and Cu<sub>20</sub>/Ag<sub>80</sub> alloy.<sup>13</sup> The diamond is ground into a powder in the 6- to 50-μm range. The powder is coated with W<sub>74</sub>/Rh<sub>26</sub> to form a carbide layer approximately 100 Å thick followed by a 1000 Å coating of copper. The copper is plated to a thickness of several micrometers to permit brazing.

The powder is packed into a form and filled in a vacuum with Cu<sub>20</sub>/Ag<sub>80</sub> alloy that melts at approximately 800°C. This material is selected over pure copper, which melts at a much higher temperature, to minimize graphitization of the diamond. The diamond loading is approximately 55 percent by volume. The parameters of Dymalloy are summarized in Table 8.16.

**TABLE 8.16 Typical Parameters for Dymalloy<sup>®</sup> (55% Diamond by Volume)**

Parameter	Units	Value
Density	g/cm <sup>3</sup>	6.4
Tensile strength	MPa	400
Specific heat*	W-sec/g-°C	0.316 + 8.372 × 10 <sup>-4</sup> T
Thermal Conductivity	W/m-K	360
TCE†	10 <sup>-6</sup> /°C	5.48 + 6.5 × 10 <sup>-3</sup> T

\*Temperature in °C from 25 to 75°C

†Temperature in °C from 25 to 200°C

## 8.9 Thick Film Technology

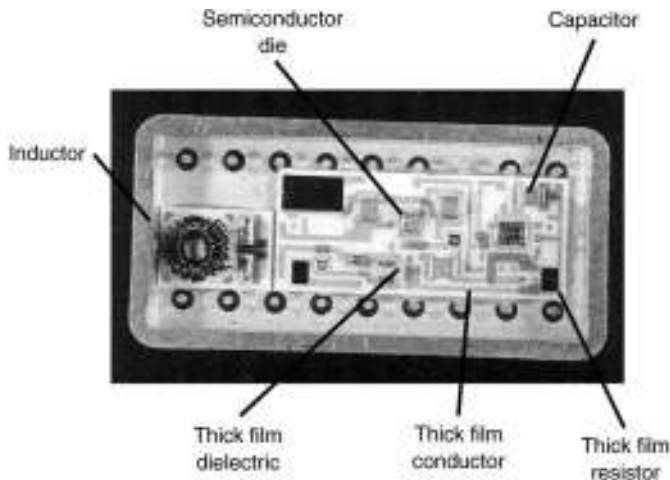
Thick film circuits as depicted in Fig. 8.12 are fabricated by screen printing conductive, resistive, and insulating materials in the form of a viscous paste onto a ceramic substrate. The printed film is dried to remove volatile components and exposed to an elevated temperature to activate the adhesion mechanism that adheres the film to the substrate. In this manner, by depositing successive layers as shown in Fig. 8.13, multilayer interconnection structures can be formed that may contain integrated resistors, capacitors, or inductors.

All thick film pastes have two general characteristics in common.

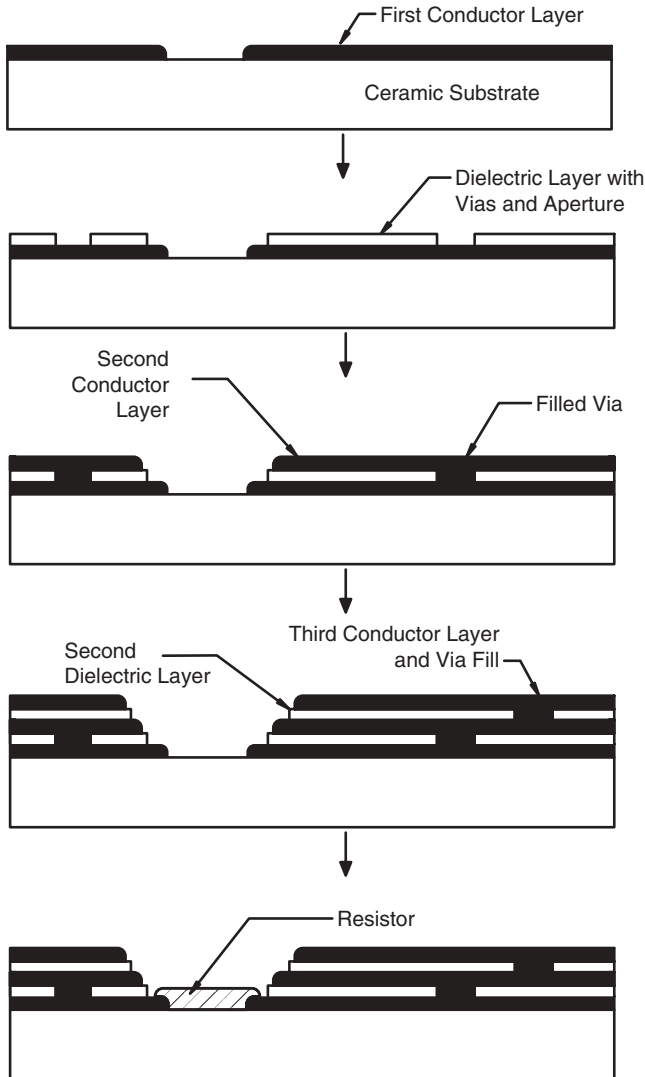
1. They are viscous fluids with a non-Newtonian rheology suitable for screen printing.
2. They are composed of two different multicomponent phases: a functional phase that imparts the electrical and mechanical properties to the finished film, and a vehicle phase that imparts the proper rheology.

There are numerous ways to categorize thick film pastes. One way is shown in Fig. 8.14, which depicts three basic categories: polymer thick films, refractory thick films, and cermet thick films. Refractory thick films are a special class of cermet thick films and are frequently categorized separately. These materials are designed to be fired at much higher temperatures (1500 to 1600°C) than conventional cermet materials and are also fired in a reducing atmosphere.

Polymer thick films consist of a mixture of polymer materials with conductor, resistor, or insulating particles. They cure at temperatures ranging from 85 to 300°C. Polymer conductors are primarily silver, with carbon being the most common resistor material. Polymer thick film materials are more com-



**Figure 8.12** Thick film hybrid circuit.



**Figure 8.13** Thick film multilayer fabrication steps.

monly associated with organic substrate materials, as opposed to ceramic, and will not be considered in further detail.

Cermet thick film materials in the fired state are a combination of glass ceramic and metal and are designed to be fired in the range 850 to 1000°C.

A conventional cermet thick film paste has four major constituents: an active element, which establishes the function of the film; an adhesion element, which provides the adhesion to the substrate and a matrix that holds the active particles in suspension; an organic binder, which provides the proper fluid properties for screen printing; and a solvent or thinner, which establishes the viscosity of the vehicle phase.

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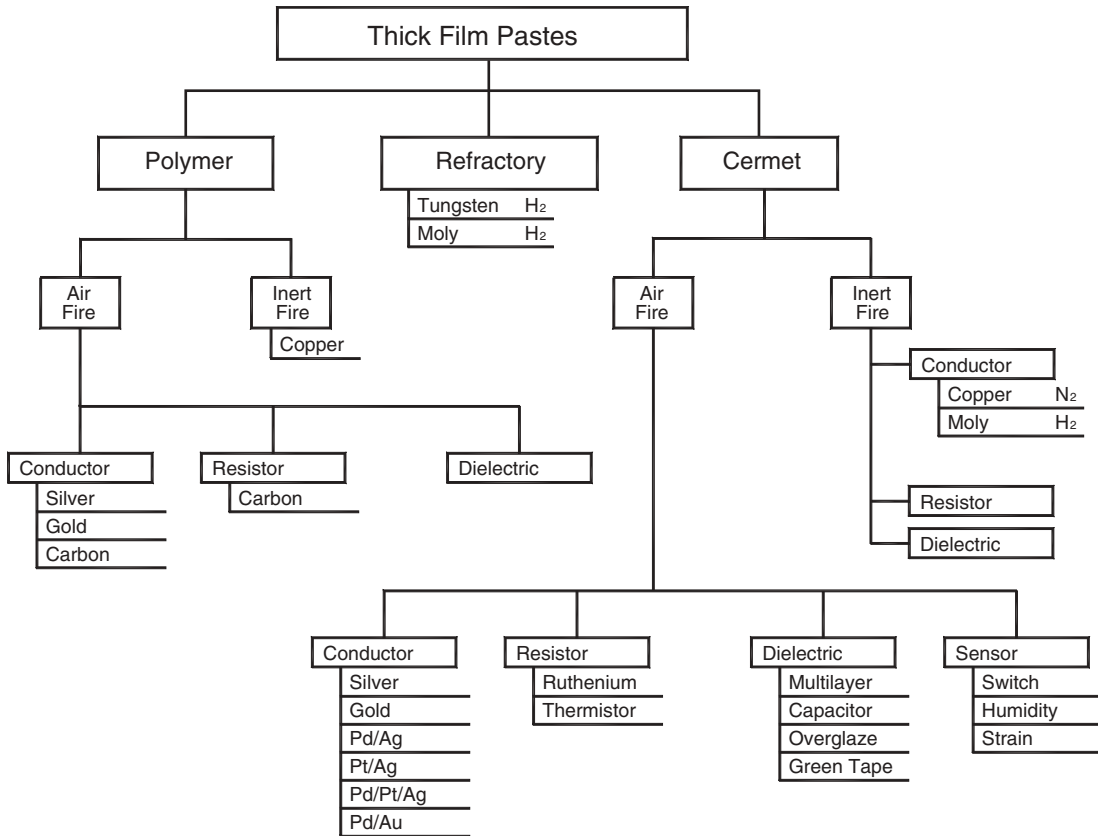


Figure 8.14 Thick film paste matrix.

## 8.9.1 The active element

The active element within the paste determines the electrical properties of the fired film. If the active element is a metal, the fired film will be a conductor; if it is a conductive metal oxide, a resistor; and, if it is an insulator, a dielectric. The active element is most commonly found in powder form ranging from 1 to 10  $\mu$  in size, with a mean diameter of about 5  $\mu$ . Particle morphology can vary greatly depending on the method used to produce the metallic particles. Spherical, flaked, or circular shapes (both amorphous and crystalline) are available from powder manufacturing processes. Structural shape and particle morphology are critical to the development of the desired electrical performance, and extreme control on the particle shape, size, and distribution must be maintained to ensure uniformity of the properties of the fired film.

## 8.9.2 The adhesion element

There are two primary constituents used to bond the film to the substrate: glass and metal oxides, which may be used singly or in combination. Films

that use a glass, or frit, are referred to as “fritted” materials and have a relatively low melting point (500 to 600°C). There are two adhesion mechanisms associated with the fritted materials: a chemical reaction and a physical reaction. In the chemical reaction, the molten glass chemically reacts with the glass in the substrate to a degree. In the physical reaction, the glass flows into and around the irregularities in the substrate surface, flowing into holes and voids and clinging to the small outcroppings of ceramic. The total adhesion is the sum of the two factors. The physical bonds are more susceptible to degradation by thermal cycling or thermal storage than the chemical bonds and are generally the first to fracture under stress. The glass also creates a matrix for the active particles, holding them in contact with each other to promote sintering and to provide a series of three-dimensional continuous paths from one end of the film to the other. Principal thick film glasses are based on  $B_2O_3$ - $SiO_2$  network formers with modifiers such as  $PbO$ ,  $Al_2O_3$ ,  $Bi_2O_3$ ,  $ZnO$ ,  $BaO$ , and  $CdO$  added to change the physical characteristics of the film, such as the melting point, the viscosity, and the coefficient of thermal expansion.  $Bi_2O_3$  also has excellent wetting properties, both to the active element and to the substrate, and is frequently used as a fluxing agent. The glass phase may be introduced as a prereacted particle or formed in situ by using glass precursors such as boric oxide, lead oxide, and silicon. Fritted conductor materials tend to have glass on the surface, making subsequent component assembly processes more difficult.

A second class of materials utilizes metal oxides to provide the adhesion to the substrate. In this case, a pure metal, such as copper or cadmium, is mixed with the paste and reacts with oxygen atoms on the surface of the substrate to form an oxide. The conductor adheres to the oxide and to itself by sintering, which takes place during firing. During firing, the oxides react with broken oxygen bonds on the surface of the substrate, forming a  $Cu$  or  $Cd$  spinel structure. Pastes of this type offer improved adhesion over fritted materials, and are referred to as *fritless*, *oxide-bonded*, or *molecular-bonded* materials. Fritless materials typically fire at 950 to 1000°C, which is undesirable from a manufacturing aspect. Ovens used for thick film firing degrade more rapidly and need more maintenance when operated at these temperatures for long periods of time.

A third class of materials utilizes both reactive oxides and glasses. The oxides in these materials, typically  $Zn$  or  $Ca$ , react at lower temperatures but are not as strong as copper. A lesser concentration of glass than found in fritted materials is added to supplement the adhesion. These materials, referred to as *mixed bonded systems*, incorporate the advantages of both technologies and fire at a lower temperature.

### 8.9.3 The organic binder

The organic binder is generally a thixotropic fluid that serves two purposes: it holds the active and adhesion elements in suspension until the film is fired, and it gives the paste the proper fluid characteristics for screen printing. The organic binder is usually referred to as the *nonvolatile* organic, because it does

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not evaporate but begins to burn off at about 350°C. The binder must oxidize cleanly during firing, with no residual carbon that could contaminate the film. Typical materials used in this application are ethyl cellulose and various acrylics.

For nitrogen-fireable films, in which the firing atmosphere can contain only a few ppm of oxygen, the organic vehicle must decompose and thermally depolymerize, departing as a highly volatile organic vapor in the nitrogen blanket provided as the firing atmosphere. This is because oxidation into CO<sub>2</sub> or H<sub>2</sub>O is not feasible because of the oxidation of the copper film.

**8.9.4 The solvent or thinner**

The organic binder in the natural form is too thick to permit screen printing, which requires the use of a solvent or thinner. The thinner is somewhat more volatile than the binder, evaporating rapidly above about 100°C. Typical materials used for this application are terpineol, butyl carbitol, and certain of the complex alcohols into which the nonvolatile phase can dissolve. The low vapor pressure at room temperature is desirable to minimize drying of the pastes and to maintain a constant viscosity during printing. Additionally, plasticizers, surfactants, and agents that modify the thixotropic nature of the paste are added to the solvent to improve paste characteristics and printing performance.

To complete the formulation process, the ingredients of the thick film paste are mixed together in proper proportions and milled on a three-roller mill for a sufficient period of time to ensure that they are thoroughly mixed and that no agglomeration exists.

**8.9.5 Fabrication of thick film paste**

The fabrication process begins with the materials in powder form. Gold powders formed by precipitating gold out of a chemical solution are mixed with finely divided glass powder, typically formed by quenching molten glass and grinding the resulting particles. The gold powder morphology is chosen for proper combination of density, surface area, and purity. A large surface-to-volume ratio provides a large surface free energy to drive the sintering reaction and lower the processing temperatures. The glass is formulated to wet the gold (to enhance liquid phase sintering), adhere to the specific substrate, and to act as the “glue” to hold the fired film together. The particle size, distribution, and density must also be controlled to ensure proper packing and a high exothermic reaction at melting from a large surface energy component. The proper glass/gold mixture must be chosen to ensure chemical and thermal expansion compatibility with the desired substrate throughout the firing temperatures and during the cooling-down cycle. Additionally, small additions of other metals or oxides may be mixed with the glass and gold to impart improved mechanical or electrical properties, such as the addition of copper or copper oxide for the reactive bonding to alumina or rhodium to prevent blistering in gold.

The vehicle is composed of a suitable solvent such as terpineol, xylene, or higher alcohols into which a thickening agent or gum is dissolved. Ethyl and methyl cellulose are common examples of gum thickeners. In addition, a wetting or hardening agent may be added to improve rheology or stability. For example, the surface of a dried but unfired film may be damaged if subjected to high-speed mechanical abrasion. The addition of a small amount of a film hardener eliminates this problem. High-contrast dyes can also be added to aid in automatic inspection or alignment.

The mixture is blended with a ball mill to reduce particle size of the glass frit or other brittle materials. The ball mill consists of a cylindrical container that is partly filled with a grinding media and the sample to be milled. The cylinder is rotated in a horizontal axis. The grinding medium, either tubular or spherical zirconia or  $\text{Al}_2\text{O}_3$ , cascades within the mill to produce a shear force to break down the particle size of the sample. The mill is rotated at a speed approximately 60 percent of the “critical speed,” which is the speed at which the grinding media would be held at the container wall by centrifugal force. The critical speed is given by

$$\text{Speed}_{\text{critical}} = \frac{57.8}{\sqrt{R}} \text{ rpm} \quad (8.20)$$

In a typical ball mill load, only 50 percent of the overall volume of the mill is filled, with 50 percent of the filled portion being grinding medium. Particle size analysis is performed to determine the degree of milling progress. A schematic diagram of a ball mill is shown in Fig. 8.15.

In practice, the paste components are dispersed in a three-roll mill, as depicted in Fig. 8.16. The principle of three-roll milling is based on the high

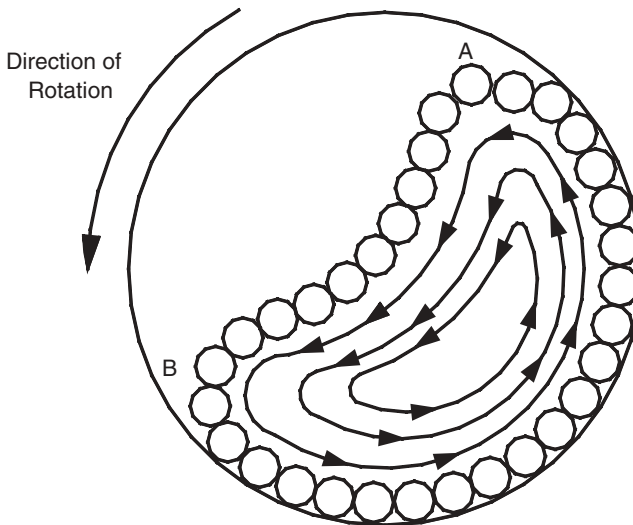
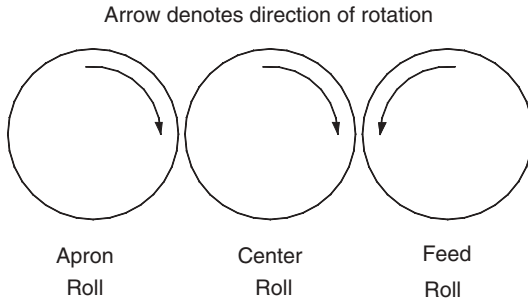


Figure 8.15 Ball mill.



**Figure 8.16** Three-roll mill.

shear force obtained in a fluid contained in the gap of a counterrotating cylinder. Material is placed between the feed roll and the center roll. Because of the narrowing space between the rolls, the majority of paste is rejected from the nap region to the feed region. However, some material will pass through the nap region, experiencing the highest shear force. After exiting the nap region, the material remaining on the center roller moves into the nap region with the apron roll, which subjects the material to higher shear forces caused by the higher speed of the apron roll. A knife blade on the apron roll removes material remaining on the apron roll. This milling process can be redone to maximize the dispersion. The gap between the rollers can be mechanically set or maintained at a constant pressure under hydraulic pressure. Typically, the gap distance (on the order of a few mils), is far greater than the average particle size. Therefore, minimal particle size milling occurs. The function of roll milling is to maximize dispersion and to remove any entrapped air.

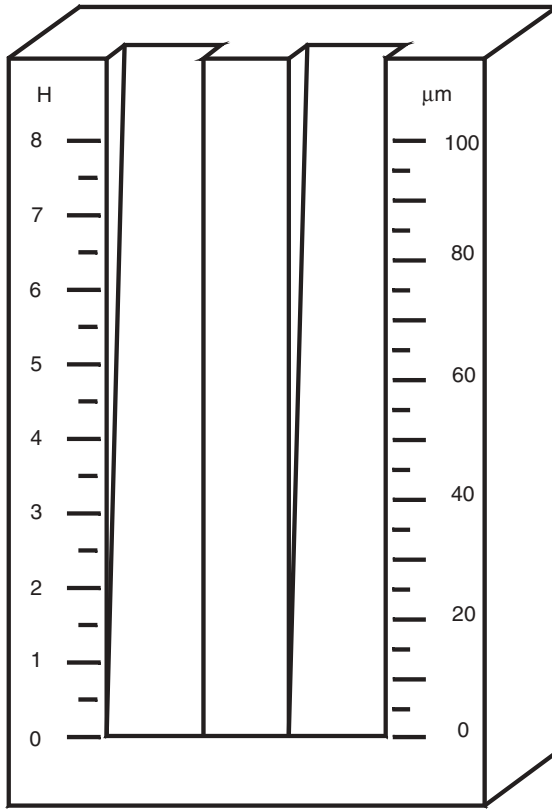
There are three important parameters that may be used to characterize a thick film paste.

- fineness of grind
- percent solids
- viscosity

### 8.9.6 Parameters of thick film paste

Fineness of grind is a measure of the particle size distribution and dispersion within the paste. A fineness-of-grind (FOG) gauge, as shown in Fig. 8.17, is a hard steel block with a tapered slot ground into one surface to a maximized depth, typically  $50\mu$ , with a micrometer scale marked along the groove. The paste is placed in the deep end and drawn down the block toward the shallow end by a tapered doctor blade. At the point where the largest particles cannot pass under the gap between the groove and the doctor blade, the film will begin to form streaks, or areas with no paste. The location of the first streak with respect to the scale denotes the largest particle, and the point where approximately half of the width of the groove is composed of streaks is the mean value of the particle size. At some point, essentially all of the particles will be trapped, which represents the smallest particle.





**Figure 8.17** Fineness-of-grind (FOG) gauge.

The percent solids parameter measures the ratio of the weight of the active and adhesion elements to the total weight of the paste. This test is performed by weighing a small sample of paste, placing it in an oven at about 400°C until all the organic material is burned away, and reweighing the sample. The percent solids parameter must be tightly controlled so as to achieve the optimal balance between printability and the density of the fired film. If the percent solids content is too high, the material will not have the proper fluid characteristics to print properly. If it is too low, the material will print well, but the fired print may be somewhat porous or may lack definition. A typical range for percent solids is 85 to 92 percent by weight. By volume, of course, the ratio is somewhat lower because of the lower density of the vehicle as compared to the active and adhesion elements.

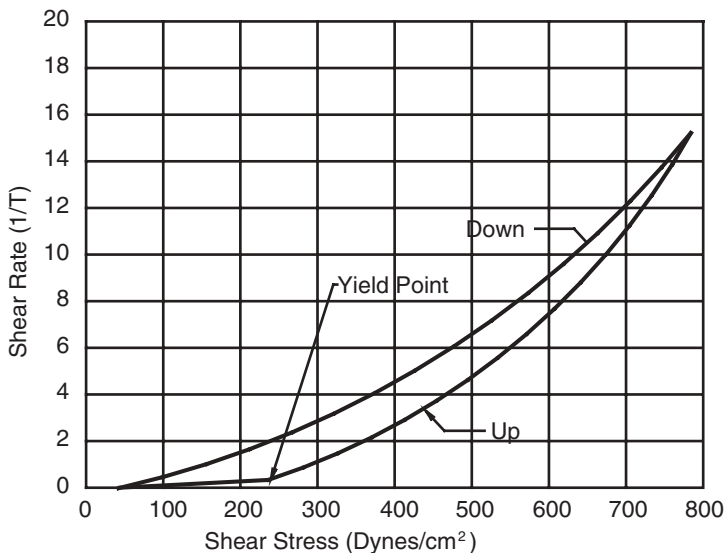
The viscosity of a fluid is a measure of the tendency of the fluid to flow and is the ratio of the shear rate of the fluid in  $\text{sec}^{-1}$  to the shear stress in force/unit area. The unit of viscosity is the poise, measured in  $\text{dynes/cm}^2\text{-sec}$ . Thick film pastes typically have the viscosity expressed in centipoise (cP), although the actual viscosity may be in the thousands of poise. An alternate unit of viscosity is the pascal-sec (Pas). One pascal-sec is equivalent to 0.001 cP.

In an ideal or “Newtonian” fluid, the relationship between shear rate and shear stress is linear, and the graph passes through the origin. Newtonian fluids are not suitable for screen printing, because the force of gravity assures that some degree of flow will always be present. As a basis for comparison, the flow properties of water approach those of Newtonian fluids.

To be suitable for screen printing, a fluid must have certain characteristics.

- The fluid must have a yield point, or minimum pressure required to produce flow, which must obviously be above the force of gravity. With a finite yield point, the paste will not flow through the screen at rest and will not flow on the substrate after printing.
- The fluid should be somewhat *thixotropic* in nature. A thixotropic fluid is one in which the shear rate /shear stress ratio is nonlinear. As the shear rate (which translates to the combination of squeegee pressure, velocity, and screen tension) is increased, the paste becomes substantially thinner, causing it to flow more readily. The corollary of this term is *pseudoplastic*. A pseudoplastic fluid is one in which the shear rate does not increase appreciably as the force is increased.
- The fluid should have some degree of hysteresis so that the viscosity at a given pressure depends on whether the pressure is increasing or decreasing. Preferably, the viscosity should be higher with decreasing pressure, as the paste will be on the substrate at the time and will have a lesser tendency to flow and lose definition.

The shear rate versus shear stress curve for a thixotropic paste with these characteristics is shown in Fig. 8.18. A third variable (time) should also be



**Figure 8.18** Typical viscosity curve for thixotropic paste.

considered in this figure. In practice, a finite and significant amount of time elapses between the application of the force and the time when the steady-state viscosity is attained. During the printing process, the squeegee velocity must be sufficiently slow to allow the viscosity of the paste to lower to the point at which printing is optimized. After the print, sufficient time must be allowed for the paste to increase to nearly the rest viscosity (leveling). If the paste is placed in the drying cycle prior to leveling, the paste will become still thinner as a result of the increased temperature, and the printed film will lose line definition.

Under laboratory conditions, the viscosity of the paste may be measured with a cone-and-plate or spindle viscometer. The cone-and-plate viscometer consists of a rotating cylinder with the end ground to a specific angle. A sample of paste is placed on a flat plate, and the cylinder is inserted into the paste parallel to the plate. The cylinder is rotated at a constant velocity, and the torque required to maintain this velocity is converted to viscosity. The spindle method utilizes a cylinder of known volume filled with paste. A spindle of known size is rotated at a constant speed inside the cylinder, and the torque measurement is converted to viscosity, as with the cone-and-plate unit. The spindle method provides a more consistent reading, because the boundary conditions can be more tightly controlled, and it is the most common method of characterizing thick film pastes in a development or manufacturing facility.

It is important to understand the limitations of viscometers for laboratory use. These are not analytical tools, in that a viscometer reading may be directly translated to the settings on the screen printer. Most viscometers of this type are designed to operate at two speeds, which would yield only two points on the curve in Fig. 8.18. This limits the utilization of the viscometer to simply compare one paste with another. When used for this purpose, the measurement conditions must be identical; the same type spindle in the same volume of paste must be used, and the sample must be at the same temperature if the correlation is to be meaningful.

Viscosity can be readily lowered by addition of an appropriate solvent. This is frequently required when the paste jar has been opened a number of times or if paste has been returned to the jar from the screen. If the original viscosity is recorded, the paste can be returned to the original viscosity with the aid of the viscometer. Increasing the viscosity is more difficult, requiring the addition of more nonvolatile vehicle followed by remilling of the paste.

Cermet thick film pastes are divided into three broad categories: conductors, resistors, and dielectrics. Each of these categories may have several sub-categories that describe materials for a specific application.

## 8.10 Thick Film Conductor Materials

Thick film conductors must perform a variety of functions in a hybrid circuit.

- The most fundamental function is to provide electrically conductive traces between the nodes of the circuit.

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- They must provide a means to mechanically mount components by solder, epoxy, or direct eutectic bonding.
- They must provide a means for the electrical interconnection of components to the film traces and to the next higher assembly.
- They must provide a means of terminating thick film resistors.
- They must provide electrical connections between conductor layers in a multilayer circuit.

Thick film conductor materials are of three basic types: air fireable, nitrogen fireable, and those that must be fired in a reducing atmosphere. Air-fireable materials are made up of noble metals that do not readily form oxides. The basic metals are gold and silver, which may be used in the pure form or alloyed with palladium and/or platinum. Nitrogen-fireable materials include copper, nickel, and aluminum, with copper being the most common. The refractory materials, molybdenum, manganese, and tungsten, are intended to be fired in a reducing atmosphere consisting of a mixture of nitrogen and hydrogen.

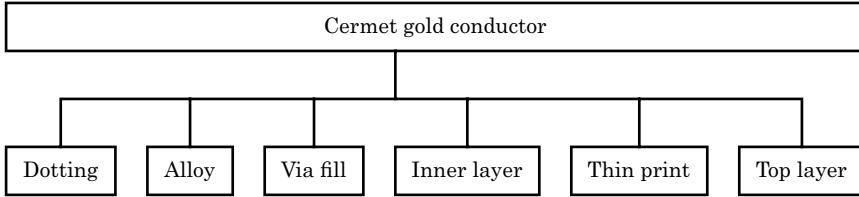
**8.10.1 Gold conductors**

Gold has many varied requirements in thick film circuits, as shown in Table 8.17. It is most often used in applications in which a high degree of reliability is required, such as military and medical applications, or wherein gold wire bonding is desirable for reasons of speed. The assembly processes (i.e., soldering, epoxy bonding, and wire bonding) used with gold thick films must be selected with care if reliability is to be maintained at a high level. For example, gold readily alloys with tin and will leach rapidly into certain of the tin-bearing solders, such as the lead-tin (Pb/Sn) alloys. Gold and tin also form brittle intermetallic compounds with a high electrical resistivity. Where Pb/Sn solders are to be used for component or lead attachment, gold must be alloyed with platinum or palladium to minimize leaching and intermetallic compound formation. Gold also forms intermetallic compounds with the aluminum that is commonly used as the contact material on semiconductor devices and for wire bonding. The diffusion coefficient of aluminum into gold is much higher than that of gold into aluminum, with the diffusion rate increasing rapidly with temperature. Consequently, when an Au-Al interface occurs, as when an aluminum wire is bonded to a gold thick film conductor, the aluminum will diffuse into the gold wire, leaving voids in the interface (Kirkendall voids) that weaken the bond strength and increase the electrical resistance. This phenomenon is accelerated at temperatures above about 170°C and represents a reliability risk. The addition of palladium alloyed with the gold lowers the rate of aluminum diffusion significantly and improves the reliability of aluminum wire bonds.

**8.10.2 Silver conductors**

Silver is often used in commercial applications where cost is a factor. Like gold, silver leaches into Pb/Sn solders, although at a slower rate. Pure silver

TABLE 8.17 Requirements for Gold in a Thick Film Circuit



may be used in applications wherein the exposure to Pb/Sn solder in the liquidus state is minimized and may also be nickel plated to further inhibit leaching.

Silver also has a tendency to migrate when an electrical potential is applied between two conductors in the presence of water in its liquid form. As shown in Fig. 8.19, positive silver ions dissolve into the water from the positive conductor. The electric field between the two conductors transports the Ag ions to the negative conductor, where they recombine with free electrons and precipitate out of the water onto the substrate as metallic silver. Over time, a continuous silver film grows between the two conductors, forming a conductive path. While other metals, including gold and lead, will migrate under the proper conditions, silver is the most notorious because of its high ionization potential.

Alloying silver with palladium and/or platinum slows down both the leaching rate and the migration rate, making it practical to use these alloys for soldering. Palladium/silver conductors are used in most commercial applications and are the most common materials found in hybrid circuits. However, the addition of palladium increases both the electrical resistance and the cost. A ratio of four parts silver to one part palladium is frequently used, providing a good compromise between performance and cost.

### 8.10.3 Copper conductors

Copper-based thick films were originally developed as a low-cost substitute for gold, but copper is now being selected when solderability, leach resistance, and low resistivity are required. These properties are particularly attractive for power hybrid circuits. The low resistivity allows the copper conductor traces to

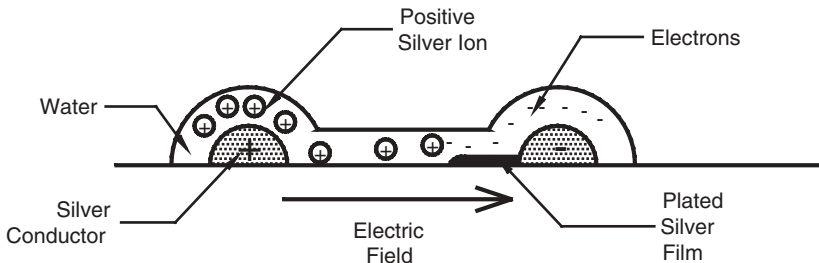


Figure 8.19 Silver migration.

handle higher currents with a lower voltage drop, and the solderability allows power devices to be soldered directly to the metallization for better thermal transfer.

Copper thick film systems are known to exhibit the following problems:

- The requirement for a nitrogen atmosphere (<10 ppm oxygen) has created problems when scaling up from a prototype effort to high-volume production. Organic materials used in air-fireable systems combine with oxygen in the furnace atmosphere and “burn” off, whereas those used in copper paste systems “boil” off (or “unzip”) and must be carried away by the nitrogen flow. It has proven difficult to maintain a consistent, uniform nitrogen blanket in the larger furnaces required for production, which has required collaboration between furnace manufacturers, paste manufacturers, and users to come up with special, innovative furnace designs for copper firing. Although some furnaces may be used for both nitrogen and air firing in prototype quantities, it is not practical to switch back and forth for production.
- Because of the large print areas normally required for dielectric materials, the problem of organic material removal is amplified when these materials are used to manufacture multilayer circuits. Consequently, multilayer dielectric materials designed to be used with copper are generally more porous than those designed for air-fireable materials, and, as a result, it has proven difficult to manufacture dielectric materials that are hermetic. This generally has required three layers of dielectric material between conductor layers to minimize short circuits and leakage, as opposed to the normal two required for air-fireable systems.
- Many resistor materials, particularly in the high ohmic range, have not proven to be as stable as air-fireable resistors when fired at temperatures below 980°C.

Refractory thick film materials, typically tungsten, molybdenum, and titanium, may also be alloyed with each other in various combinations. These materials are designed to be cofired with ceramic substrates at temperatures ranging up to 1600°C and are postplated with nickel and gold to allow component mounting and wire bonding. The properties of thick film conductors are summarized in Table 8.18.

### 8.11 Thick Film Resistor Materials

Thick film resistors are formed by mixing metal oxide particles with glass particles and firing the mixture at a temperature/time combination sufficient to melt the glass and sinter the oxide particles together. The resulting structure consists of a series of three-dimensional chains of metal oxide particles embedded in a glass matrix. The higher the metal oxide-to-glass ratio, the lower will be the resistivity of the fired film and vice versa.

Thick film resistor materials are blended approximately to Lichtenecker’s logarithmic mixing rule,

TABLE 8.18 Thick Film Conductor Capabilities

	Au wire bonding	Al wire bonding	Eutectic bonding	SN/PB solder	Epoxy bonding
Au	Y	N	Y	N	Y
Pd/Au	N	Y	N	Y	Y
Pt/Au	N	Y	N	Y	Y
Ag	Y	N	N	Y	Y
Pd/Ag	N	Y	N	Y	Y
Pt/Ag	N	Y	N	Y	Y
Pt/Pd/Ag	N	Y	N	Y	Y
Cu	N	Y	N	Y	N

$$\log R_m = V_j \sum_{j=1}^n \log R_j \quad (8.21)$$

where  $R_m$  = bulk resistivity of the mixture  
 $V_j$  = volume fraction of the individual component  
 $R_j$  = bulk resistivity of the component

Referring to Fig. 8.20, the electrical resistance of a material in the shape of a rectangular solid is given by the classic formula,

$$R = \frac{\rho_B L}{WT} \quad (8.22)$$

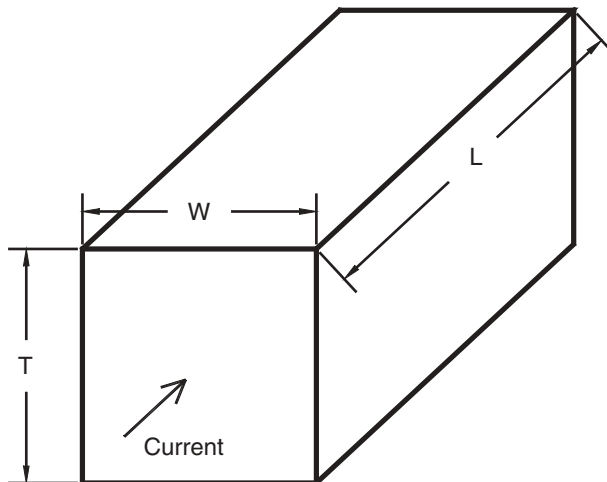


Figure 8.20 Definition of resistance.

where  $R$  = electrical resistance in ohms  
 $\rho_B$  = bulk resistivity of the material in ohms-length  
 $L$  = length of the sample in the appropriate units  
 $W$  = width of the sample in the appropriate units  
 $T$  = thickness of the sample in the appropriate units

A “bulk” property of a material is one that is independent of the dimensions of the sample.

When the length and width of the sample are much greater than the thickness, a more convenient unit to use is the “sheet” resistivity, which is equal to the bulk resistivity divided by the thickness.

$$\rho_s = \frac{\rho_B}{T} \quad (8.23)$$

where  $\rho_s$  = sheet resistivity in ohms/square/unit thickness

The sheet resistivity, unlike the bulk resistivity, is a function of the dimensions of the sample. Thus, a sample of a material with twice the thickness as another sample will have half the sheet resistivity, although the bulk resistivity is the same. In terms of the sheet resistivity, the electrical resistance is given by

$$R = \frac{\rho_s L}{W} \quad (8.24)$$

For a sample of uniform thickness, if the length is equal to the width (i.e., the sample is a square), the electrical resistance is the same as the sheet resistivity independent of the actual dimensions of the sample. This is the basis of the units of sheet resistivity, “ohms/square/unit thickness.” For thick film resistors, the standard adopted for unit thickness is 0.001 in or 25  $\mu$  of dried thickness. The dried thickness is chosen as the standard as opposed to the fired thickness for convenience in process control. The dried thickness can be obtained in minutes, whereas obtaining the fired thickness can take as much as an hour. The specific units for thick film resistors are  $\Omega/\square/0.001$  in of dried thickness, or simply  $\Omega/\square$ .

One of the difficulties in developing a conduction model has been the large number of variables that influence the conduction process, including the particle size, the particle shape, the substrate, and the type of glass. It is correspondingly difficult to manufacture thick film resistor pastes. The same ingredients mixed in the same proportions and milled in the same fashion will not always produce the same results, particularly where the TCR is concerned. When the TCR is not within specification, a modifier, usually a metal oxide, must be added and the paste remilled. For this reason, a paste with a low TCR is generally more expensive, even though it may contain the same basic ingredients as one with a higher TCR.

A group of thick film materials with identical chemistries that are blendable is referred to as a “family” and will generally have a range of values from



10  $\Omega/\square$  to 1  $M\Omega/\square$  in decade values, although intermediate values are available as well. There are both high and low limits to the amount of material that may be added. As more and more material is added, a point is reached at which there is not enough glass to maintain the structural integrity of the film. With conventional materials, the lower limit of resistivity is about 10  $\Omega/\square$ . Resistors with a sheet resistivity below this value must have a different chemistry and often are not blendable with the regular family of materials. At the other extreme, as less and less material is added, a point is reached at which there are not enough particles to form continuous chains, and the sheet resistance rises very abruptly. Within most resistor families, the practical upper limit is about 2  $M\Omega/\square$ . Resistor materials are available to about 20  $M\Omega/\square$ , but these are not amenable to blending with lower-value resistors.

The active phase for resistor formulation is the most complex of all thick film formulations because of the large number of electrical and performance characteristics required. The most common active material used in air-fireable resistor systems is ruthenium, which can appear as  $RuO_2$  (ruthenium dioxide) or  $BiRu_2O_7$  (bismuth ruthenate). With the addition of TCR modifiers, these materials can be formulated to provide a temperature coefficient of resistance [as defined in Eq. (8.33)] of  $\pm 50$  ppm with a stability of better than 1 percent after 1000 hr at 150°C.

Certain properties of thick film resistors as a function of ohmic value are predictable with qualitative conduction models.<sup>14</sup>

- High-ohmic-value resistors tend to have a more negative TCR than low-ohmic-value resistors. This is not always the case in commercially available systems, a result of the presence of TCR modifiers, but it always holds true in pure metal oxide-glass systems.
- High-ohmic-value resistors exhibit substantially more current noise than low-ohmic-value resistors as defined in MIL-STD-202. Current noise is generated when a carrier makes an abrupt change in energy levels, as it must when it makes the transition from one metal oxide particle to another across the thin film of glass. When the metal oxide particles are directly sintered together, the transition is less abrupt, and little or no noise is generated.
- High-ohmic-value resistors are more susceptible to high-voltage pulses and static discharge than are low-ohmic-value resistors. The high-voltage impulse breaks down the thin film of glass and forms a sintered contact, permanently lowering the value of the resistor. The effect of static discharge is highly dependent on the glass system used. Resistors from one manufacturer may drop by as much as half when exposed to static discharge, while others may be affected very little. This can be verified experimentally by heating a previously pulsed resistor to about 200°C. The value increases somewhat, indicating a regrowth of the glass oxide layer.

### 8.11.1 Electrical properties of thick film resistors

The electrical properties of resistors can be divided into two categories.

1. Time-zero (as-fired) properties
  - temperature coefficient of resistance (TCR)
  - voltage coefficient of resistance (VCR)
  - resistor noise
  - high-voltage discharge
2. Time-dependent (aged) properties
  - high-temperature drift
  - moisture stability
  - power handling capability

### 8.11.2 Time-zero properties

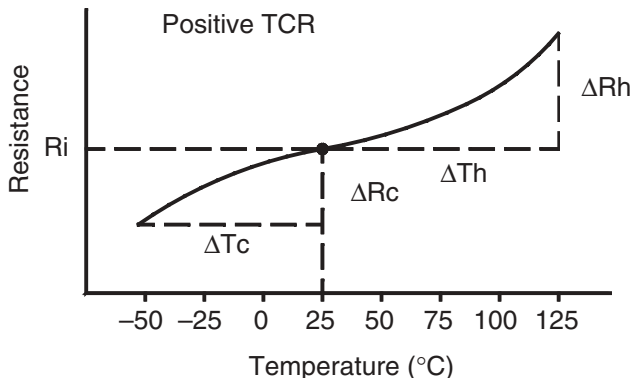
**8.11.2.1 Temperature coefficient of resistance (TCR).** Referring to Eq. (8.40), all real materials exhibit some change in resistance with temperature, and most are nonlinear to a greater or lesser degree. Figure 8.21 shows a graph of resistance versus temperature for a typical material. The TCR is a function of temperature and is defined as the slope of the curve at the test temperature,  $T$ .

$$TCR(T) = \frac{dR(T)}{dT} \quad (8.25)$$

Referring again to Fig. 8.21, the TCR is often linearized over a range of temperatures as depicted in Eq. (8.26).

$$TCR = \frac{\Delta R}{\Delta T} \quad (8.26)$$

In general, this result is a small number expressed as a decimal with several preceding zeroes. For convenience, Eq. (8.41) is typically normalized to



**Figure 8.21** Typical resistance vs. temperature curve for a thick film resistor.

the initial value of resistance and is multiplied by 1 million to produce a whole number as shown in Eq. (8.27).

$$TCR = \frac{R(T_2) - R(T_1)}{R(T_1)(T_2 - T_1)} \times 10^6 \text{ ppm/}^\circ\text{C} \quad (8.27)$$

where  $R(T_2)$  = resistance at a temperature  $T_2$   
 $R(T_1)$  = resistance at a temperature  $T_1$

Most paste manufacturers present the TCR as two values.

1. The average from 2 to 125°C (the “hot” TCR)
2. The average from 25 to –55°C (the “cold” TCR)

An actual resistor paste carefully balances the metallic, nonmetallic, and semiconducting fractions to obtain a TCR as close to zero as possible. This is not a simple task, and the “hot” TCR may be quite different from the “cold” TCR. While linearization does not fully define the curve, it is adequate for many design applications.

It is important to note that the TCR of most materials is not linear, and the linearization process is at best an approximation. For example, the actual TCR of most thick film resistor materials at temperatures below –40°C tends to drop very rapidly and may be somewhat below the linearized value. The only completely accurate method of describing the temperature characteristics of a material is to examine the actual graph of temperature versus resistance. The TCR for a material may be positive or negative. By convention, if the resistance increases with increasing temperature, the TCR is positive. Likewise, if the resistance decreases with increasing temperature, the TCR is negative.

In general, metals exhibit positive TCRs, and nonmetals exhibit negative TCRs. In metals, the electron cloud is more disordered with increasing thermal energy, and resistance increases. Nonmetals (or semiconductors), which have electrons firmly bonded to crystal locations, become more mobile with energy and are better conductors as temperature is increased. They have a negative TCR.

While the absolute TCR of a resistor is critical to the operation of an electronic circuit, in some cases, the ratio of resistance change between two resistors is even more important. For example, assume that two resistors with a value of 1 kΩ have TCRs of +75 ppm and –40 ppm, respectively, at 0°C. After a change in temperature of +100°C, the respective values of resistance would be 1008 Ω and 996 Ω. The ratio of these two resistors at 100°C is

$$\frac{R_1}{R_2} = \frac{1008}{996} = 1.012$$

which translates to a net TCR of 115 ppm/°C, or the algebraic difference of the TCRs of the individual resistors.

Now consider that the TCRs of the two resistors are 200 ppm/°C and 175 ppm/°C, substantially higher in magnitude than the previous example. For this case,  $R_1 = 1020 \Omega$  and  $R_2 = 1018 \Omega$  at 100°C, and the ratio is

$$\frac{R_1}{R_2} = \frac{1020}{1018} = 1.002$$

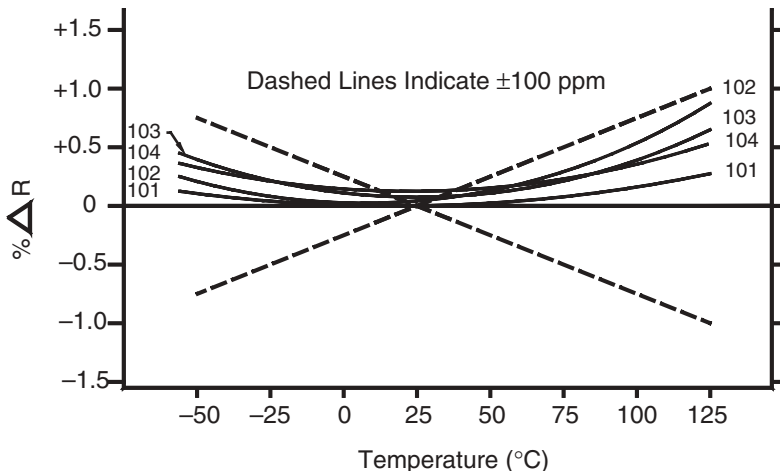
which is equivalent to a TCR of only 24.6 ppm/°C for the ratio.

It is therefore possible to have low TCR tracking with high absolute TCR if both resistors move in the same direction with temperature variations. In many circuit designs, this parameter is more important than a low absolute TCR. Following these guidelines can enhance the TCR tracking of two resistors:

- Resistors made from the same value paste will track more closely than resistors made from different decades.
- Resistors of the same length will track more closely than resistors of different lengths.
- Resistors printed with the same thickness will track more closely than resistors of different thicknesses.

Typical TCRs for decade values of thick film paste are shown in Fig. 8.22.

**8.11.2.2 Voltage coefficient of resistance (VCR).** Certain resistor materials also exhibit sensitivity to high voltages or, more specifically, to high electric fields as defined in Eq. (8.28). Note that the form of this equation is very similar to that of the TCR.



**Figure 8.22** Typical TCR of resistor paste decades.

$$VCR = \frac{R(V_2) - R(V_1)}{R(V_1)(V_2 - V_1)} \times 10^6 \text{ ppm/V} \quad (8.28)$$

where  $R(V_1)$  = resistance at  $V_1$   
 $R(V_2)$  = resistance at  $V_2$   
 $V_1$  = voltage at which  $R(V_1)$  is measured  
 $V_2$  = voltage at which  $R(V_2)$  is measured

Because of the semiconducting component in resistor pastes, the VCR is invariably negative. That is, as  $V_2$  is increased, the resistance decreases. Also, because higher resistor decade values contain more glass and oxide constituents and are more semiconducting, higher paste values tend to have more negative VCRs than lower values.

Finally, the VCR is dependent on resistor length. The voltage effect on a resistor is a gradient, and it is the volts/unit length rather than the absolute voltage that causes resistor shift. Therefore, long resistors show less voltage shift than short resistors, for similar compositions and voltage stress. Typical VCRs of thick film resistors are shown in Fig. 8.23.

**8.11.2.3 Resistor noise.** On a fundamental level, noise occurs when an electron is moved to a higher or lower energy level. The greater the potential difference between the energy levels, the greater the noise. Metals with many available electrons in the “electron cloud” have low noise, whereas semiconducting materials have fewer free electrons and exhibit higher noise.

There are two primary noise sources present in thick film resistors: thermal, or “white” noise, and current, or “pink” noise. The thermal noise is gener-

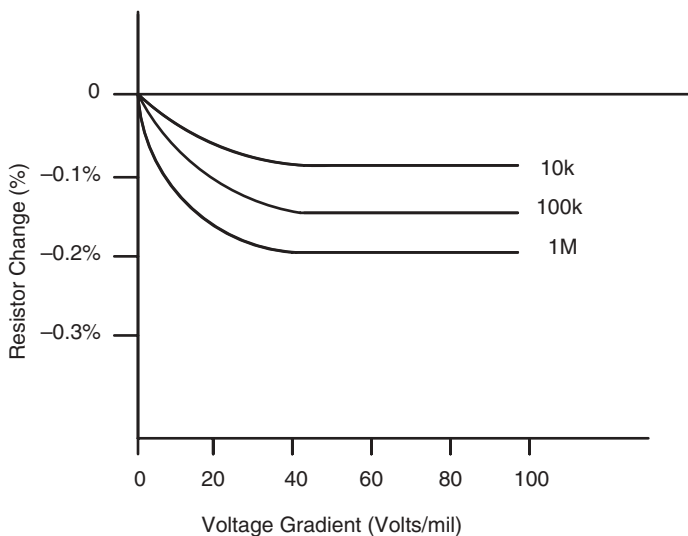


Figure 8.23 Typical VCR of resistor paste decades.

ated by the random transitions between energy levels as a result of heat and is present to some degree in all materials. Current noise occurs as a result of a transition between boundaries in a material, such as grain boundaries, where the energy levels may undergo abrupt changes from one region to another. In thick film resistors, the prime source of current noise is the thin layer of glass that may exist between the active particles.

The frequency spectrum of thermal noise is independent of frequency and is expressed in dB/Hz. The total noise is calculated by multiplying the noise figure by the bandwidth of the system. Current noise, on the other hand, has a frequency spectrum proportional to the inverse of the frequency, or  $1/f$ , and is expressed in units of dB/decade. The level of current noise in most applications is insignificant after the frequency exceeds 10 to 20 kHz.

In applications in which the noise level is of significance, these guidelines may help to improve performance:

- High-value resistors exhibit a higher noise level than low-value resistors.
- Large-area resistors exhibit a lower noise level.
- Thicker resistors exhibit a lower noise level.

Noise information is particularly important for low-signal applications as well as a quality check on processing. A shift in noise index, with constant resistor value, geometry, and termination, indicates a process variation that must be investigated. For example, thin or underfired resistors generate higher noise than normal. The conductor–resistor interface can also be an important noise generator if it is glassy or otherwise imperfect. Finally, poor or incomplete resistor trimming also generates higher noise. A resistor noise test is an excellent method of measuring a resistor attribute that is not easily obtained by other methods. Typical noise characteristics of thick film resistors are shown in Fig. 8.24.

### 8.11.3 Time-dependent properties

**8.11.3.1 High-temperature drift.** Thick film resistors in the untrimmed state exhibit a slight upward drift in value, primarily as a result of stress relaxation in the glasses that make up the body of the resistor. In properly processed resistors, the magnitude of the drift over the life of the resistor is measured in fractions of a percent and is not significant for most applications. At high temperatures, however, the drift is accelerated and may affect circuit performance in resistors that have not been properly fired or terminated or that are incompatible with the substrate.

To characterize the drift parameters, accelerated testing is frequently performed. A standard test condition is 125°C for 1000 hr at normal room humidity, corresponding to test condition S of MIL-STD-883C, method 1005.4 This test is considered to be equivalent to end-of-life conditions. More aggressive testing conditions are 150°C for 1000 hr or 175°C for 40 hr.

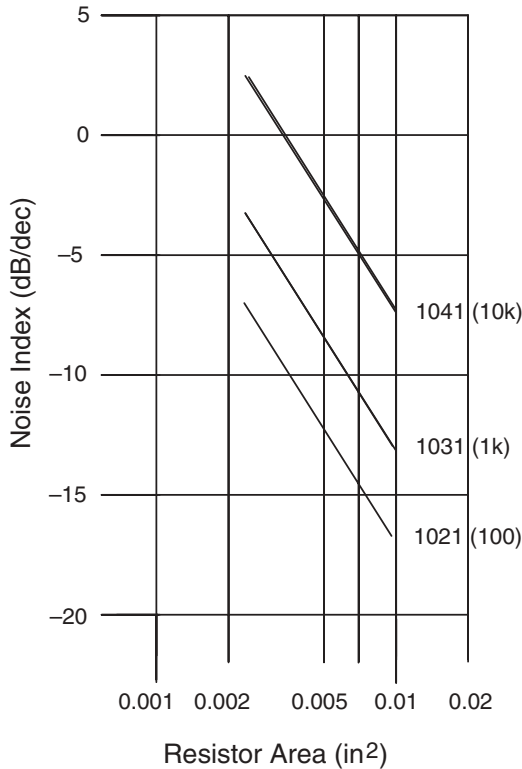
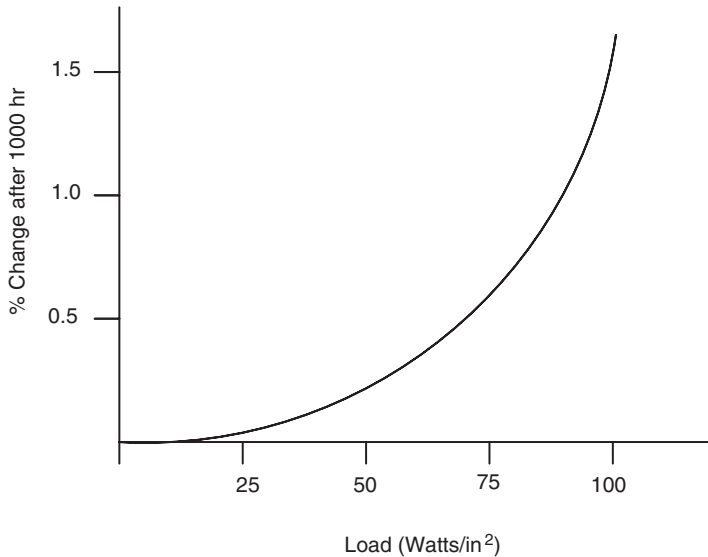


Figure 8.24 Effect of resistor area on noise level.

**8.11.3.2 Moisture stability.** Resistance drift in the presence of moisture is a discriminating and important test. The most common test condition is 85 percent relative humidity and 85°C. Past studies indicate that this condition accelerates failure in thick film circuits by a factor of almost 500, compared to normally stressed circuits in the field. Humidity testing of resistors and circuits is more expensive than simple heat aging, but all the evidence indicates that it is a good predictor of reliability.

**8.11.3.3 Power-handling capability.** Drift resulting from high power is primarily caused by internal resistor heating. It is different from thermal aging in that the heat is generated at the point-to-point metal contacts within the resistor film. When a resistor is exposed to elevated temperature, the entire bulk of the resistor is uniformly heated. Under power, local heating can be much greater than the surrounding area. Because lower-value resistors have more metal and, therefore, many more contacts, low-value resistors tend to drift less than higher-value resistors under similar loads. For most resistor systems, the shape of the power aging curve is a “rising exponential” as shown in Fig. 8.25.



**Figure 8.25** Load life of a typical thick film resistor under extreme power stress.

The most generally accepted power rating of thick film resistors to achieve a drift of less than 0.5 percent over the resistor life is 50 W/in<sup>2</sup> of active resistor area. If more drift can be tolerated, the resistor can be rated at up to 200 W/in<sup>2</sup>, as catastrophic failure will not occur until this rating is exceeded by a factor of several times. Typical properties of thick film resistors are shown in Table 8.19.

**TABLE 8.19** Typical Characteristics of Thick Film Resistors

Parameter	Value*
Tolerances, as fired	±10–20%
Tolerances, laser trimmed	±0.5–1.0%
TCRs (–55 to +125°C)	
5 to 100 kΩ/□	±100–150 ppm/°C
100 kΩ/□ to 10 MΩ/□	±150–750 ppm/°C
Resistance drift after 1000 hr at 150°C, no load	±0.3%
Resistance drift after 1000 hr at 85°C, with 25 W/in <sup>2</sup>	0.25–0.3%
Resistance drift, short-term overload (2.5 times rated voltage)	<0.5%
Voltage coefficient	–20 ppm/V-in
Noise (Quan-tech)	
100 Ω/□	–30 to –20 dB
100 Ω/□	0 to +20 dB
Power rating	40–50 W/in <sup>2</sup>

\*Selected materials may exceed these ratings.



#### 8.11.4 Process considerations for thick film resistors

The process windows for printing and firing thick film resistors are extremely critical in terms of both temperature control and atmosphere control. Small variations in temperature or time at temperature can cause significant changes in the mean value and distribution of values. In general, the higher the ohmic value of the resistor, the more dramatic will be the change. As a rule, high ohmic values tend to decrease as temperature and/or time is increased, while very low values ( $<100 \Omega/\square$ ) may tend to increase.

Thick film resistors are very sensitive to the firing atmosphere. For resistor systems used with air-fireable conductors, it is critical to have a strong oxidizing atmosphere in the firing zone of the furnace. In a neutral or reducing atmosphere, the metallic oxides composing the active material will reduce to pure metal at the temperatures used to fire the resistors, dropping resistor values sometimes by more than an order of magnitude. Again, high-ohmic-value resistors are more sensitive than low-ohmic-value devices. Atmospheric contaminants, such as vapors from hydrocarbons or halogenated hydrocarbons, will break down at firing temperatures, creating a strong reducing atmosphere. For example, one of the breakdown components of hydrocarbons is carbon monoxide, one of the strongest reducing agents known. Concentrations of fluorinated hydrocarbons in a firing furnace of only a few ppm can drop the value of a 100 k $\Omega$  resistor to below 10 k $\Omega$ . As a rule of thumb, no solvents, halogenated or carbon based, should be permitted in the vicinity of a furnace used to fire thick film materials.

### 8.12 Thick Film Dielectric Materials

Thick film dielectric materials are used primarily as insulators between conductors, either as simple crossovers or in complex multilayer structures. Small openings, or vias, may be left in the dielectric layers so that adjacent conductor layers may interconnect. In complex structures, as many as several hundred vias per layer may be required. In this manner, complex interconnection structures may be created. Although the majority of thick film circuits can be fabricated with only three layers of metallization, others may require several more. If more than three layers are required, the yield begins dropping dramatically with a corresponding increase in cost.

Dielectric materials used in this application must be of the devitrifying or recrystallizable type. These materials in the paste form are a mixture of glasses that melt at a relatively low temperature. During firing, when they are in the liquid state, they blend together to form a uniform composition with a higher melting point than the firing temperature. Consequently, on subsequent firings, they remain in the solid state, which maintains a stable foundation for firing sequential layers. By contrast, vitreous glasses always melt at the same temperature and would be unacceptable for layers to either “sink” and short to conductor layers underneath or “swim” and form an open circuit. Additionally, secondary loading of ceramic particles is used to enhance devitrification and to modify the temperature coefficient of expansion (TCE).

Dielectric materials have two conflicting requirements in that they must form a continuous film to eliminate short circuits between layers. At the same time, they must maintain openings as small as 0.010 in. In general, dielectric materials must be printed and fired twice per layer to eliminate pinholes and prevent short circuits between layers.

The TCE of thick film dielectric materials must be as close as possible to that of the substrate to avoid excessive bowing, or warpage, of the substrate after several layers. Excessive bowing can cause severe problems with subsequent processing, especially if the substrate must be held down with a vacuum or if it must be mounted on a heated stage. In addition, the stresses created by the bowing can cause the dielectric material to crack, especially if it is sealed within a package. Thick film material manufacturers have addressed this problem by developing dielectric materials that have an almost exact TCE match with alumina substrates. Where a serious mismatch exists, matching layers of dielectric must be printed on the bottom of the substrate to minimize bowing, which obviously increases the cost. The effects of a TCE mismatch for two different dielectrics, one recrystallizable and one specially formulated to match the TCE of alumina, are shown in Table 8.20.

**TABLE 8.20 Substrate Bowing (%) vs. Number of Layers**

Dielectric	Number of layers			
	2	4	6	8
Two crystalline fillers	0.6	0.8	1.2	2.4
Recrystallizable	1.6	5.5	—	—

Dielectric materials with higher dielectric constants are also available for manufacturing thick film capacitors. These generally have a higher loss tangent than chip capacitors and utilize a great deal of space. While the initial tolerance is not good, thick film capacitors can be trimmed to a high degree of accuracy.

Another consideration for selecting a thick film dielectric is the compatibility with a resistor system. As circuits become more complex, the necessity of printing resistors on dielectric as opposed to directly on the substrate becomes greater. In addition, it is difficult to print resistors on the substrate in the proximity of dielectric several dielectric layers. The variations in the thickness affect the thickness of the substrate and, therefore, affect the spread of the resistor values.

### 8.13 Overglaze Materials

Dielectric overglaze materials are vitreous glasses designed to fire at a relatively low temperature, usually around 550°C. They are designed to provide mechanical protection to the circuit, to prevent contaminants and water from

spanning the area between conductors, to create solder dams, and to improve the stability of thick film resistors after trimming.

Noble metals, such as gold and silver, are somewhat soft by nature. Gold, in particular, is the most malleable of all metals. When subjected to abrasion or to scraping by a sharp object, the net result is likely to be a bridging of the metal between conductors, resulting in a short circuit. A coating of overglaze can minimize the probability of damage and can also protect the substrates when they are stacked during the assembly process.

Contaminants that are ionic in nature, combined with water in the liquid form, can accelerate metal migration between two conductors. An overglaze material can help to limit the amount of contaminant actually contacting the surface of the ceramic and can help to prevent a film of water from forming between conductors. A ceramic substrate is a very “wetable” surface in that it is microscopically very rough, and the resulting capillary action causes the water to spread rapidly, creating a continuous film between conductors. A vitreous glass, being very smooth by nature, causes the water to “bead up,” much like on a waxed surface, helping to prevent the water from forming a continuous film between conductors, thereby inhibiting the migration process.

When soldering a device with many leads, it is imperative that the volume of solder under each lead be the same. A well designed overglaze pattern can prevent the solder from wetting other circuit areas and flowing away from the pad, keeping the solder volume constant. In addition, overglaze can help to prevent solder bridging between conductors.

Overglaze material has long been used to stabilize thick film resistors after laser trim. In this application, a green or brown pigment is added to enhance the passage of an yttrium-aluminum-garnet (YAG) laser beam. Colors toward the shorter-wavelength end of the spectrum, such as blue, tend to reflect a portion of the YAG laser beam and reduce the average power level at the resistor. There is some debate as to the effectiveness of overglaze in enhancing the resistor stability, particularly with high ohmic values. Several studies have shown that, although overglaze is undoubtedly helpful at lower values, it can actually increase the resistor drift of high-value resistors by a significant amount.

## 8.14 Screen Printing

Three fundamental processes are required to produce a thick film circuit; screen printing, drying, and firing. The screen printing process applies the paste to the substrate, the drying process removes the volatile solvents from the paste before firing, and the firing process activates the adhesion mechanism, adhering the print to the substrate.

Thick film paste is applied to the substrate by screen printing through a stainless steel mesh screen. During the design process, artwork corresponding to each of the individual layers is generated. These artworks are used to expose a screen coated with a photosensitive material, or *emulsion*, to generate the pattern. The emulsion not protected by the dark areas of the film is hardened by the UV light, and the protected portions may be simply washed away

with water, leaving openings in the emulsion corresponding to the dark areas in the film.

Commercial screen printers are designed to hold the screen parallel to and in proximity with the substrate. A squeegee is used to provide the force necessary to force the paste through the openings onto the substrate. The process sequence is as follows:

- The screen is placed in the screen printer
- The substrate is placed directly under the screen
- Paste is applied to the top of the screen

The squeegee is activated and travels across the surface of the screen, forcing the paste through the openings onto the substrate. In this manner, the paste can be applied in very precise geometries, allowing complex interconnection patterns to be generated.

Screen printing has been used for thousands of years to generate designs. In ancient China, silk was one of the first materials used as a mesh. A pattern was created in the silk using pitch or similar materials to block out unwanted areas, and dye was forced through the pattern by hand onto cloth or other surfaces to create colored patterns. By performing several sequential screenings with different colors and patterns, complex decorative patterns could be formed.

Silk continued to be one of the most common materials used until the development of synthetic materials, and the term “silk screening” is still commonly used to describe the screen printing process. The development of synthetic fibers, such as nylon, made possible greater control of the mesh materials, and the added development of photosensitive materials used for creating the patterns allowed screen printing to become much more precise, repeatable, and controllable.

Today, in the hybrid microelectronics industry, the primary mesh material is stainless steel, which adds an additional degree of control and precision over nylon in addition to added resistance to wear and stretching. The crude hand methods of printing have evolved to sophisticated, microprocessor-controlled machines that are self-aligning, have the ability to measure the thickness of the film, and have the ability to adjust the printing parameters to compensate for variations in the properties of the paste.

Still, of all the processes used to manufacture thick film hybrid microcircuits, the screen printing process is the least analytical. Because of the large number of variables involved, it is not possible to measure the parameters of the paste and convert them to the proper printer settings to produce the desired results. Many of the variables are not in the direct control of the process engineer and may change as the printing process proceeds. For example, the viscosity of the paste may change during printing because of solvent evaporation.

There are two basic methods of screen printing: the contact process and the off-contact process. In the contact process, the screen remains in contact with the substrate during the print cycle and then is separated abruptly by either lowering the substrate or raising the screen. In the off-contact process, the

screen is separated from the substrate by a small distance and is stretched by the squeegee until it contacts the substrate only at a point directly under the squeegee. Once the squeegee passes, the screen “snaps back,” leaving the paste on the substrate. In general, the best line definition is obtained with the off-contact process, and most printing of thick film pastes is performed in this manner. The contact process is generally used when a stencil is utilized to print solder paste. The stencil, being solid metal, cannot be stretched continually in the same manner as a screen without permanent deformation.

In the printing process, the paste is applied to the screen, and the squeegee is activated, sweeping across the screen. The pressure from the squeegee forces the paste through the openings in the screen onto the substrate. The rough substrate surface creates somewhat more surface tension than does the smooth wires of the screen mesh, causing the paste to stay on the substrate when the squeegee passes. The process is facilitated by the thixotropic nature of the paste. As the squeegee applies force to the paste, it becomes thinner and flows more readily. As the squeegee passes, the paste becomes thicker again and retains the line definition on the substrate.

### 8.15 Drying Thick Film Paste

Two organic components compose the vehicle in the printed film: the volatile component and the nonvolatile component. Immediately after printing, thick film materials are simply discrete particles of glass or metal suspended in a thickened vehicle and are somewhat tacky and fragile. The volatile component must be removed at a low temperature prior to firing. The volatile solvents evaporate rapidly at temperatures above 100°C and may cause extreme voiding of the fired film if exposed to elevated temperatures.

After printing, parts are usually allowed to “level” in air for a period of time (usually, 5 to 15 min). The leveling process permits screen mesh marks to fill in and some of the more volatile solvents to evaporate slowly at room temperature. The leveling process is critical to the precision of the fired film. The viscosity drops considerably during the printing process as a result of the thixotropic nature of the paste. Immediately after printing, the viscosity is still quite low and requires a period of time to return to a higher viscosity before drying. If the film is exposed to elevated temperatures immediately after printing, the viscosity will drop still lower, and the paste may spread across the substrate, degrading the definition of the printed film.

After leveling, the parts are force dried at temperatures ranging from 70 to 150°C for about 15 min. Drying is usually accomplished in a low-temperature, moving-belt dryer. For smaller or laboratory operations, drying may be accomplished in batch, forced-air dryers or even by placing the substrates on a hot-plate. In a production environment, it is important to have an exhaust system to remove the solvent vapor from the environment. Certain of the solvents have a strong odor and may also adversely affect the atmosphere in a firing furnace if allowed to remain in the immediate area.

There are two important considerations in drying: the cleanliness of the atmosphere and the drying rate. Drying must be accomplished in a clean room

(<Class 100,000) to prevent dust and lint particles from accumulating in the dried film. During firing, the particles will burn away, leaving voids in the film. The rate of temperature rise during the drying process must be controlled to prevent cracking of the film as a result of rapid solvent evaporation.

Drying removes the most volatile fraction of the paste. Perhaps 90 percent of the solvents and gums are removed in the drying step. Such solvents may be terpeneol, butyl carbitol, higher alcohols such as decanol and octanol, or xylene. Because of the potentially toxic nature of these solvents, drying must be carried out under a hood or other extraction device. Because each paste system has its own solvents, gums, and wetting agents, the paste manufacturer will recommend the exact drying schedule for their materials.

### 8.16 Firing Thick Film Paste

After drying, the parts are placed on a moving belt or conveyor furnace. As with the drying profile, each paste manufacturer develops precise profiles for its products and should be consulted for the most current information.

A thick film furnace must provide the following:

1. A clean furnace environment
2. A uniform and controllable temperature profile
3. A uniform and controllable atmosphere

To provide for both a clean environment and a controllable atmosphere, all modern thick film furnaces have impervious muffles. Both metal and quartz muffles are used, and both are satisfactory when properly designed. Larger production furnaces and multi-atmosphere furnaces all must use metal muffles (usually Inconel), because a large cross section of impervious quartz is too expensive to fabricate. Thick film furnaces are designed to operate under 1000°C, and resistive heated furnaces use wound nichrome heating elements.

In some designs, traditional firebrick insulation has been replaced with lightweight foam insulation. Lightweight insulation has many advantages over heavy brick. Because lightweight insulation does not absorb moisture to the same extent as brick, the furnace may be turned off if not being used. This is not recommended with brickwork furnaces, because the evaporating steam will damage the bricks. Given the high cost of electricity in many parts of the country today, the ability to shut a furnace down if it is not being used offers a tremendous cost saving. Conversely, in the case of brickwork furnaces, the furnace may be “banked” to a somewhat lower temperature if not being used, but it must not be turned off.

Lightweight insulation, by nature, has lower thermal mass and responds to temperature changes more rapidly than brick. In fact, it can be integrated with the heating elements, making it is possible to use a single furnace for two or more profiles. A traditional furnace could take up to 12 hr to stabilize from an 850 to a 600°C profile. A furnace made with foam or fiber insulation can stabilize in one or two hours.

## 8.17 Thick Film—Summary

It is apparent that cermet thick film materials are complex structurally and electrically. More than 120 variables related to material properties and processes have been identified with thick film resistors alone. Clearly, it is impossible to control all these variables in a manufacturing environment. To achieve the best results, it is important that the user know how the various constituents interact and the role each plays in the final product. Although the user need not know all the ingredients making up a particular paste, it is critical that the degree of compatibility with other pastes to be used in the circuit be assured. Very few hybrid circuits can be made with only one thick film paste, and if one or more of the pastes are incompatible with the others, unexpected reactions can occur that result in circuit failure. Usually, the only source of information, other than direct experimentation, is the paste manufacturer. A close working relationship with the manufacturer is a vital element toward creating a successful operation.

## 8.18 Thin Film Technology

The thin film technology, in contrast to the thick film technology, is a subtractive technology in that the entire substrate is coated with several layers of metallization, and the unwanted material is etched away in a succession of photoetching processes. The use of photolithographic processes to form the patterns enables much narrower and more precisely defined lines than can be formed by the thick film process. This feature promotes the use of the thin film technology for high-density and high-frequency applications.

Thin film circuits typically consist of three layers of material deposited on a substrate as shown in Fig. 8.26. The bottom layer serves two purposes: it is the resistor material, and it provides the adhesion to the substrate. The middle layer acts as an interface between the resistor layer and the conductor layer, either by improving the adhesion of the conductor or by preventing diffusion of the resistor material into the conductor. The top layer acts as the conductor layer.

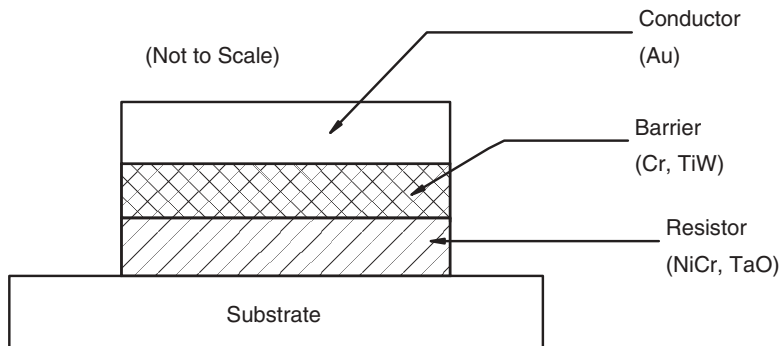


Figure 8.26 Thin film structure.

## 8.19 Deposition Technology

The term *thin film* refers more to the manner in which the film is deposited onto the substrate than to the actual thickness of the film. Thin films may be deposited by one of the vacuum deposition techniques or by electroplating.

### 8.19.1 Sputtering

Sputtering is the prime method by which thin films are applied to substrates. In ordinary triode sputtering, as shown in Fig. 8.27, a current is established in a conducting plasma formed by striking an arc in a partial vacuum of approximately  $10^{-6}$  pressure. The gas used to establish the plasma is typically an inert gas, such as argon, that does not react with the target material. The substrate and a target material are placed in the plasma with the substrate at ground potential and the target at a high potential, which may be AC or DC. The high potential attracts the gas ions in the plasma to the point at which they collide with the target with sufficient kinetic energy to dislodge microscopically sized particles with enough residual kinetic energy to travel the distance to the substrate and adhere.

The adhesion mechanism of the film to the substrate is an oxide layer that forms at the interface. The bottom layer must therefore be a material that oxidizes readily. The adhesion is enhanced by presputtering the substrate surface by random bombardment of argon ions prior to applying the potential to the target. This process removes several atomic layers of the substrate sur-

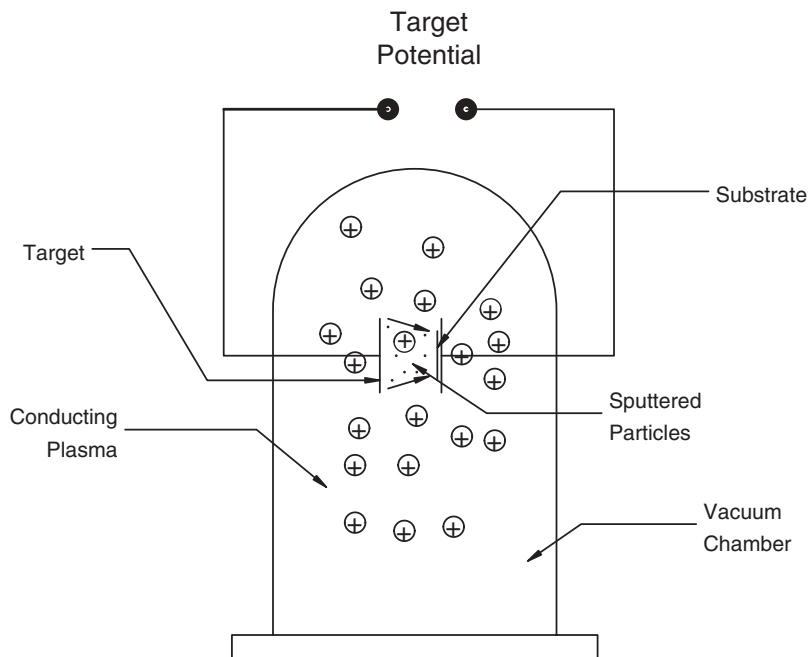


Figure 8.27 Triode sputtering.



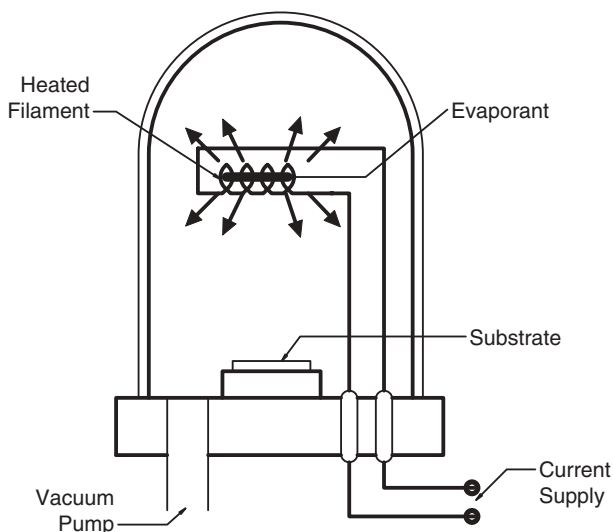
face, creating a large number of broken oxygen bonds and promoting the formation of the oxide interface layer. The oxide formation is further enhanced by the residual heating of the substrate that results from the transfer of the kinetic energy of the sputtered particles to the substrate when they collide.

Ordinary triode sputtering is a very slow process, requiring hours to produce usable films. By utilizing magnets at strategic points, the plasma can be concentrated in the vicinity of the target, greatly speeding up the deposition process. The potential applied to the target is typically RF energy at a frequency of approximately 13 MHz. The RF energy may be generated by a conventional electronic oscillator or by a magnetron. The magnetron is capable of generating considerably more power with a correspondingly higher deposition rate.

By adding small amounts of other gases, such as oxygen and nitrogen, to the argon, it is possible to form oxides and nitrides of certain target materials on the substrate. This technique, called *reactive sputtering*, is used to form tantalum nitride, a common resistor material.

### 8.19.2 Evaporation

The evaporation of a material into the surrounding area occurs when the vapor pressure of the material exceeds the ambient pressure, and it can take place from either the solid state or the liquid state. In the thin film process, the material to be evaporated is placed in the vicinity of the substrate and heated until the vapor pressure of the material is considerably above the ambient pressure as depicted in Fig. 8.28. The evaporation rate is directly proportional to the difference between the vapor pressure of the material and the ambient pressure and is highly dependent on the temperature of the material.



**Figure 8.28** The evaporation process.

Evaporation must take place in a relatively high vacuum ( $<10^{-6}$  torr) for three reasons.

1. To lower the vapor pressure required to produce an acceptable evaporation rate, thereby lowering the required temperature required to evaporate the material.
2. To increase the mean free path of the evaporated particles by reducing the scattering due to gas molecules in the chamber. Furthermore, the particles tend to travel in more of a straight line, improving the uniformity of the deposition.
3. To remove atmospheric contaminants and components, such as oxygen and nitrogen, that might tend to react with the evaporated film.

At  $10^{-6}$  torr, a vapor pressure of  $10^{-2}$  torr is required to produce an acceptable evaporation rate. A list of common materials, their melting points, and the temperature at which the vapor pressure is  $10^{-2}$  torr are shown in Table 8.21.

**TABLE 8.21 Melting Points and  $P_v = 10^{-2}$  Torr Temperatures of Selected Metals Used in Thin Film Applications**

Temperature	Melting point (°C)	Temperature at which $P_v = 10^{-2}$ torr (°C)
Aluminum	659	1220
Chromium	1900	1400
Copper	1084	1260
Germanium	940	1400
Gold	1063	1400
Iron	1536	1480
Molybdenum	2620	230
Nickel	1450	1530
Platinum	1770	2100
Silver	961	1030
Tantalum	3000	3060
Tin	232	1250
Titanium	1700	1750
Tungsten	3380	3230

The “refractory” metals (metals with a high melting point), such as tungsten, titanium, and molybdenum, are frequently used as carriers or “boats” to hold other metals during the evaporation process. To prevent reactions with the metals being evaporated, the boats may be coated with alumina or other ceramic materials.

If it is assumed that the evaporation takes place from a point source, the density of the evaporated particles assumes a cosine distribution from the normal as shown in Fig. 8.29. The distance of the substrate from the source then becomes a compromise between deposition uniformity and deposition rate; if the substrate is closer (farther away), the deposition is greater (lesser), and the deposition is less (more) uniform over the face of the substrate.

In general, the kinetic energy of the evaporated particles is substantially less than that of sputtered particles. This requires that the substrate be heated to about 300°C to promote the growth of the oxide adhesion interface. This may be accomplished by direct heating of the substrate mounting platform or by radiant infrared heating.

There are several techniques by which evaporation can be accomplished. The two most common of these are resistance heating and electron-beam (E-beam) heating.

Evaporation by resistance heating usually takes place from a boat made with a refractory metal, a ceramic crucible wrapped with a wire heater, or a wire filament coated with the evaporant. A current is passed through the element, and the heat generated heats the evaporant. It is somewhat difficult to monitor the temperature of the melt by optical means because of the propensity of the evaporant to coat the inside of the chamber, and control must be done by empirical means. Closed-loop systems exist that can control the deposition rate and the thickness, but these are quite expensive. In general, adequate results can be obtained from the empirical process if proper controls are used.

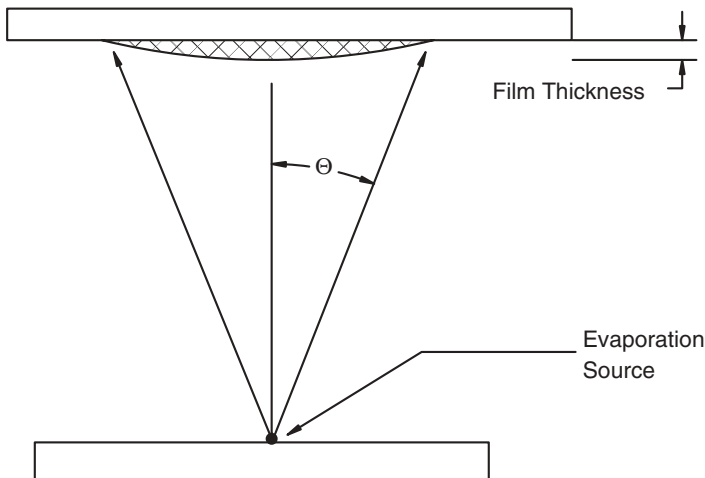


Figure 8.29 Evaporation from a point source.

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The E-beam evaporation method takes advantage of the fact that a stream of electrons accelerated by an electric field tends to travel in a circle when entering a magnetic field. This phenomenon is utilized to direct a high-energy stream of electrons onto an evaporant source. The kinetic energy of the electrons is converted into heat when they strike the evaporant. E-beam evaporation is somewhat more controllable, because the resistance of the boat is not a factor, and the variables controlling the energy of the electrons are easier to measure and control. In addition, the heat is more localized and intense, making it possible to evaporate metals with higher  $10^{-2}$  torr temperatures and lessening the reaction between the evaporant and the boat.

**8.19.3 Comparison between sputtering and evaporation**

Evaporation allows a rapid deposition rate, but there are certain disadvantages as compared with sputtering.

1. It is difficult to evaporate alloys such as NiCr because of the difference between the  $10^{-2}$  torr temperatures. The element with the lower temperature tends to evaporate somewhat faster, causing the composition of the evaporated film to be different from the composition of the alloy. To achieve a particular film composition, the composition of the melt must contain a higher portion of the material with the higher  $10^{-2}$  torr temperature, and the temperature of the melt must be tightly controlled. By contrast, the composition of a sputtered film is identical to that of the target.
2. Evaporation is limited to the metals with lower melting points. Refractory metals and ceramics are virtually impossible to deposit by evaporation.
3. Reactive deposition of nitrides and oxides is very difficult to control.

**8.19.4 Electroplating**

Electroplating is accomplished by applying a potential between the substrate and the anode, which are suspended in a conductive solution of the material to be plated. The plating rate is a function of the potential and the concentration of the solution. In this manner, most metals can be plated to a conducting surface.

In the thin film technology, it is a common practice to sputter a film of gold that is only a few angstroms ( $\text{\AA}$ ) thick and to build up the thickness of the gold film by electroplating. This is considerably more economical and results in much less target usage. For added savings, some companies apply photoresist to the substrate and electroplate gold only where actually required by the pattern.

**8.19.5 Photolithographic processes**

In the photolithographic process, the substrate is coated with a photosensitive material and exposed to ultraviolet light through a pattern formed on a glass plate. The photoresist may be of the positive or negative type, with the positive type being prevalent because of its inherently higher resistance to the etchant materials. The unwanted material not protected by the photoresist may be removed by *wet* (chemical) etching or by *dry* (sputter) etching.

In general, two masks are required, one corresponding to the conductor pattern and the other corresponding to a combination of both the conductor and resistor patterns, generally referred to as the *composite* pattern. As an alternative to the composite mask, a mask containing only the resistor pattern plus a slight overlap onto the conductor to allow for misalignment may be used. The composite mask is preferred, because it allows a second gold etch process to be performed to remove any bridges or extraneous gold that might have been left from the first etch.

Although chemical etching remains the most common method of etching thin films, more and more companies are turning to sputter etching despite the added capital equipment required. In this technique, the substrate is coated with photoresist, and the pattern is exposed in exactly the same manner as with chemical etching. The substrate is then placed in a plasma and connected to a potential. In effect, the substrate acts as the target during the sputter etching process, with the unwanted material being removed by the impingement of the gas ions on the exposed film. The photoresistive film, being considerably thicker than the sputtered film, is not affected. Sputter etching has two major advantages over chemical etching.

1. There is virtually no undercutting of the film. The gas ions strike the substrate in approximately a cosine distribution with respect to the normal direction of the substrate. This means that virtually no ions strike the film tangentially, leaving the edges intact. This results in more uniform line dimensions, which further results in better resistor uniformity. By contrast, the rate of the chemical etching process in the tangential is the same as in the normal direction, which results in the undercutting of the film by a distance equal to the thickness converted into heat when the ions strike the evaporant. E-beam evaporation is somewhat more controllable.
2. The potent chemicals used to etch thin films are no longer necessary, resulting in fewer hazards to personnel and no disposal problems.

The major impediment to the use of sputter etching is the investment in capital equipment. Most of the new systems have this as an option, and, as more users invest in new equipment or start a new thin film operation, this method will become more widely used.

## 8.20 Thin Film Materials

The sputtering process may deposit virtually any inorganic material, but the outgassing of most organic materials is too extensive to allow sputtering to take place. A wide variety of substrate materials are also available, but these generally must contain an oxygen compound to permit adhesion of the film.

### 8.20.1 Thin film resistors

Materials used for thin film resistors must perform a dual role in that they must also provide the adhesion to the substrate, which narrows the choice to

materials that form oxides. The resistor film begins forming as single points on the substrate in the vicinity of substrate faults or other irregularities that might have an excess of broken oxygen bonds. The points expand into islands that, in turn, join to form continuous films. The regions where the islands meet are called *grain boundaries*, which are a source of collisions for the electrons. The more grain boundaries that are present, the more negative will be the TCR. Unlike thick film resistors, however, the boundaries do not contribute to the noise level. Furthermore, laser trimming does not create microcracks in the glass-free structure, and the inherent mechanisms for resistor drift are not present in thin films. As a result, thin film resistors have better stability, noise, and TCR characteristics than thick film resistors.

The most common resistor material types are nichrome (NiCr), tantalum nitride (TaN), and chrome disilicide. Although NiCr has excellent stability and TCR characteristics, it is susceptible to corrosion by moisture if not passivated by sputtered quartz or by evaporated silicon monoxide (SiO). TaN, on the other hand, may be passivated by simply baking the film in air for a few minutes. This feature has resulted in the increased use of TaN at the expense of NiCr, especially in military programs. The stability of passivated TaN is comparable to that of passivated NiCr, but the TCR is not as good unless annealed for several hours in a vacuum to minimize the effect of the grain boundaries. Both NiCr and TaN have a relatively low maximum sheet resistivity on alumina—about  $400 \Omega/\square$  for NiCr and  $200 \Omega/\square$  for TaN. This requires complex patterns to achieve a high value of resistance, resulting in a large required area and the potential for low yield. Chrome disilicide has a maximum sheet resistance of  $1000 \Omega/\square$  and overcomes this limitation to a large extent. The stability and TCR of chrome disilicide are comparable to those of TaN.

The TaN process is the most commonly used because of its inherently high stability. In this process,  $N_2$  is introduced into the argon gas during the sputtering process, forming TaN by reacting with pure Ta atoms on the surface of the substrate. Heating the film in air at about  $425^\circ\text{C}$  for 10 min forms a film of TaO over the TaN that is virtually impervious to further  $O_2$  diffusion at moderately high temperatures. The film helps to maintain the composition of the TaN film and stabilizes the value of the resistor. TaO is essentially a dielectric, and, during the stabilization of the film, the resistor value is increased. The amount of increase for a given time and temperature is dependent on the sheet resistivity of the film. Films with a lower sheet resistivity increase proportionally less than those with a higher sheet resistivity. The resistance increases as the film is heated longer, making it possible to control the sheet resistivity to a reasonable accuracy on a substrate-by-substrate basis.

### 8.20.2 Barrier materials

When Au is used as the conductor material, a barrier material between the Au and the resistor is required. When gold is deposited directly on NiCr, the Cr has a tendency to diffuse through the Au to the surface, which interferes with both wire bonding and eutectic die bonding. To alleviate this problem, a thin

layer of pure Ni is deposited over the NiCr. In addition, the Ni improves the solderability of the surface considerably.

The adhesion of Au to TaN is very poor. To provide the necessary adhesion, a thin layer of 90Ti/10W may be used between the Au and the TaN.

### 8.20.3 Conductor materials

Gold is the most common conductor material used in thin film hybrid circuits because of the ease of wire and die bonding and the high resistance of the gold to tarnish and corrosion. Aluminum and copper are also frequently used in certain applications. It should be noted that copper and aluminum will adhere directly to ceramic substrates, but gold requires one or more intermediate layers, because it does not form the necessary oxides for adhesion.

### 8.20.4 Thin film substrates

Although the substrate gets quite warm during the deposition process, the temperature does not approach that of the thick film firing process. This enables a wider choice of substrate materials for the thin film process, permitting such materials as glass and low-temperature ceramics to be used.

Still, the prime material remains high purity (99.5%) alumina, with sapphire, a form of alumina, used in critical high-frequency applications. Substrates for thin film applications must have a smoother surface than for thick film, about 3 to 4  $\mu\text{m}$  CLA. Substrates with an as-fired finish are preferred to polished substrates because of the surface pitting typically created during the polishing process.

The surface finish is crucial for consistent and reliable results because, even with a 3 to 4  $\mu\text{m}$  finish, the thickness of the deposited film is significantly less than the variations found in the finish, and the stability of resistors is worse. In addition, the conductor is also thinner in spots, and this contributes to wire and die bond failures.

Certain of the newer materials, such as AlN, are more likely to be used initially in the thin film process, rather than thick film, because no special treatment of the substrate is required.

## 8.21 Comparison of Thick Film and Thin Film

Although the thin film process provides better line definition, smaller line geometry, and better resistor properties, several factors contribute to its relatively infrequent use as compared to thick film.

1. Because of the added labor involved, the thin film process is almost always more expensive than the thick film process. Only when a number of thin film circuits can be fabricated on a single substrate can thin film compete in price.
2. Multilayer structures are extremely difficult to fabricate. Although they are a possibility with multiple deposition and etching processes, this is a

very expensive and labor-intensive process and is limited to a very few applications.

3. The designer, in most cases, is limited to a single sheet resistivity. This requires a large area to fabricate both large- and small-value resistors.

A common practice is to use thin film arrays on thick film substrates where dictated by performance or space limitations. The use of thin film and thick film deposition on the same substrate has been reported in the literature, but it is not widely employed. A comprehensive comparison of the thick and thin film processes is shown in Table 8.22.

**TABLE 8.22 Comparison of Thick Film and Thin Film**

Thin film	Thick film
50 to 24,000 Å	24,000 to 240,000 Å (1 mil)
Indirect (subtractive) process—evaporate, photoetch	Direct process—screen, dry, and fire
Problems with disposal and handling of dangerous chemicals, etchants, developers, plating solutions	No chemical etchants or plating solutions used
Problems with recovery of precious metals from etching solutions	No recovery of precious metals
Multilayering difficult; usually only one layer; multilayer using polyimide as dielectric for multichip module circuits	Low-cost multilayering process
Limited to low sheet resistivity materials; NiCr and TaN, 100 to 300 $\Omega/\square$	Wide range of resistor values by using several pastes with different sheet resistivities, from 1 $\Omega/\square$ to 20 M $\Omega/\square$
Resistors susceptible to chemical corrosion	Rugged resistors able to withstand harsh environments and high temperatures
Low-TCR resistors, $0 \pm 50$ ppm	TCRs $\pm 50$ to 300 ppm/ $^{\circ}\text{C}$
Line definition to 1 mil; 0.1 mil possible with sputter etching	Line definition 5 to 10 mils
High-cost batch process	Low-cost process, continuous, conveyORIZED
Initial equipment investment high (>\$2 million)	Initial equipment investment low (<\$500,000)
More precise line definition; better for RF signals	Line definition not good for RF
Wire bondability better; homogeneous material; plating bath impurities can affect wire bonds	Wire bondability affected by impurities in paste; conductors are heterogeneous

## 8.22 Copper Metallization Technologies

The thick film and thin film technologies are limited in their ability to deposit films with a thickness greater than 1 mil (25  $\mu\text{m}$ ). This factor directly affects the ohmic resistance of the circuit traces and affects their ability to handle



large currents or high frequencies. The copper metallization technologies provide conductors with greatly increased conductor thickness, which offer improved circuit performance in many applications. There are three basic technologies available to the hybrid designer: direct bond copper (DBC), active metal braze (AMB), and the various methods of plating copper directly to ceramic.

### 8.22.1 Direct bond copper

Copper may be bonded to alumina ceramic by placing a film of copper in contact with the alumina and heating to about 1065°C, just below the melting point of copper, 1083°C. At this temperature, a combination of 0.39 percent O<sub>2</sub> and 99.61 percent Cu form a liquid that can melt, wet, and bond tightly to the surfaces in contact with it when cooled to room temperature. In this process, the copper remains in the solid state during the bonding process, and a strong bond is formed between the copper and the alumina with no intermediate material required. The metallized substrate is slowly cooled to room temperature at a controlled rate to avoid quenching. To prevent excessive bowing of the substrate, copper must be bonded to both sides of the substrate to minimize stresses caused by the difference in TCE between copper and alumina.

In this manner, a film of copper from 5 to 25 mils thick can be bonded to a substrate and a metallization pattern formed by photolithographic etching. For subsequent processing, the copper is usually plated with several hundred microinches of nickel to prevent oxidation. The nickel-plated surface is readily solderable, and aluminum wire bonds to nickel constitute one of the most reliable combinations.<sup>15</sup> Aluminum wire bonded directly to copper is not as reliable and may result in failure on exposure to heat and/or moisture.<sup>16</sup>

Multilayer structures of up to four layers have been formed by etching patterns on both sides of two substrates and bonding them to a common alumina substrate. Interconnections between layers are made by inserting oxidized copper pellets into holes drilled or formed in the substrates prior to firing. Vias may also be created by using one of the copper plating processes.

Bonding a copper sheet larger than the ceramic substrate and etching a lead frame at the same time as the pattern may create integral leads extending beyond the substrate edge.

The line and space resolution of DBC are limited by the difficulty of etching thick layers of metal without substantial undercutting. Although the DBC technology does not have a resistor system, the thick film technology can be used in conjunction with DBC to produce integrated resistors and areas of high-density interconnections.

Aluminum nitride can also be used with copper, although the consistency of such factors as grain size and shape are not as good as with aluminum oxide at this time. Additional preparation of the AlN surface is required to produce the layer of oxide required to produce the bond. This can be accomplished by heating the substrate to about 1250°C in the presence of oxygen.

Direct bond copper offers considerable advantages when packaging power circuits. The thick layer of copper can handle considerable current without ex-

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cessive voltage drops and heat generation, and it allows the heat to spread rapidly outward from semiconductor devices, which dramatically lowers the thermal impedance of the system. The layer of copper on the bottom also contributes to heat spreading.

**8.22.2 Plated copper technology**

Although a copper film can be mechanically bonded to a rough substrate surface, the adhesion is usually inadequate for most applications. The various methods of plating copper to a ceramic all begin with the formation of a conductive film on the surface. This film may be vacuum deposited by thin film methods, screen printed by thick film processes, or deposited with the aid of a catalyst. A layer of electroless copper may be plated over the conductive surface, followed by a layer of electrolytic copper to increase the thickness.

A pattern may be generated in the plated surface by one of two methods. Conventional photolithographic methods may be used to etch the pattern, but this may result in undercutting and loss of resolution when used with thicker films. To produce more precise lines, a dry film photoresist may be utilized to generate a pattern on the electroless copper film that is the negative of the one required for etching. The traces may then be electroplated to the desired thickness using the photoresist pattern as a mold. Once the photoresist pattern is removed, the entire substrate may be immersed in an appropriate etchant to remove the unwanted material between the traces. Plated copper films created in this manner may be fired at an elevated temperature in a nitrogen atmosphere to improve adhesion.

**8.22.3 Active metal brazing copper technology**

The active metal brazing (AMB) process utilizes one or more of the metals in the IV-B column of the periodic table (e.g., titanium, hafnium, and zirconium) to act as an activation agent with ceramic. These metals are typically alloyed with other metals to form a braze that can be used to bond copper to ceramic. One such example is an alloy of 70Ti/15Cu/15Ni, which melts at 960 to 1000°C. Numerous other alloys can also be used.<sup>14</sup>

The braze may be applied in the form of a paste, a powder, or a film. The combination is heated to the melting point of the selected braze in a vacuum to minimize oxidation of the copper. The active metal forms a liquidus with the oxygen in the system that acts to bond the metal to the ceramic. After brazing, the copper film may be processed in much the same manner as DBC.

**8.23 Comparison of Copper Metallization Technologies**

The DBC and AMB processes are advantageous for applications in which a thicker copper layer is beneficial. In particular, these technologies are highly suitable for use in power circuits, where their ability to handle high currents and to aid heat dissipation can be utilized. Plated copper is most applicable to applications in which fine lines and precise geometries are required, such as

RF circuits. Design guidelines for each of these technologies is given in Table 8.23.

## 8.24 Summary of Substrate Metallization Technologies

The applications of the various substrate metallization technologies rarely overlap. Given a particular set of requirements, the choice is usually very apparent. Table 8.24 illustrates the properties of the different technologies.

## 8.25 Assembly of Hybrid Circuits

There are two basic methods of assembling hybrid circuits: the “chip-and-wire” approach, in which semiconductor devices in the unpackaged form are mechanically attached to the substrate metallization by epoxy, solder, or eutectic bonding, and electrically connected by wire bonding; and the “surface mount” approach, in which packaged devices are soldered to the substrate, making both the electrical and mechanical connections simultaneously. These methods are not mutually exclusive, and it is very common to combine these approaches on a single substrate. This treatise is primarily concerned with the chip-and-wire technology.

### 8.25.1 Chip-and-wire technology

Semiconductor devices in the unpackaged state are very delicate. The metallization patterns are extremely thin and easily damaged, even with normal handling. The input/output (I/O) terminals are electrically open, and an electrical charge has no path to ground, making the die extremely susceptible to damage by electrostatic discharge (ESD). ESD can be generated from a variety of sources, as shown in Table 8.25. The die must be handled with extreme care, using a vacuum pickup (as opposed to tweezers) designed to dissipate electrical charge. Operators must be properly grounded, and ionized air blowers may be necessary when especially susceptible devices are being mounted.

### 8.25.2 Direct eutectic bonding of semiconductor devices

Silicon forms a eutectic composition with gold in the ratio of 94 percent gold and 6 percent silicon by weight, which melts at 370°C. Gold is the only metal that has a sufficiently low eutectic temperature in combination with silicon to be practical. By contrast, the eutectic temperature of silicon and silver is nearly 800°C.

In the eutectic bonding process, the substrate is preheated to about 200°C to minimize thermal shock and then transferred to a heated stage at about 400°C. The silicon die is picked up by a heated collet to further minimize thermal shock. The collet is sized to match the size of the die and is connected to a small vacuum pump for the purpose of holding the die in place. The collet is also connected to a motor capable of providing mechanical scrubbing to assist in making the bond. The die is picked up by the collet and transported to the

**TABLE 8.23 Comparison of Design Rules for Pure Copper Metallization**

Technology	Line width (in)		Etch factors* (in)	Registration† (in)	Copper thickness ‡ (in)			Via diameters (in)		Integral leads from edge of substrate	Camber** (in/linear in)
	Min.	Typ.			Min.	Typ.	Max.	Min.	Typ.		
Direct bond copper	0.015	0.020	0.004 to 0.008††	±0.008	0.005	0.012	0.050	0.016	0.064	‡‡	±0.004
Plated copper	0.002	0.005	0.0005	±0.005	0.001	0.002	0.005	0.005	0.025	‡‡	±0.003
Active metal braze	0.015	0.020	0.004 to 0.006***	±0.005	0.008	0.010	0.012	‡‡	‡‡	***	±0.004

\*The width of the artwork pattern determines final conductor width. Etching will reduce the original artwork width by several mils, depending on copper thickness. Therefore, the artwork must have a wider dimension to compensate.

†The artwork is registered to a feature on the ceramic substrate, usually a corner of the ceramic surface.

‡Copper layers can be lapped to a lesser thickness after metallization.

\*\* Assume that both ceramic sides have copper metallization. Then camber depends on differences in percentage of ceramic surface area coverage by copper.

††0.020-in pullback required from ceramic edge.

‡‡Not possible

\*\*\*0.100 in<sup>2</sup> required on ceramic for integral leads

**TABLE 8.24 Comparison of Hybrid Metallization Technologies**

Technology	Ceramic selection	Metallization description	Adhesion mechanism	Geometry (typical)	Electrical and thermal	Hybrid assembly	Reliability	Cost
Thick film	Usually oxide, most types possible	Metal + glass	Chemical + mechanical	0.010 in (250 $\mu\text{m}$ lines and more than 0.0005 in (12 $\mu\text{m}$ ) thickness	Adequate	Good; solder rework can be a problem	Good; well understood	Variable; can use expensive precious metals
Thin film	All types	Pure metal, requires adhesion layers	Mechanical + chemical	0.002 in (50 $\mu\text{m}$ ) lines and less than 0.0005 in (12 $\mu\text{m}$ ) thickness	Adequate	Adequate, not easily soldered	Good, well understood	High for equipment, process, and materials
Direct bond copper	More selective, oxide based	Pure copper	Chemical + mechanical	0.020 in (400 $\mu\text{m}$ ) lines and 0.008 in to 0.020 in (200 to 500 $\mu\text{m}$ ) thickness	Good	Good	Good, well understood	Reasonable
Plated copper	All types	Pure, copper, usually thin adhesion layer	Mechanical (chemical?)	0.004 in (100 $\mu\text{m}$ ) lines and 0.0005 in to 0.005 in (12 to 125 $\mu\text{m}$ ) thickness	Good	Good	Less understood	Reasonable
Active metal braze copper	All types	Pure copper, with braze adhesion layer	Chemical + mechanical	0.020 in (400 $\mu\text{m}$ ) lines and 0.008 in to 0.020 in (200 to 500 $\mu\text{m}$ ) thickness	Good	Good	Adequate	Reasonable

TABLE 8.25 Typical Electrostatic Voltages<sup>17</sup>

Event	Relative humidity, %		
	10	40	55
Walking across carpet	35,000	15,000	7,500
Walking across vinyl floor	12,000	5,000	3,000
Motions of bench worker	6,000	800	400
Remove DIPs from plastic tubes	2,000	700	400
Remove DIPs from vinyl trays	11,500	4,000	2,000
Remove DIPs from styrofoam	14,500	5,000	3,500
Remove bubble pack from PWBs	26,000	20,000	7,000
Pack PWBs in foam-lined box	21,000	11,000	5,500

desired metallization pattern on the substrate. Simply placing the die in contact with the heated substrate will not automatically form the bond; the materials must be in the proper proportion. This is accomplished by mechanically scrubbing the die into the gold metallization. During the scrubbing process, the eutectic alloy will be formed at some random point along the interface, which will then become molten. This, in return, will rapidly dissolve more material until the entire interface is liquid and the bond is formed. Devices larger than  $0.020 \times 0.020$  in tend to crack when mechanically scrubbed and require a gold-silicon preform to make the bond.

The eutectic process makes a very good bond, mechanically, electrically and thermally, but the high bonding temperature is an extreme disadvantage for a variety of reasons, and this process is generally used only in single-chip applications. Where a metallurgical bond is required, solder is the preferred process. Semiconductor devices intended for solder bonding are typically metallized with a titanium/nickel/silver alloy on the bottom.

### 8.25.3 Organic bonding materials

The most common method of mechanically bonding active and passive components to a metallized substrate is with epoxy. Most epoxies for hybrid circuit applications have a filler added for electrical and/or thermal conductivity, with silver being the most common. Silver has a high electrical conductivity, and a smaller proportion of silver to epoxy is required to produce a given resistivity than other metals. Silver epoxy, therefore, has a higher mechanical strength, because a higher ratio of epoxy to filler is present for a given volume. Other conductive filler materials include gold, palladium-silver for reduced silver migration, and tin-plated copper. Nonconductive filler materials include aluminum oxide, beryllium oxide, and magnesium oxide for improved thermal conductivity.

Epoxy may be dispensed by screen printing, pneumatic dispensing through a nozzle, and die transfer. Screen printing requires a planar surface, whereas pneumatic dispensing and die transfer may be used with irregular surfaces. If many die are to be mounted on a single substrate, screen printing is the preferred method, because epoxy can be applied to all mounting pads in a single pass of the screen printer with a more uniform and repeatable cross section.

If large surfaces such as substrates are to be mounted, liquid epoxies are difficult to use. For this application, a large sheet of glass cloth can be impregnated with epoxy, which is then B-staged, or partially cured, to produce a solid structure of epoxy generally referred to as a *preform*. Heating the preform further will soften the partially cured epoxy to facilitate bonding and will then complete the curing process. The sheet may then be cut into smaller pieces and used to mount large components and substrates. If high thermal conductivity is required, the mesh may be made from silver wire, and silver epoxy may be used.

Epoxy as a die attach material suffers from two major disadvantages.

1. The thermal and electrical resistances are quite high as compared to direct methods of bonding such as soldering or eutectic bonding.
2. The operating temperature is limited to about 150°C, as many epoxies begin breaking down and outgassing at temperatures above this figure.

These factors inhibit the use of epoxy in mounting power devices, in applications where a high processing temperature is required, where performance at a high ambient temperature is required, and where a low bond resistance is needed. One phenomenon that can occur when the epoxy is operated at elevated temperatures near or above the glass transition temperature ( $T_g$ ) is the settling of the filler away from the device interface, leaving a thin layer of resin at the bond line and increasing the electrical resistance of the bond to the point at which circuit failure occurs. Another failure mechanism that can occur is silver migration, which can be accelerated by water absorption of a resin with a relatively high mobile ion content.

Other materials utilized for die bonding include polyimide and certain of the thermoplastic materials. Polyimide is stable out to around 350°C unless filled with silver, which acts as a catalyst to promote adhesion loss. Polyimides are typically dissolved in a solvent, such as xylene, requiring a two-step curing process. The first step, at a low temperature, evaporates the solvent, and the second step, at an elevated temperature, cross-links the polyimide. Thermoplastic materials are particularly advantageous in high-volume applications, because the cure cycle is much shorter than that of either epoxy or polyimide. Properties of selected die attach materials are shown in Table 8.26.

#### 8.25.4 Solder attachment

In the soldering process, an alloy of two or more metals is melted at the interface of two metal surfaces. The molten solder dissolves a portion of the two

TABLE 8.26 Properties of Selected Organic Die Attach Materials

Type	Advantages and limitations of various adhesive types	
	Advantages	Limitations
Phenolics	Very high bond strength	Used mostly for structural applications, possibly corrosive, difficult to process at low temperatures
Polyurethanes	Easy to rework	Not suitable for temperatures above 120°C; relatively high outgassing, some decomposition
Polyamides	Easy to rework	High moisture absorption, high outgassing, variations in electrical insulation properties, especially when exposed to high humidity
Polyimides	Very high temperature stability	High cure temperatures, require solvents as vehicles
Silicones	High-temperature stability, easy to rework, high purity, low outgassing	Moderate-to-poor bond strength, high CTE
Epoxies	Some easy to rework by thermomechanical means, some low outgassing, easy to process, can be filled to 60 to 70 percent with a variety of conductive or nonconductive fillers	Depending on type of curing agent used and degrees of cure, outgassing, catalyst leaching, and corrosivity
Cyanoacrylates	Very rapid setting (<10 sec); very high initial bond strengths	Bond strengths often degrade under moist or elevated temperature (>150°C) conditions

surfaces and, when the solder cools, a junction, or “solder joint,” is formed, joining the two metal surfaces.

For the solder joint to occur, both metal surfaces and the solder must be clean and free from surface oxides so that the solder is able to “wet” both surfaces as shown in Fig. 8.30. Removal of the oxides is accomplished by the use of a “flux,” an organically based acid. Fluxes are categorized by their strength and by the requirement for cleaning. Fluxes requiring solvent cleaning are rapidly being phased out because of environmental regulations, and the so-called “no-clean” fluxes, which remain on the circuit after the soldering process, are seeing extensive use in commercial applications. Water-soluble fluxes are still widely used in the printed circuit board industry. Surfaces that are

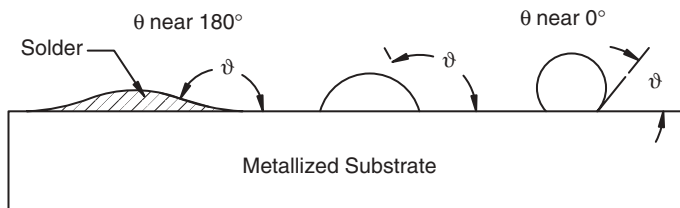


Figure 8.30 Degrees of wetting.



heavily oxidized before soldering may require the use of a stronger flux such as an resin mildly activated (RMA) flux.

Solder materials are selected primarily for their compatibility with the surfaces to be soldered, their reliability under conditions of temperature extremes, and their melting point. Solders are generally divided into two categories: “hard” solders, which have a melting point above about 500°C and are often referred to as “brazes,” and “soft” solders, which have a lower melting point. Soft solders are used primarily in the assembly process, whereas hard solders are used in lead attachment and package sealing.

Soft solders may also be divided into two categories: eutectic and noneutectic solders. Eutectic solders have the lowest melting point and are typically more rigid in the solid state than other solders with the same constituents. This is partly a result of the fact that eutectic solders go directly from the liquid to the solid state without going through a “plastic” region. Their lower melting point makes them very attractive in many applications, and their use is quite common. Some of the more common solders and their characteristics are listed in Table 8.27.

The compatibility of the solder with the material in the metal surfaces must be a prime consideration when selecting a solder, in particular the tendency of the metal to “leach” into the solder and the tendency to form intermetallic compounds that might prove detrimental to reliability. Leaching is the process by which a material is absorbed into the molten solder to a high degree. While a certain degree of leaching must occur to produce the solder joint, excessive leaching can cause the metallization pattern to vanish into the molten solder, creating an open circuit. Tin-bearing solders used in conjunction with gold or silver conductors are especially prone to this phenomenon, because these materials have a strong affinity with tin. A thick or thin film gold or silver conductor will dissolve into a tin-lead solder in a matter of seconds. The addition of platinum and/or palladium to the thick film conductor materials will greatly enhance the leach resistance to tin-bearing solders, but it must still be a consideration. The leach resistance is proportional to the amount of Pt and Pd added, but this has the adverse effect of adding to both the cost and the electrical resistance. Soldering at the lowest possible temperature for the shortest possible time consistent with forming the solder joint can minimize leaching. The addition of a small amount of silver to the solder lowers the melting point slightly, and, with proper control of the soldering temperature, the silver already present in the solder partially saturates the solution, further inhibiting leaching. Soldering directly to gold requires the use of AuSn, PbIn, or other solders that do not leach gold. The added Au in the AuSn combination inhibits leaching of the gold in the film.

Intermetallic compound formation is also a consideration. Certain compounds have a high electrical resistance and are susceptible to mechanical failure when exposed to temperature cycling or storage at temperature extremes. Tin forms intermetallic compounds with both gold and copper, and indium also forms intermetallic compounds with copper. The most commonly used solders are the tin-lead solders, which are used extensively on copper and the PdAg and PtAg alloys.

**TABLE 8.27 Processing Temperatures of Selected Organic and Metallic Attachment Materials**

Organic attachment materials		
Material	Temperature, °C	
Polyimide	259–300*	
Epoxy	150	
Metallic attachment materials		
Alloy	Liquidus, °C†	Solidus, °C
In52/Sn48‡	118	118
Sn62.5/Pb36.1/Ag1.4‡	179	179
Sn63/Pb37‡	183	183
In60/Pb40	185	174
Sn60/Pb40	188	183
Sn96.5/Ag3.5‡	221	221
Pb60/Sn40	238	183
Pb70/Sn27/Ag3	253	179
Pb92.5/Sn5/Ag2.5	280	179
Sn90/Ag10	295	221
Pb90/Sn10	302	275
Au88/Ge12‡	356	356
Au96.4/Si3.6‡	370	370
Ag72/Cu28‡	780	780

\*Polyimide materials require a precure step at 70°C to remove solvents.

†The processing temperature of most alloys is  $\geq 20^\circ\text{C}$  above the liquidus.

‡Eutectic composition.

Lead-free solders, such as the tin/silver combinations, are becoming more widely used. Apart from environmental concerns, the tin/silver solders have proven to be more resilient to extensive temperature cycling conditions. Table 8.28 shows the comparative fatigue characteristics of various solders.

In the soldering process, it is desirable to minimize the exposure of the part to elevated temperatures. High temperatures accelerate the rate of chemical reactions that may be detrimental to the reliability of the circuit. Furthermore, excessive exposure of metal surfaces to liquid solder increases the rate of formation of intermetallic compounds and also increases leaching.

TABLE 8.28 Comparative Fatigue Characteristics of Solder Alloys

Performance	Composition	Performance	Composition
Worst	Sn63/Pb37 Sn60/Pb40	Fair	In99/Cu1 Sn90/Pb10 Sn99.25/Cu0.75
Poor	Sn62/Pb36/Ag2 Sn65/In35 Sn42/Bi58 Sn50/In50 Sn50/Pb50	Good	Sn99/Sb1 Pb50/In50 Sn100
		Excellent	Sn96/Ag4 Sn95/Sb5

Solders for microelectronic applications are generally in the form of a paste, with the solder in powder form mixed with an appropriate flux and a dispensing vehicle. Solder in paste form may be screen printed or dispensed pneumatically. The part is placed in the wet solder paste prior to soldering manually or by an automatic pick-and-place system.

The most effective method of soldering is to place the part in conjunction with the solder paste into a tunnel furnace with several heated zones. By controlling the speed of the belt and the temperature of the individual zones, a time-temperature relationship, or “profile,” can be established that will optimize the soldering process. Heating of the part may be accomplished by resistance heating, by infrared (IR) heating, or by a combination of both.

The use of a nitrogen or forming gas blanket during the soldering process to prevent oxidation of the solder and/or the surfaces aids greatly in soldering, particularly to nickel, and improves the wetting of tin-bearing solders. The formation of a gas blanket can be easily accomplished by connecting a gas source to the furnace and by the use of baffles at the ends of the furnace to minimize the intrusion of air into the heated region. A typical profile has a duration of several minutes and has a plateau just below the melting point of the solder for a period of time followed by a rapid rise in temperature, or “spike,” above the melting point for a short duration and a gradual decline down to room temperature. In general, the duration of the spike should be held as short as possible, consistent with good solder flow and wetting, to minimize such effects as leaching of conductor materials and the effect of high temperatures on the components.

### 8.25.5 Wire bonding

Ohmic contacts to semiconductor devices are typically made with aluminum, because that material diffuses well into the silicon structure at a moderate temperature. Wire bonding is used to make the electrical connections from the aluminum contacts to the substrate metallization or to a lead frame; from other components, such as chip resistors or chip capacitors, to substrate metallization; from package terminals to the substrate metallization; or from one point on the substrate metallization to another.

There are two basic methods of wire bonding: thermocompression wire bonding, which uses primarily gold wire; and ultrasonic wire bonding, which uses primarily aluminum wire. Thermocompression wire bonding, as the name implies, utilizes a combination of heat and pressure to form an intermetallic bond between the wire and a metal surface. In thermocompression bonding (Fig. 8.31), a gold wire is passed through a hollow capillary, generally

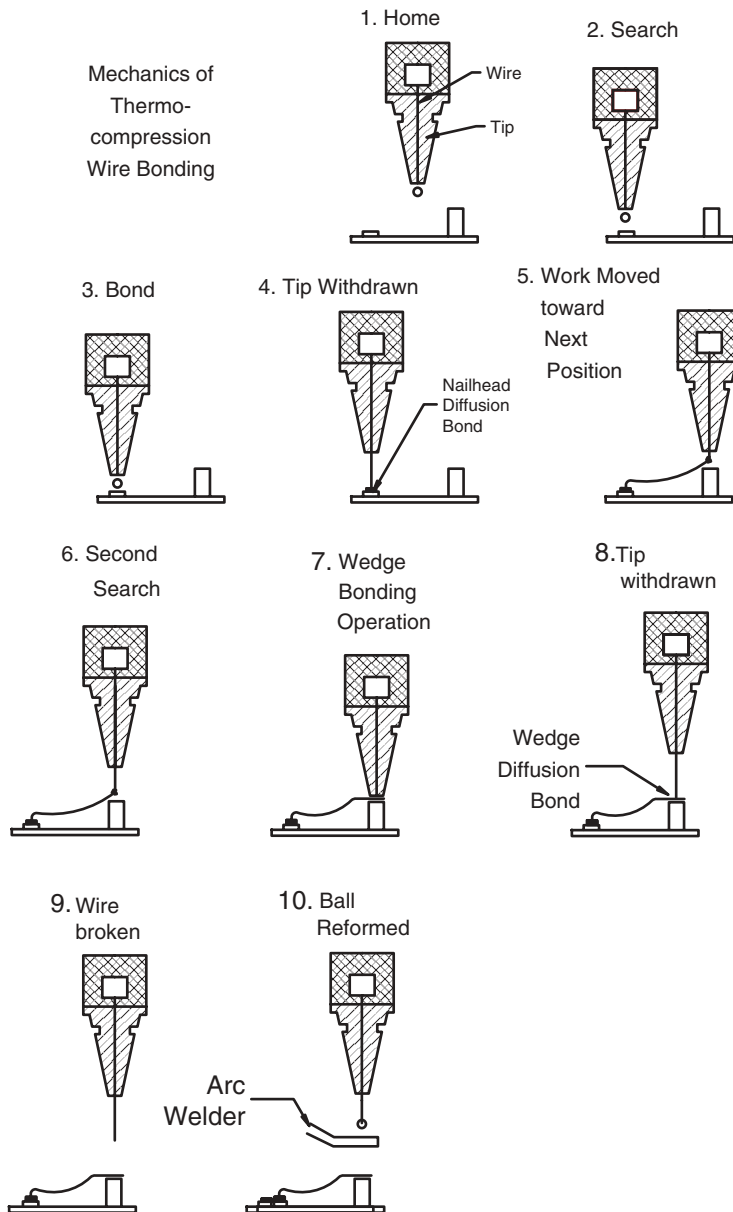


Figure 8.31 Thermocompression bonding sequence.

made from a refractory metal such as tungsten, and a ball is formed on the end by means of an electrical arc. The substrate is heated to about 300°C, and the ball is forced into contact with the bonding pad on the device with sufficient force to cause the two metals to bond. The capillary is then moved to the bond site on the substrate, feeding the wire as it goes, and the wire is bonded to the substrate by the same process, except that the bond is in the form of a “stitch” as opposed to the “ball” on the device.

The wire is then clamped and pulled to break just above the stitch, and another ball is formed as above. Thermocompression bonding is rarely used for a variety of reasons.

- The high substrate temperature precludes the use of epoxy for device mounting.
- The temperature required for the bond is above the threshold temperature for gold-aluminum intermetallic compound formation. The diffusion rate for aluminum into gold is much greater than for gold into aluminum. The aluminum contact on a silicon device is very thin and, when it diffuses into the gold, voids (called *Kirkendall voids*) are created in the bond area, increasing the electrical resistance of the bond and decreasing the mechanical strength.
- The thermocompression bonding action does not effectively remove trace surface contaminants that interfere with the bonding process.

The ultrasonic bonding process (Fig. 8.32) uses ultrasonic energy to vibrate the wire against the surface to combine the atomic lattices together at the surface as depicted in Fig. 8.33. Localized heating at the bond interface caused by the scrubbing action, aided by the oxide on the aluminum wire, assists in forming the bond. The substrate itself is not heated. Intermetallic compound formation is not as critical as with the thermocompression bonding process, because both the wire and the device metallization are aluminum. Kirkendall voiding on an aluminum wire bonded to gold substrate metallization is not as critical, given that there is substantially more aluminum available to diffuse than on device metallization. Ultrasonic bonding makes a stitch on both the first and second bonds. For this reason, ultrasonic bonding is somewhat slower than thermocompression, because the capillary must be aligned with the second bond site when the first bond is made. Ultrasonic bonding to package leads may be difficult if the leads are not tightly clamped, because the ultrasonic energy may be propagated down the leads instead of being coupled to the bond site.

The use of thermosonic bonding largely overcomes the difficulties noted with thermocompression bonding. In this process, used with gold wire, the substrate is heated to 150°C, and ultrasonic energy is coupled to the wire through the transducer action of the capillary, scrubbing the wire into the metal surface and forming a ball-stitch bond from the device to the substrate, as in thermocompression bonding.

Thermosonic gold bonding is the most widely used bonding technique, primarily because it is faster than ultrasonic aluminum bonding. Once the ball

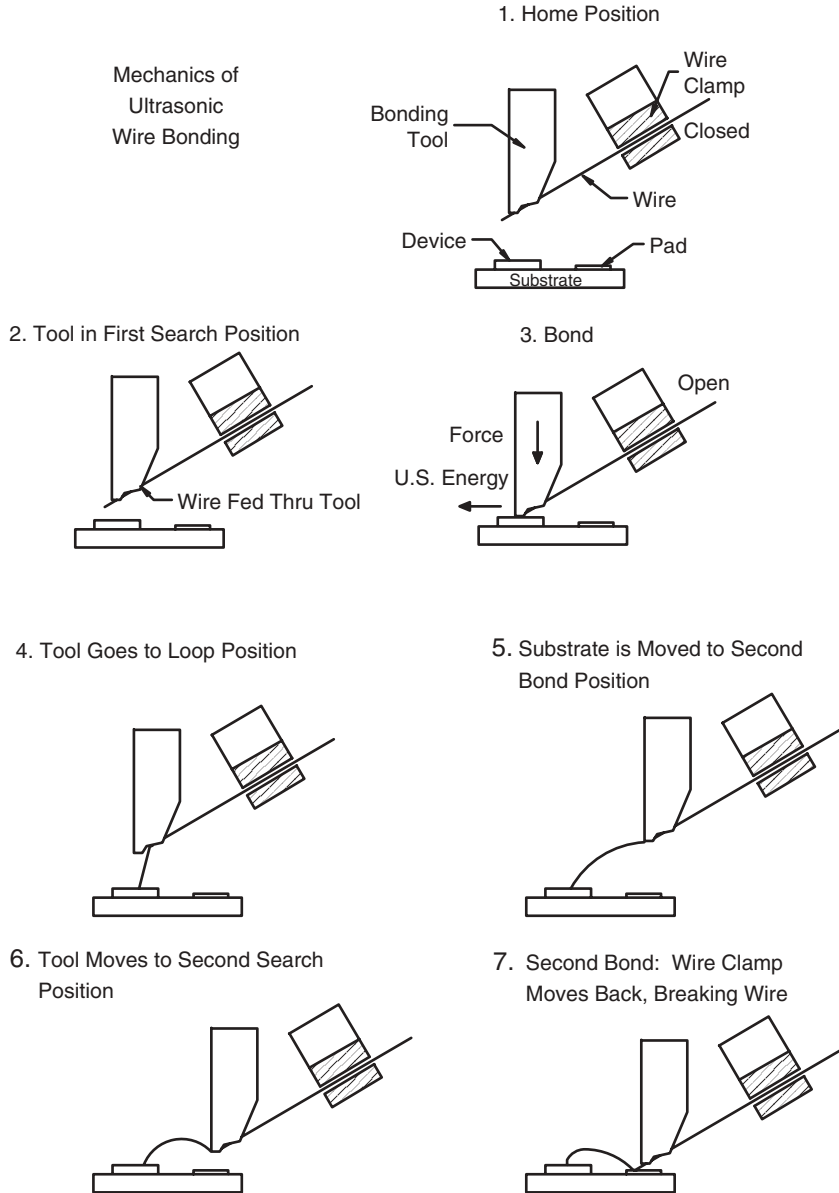


Figure 8.32 Ultrasonic bonding sequence.

bond is made on the device, the wire may be moved in any direction without stress on the wire, which greatly facilitates automatic wire bonding, as the movement need only be in the x and y directions. An example of thermosonic bonding is shown in Fig. 8.34.

By contrast, before the first ultrasonic stitch bond is made on the device, the circuit must be oriented so that the wire will move toward the second bond

### Wire Bonding Mechanism

#### Metallurgical Bond Similar to Blacksmith Weld

Deformation of two metals in contact produces shearing action along surfaces of both metals. The resulting cleaning action results in atomically clean surfaces where interatomic forces bond the two metals

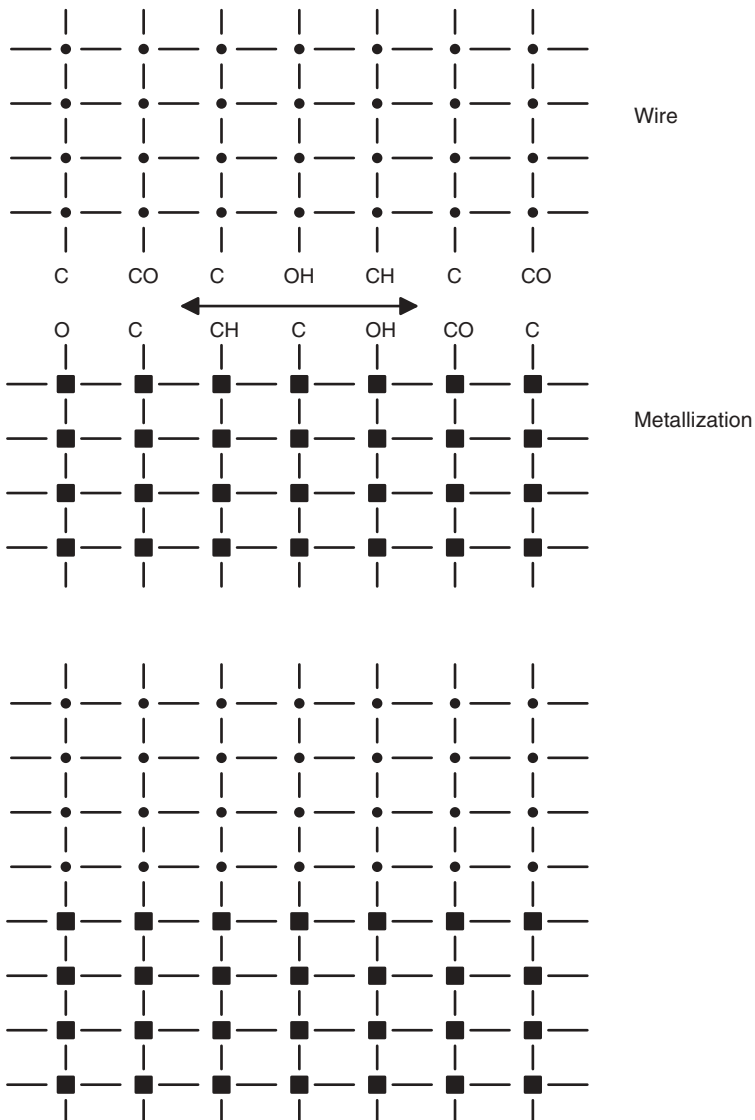


Figure 8.33 Lattice formation in ultrasonic bonding.

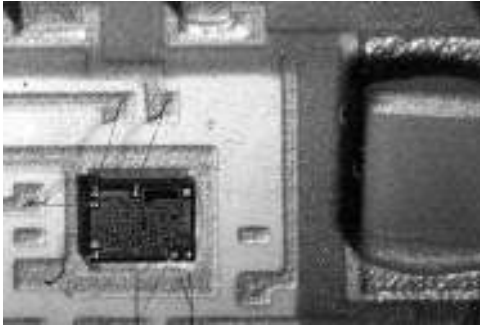


Figure 8.34 Thermosonic wire bonding.

site only in the direction of the stitch. This requires rotational movement, which not only complicates the design of the bonder but increases the bonding time as well.

Attempts at designing an aluminum ball bonder have not proven successful to date, because of the difficulty in making a ball on the end of the wire. Aluminum bonding is commonly used in hybrids or chip carriers where the package-sealing temperature may exceed the threshold temperature for the formation of intermetallic compounds, in power hybrids where the junction temperature is high, and in applications where large wires are required. Gold wire is difficult to obtain in diameters above 0.002 in, whereas aluminum wire is available up to 0.022 in. An example of power devices bonded with large aluminum wire is shown in Fig. 8.35.

Automatic thermosonic gold bonding equipment now exists that can bond up to four wires per second under optimal conditions. The actual rate depends on the configuration of the bonding pattern and the number of devices to be bonded. The utilization of an automatic bonder with pattern recognition is strongly dependent on the accuracy of the device placement and on the quality of the substrate metallization. If the devices are not placed within a few mils of the bond site and within a few degrees of rotation, the pattern recognition

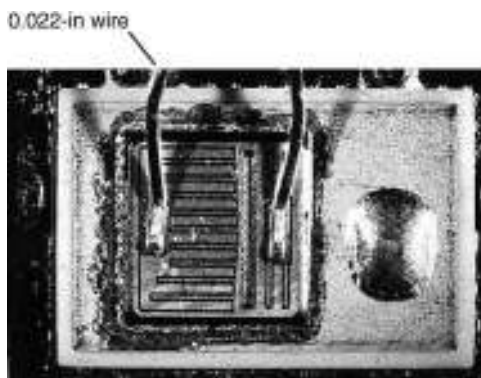


Figure 8.35 Large aluminum wire bonding.



system will not be able to locate the device, resulting in lost production time while the operator feeds in the coordinates. An ideal stitch bond is shown in Fig. 8.36.

The substrates must be kept very clean and should be handled only with finger cots during the assembly process. In storage, the substrates should be kept in a clean, dry area. Thin film metallization makes the best bonding surface, because it is uniform in thickness and is almost pure gold. There exists a considerable variation in bondability among the various thick film gold conductors, and bonding studies under a variety of conditions must be an integral part of the selection process of a thick film gold material. Thick film gold for use with aluminum wire must contain palladium to improve the strength of the bond under conditions of thermal aging. The same principle applies to aluminum bonding on palladium-silver materials. As the palladium-to-silver ratio is increased, the reliability of the bonds increases.

The integrity of the wire bonds may be tested by placing a small hook under the wire and pulling at a constant rate of speed, usually very slow, until the bond fails. The amount of force required is the *bond strength*. The mode of failure is just as important as the actual bond strength. There are five points at which a bond can fail.

1. The ball (or stitch) at the device may fail.
2. The wire may break just above the stitch at the device end.
3. The wire may break in the center.
4. The wire may break just above the stitch at the substrate end.
5. The stitch at the substrate may lift.

Of the five options, number three is the most desirable, with two and four following in turn. If an excessive number of lifts occur, particularly at the device end, a serious bonding problem may be indicated. Some of the more common bonding problems and their possible causes are listed below.

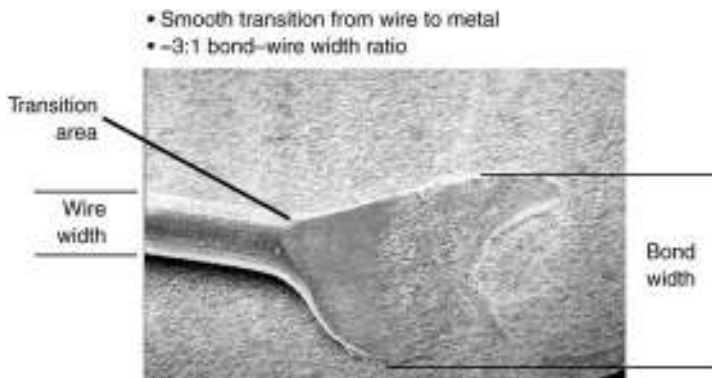


Figure 8.36 Ideal stitch bond.

- *Excessive bond lifts at the device.* This problem may be a result of one of three factors: improper bond setup, contamination on the device, or incomplete etching of the glass passivation on the device.
- *Excessive bond breaks just above the device.* This is probably caused by either a worn bonding tool or by excessive bonding pressure, both of which can crimp the wire and create a weak point.
- *Excessive bond breaks just above the substrate.* This is probably caused by excessive bonding pressure. This may result from improper bonding setup, which in turn may be due to contamination or to poor substrate metallization. A worn bonding tool may result in the wire being nicked, creating a possible failure point.
- *Excessive stitch lifts at the substrate.* This may be the result of a worn bonding tool, poor bonder setup, or poor device metallization.

The wire size is dependent on the amount of current that the wire is to carry, the size of the bonding pads, and the throughput requirements. Table 8.29 provides the wire size for a specified current for both gold and aluminum wire. For applications where current and bonding size is not critical, 0.001-in wire is the most commonly used size. Although 0.0007-in wire is less expensive, it is difficult to thread through a capillary and bond without frequent breaking and consequent line stoppages.

**TABLE 8.29 Maximum Current for Wire Size**

Material	Diameter (in)	Maximum current	
		L < 0.040 in	L > 0.040 in
Gold	0.001	0.949	0.648
	0.002	2.683	1.834
Aluminum	0.001	0.696	0.481
	0.002	1.968	1.360
	0.005	7.778	5.374
	0.008	15.742	10.876
	0.012	28.920	19.981
	0.015	40.417	27.924
	0.022	71.789	49.600

## 8.26 Packaging

Packaging for individual devices or complete hybrid assemblies can be characterized as shown in Table 8.30 with examples depicted in Fig. 8.37. There are

many driving forces and considerations in the choice of technology for packaging and the subsequent next level assembly technologies.

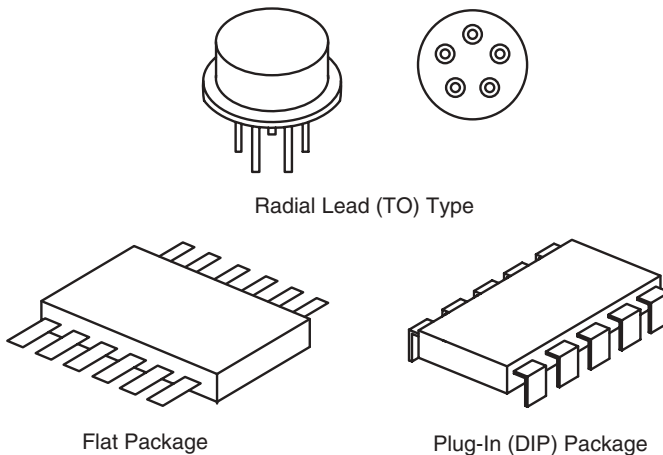
**TABLE 8.30 Characterizations of Package Types**

Leads	Type
Through-hole	Hermetic
Plug-in Dual-in-line (DIP) Pin grid array (PGA) TO types	Metal Ceramic
Surface mount	Nonhermetic
Flat package Ball grid array (BGA)	Plastic molded Conformal coated

### 8.26.1 Hermetic packages

A true hermetically sealed package would prevent intrusion of contaminants (liquid, solid, or gas) for an indefinite period of time. In practice, however, this is not realistic. Even in a perfectly sealed structure, diffusion phenomena will occur over time, allowing the smaller molecules, such as helium or water vapor, to penetrate the barrier medium and ultimately reach equilibrium within the package interior. A hermetic package is defined as one in which the leak rate of helium after pressurization is below a specified rate with reference to the package size as shown in Table 8.31.

A hermetic package must either be metal, ceramic, or glass. Organic packages, or packages with an organic seal, may initially pass the pressurization



**Figure 8.37** Package types.

**TABLE 8.31 Acceptable Leak Rates for Hermetic Packages per MIL-STD-883**

Package volume (cm <sup>3</sup> )	PSIG	Bomb condition exposure time (hr)	Maximum dwell (hr)	Reject limit (atm-cm <sup>3</sup> /sec-He)
V < 0.05	75 ± 2	2.0, +0.2, -0	1	5 × 10 <sup>-8</sup>
0.05 ≤ V < 0.5	75 ± 2	4.0 +0.4, -0	1	5 × 10 <sup>-8</sup>
0.5 ≤ V < 10.0	45 ± 2	2.0, +0.2, -0	1	1 × 10 <sup>-7</sup>
1.0 ≤ V < 10.0	45 ± 2	4.0 +0.4, -0	1	5 × 10 <sup>-8</sup>
10.0 ≤ V < 20.0	45 ± 2	10.0, +1.0, -0	1	5 × 10 <sup>-8</sup>

test described above but will allow water vapor to pass back and forth from the atmosphere to the package interior. Therefore, they are not truly hermetic. Interconnections through a metal package may be insulated by glass-to-metal seals utilizing glass that matches the coefficient of expansion to that of the metal.

A hermetic package allows the circuit mounted inside to be sealed in a benign environment—generally nitrogen, which is obtained from a liquid nitrogen source. Nitrogen of this type is extremely dry, with a moisture content of less than 10 ppm. As a further precaution, the open package with the enclosed circuit mounted inside is subjected to an elevated temperature, usually 150°C, in a vacuum, to remove absorbed and adsorbed water vapor and other gases prior to sealing. For added reliability, the moisture content inside a package should not exceed 5000 ppm. This figure is below the dew point of 6000 ppm at 0°C, ensuring that any water that precipitates out will be in the form of ice, which is not as damaging as water in the liquid form.

A hermetic package adds considerably to the reliability of a circuit by guarding against contamination, particularly of the active devices. An active device is susceptible to a number of possible failure mechanisms, such as corrosion and inversion, and may be attacked by something as benign as distilled, deionized water, which can leach phosphorous out of the passivating oxide to form phosphoric acid. This, in turn, can attack the aluminum bonding pads.

### 8.26.2 Metal packages

The most common type of hermetic package is the metal package, which is fabricated primarily from ASTM F-15 alloy, Fe52Ni29Co18 (known also as Kovar<sup>®</sup>). The so-called bathtub type package is fabricated by forming a sheet of the F-15 alloy over a set of successive dies. Holes for the leads are then punched in the bottom for plug-in packages and in the side for flat packages. A layer of oxide is then grown over the package body. Beads of borosilicate glass, typically Corning 7052 glass, are placed over the leads and in the holes in the package body. Heating the structure above the melting point of the glass (approximately 500°C) forms a reactive glass-to-metal seal. The molten glass dis-

solves some of the oxides on the alloy (primarily iron oxide), which, on cooling, provides the adhesion mechanism (see Fig. 8.38). The glass-to-metal seal formed in this manner has four distinctive layers.

1. Metal
2. Metal oxide
3. Metal oxide dissolved in glass
4. Glass

After the glass-to-metal seals have been formed, the oxide not covered by the glass must be removed and the metal surface plated to allow the package to be sealed and to allow the package leads to be soldered to the next higher assembly. The prime plating material is electrolytic nickel, although gold is frequently plated over the nickel to aid in sealing and to prevent corrosion. In either case, the package leads are plated with gold to allow wire bonding and to improve solderability. Although electroless nickel has better solderability, it tends to crack when the leads are flexed.

The glass-to-metal seal formed in this manner provides an excellent hermetic seal, and the close match in TCE between the glass and the F-15 alloy (approximately  $5.0 \times 10^{-6}/^{\circ}\text{C}$ ) maintains the hermeticity through temperature cycling and temperature storage. A cross section of metal package types is shown in Figs. 8.39 through 8.41.

Three types of lids are commonly used on metal packages: the domed lid, the flat lid, and the stepped lid. These are also fabricated with ASTM F-15 alloy with the same plating requirements as the packages. The domed lid is designed for use with platform packages and may be projection welded or soldered. The flat lid is designed for use with the tub package and is primarily soldered to the package. The stepped lid is fabricated by photoetching a groove in a solid sheet of F-15 alloy such that the flange is about 0.004 in thick. This lid is designed to be seam welded to a tub package. When lids are designed for

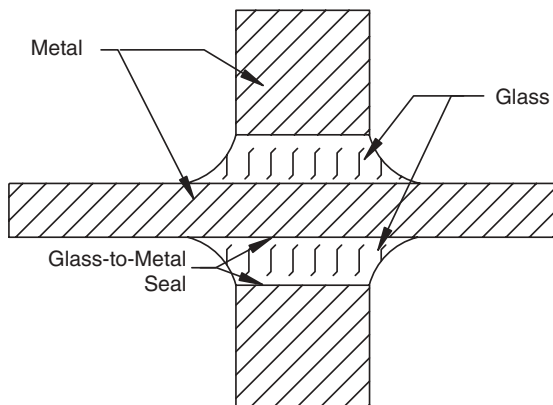
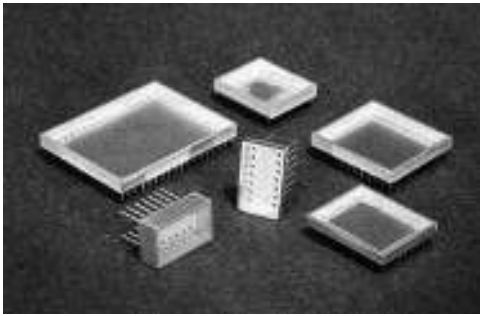


Figure 8.38 Glass-to-metal seal.



**Figure 8.39** Metal packages, platform and "bathtub."



**Figure 8.40** Metal packages, through-hole.



**Figure 8.41** Flat ("butterfly") package.

soldering, a preform of the desired solder material is generally attached to the outer perimeter of the bottom of the lid.

### 8.26.3 Methods of sealing metal packages

A flat or stepped lid may be soldered to the package by hand by the use of a heated platen or in a furnace. Although the platen is somewhat faster, the metal package acts as a heat sink, simultaneously drawing heat away from the seal area and raising the temperature inside the package unless the glass beads used for insulating the leads extend entirely around the periphery of the package—an obviously impractical arrangement. In addition, leaks through the solder, or "blow holes," caused by a differential in pressure be-

tween the inside and outside of the package, will occur unless the ambient pressure outside the package is increased simultaneously with the pressure that is created inside by heating the package. Because of the temperature rise inside the package, it is risky to use epoxy to mount components unless the glass beads extend around the periphery of the package as described above. Solder sealing may be accomplished in a conveyor-type furnace that has a nitrogen atmosphere. The nitrogen prevents the oxidation of the solder and also provides a benign environment for the enclosed circuit. Furnace sealing requires a certain degree of fixturing to provide pressure on the lid.

Parallel seam welding (Fig. 8.42) is accomplished by the generation of a series of overlapping spot welds by passing a pair of electrodes along the edge of the lid. The alignment of the lid to the package is quite critical and is best accomplished outside the sealing chamber, with the lid being tacked to the package in two places by small spot welds. A stepped lid greatly facilitates the process and improves the yield, because it requires considerably less power than a flat lid of greater thickness. The sealing process is relatively slow compared to other methods, but a package sealed by parallel seam welding can be easily delidded by grinding the edge of the lid away. Because the lid is only about 0.004 in thick in the seal area, this may be readily accomplished with a single pass of a grinding wheel. With minimal polishing of the seal area of the package, another lid may be reliably attached.

Certain classes of packages with a flange on the package may be sealed by a process called *projection* or *one-shot* welding. In this process, an electrode is placed around the flange on the package and a large current pulse is passed through the lid and the package, creating a welded seam. Heavy-duty resistance welding equipment capable of supplying 500 lb of pressure and 12,000 A per linear inch of weld is required for these packages. The major advantages of one-shot welding are process time and a less-expensive package. The major disadvantage is the difficulty of removing the lid and repairing the circuit inside. Delidding a projection-welded package is a destructive process, and the package must be replaced.

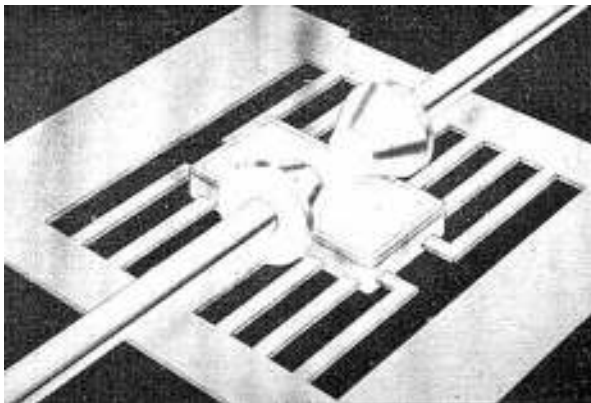


Figure 8.42 Parallel seam welding.

## 8.26.4 Ceramic packages



**Figure 8.43** Leadless ceramic chip carrier (internal).

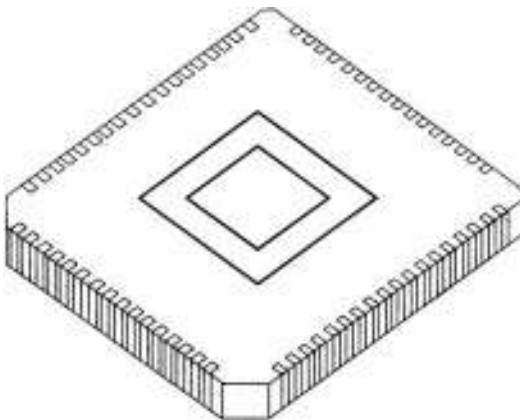
Ceramic packages in this context are considered to be structures that permit a thick or thin film substrate to be mounted inside in much the same manner as a metal package. Ceramic structures that have metallization patterns, which allow direct mounting of components, are referred to as *multichip ceramic packages*. Ceramic packages for hybrid circuits generally consist of three layers of alumina. The bottom layer may or may not

be metallized, depending on how the substrate is to be mounted. A ring of alumina is attached to the bottom layer with glass, and a lead frame is sandwiched between this ring and a top ring with a second glass seal. The top ring may be metallized to allow a solder seal of the lid or may be left bare to permit a glass seal. Various types of ceramic packages are shown in Figs. 8.43 through 8.45.

## 8.26.5 Methods of sealing ceramic packages

The most common method of sealing ceramic packages is solder sealing. During the manufacturing process, a coating of a refractory metal or combination of metals, such as tungsten or an alloy of molybdenum and manganese, is fired onto the ceramic surface around the periphery of the seal area. On completion, the surface area is successively nickel plated and gold plated. A lid made from ASTM F-15 alloy is plated in the same manner and soldered onto the package, usually with an alloy of Au80Sn20, in a furnace with a nitrogen atmosphere.

A less expensive, but also less reliable, method of sealing is to use a glass with a low melting point to seal a ceramic lid directly to a ceramic package. This avoids the use of gold altogether, lowering the material cost considerably.



**Figure 8.44** Leadless ceramic chip carrier (external).



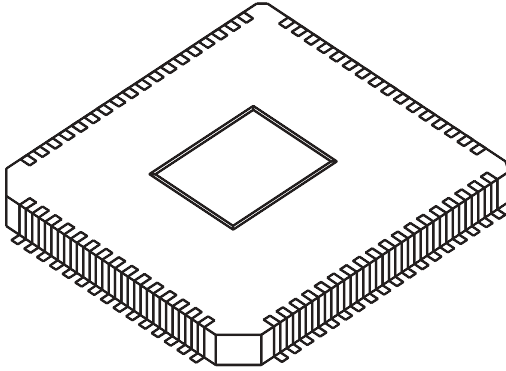


Figure 8.45 Leaded ceramic chip carrier.

The glass requires a temperature of about 400°C for sealing, as opposed to about 300°C for the AuSn solder. The glass seal is somewhat susceptible to mechanical and thermal stress, particularly at the interface between the glass and the package.

These two techniques have a common problem: it is difficult to remove the lid for repair without rendering the package useless for further sealing. An alternative approach seeing increased use is to braze a ring of ASTM F-15 alloy that has been nickel and gold plated as described above onto the sealing surface of the ceramic package. It is then possible to use parallel seam welding, with its inherent advantages for repair. This approach is also frequently used for ceramic multilayer packages designed for multichip packaging.

#### 8.26.6 Nonhermetic packaging approaches

The term *nonhermetic* package encompasses a number of configurations and materials, all of which ultimately allow the penetration of moisture and/or other contaminants to the circuit elements. Most techniques involve encapsulation with one or more polymer materials, with the most common being the molding and fluidized bed approaches.

Both injection and transfer molding techniques employ thermoplastic polymers, such as acrylics or styrenes, to coat the circuit. In transfer molding, the material is heated and transferred under pressure into a closed mold in which the circuit has been placed; in injection molding, the material is heated in a reservoir and forced into the mold by piston action.

The fluidized bed technique uses an epoxy powder kept in a constant state of agitation by a stream of air. The circuit to be coated is heated to a temperature above that of the melting point of the epoxy and is placed in the epoxy powder. The epoxy melts and clings to the circuit, with the thickness controlled by the time and the preheat temperature.

Both methods are used to encapsulate hybrids and individual devices, and both are amenable to mass production techniques. The overall process may be performed at a cost of only a few cents per circuit. The coatings are quite rug-

ged mechanically, are resistant to many chemicals, and have a smooth, hard surface suitable for marking.

### 8.26.7 Plug-in packages

Plug-in packages have leads protruding from the bottom with a lead spacing of 0.100 in. A special case of plug-in packages is the DIP package. Standard DIP packages are used to package individual die and have two rows of leads on 0.100-in centers, separated with each row being 0.300 in apart. Other package types designed for hybrid use (platform or bathtub) often are found to have a lead configuration consistent with the DIP design for commonality with test mounting sockets. An example is shown in Fig. 8.40.

Plug-in packages are designed for through-hole insertion into printed wiring boards. In addition to DIP packages, a single-in-line (SIP) packaging technique was developed for resistor and capacitor components and networks. For all plug-in packages, the leads provide a convenient method for ensuring clearance on assembly and providing a degree of compliance into the mechanical stress established by assembly or expansion coefficient mismatch between the package and the mounting substrate. DIP packages were the mainstay of discrete device packaging while device complexity was low. However, with the advent of very large scale integration (VLSI) devices and high I/O counts, the 100-mil lead centers required the development of very large packages. A standard 40-pin device required a length exceeding 2.00 in, and higher pin counts became increasingly difficult to package in DIP form.

### 8.26.8 Small-outline package

A small-outline (SO) package is shown in Fig. 8.46. The leads on the SO package are on 0.050-in centers, as opposed to 0.100-in centers for the DIP package. The SO has a low profile and occupies less than 50 percent of the area of the DIP. It weighs about one-tenth that of a DIP. The SO package family in-

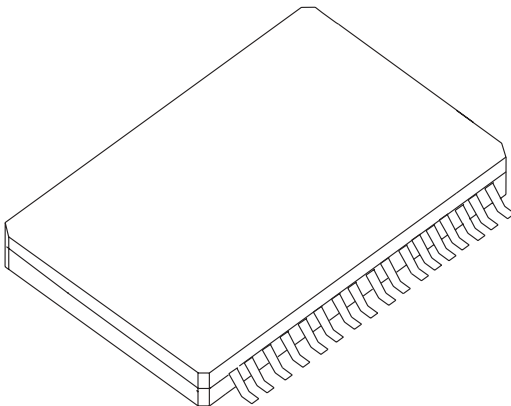


Figure 8.46 Small-outline package.

cludes packaging of passive devices; packages that contain ICs, known as SOIC packages; and packages that contain transistors, known as SOTs. Both plastic and ceramic SO packages are available.

### 8.26.9 Ceramic chip carriers

A special case of the ceramic package is the hermetic chip carrier as shown in Figs. 8.43 through 8.45. The wire bonding pads are routed to the outside between layers of ceramic and are connected to semicircular contacts called *castellations*. The most common material is alumina, which is metallized with a refractory metal during fabrication and then successively plated with nickel and gold. Most multilayer chip carriers are designed to be sealed with solder, usually Au80/Sn20.

Configurations of chip carriers for military applications have been standardized by JEDEC in terms of size, lead count, lead spacing, and lead orientation, although nonstandard carriers can be used for specialized applications. The most common lead spacing is 0.050 in, with high lead count packages having a spacing of 0.040 in.

The removal of heat from chip carriers in the standard “cavity-up” configuration has been a problem, because the only path for heat flow is along the bottom of the carrier and out to the edge of the carrier, where it flows down to the substrate through the solder joints. This problem can be alleviated to a certain extent by printing pads on the bottom of the carrier, which are soldered directly to the substrate. This lowers the thermal impedance by a factor of several times. If this does not prove adequate, carriers with the cavity pointing down can be utilized. In this configuration, the chip is mounted on the top of the carrier in the upside-down position, the lid is mounted in a recess on the bottom of the carrier, and a heat sink is mounted to the top to enable the heat to be removed by convection. Beryllia and aluminum nitride chip carriers are being used to package high-power devices,

Devices mounted in chip carriers can be thoroughly tested and burned in before mounting on a substrate or printed circuit board. This process can be highly automated and is frequently done in military applications. Sockets exist for standard sizes that make contacts to the castellations without the necessity of solder.

Chip carriers have proven to be a viable approach for packaging hybrid circuits of minimal size. Although available with pin counts up to 128, chip carriers have proved to be a reliability risk when the pin count is greater than 84, because the net expansion of the carrier at temperature extremes (and therefore the stress on the solder joints) is proportional to its size. Furthermore, the temperature at which chip carriers may be used on PC boards is limited because of the difference in the coefficient of expansion (TCE) between the carrier and board material.

As the solder joint is made higher, the difference in TCE becomes less significant. The highest solder column that can be made by ordinary means is about 0.007 in. Above this height, a molten solder column begins collapsing of its own weight. Power cycling, in which the device in the carrier is powered on

and off at periodic intervals, has proven to be a serious reliability risk, even more than temperature cycling, when power devices are mounted. While the device in the carrier is being power cycled, the carrier and the board are in a nonequilibrium state with respect to temperature. This causes considerable stress on the solder joints, ultimately resulting in failure from metal fatigue.

#### 8.26.10 Packages for power hybrid circuits

As the power requirements of package materials have become more demanding, ASTM F-15 alloy and alumina become less attractive because of their relatively low thermal conductivity. Copper, molybdenum, copper-clad materials, aluminum nitride, and beryllia have all been used to manufacture packages. This requires some innovation on the part of the package manufacturer to develop methods of sealing and through-hole connections, given that copper is not amenable to seam welding or glass-to-metal sealing.

One type of power package uses a cavity machined from a solid block of copper, plated with nickel and gold, with a stainless steel seal ring brazed around the perimeter as shown in Fig. 8.47. The leads are made from copper-cored Alloy 52 material with a ceramic insulator. The insulator is generally metallized on the outside with an alloy of MbMn successively plated with Ni and Au. The pins are individually soldered to the package body with 80Au/20Sn solder. This package is compatible with conventional seam welding and offers the best thermal conductivity of the various configurations when oxygen-free high-conductivity (OFHC) copper is used. The copper must be processed such that the cold-worked mechanical properties are not destroyed to enable the package to withstand the constant acceleration test. This limits the temperature range that the package can see during processing and use.

An alternative method of attaching the leads to the package is to use a glass with a low melting point, such as potash soda barium glass, which has a dif-

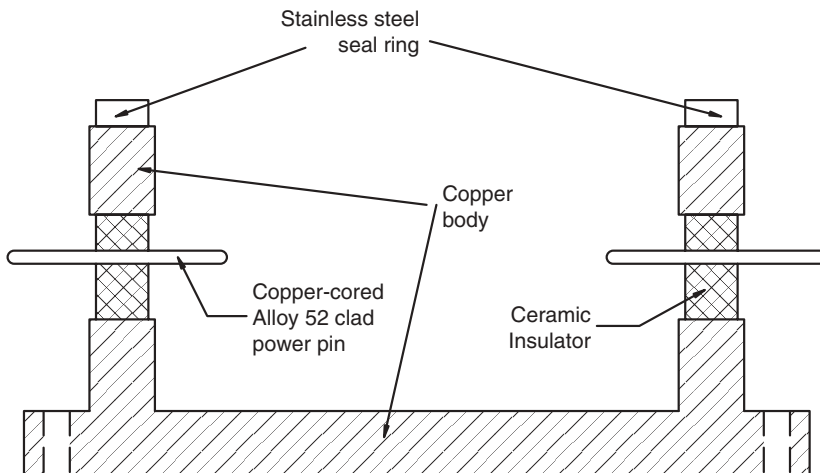


Figure 8.47 Solid copper package.

ferent temperature coefficient of expansion (TCE) from that of the package material such that a compression seal is formed.

Another approach uses a copper base that has an ASTM F-15 lead frame brazed to it and is plated with Ni and Au. This package can use conventional glass-to-metal sealing in the manufacturing process and is compatible with parallel seam welding. This package must be less than 1 × 1 in and must use a copper base less than 0.060 in thick because of the large TCE mismatch between copper and ASTM F-15 alloy.

## 8.27 Multichip Modules

Multichip modules are an extension of the hybrid technology. They permit a higher packaging density than can be attained with other approaches, allowing a silicon-to-substrate area ratio of greater than 30 percent. There are three branches of the MCM technology as depicted in Table 8.32:<sup>17</sup> MCM-L, based on a laminated printed circuit board structure; MCM-C, based on cofired ceramic structures; and MCM-D, which utilizes deposited conductors and dielectrics.

**TABLE 8.32** Types of Multichip Modules

MCM-L	Substrates formed by <i>laminating</i> layers of printed circuit board material to form multilayer interconnection structures
MCM-C	Substrates formed by cofired <i>ceramic</i> or glass/ceramic structures, similar to the thick film process
MCM-D	Interconnections formed by depositing alternate layers of conductors and dielectrics onto an underlying substrate, similar to the thin film process

### 8.27.1 The MCM-L technology

The MCM-L technology is based on printed circuit board technology. Multilayer structures are formed by etching patterns in copper foil laminated to both sides of resin-based organic panels (“cores”) that are laminated together with one or more layers of the basic resin in between to act as an insulator. Interconnections between layers may be formed by “through” vias, which extend all the way through the board; “blind” vias, which extend from the surface part way through the board; or “buried” vias, which connect only certain of the inner layers and do not extend to the surface in either direction as shown in Fig. 8.48. Through vias may be drilled and plated after laminating, whereas blind and buried vias must be drilled and plated prior to laminating.

A number of materials may be used to fabricate MCM-L structures as shown in Table 8.33.<sup>18</sup> The criteria for selection will vary with the application. Cyanate ester, for example, has a very low dielectric constant and excellent high-frequency characteristics.

Design guidelines for MCM-L substrates are presented in Table 8.34. Printed circuit boards for MCM applications must be suitable for wire bond-

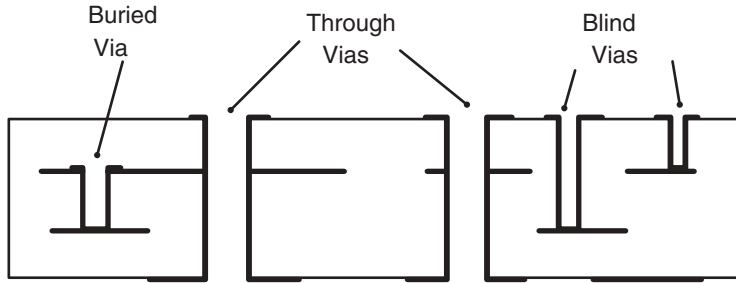


Figure 8.48 Buried, through, and blind vias.

TABLE 8.33 Properties of MCM-L Substrate Materials

Property	Units	Bismaleimide-triazine/epoxy	Polyimide	Cyanate ester	Sycar
Physical					
Water absorption	%	1.3	0.35	0.8	0.02
Specific gravity			1.7		1.6
Chemical resistance (solvents)		Excellent	Excellent	Excellent	Excellent
Mechanical					
Glass transition temperature by DMA ( $T_g$ )	°C	175–200	220–280	180–260	180
Coefficient of thermal expansion (z-axis)*	in/in/°C	$7.0 \times 10^{-5}$ 25–2208°C	$3.5 \times 10^{-5}$ 25–220°C	$8.1 \times 10^{-5}$ 25–245°C	$8.5 \times 10^{-5}$ 25–190°C
Coefficient of thermal expansion (x-y axis)*	in/in/°C		$1.4 \times 10^{-5}$ 25–220°C	$1.5 \times 10^{-5}$ 25–245°C	$1.5 \times 10^{-5}$ 25–190°C
Dimensional stability (x-y axis) after elevated temperature	in/in	0.0005	0.0005	0.0003	0.00036
Flexural strength (>0.020 in)	psi				
Lengthwise			80,000		50,000
Crosswise			65,000		43,000

\*CTE can be lowered by selection of alternative fibers such as Kevlar or by use of constraining metal cores such as Cu-In-Cu.

ing. This is accomplished by selectively plating nickel and gold on the copper traces as required. The difference in gold thickness is a result of the different bonding mechanism between gold and aluminum wire. Gold wire bonding is accomplished by thermosonic bonding and is fundamentally a gold-to-gold bond, whereas aluminum wire bonding is accomplished by ultrasonic bonding and is an aluminum-nickel bond. Gold plating for aluminum bonding is thin-

TABLE 8.34 Design Guidelines for MCM-L Substrates

Parameter	Value
Minimum metal spacing	0.003 in
Minimum trace width/maximum trace thickness	0.003/0.0018 in
Minimum Pth pad diameter	0.015 in
Surface layer nickel thickness, $\mu$ n	30+
Aluminum/gold wire bonding, $\mu$ in	100–200
Surface layer gold thickness, $\mu$ in	10+
Aluminum wire bonding, $\mu$ in	10–40
Gold wire bonding, $\mu$ in	50–100
Minimum blind via diameter	0.006 in
Minimum finished hole diameter	0.010–0.000 in
Minimum buried via diameter	0.006 in
Minimum via pitch (no tracks)	0.015 in

ner, because it acts only to keep the nickel from oxidizing and interfering with the bonding process.

### 8.27.2 The MCM-C technology

MCM-C multilayer structures are fabricated from ceramic or ceramic/glass materials, with alumina being the primary base. There are two basic types of MCM-C substrates: high-temperature cofired ceramic (HTCC) and low-temperature cofired ceramic (LTCC). Both processes begin with thin sheets of unfired material, approximately the consistency of putty. The sheets are referred to as *green tape*. Green tape is created by mixing the base powder with an organic vehicle and forming it into sheets by doctor blading or other means. Vias are punched in the green tape where interconnections between layers are to be made and filled with thick film paste designed specifically for via filling. The individual layers are printed with thick film paste to create the metallization patterns, aligned with the other layers, and laminated at elevated temperature and pressure. The laminated structures are then subjected to a lengthy bake-out cycle to remove the organic material and cofired at an elevated temperature to form a monolithic structure.

The HTCC and the LTCC processes differ in two primary ways: the firing temperatures and the thick film materials.<sup>5</sup> HTCC ceramics are designed to be fired at approximately 1600°C, which requires the use of refractory metals such as tungsten and molybdenum/manganese alloys as the conductors, and the firing process must take place in a reducing atmosphere to avoid oxidation of the metals. The top and bottom metallization layers are plated with nickel

and gold to permit die and wire bonding. LTCC materials primarily consist of glass/ceramics and are designed to be fired at much lower temperatures, in the range of 850 to 1050°C. This permits the use of standard thick film materials, such as silver and gold, which have much lower sheet resistivity than the refractory metals and do not require subsequent processing for assembly. A comparison of the HTCC and LTCC processes is shown in Table 8.35.

**TABLE 8.35 Comparison of HTCC and LTCC MCM-C Substrates**

Parameter	Units	Cofired ceramic (Al <sub>2</sub> O <sub>3</sub> )	Cofired glass/ceramic
Line width	μm (min.)	100	100
Via diameter	μm (min.)	125	125
Number of metal layers		1–75	1–75
Conductor resistance	mΩ/□	8–12	3–20
Relative permeability	@ 1 MHz	9–10	5–8
Dissipation factor	@ 1 MHz	5–15 × 10 <sup>-4</sup>	15–30 × 10 <sup>-4</sup>
Insulation resistance	Ω-cm	> 10 <sup>14</sup>	10 <sup>12</sup> –10 <sup>15</sup>
Breakdown voltage	V/25 μm	550	800
Resistor values	Ω	N/A	0.1–1 M
Coefficient of thermal expansion	ppm/°C	6.5	3–8
Thermal conductivity	W/m-°C	15–20	2–6
Camber	mils/in	1–4	Conforms to setter
Surface roughness	μin	10–25	8–10
Flexural strength	MPa	275–40	150–250

As a result of the organic burnout, the substrates shrink during firing. The shrinkage is very predictable, however, and may be accounted for during the design stage. This property is very critical when selecting a via fill material. The shrinkage of the via fill material must match that of the ceramic to prevent open circuits between layers.

Resistors and capacitors that are compatible with the LTCC green tape process may also be fabricated.<sup>19</sup> A distinction is made here between a sandwiched resistor, which is formed between two layers of green tape, and a buried resistor, which is printed on an alumina substrate and covered with layers of green tape. The resistor pastes developed for this process show a high degree of stability after several refrings at high temperatures and exhibit TCRs comparable to those of standard materials (<100 ppm/°C). Although the accuracy of untrimmed resistors is adequate for many digital circuit applications, buried resistors printed and fired on the substrate may be



laser trimmed prior to lamination with green tape. These show excellent stability under conditions of high-temperature storage, temperature cycling, and harsh environments, because they are covered with hermetic dielectric.

### 8.27.3 The MCM-D technology

The MCM-D technology utilizes processes similar to those used to fabricate thin film hybrid circuits. The conductors are primarily sputtered or plated metals, gold, aluminum, or copper deposited on a variety of substrate materials, including ceramic and silicon. The dielectric materials are primarily used in the liquid state and are applied by spinning. Vias may be opened in the dielectric film by applying photoresist and etching or by using photosensitive dielectric materials. A list of common dielectric materials is shown in Table 8.36.<sup>20</sup>

MCM-D structures can be made much denser than the other types as a result of the photoetching process. Line widths of 10  $\mu$  and via diameters of 15  $\mu$  are common.

### 8.27.4 Summary

Multichip modules are an important part of the repertoire of the packaging engineer for at least two reasons.

1. By utilizing the increased density available with this technology, more functionality can be incorporated into a smaller volume with all the advantages that this ability encompasses.
2. The variety of materials enables the substrate/interconnection structures to be more nearly tailored to a particular application.

A comparison of the various MCM technologies is given in Table 8.37.

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**TABLE 8.36 Properties of Selected Commercial Polymer Dielectrics**

Vendor	Material	Photosensitive	Wet etchable?	Dielectric constant	CTE (ppm)	T <sub>g</sub> (°C)	Flexural modulus (GPa)	Tensile strength (MPa)	Elongation (%)
Amoco	UD-4212		Y	2.9	50	300		110	15–20
Ciba-Geigy	PROB-400	Y		3.3	40		3.5	124	10
Dow	BCB-3002			2.7	52	>350	3.3	80	8
	BCB-19010	Y		2.7	52	>350			
DuPont	PI-2555			3.3	40	>320	2.4	130	15
	PI-2611D			2.9(z), 3.9 (x, y)	20.3*	>400	8.9	340	25
	PI-2722	Y		3.3	40	310	–	130	15
	PI-2741	Y		2.9(z)	10*	365		330	50
	PI-1111		Y	2.8(z)	19*	385		300	55
Hitachi	PIQ-13			3.4	45–48	>350		116	10
	PI-L100				3*			385	35
	PL-2315	Y		3.3	40	–	3.5	124	10
Nat'l. Starch	EL-5010			3.2	38	214		154	7
Toray	UR-3800	Y		3.3	45	280	3.4	145	30

\*Properties are anisotropic.

TABLE 8.37 Comparison of MCM Technologies

Parameter	Units	MCM-L	MCM-C	MCM-D
Description		High-density laminated printed circuit board	Cofired low dielectric constant ceramic substrate	Thin film on silicon
Maximum wiring density	cm/cm <sup>2</sup>	300	800	250–750
Minimum line width	μm	60–100	75–100	8–25
Line space	μm	625–2250	50–450	25–75
Maximum substrate dimension	mm	700	245	50–225
Dielectric constant		3.7–4.5	5–5.9	3.5
Pinout grid	mm	Array 2.54	Array 1.00–2.54 (staggered)	Peripheral 0.63
Maximum number of wiring layers		46	63	8
Via grid	μm	1250	125–450	25–75
Via diameter	μm	150–500	50–100	8–25

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# Adhesives, Underfills, and Coatings in Electronics Assemblies

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## 9.1 Introduction

Adhesives play an important role in the manufacturing of high-density surface mount assemblies. Adhesives are used to secure components during processing (chip bonders or surface mount adhesives), form an electrical or thermal interconnection (conductive), increase reliability (flip-chip and CSP underfill), and even protect the entire device once assembly is completed (conformal coating). This chapter will discuss some of the important physical properties related to these polymeric materials such as rheology, glass transition temperature ( $T_g$ ), coefficient of thermal expansion (CTE), and methods of curing. With respect to the various applications, a majority of the discussion will focus on the surface mount adhesives, but other applications will also be discussed.

When choosing an adhesive system to use within an application, several factors need to be considered. First are the properties of the uncured material, such as shelf life, pot life, and rheology. Second, the method by which the adhesive is processed, dispensed, and applied relates back to the rheology, and the method of curing must also be considered (e.g., heat or ultraviolet radiation). Finally, the properties of the final cured material are significant. Typically, one starts with the final item and works backward, but all three factors play an important role in selecting the correct material for an application.

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This chapter will first discuss these properties in detail to provide a better understanding of adhesives. Then, different applications using adhesive materials will be reviewed. Knowledge of these properties and an understanding of the applications will aid design and production engineers in selecting the right material for a particular product.

## 9.2 Rheology

Rheology is an often misunderstood but important property for adhesives used in electronics assembly. Rheology is the science of the deformation and flow of matter. Simply, how does matter react when you push it? Does it flow easily or with difficulty, or does it not flow at all but bounce back? The whole concept of rheology, flow behavior, and the terms involved can be summarized in Fig. 9.1.

Consider an amount of liquid of thickness  $x$  between two parallel plates. (For clarity, Fig. 9.1 shows this as a two-dimensional area.) The bottom plate is kept stationary while the top plate is forced to move. The liquid can be considered to be made up of layers that move relative to each other. This relative movement of layers is known as *shearing*. To characterize this process, only three parameters can be measured.

1. *Dimensions of the material.* This is trivial and is governed by the geometry of the particular system. Units are meters.
2. *Force applied.* This is how hard the upper plate is pushed. Units are newtons (N). The force required to move the upper plate is obviously related to the area of the plate. It is therefore conventional to divide the force by the area to give the *stress*,  $\tau$ .

$$\text{Stress} = \tau = \frac{\text{Force (N)}}{\text{Area (m}^2\text{)}} \quad \text{Units} = \text{N}\cdot\text{m}^{-2} = \text{Pa}$$

3. *Velocity.* This is the speed of the upper plate relative to the lower. Units are meters per second ( $\text{ms}^{-1}$ ).

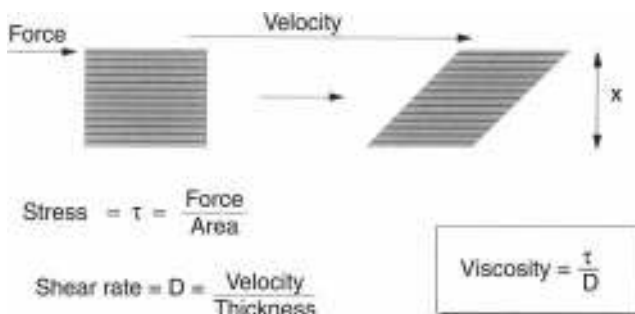


Figure 9.1 Basic rheology concepts.

The layered structure of the material is analogous to a pack of cards. The thicker the pack, the less each card moves relative to its neighbors for a given movement of the upper plate, and the lower the shearing. Thus, we can define a *shear rate*,  $D$  (or  $\dot{\gamma}$ ), as

$$\text{Shear rate} = D = \frac{\text{Velocity (m}\cdot\text{s}^{-1})}{\text{Thickness (m)}} \quad \text{Units} = \text{s}^{-1}$$

The shear rate is obviously related to the shear stress in some manner. We define the ratio of these two to be the *viscosity*,  $\eta$ .

$$\text{Viscosity} = \eta = \tau/D \quad \text{Units} = \text{Pa/s}^{-1} = \text{Pa}\cdot\text{s}$$

So, it can be seen that the *viscosity is not a fundamental, measurable property of a material* in the same way that mass is. It is merely the constant of proportionality between shear stress and shear rate.

Some typical viscosities are shown in Table 9.1. Although the formal unit is Pas, it is common to see viscosity represented in mPa, because water has a viscosity of 1 mPa. Note that air has a viscosity of approximately 1/100 of that of water (0.01 mPa) even though it is a gas.

**TABLE 9.1 Typical Viscosities**

Material	Viscosity/Pa
Bitumen	100,000,000
Polymer melt	1,000
Golden syrup	100
Liquid honey	10
Glycerol	1
Olive oil	0.01
Water	0.001
Air	0.00001

Typical shear rates of some common processes are shown in Table 9.2. Processes that have very small sample thicknesses, such as brushing or rubbing, have extremely high shear rates, up to  $10^6 \text{ s}^{-1}$ . At the other extreme, sedimentation involves very small relative movement of layers and therefore is still a shearing process, with a typical value of  $10^{-6} \text{ s}^{-1}$ .

### 9.2.1 Rheological response and behavior

If a sample is sheared at different shear rates, and the corresponding stress required is measured, the data can be plotted to form a *flow curve* (see Fig. 9.2). This is basically a spectrum that can be used to characterize the flow behavior of a material. The simplest response is termed *Newtonian*. This designates that the shear stress varies linearly with shear rate over the entire range. If the corresponding viscosity is calculated and plotted, the resulting

TABLE 9.2 Typical Shear Rates

Process	Shear rate/s <sup>-1</sup>
Sedimentation	0.000001 – 0.0001
Leveling	0.01 – 0.1
Draining	0.1 – 10
Chewing	1 – 100
Brushing/pumping	1 – 1,000
Rubbing	10,000 – 1,000,000

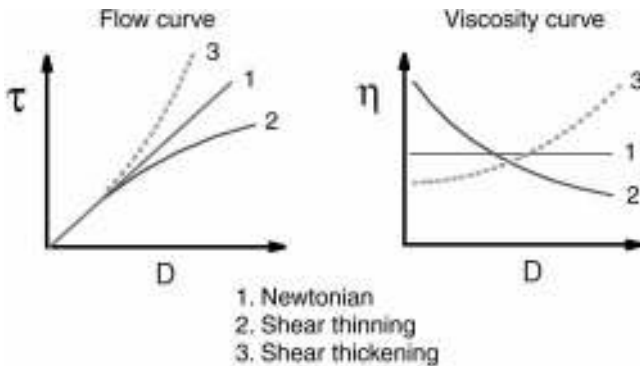


Figure 9.2 Simple rheological response.

graph is termed a *viscosity curve*. For Newtonian materials, the viscosity is constant at all shear rates. Examples of Newtonian fluids include water, ethylene glycol, simple oils, Loctite 270, and cyanoacrylate monomers.

The majority of fluids are not Newtonian. Most materials require less stress than might be expected at higher shear rates. The viscosity will therefore decrease with increasing shear rate. Such materials are described as being *shear thinning* or *pseudoplastic*. Examples are polymer melts, blood, and solder paste.

A wide variety of molecular arrangements can give rise to shear thinning behavior. Some of these are illustrated in Fig. 9.3. A common example occurs when irregularly shaped particles line up in the direction of the flowing liquid. They present a smaller surface area, there is less viscous drag, and consequently less shear stress is required than might be expected. As soon as the shearing is stopped, Brownian motion ensures that the particles become randomly oriented once again.

Other processes that can lead to shear thinning behavior are also shown in Fig. 9.3. These include stretching of long-chain polymer molecules, deformation of soft pliable particles, and the breaking up of agglomerates (disaggregation). A classic example of a shear thinning fluid is blood. On shearing, the red blood cells deform to thimble shapes. This reduces their diameter and facilitates passage through the smaller blood vessels.

**9.2.1.1 Thixotropy.** The shear thinning behavior described above is not time dependent. This means that the same viscosity is obtained at a particular



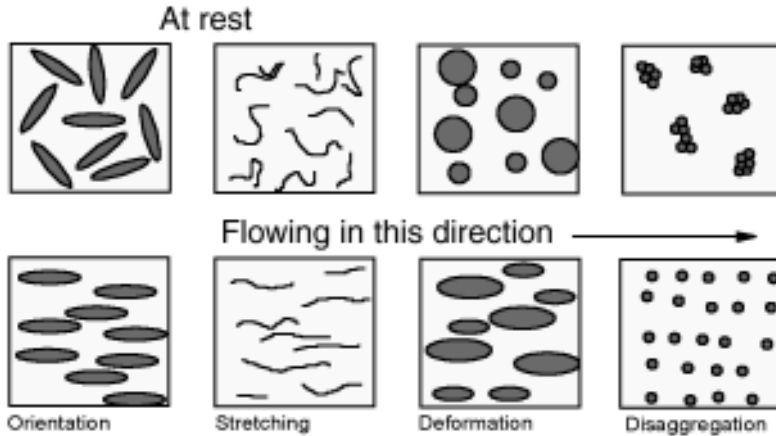


Figure 9.3 Shear thinning behavior of dispersions.

shear rate no matter how long the sample is sheared at this rate. In other words, there is no hysteresis in the viscosity curves for increasing or decreasing shear rates. The situation in which there *is* time dependency is called *thixotropy*. This is illustrated in Fig. 9.4. A material whose viscosity drops with time when held at a constant shear rate is termed thixotropic.

The effect on such a material of cycling the shear rate is shown in Fig. 9.4. Increasing the shear rate (*up curve*) gives rise to the normal shear thinning behavior. However, on subsequently decreasing the shear rate (*down curve*), much less stress is required. The result is a hysteresis or *thixotropic loop* between the two curves. An alternative way of detecting thixotropy is by plotting the viscosity at a constant shear rate as a function of time. A Newtonian or simple shear thinning product will show no change, but a thixotropic material will show a decrease in viscosity with time. Another characteristic of thixotropy is that a sample will regain its original structure when left unsheared for a while.

The standard everyday example of a thixotropic material is tomato ketchup. Ketchup is so thick that it will not pour out of the bottle. However, a few moments of rapid shaking (shearing) will reduce its viscosity sufficiently so that

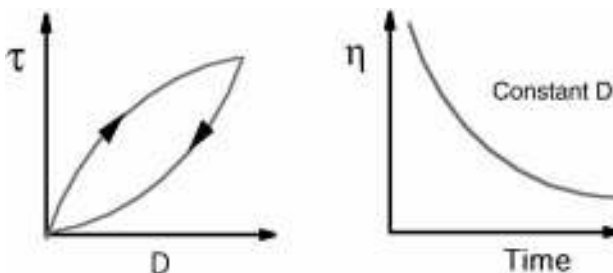


Figure 9.4 Rheological response of a thixotropic fluid.

it can be poured. It is not simply shear thinning—the longer it is shaken, the lower its viscosity. When the ketchup is left for a few hours, the structure rebuilds. Cough syrup is also thixotropic. When it is formulated in the plant, it is capable of being pumped down pipelines into the bottles. Its thixotropic nature means that it rebuilds its structure in the bottle, thereby preventing sedimentation of the drug from the syrup.

Thixotropy is a very useful property in some adhesive products. Whenever there is a need to pump a high-viscosity paste through a nozzle, thixotropy is of great benefit. For example, epoxy chip bonders have very high viscosities, but they are capable of being pumped through syringe needles of 400  $\mu\text{m}$  or less. They restructure rapidly to prevent slumping of the product on the circuit board. The rheology of SMA is discussed in more detail later (Sec. 9.3).

The most common raw material that imparts thixotropy (a *thixotrope*) is silica. This consists of roughly spherical silicon dioxide particles with diameters in the region of 100 nm. These do not exist individually but form *aggregates*. These in turn clump together to form *agglomerates*. When a dispersion of such agglomerates is left to stand, a three-dimensional network builds up (Fig. 9.5). This gives the product (which is now a *gel*) its structure, very much like reinforcements in concrete. The attractive forces between the agglomerates that drive this structuring can be either hydrogen bonding or Van der Waals' forces.

When the gel is sheared, the network breaks down and flow is facilitated. The cycle is reversible but *time dependent*. The longer the shearing, the more the structure breaks down. At rest the material gradually regains its structure until the entire network is rebuilt.

## 9.2.2 Measuring rheology

**9.2.2.1 Brookfield viscometry.** One piece of equipment used to measure viscosity is the Brookfield viscometer, shown schematically in Fig. 9.6. This consists of a disk, or spindle, which is placed in a beaker of the product (400 ml) in a wa-

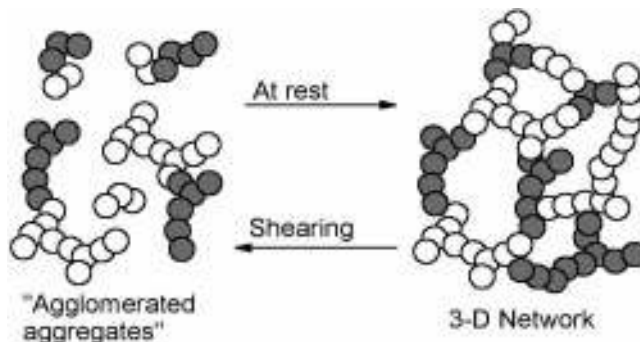


Figure 9.5 Particle interactions in a silica dispersion.

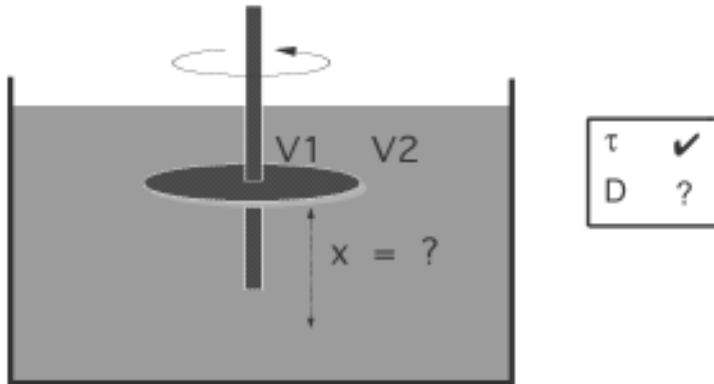


Figure 9.6 Brookfield viscometer.

ter bath at 25°C. For the majority of instruments, the spindle can rotate at a limited number of defined speeds, and the instrument gives a reading of “viscosity.” This is suitable for Newtonian products, but measurement of shear thinning materials presents problems.

This is shown by an examination of Fig. 9.6. The two parameters required for the determination of viscosity are shear stress,  $\tau$ , and shear rate,  $D$ . The stress required to keep the spindle rotating at a particular rpm is measured accurately by a torque spring on the instrument. The shear rate, however, is more problematic. Recall that this is defined as the velocity,  $v$ , divided by the sample thickness,  $x$ . Neither of these parameters can be accurately measured. A rotating disk has a wide range of velocities, with the outside of the disk moving much faster than the inside. The thickness of a sample that is undergoing shear,  $x$ , is undefined. Hence, it is impossible for the shear rate,  $v/x$ , to be determined.

This is not a problem for Newtonian liquids, given that the viscosity is independent of the shear rate. In fact, the Brookfield system was developed for the petroleum industry, where many fractions of Newtonian oils of various viscosities need to be examined. However, for shear thinning materials, an undefined shear rate means that *the viscosity cannot be defined*. This is particularly relevant at low shear rates at which the viscosity declines rapidly.

Therefore, any measurement of Brookfield “viscosity” for non-Newtonian fluids is not an absolute value. It is only a relative number, which depends on the *particular spindle* used, the *spindle speed*, and the *time taken*.

**9.2.2.2 Cone-and-plate (Haake) rheometry.** Many of the problems with Brookfield viscosity, outlined above, can be overcome using a cone-and-plate system. There are a number of manufacturers of such equipment, including TA Instruments, Rheometrics, Bohlin, and Haake. Figure 9.7 shows a schematic diagram of the Haake configuration. The sample (1 to 2 ml) is placed between a cone and a plate that is thermostatically controlled to  $\pm 0.1^\circ\text{C}$ . The plate is stationary, but the cone (which can be 2 to 5 cm in diameter, with an angle of  $1^\circ$  to

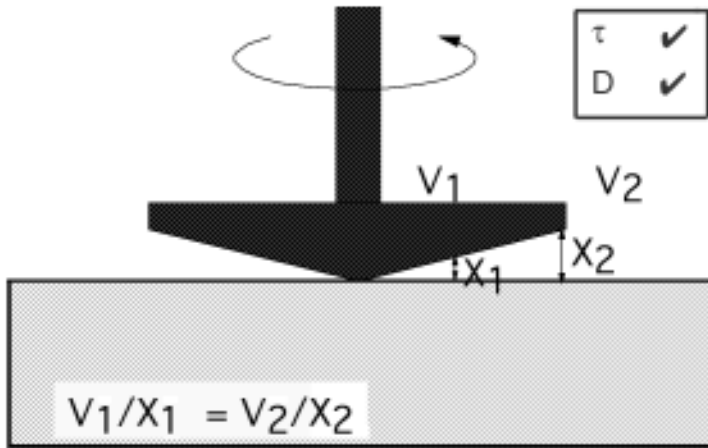


Figure 9.7 Cone-and-plate configuration.

4°) rotates at controlled, programmable rates. As in the case of the Brookfield, the stress required to turn the cone can be measured accurately.

Analysis of the shear rate measurement is shown in Fig. 9.7. As before, the velocity along the cone is greatest at the outside (i.e.,  $v_2 > v_1$ ). However, this time, the thickness of the sample is well defined and greater at the outside of the cone than the inside (i.e.,  $x_2 > x_1$ ). The angle of the cone is designed such that  $v_2/x_2 = v_1/x_1$ . In other words, *the shear rate is precisely defined and constant throughout the whole of the sample*. The viscosity,  $\tau/D$ , can therefore be calculated accurately and can be compared with the results obtained from any system that uses a well defined shear rate.

There are a number of advantages of the cone-and-plate system.

- As outlined above, the shear rate, and therefore the viscosity, are precisely defined.
- A very small sample size is used.
- The temperature of the sample is controlled very precisely, and temperature equilibrium is reached within a matter of minutes.
- A wide range of shear rates is possible—up to  $1,000 \text{ s}^{-1}$ . The shear rates are programmable, so a continuous “spectrum” can be obtained.
- It is possible with the cone-and-plate system to perform a number of sophisticated measurements, such as yield point determination, pipe flow prediction, and temperature profile.

An example of the importance of using this method with a non-Newtonian fluid is the type of output obtained from the cone-and-plate rheometer of an SMA material in Fig. 9.8. Clearly, this is a dramatically shear thinning product, so the question, “what is the viscosity of this SMA?” is meaningless unless the shear rate is specified. The Brookfield viscometer will give a number, but what does that mean? The shear rates involved in the Brookfield are low (ap-

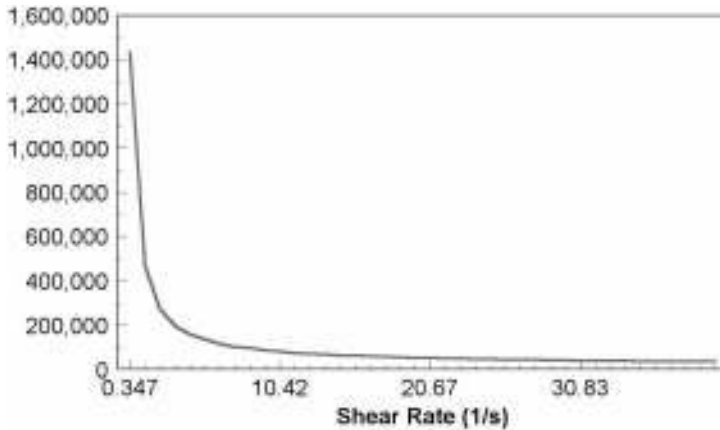


Figure 9.8 Viscosity curve for a chip bonder.

prox. 1 to 10  $s^{-1}$ ). This is where the curve is most steeply sloped and therefore where the greatest error occurs. The Brookfield and cone-and-plate systems are compared in Table 9.3.

TABLE 9.3 Comparison of Brookfield and Cone-and-Plate Systems

Haake cone-and-plate	Brookfield
• Small sample size (2 ml)	• Large sample size (400 ml)
• Shear rate defined	• Shear rate undefined
• Wide range possible	• Single “point” measurement only
• Rapid temperature equilibration	• Long temperature equilibration time
• Yield point	• Cheap (approx. \$3,000)
• Temperature profile	
• Pipe flow prediction	
• Expensive (approx. \$40,000)	

**9.2.2.3 Yield point measurement.** If the viscosity curve of Fig. 9.8 is replotted as a flow curve (stress versus shear rate), the result is Fig. 9.9. Again, it is clearly shear thinning behavior; however, the most obvious feature is the fact that there is a distinct intercept on the y-axis. This intercept is termed the *yield point*,  $\tau_0$ , or *yield stress*, and can be defined as the minimum stress required to get the material to flow. It can be thought of as being the material’s inertia. It is analogous to the force required to push start a motorbike (low  $\tau_0$ ) compared to a Mercedes car (high  $\tau_0$ ).

Examination of the flow curve of Fig. 9.9 shows that stresses of up to 400 Pa are insufficient to get the sample to move. This is particularly evident when

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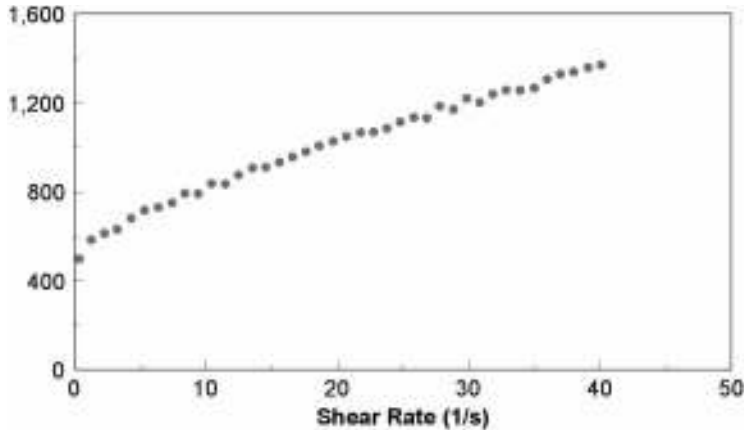


Figure 9.9 Flow curve (linear) for a typical chip bonder.

the data are replotted on a logarithmic scale (Fig. 9.10). Above 500 to 600 Pa, a low shear rate is achieved. The value of  $\tau_0$  is therefore somewhere between 400 and 600 Pa. Calculation of the yield point is not particularly straightforward. Figure 9.9 indicates that the curve is very rapidly changing at low shear rates. Therefore, an intercept cannot be manually read from the graph; some sort of mathematical equation must be used.

There are quite a number of mathematical models describing rheological behavior, the simplest of which is Newtonian ( $\tau = \eta D$ ). Table 9.4 shows just some examples. The Haake software can be used to fit the data from a flow curve to a model. Often, a number of different models fit the data equally well. So which one should be used? An equation that may be used to calculate the yield point is the *Casson model*. This is partly because it generally fits the data very well, but it is also used for reasons of consistency. The yield points derived from different equations cannot be compared to one another. Therefore, once it

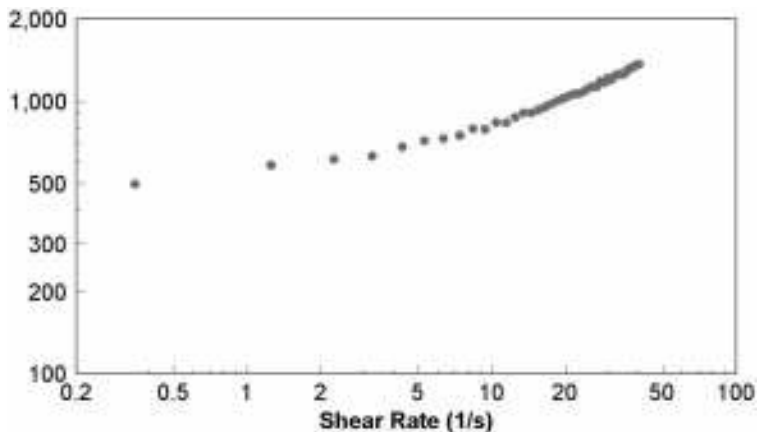


Figure 9.10 Flow curve (logarithmic) for a typical chip bonder.

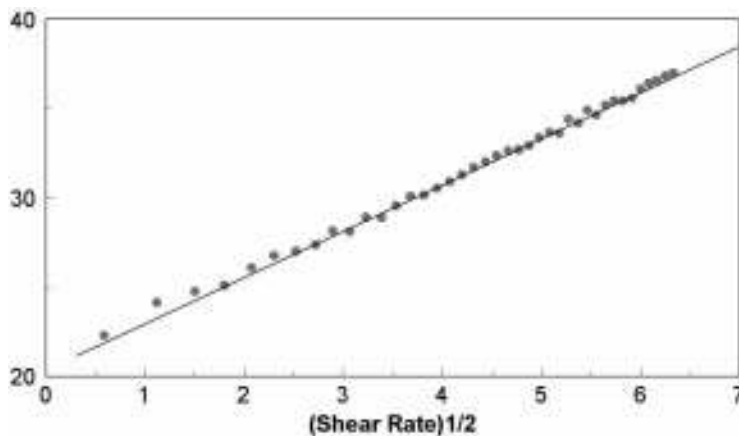
has been decided to use a particular model to characterize a particular adhesive, it makes sense to continue to use it.

**TABLE 9.4 Mathematical Models**

Model	Expression
Bingham	$\tau = \tau_0 + \eta D$
Ostwald (power law)	$\tau = aD^n$
Herschel Bulkley	$\tau = \tau_0 + aD^n$
Casson	$\sqrt{\tau} - \sqrt{\tau_0} = \sqrt{\eta_\infty} D$

The Casson model predicts that the square root of shear stress varies linearly with the square root of shear rate. When the data of Fig. 9.10 are plotted in this way, the result is Fig. 9.11. A straight line is indeed obtained. The intercept,  $\tau_0^{1/2}$ , is just above 20, which gives a yield point of just over 400 Pa as expected.

A word of caution about yield point: the estimated value of  $\tau_0$  depends to a large extent on the experimental conditions. When a force is applied against any material, it will eventually flow or deform if the time scale of the experiment is sufficiently long. For example, even though a glacier is a mass of solid ice (which apparently would have a huge yield point), it still flows like a river on geological time scales. Also, it is well known that glass can flow. Windows in very old buildings are significantly thicker at the bottom than at the top, as a result of the “solid” glass flowing merely under the force of gravity. There-



**Figure 9.11** Casson plot data.

fore, there is no absolute value of yield point for a material. Its significance lies in comparing values of different materials under the exact same experimental conditions. For an example of how this parameter is useful in predicting material behavior, see Sec. 9.7.1.10.

### 9.3 Curing of Adhesive Systems

The adhesive and polymer systems discussed in this chapter all start as a liquid or a paste that must be cured to achieve the final properties presented in their respective technical data sheets. Polymers can cure via a number of mechanisms. The most common with regard to the materials used in the assembly of high-density electronic devices are thermal, ultraviolet, room-temperature vulcanization (RTV), and catalyzed (two-part). Also, the path and/or conditions of the cure will affect the final properties of the material.

#### 9.3.1 Thermal cure

Many polymer systems used in high density electronic assemblies are cured via thermal energy. This can include curing during a solder reflow profile (e.g., Loctite 3515), multiple hours in a batch oven (e.g., potting compounds), or seconds on a hotplate or curing station (e.g., QMI SkipCure™ systems). Also, some curing reactions that will progress at room temperature can be accelerated through the application of thermal energy. The data sheets supplied with these materials often contain the optimal cure profile. Deviations from that profile will result in the final properties of the material being different from those of materials cured at a different temperature. The most notable affect is on the glass transition temperature ( $T_g$ , see Sec. 9.4).

The most common heat-cured system are premixed frozen epoxies (e.g., SMAs and underfills). These materials have already begun to cure once they are mixed, but to obtain the optimal properties (and also to achieve reasonable cycle time), heat cure cycles are used to complete the curing. The higher the temperature, the more rapid the cure time, but there is a trade-off. Higher temperatures result in a larger stresses and can quickly evaporate volatile materials, leading to voids. On the other hand, with too low a temperature, you may not achieve sufficient temperature to “kick-off” the reaction, leading to long cycle times and unfavorable final properties.

As an example of a heat-cure system, let's examine a surface mount adhesive (SMA). Most surface mount adhesives are one-part, epoxy-based, heat-cure materials that are liquid or paste-like at ambient temperature. However, when exposed to relatively high temperatures, they will harden to a tough glass-like polymer within minutes. The active raw materials in the adhesive (from the point of view of curing) are the epoxy resins (Fig. 9.12) and the curing agent (latent hardener), typically an amine.

The curing agent, or latent hardener, is normally dispersed as a very fine powder into a specific blend of various epoxy resins of different viscosity (chosen to give an overall target viscosity that is suited to the rheological requirements of the particular mode of application). Under ambient temperature



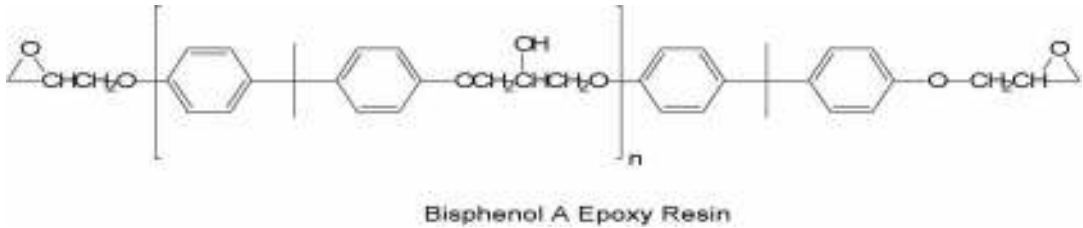


Figure 9.12 Bisphenol A diglycidyl ether epoxy resin.

conditions, minimal chemical reaction occurs between the curing agent and the epoxy groups. To effect cure, the adhesive must be heated to elevated temperature—i.e., sufficient energy must be applied for the latent hardener to undergo a melting process/phase change such that it can chemically react by a ring-opening of the epoxy as illustrated in Fig. 9.13.

The latent hardener usually possesses more than one active site that is capable of reacting with an epoxy group. A particular epoxy resin chain also usually possesses more than one epoxy group; for example, bisphenol A diglycidyl ether is difunctional. Hence, the adhesive initially consists of a blend of low-viscosity, multifunctional epoxy resins and a dispersed, powdered (of fine particle size) latent hardener. No chemical reaction takes place between the hardener and the epoxy groups under ambient temperature storage conditions. As heat is applied to the adhesive, the hardener starts to dissolve, and the reactive sites on the latent hardener start to chemically react with the epoxy groups on the individual epoxy resin chains such that these chains become increasingly chemically linked. This chain growth process is accompanied by an increase in viscosity.

Once ring-opened by chemical reaction with the hardener, the epoxy group is converted to a new chemical entity known as an alkoxide ( $-O^-$ ). Such alkoxide groups are themselves reactive toward other epoxy groups (if heated to sufficiently high temperatures), and this results in the formation of new ether linkages between adjacent polymer chains; i.e., polyetherification. This pro-

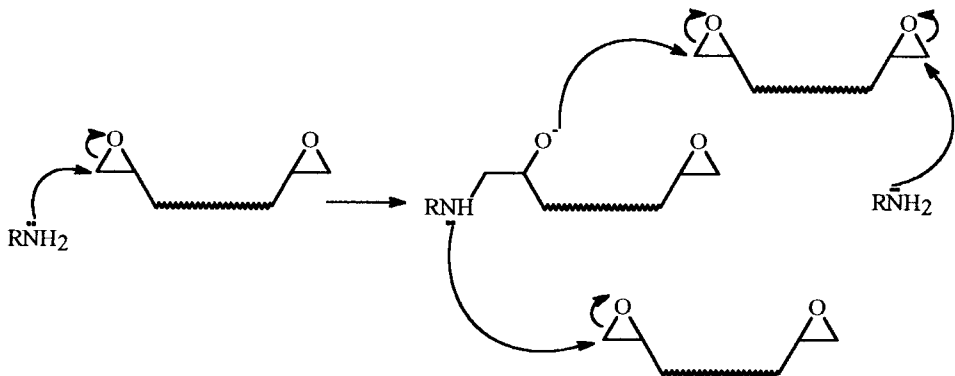


Figure 9.13 Ring-opening of epoxy by curing agent  $RNH_2$ .

cess produces a highly cross-linked three-dimensional network. As the number of cross-linked chains increases, the viscosity of the adhesive increases until the adhesive eventually becomes a solid polymer when cure is complete. The cure process is illustrated in Fig. 9.14. As the adhesive approaches 100 percent cure, it assumes 100 percent of its cured properties. Incomplete cure will reduce the cured properties of the adhesive.

A typical oven temperature profile for heat curing the epoxy chip bonders is shown in Fig. 9.15. This shows a residence time of 65 sec above 150°C and 130 sec above 125°C with a peak of 155°C. This is more than adequate to fully cure the adhesive. The cure profile can be further optimized to reduce dwell time in the oven and peak temperature by monitoring the effect on bond strength

The degree and rate of cure are most often modeled using differential scanning calorimetry (DSC). An isothermal DSC curve gives a measure of the time required to achieve 100 percent cure when heated at a constant temperature. In this test, the adhesive sample is heated up at a rapid rate (100°C/min) to a target temperature (e.g., 125°C) and then held at this temperature over a period of several minutes. The degree of conversion of the adhesive from the uncured, liquid state to the cured, solid state can then be expressed as a percentage degree of cure for different time periods of, for example, 3 min, 4 min, 5 min, etc. A typical isothermal DSC curve is shown in Fig. 9.16 as a graph of percent conversion (%) against time (minutes).

The isothermal curve indicates how long the adhesive should be heated at a certain fixed temperature to achieve full cure. The curing oven must be set

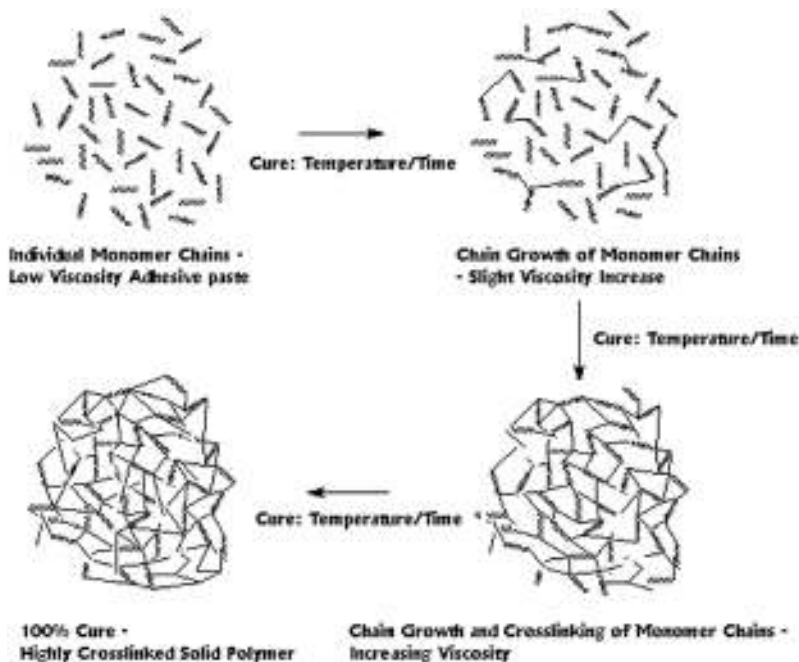


Figure 9.14 Illustration of the curing process.

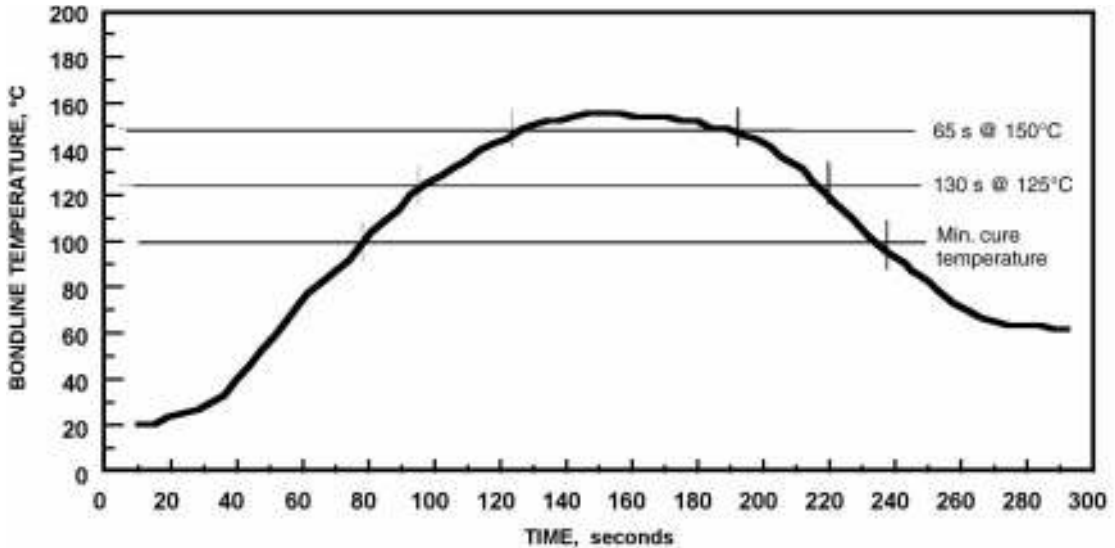


Figure 9.15 Typical oven profile for curing chip bonders.

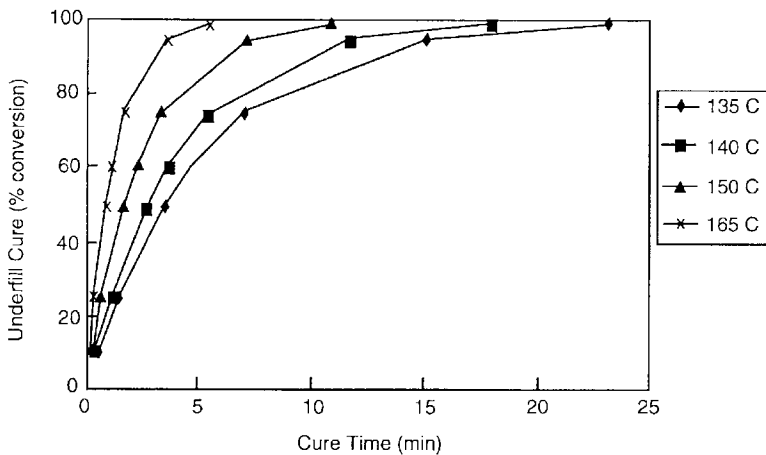


Figure 9.16 DSC curves illustrating the effect of temperature on degree of cure on an underfill material.

and maintained to give a temperature-time profile that matches or exceeds the heat input required by the adhesive. Although the heater panels of a typical conveyor oven may be set to attain a certain target temperature, the actual temperature that the adhesive experiences will depend on several factors. These include the heat capacity of the PCB and the individual components, the component population density on the PCB surface, and the conveyor belt speed (which depends on the total number of boards to pass through the oven). Consequently, the actual temperature achieved on the board should be measured against time to produce a cure profile. The temperature-time profile of

the cure station should be checked regularly to confirm adequate curing conditions. It is important to measure the temperature of the adhesive at the bond-line of a fully populated PCB so as to take into account all thermal transfer effects. The bond-line temperature of components located in regions of the board adjacent to large heat sinks (such as large PLCC components) should be checked to confirm that they are receiving the minimum cure requirement.

DSC can also be run in a dynamic mode to measure changes in the heat flow characteristics of an adhesive when the material is heated under precisely controlled conditions. It measures the heat of reaction generated when a liquid adhesive product is converted to a cured or solid state. In a dynamic DSC run, the temperature of a liquid adhesive sample is ramped up at a rate of (typically) 10°C/minute, from room temperature to 250°C, and the heat of reaction is measured. Three key pieces of information are available from dynamic DSC tests.

- The temperature at which the adhesive starts to undergo cure or polymerize ( $T_{onset}$ )
- The temperature at which the maximum rate of reaction is achieved ( $T_{peak}$ )
- The total amount of heat evolved in the polymerization reaction ( $\Delta H$ , in joules per gram of product)

A typical dynamic DSC curve is shown in Fig. 9.17.

The dynamic DSC trace illustrates the reaction profile of a typical surface mount adhesive, and it indicates that a certain minimum threshold temperature is required to initiate the cure mechanism.

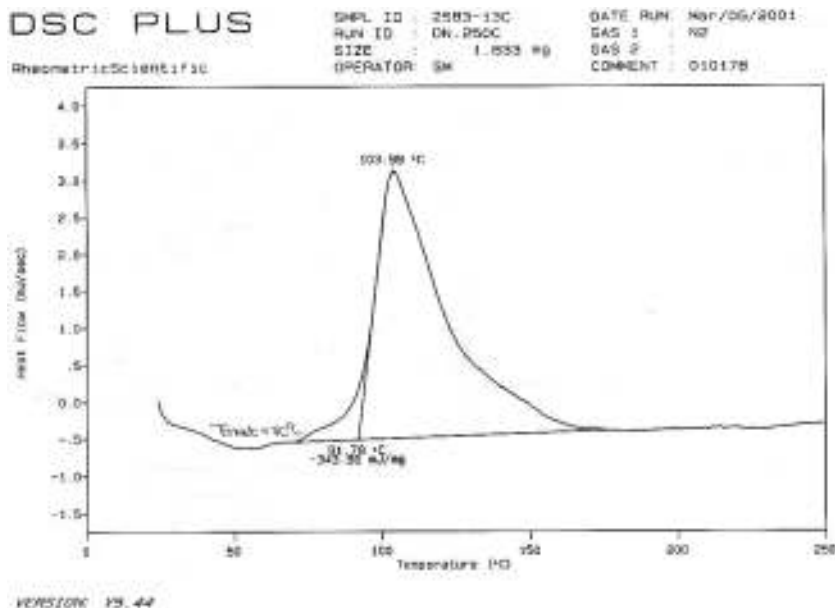


Figure 9.17 Dynamic DSC trace.

Ideally, the recommended cure conditions should be observed, with the understanding that the true bond-line temperature of the adhesive may not necessarily be identical to the oven set temperature. If a cure profile other than the recommended one is needed, DSC studies can be used to determine the appropriate cure schedule, and the final physical properties of the cured material should be determined with the cure schedule being utilized.

### 9.3.2 Ultraviolet (UV) curing

An ultraviolet light curing material has a curing mechanism that is initiated with exposure to ultraviolet and/or visible light. Within the electromagnetic spectrum, ultraviolet light refers to the wavelengths in the range of approximately 200 to 400 nm, whereas visible light encompasses those from 400 to 750 nm (Fig. 9.18). The wavelength of light is inversely proportional to energy. Therefore shorter wavelengths (e.g., UV) possess higher energy.

$$\lambda = h\nu$$

where  $\nu$  = frequency

$\lambda$  = wavelength

$h$  = Planck's constant,  $4.135 \times 10^{-15}$  eV-sec

Polymerization begins when the energy from light of a specific wavelength contacts the photoinitiators present in the resin. The free radicals that form as a result initiate polymerization reactions between the monomers of the resin leading to varying degrees of cross-linked polymer chains.

The cure begins at the surface and continues as far as the wavelengths can penetrate the material. Curing starts instantly and can occur over a time span as short as 1 or 2 sec, depending on the intensity of light and volume of material. The chemical type of these adhesives includes acrylates, modified acrylates, acrylated urethanes, modified acrylic esters, epoxies (cationic), plus many others.

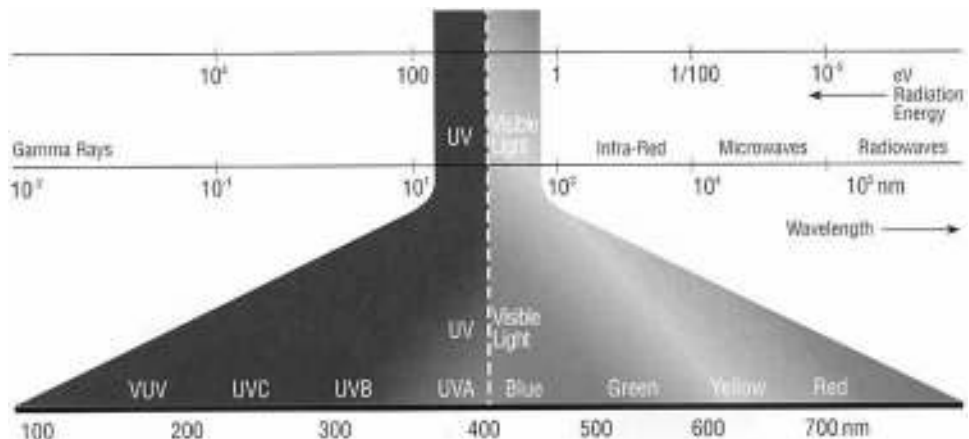


Figure 9.18 The electromagnetic spectrum.

Two important process demands that must be addressed when using a UV cure material are depth of cure and surface cure. When a deeper cure of the UV material is needed, high-intensity light ranging between 300 to 400 nm is required. The longer wavelengths are able to penetrate farther into the material, yielding a higher cure depth. It is also important to note that, if the UV material is colored, this will significantly inhibit the depth of cure because of a boundary layer of dark, cured material forming on the surface that blocks any further light penetration.

On the other hand, if a hard, tack-free surface is required, it is necessary to expose the material to high-intensity light in the wave bands below 300 nm. The shorter wavelengths will provide the energy needed to polymerize the surface of the material.

When using a UV cure material, it is important to choose a UV curing system that is capable of delivering both the proper intensity and wavelength needed to cure the material in question (for examples of UV curing systems, see Fig. 9.19). Most UV curing materials cure on the order of seconds at an intensity of in the range of milliwatts per square centimeter (given a thickness on the order of 0.1 mm) *at the photoinitiator wavelength*. Specifications for a UV curing system may list an intensity on the order of hundreds of watts per square centimeter. At first, this appears to be more than sufficient—several magnitudes above what is needed. This output is measured over the entire spectral output of the bulb. Therefore, before choosing a UV curing oven, it is important to know the spectral output (what wavelengths are emitted by the bulb) and the intensities at the wavelengths of choice.

One common observation with certain UV-cured materials is that the surface may be tacky to the touch after irradiation with UV light. Some UV photo initiators experience what is termed *oxygen inhibition*. This is caused by the oxygen molecules in the atmosphere interacting and “using-up” the cure initiator at the surface of the material being cured. This can be alleviated in three ways. First would be to blanket the material in an oxygen reduced atmosphere (e.g., nitrogen). This can be costly to set up and operate with large batches of materials. Second would be to have a secondary cure mechanism available (e.g., heat, moisture, and so on) that can complete the curing on the surface. Finally, sometimes this can be overcome through the use of a higher-intensity and/or higher-energy light source.

Some materials may be cured by both UV and other mechanisms, and these are termed *dual-cure systems*. These materials, first partially cured using UV



Figure 9.19 Sample UV curing systems.

light, are subsequently fully cured using another mechanism. These secondary cure mechanisms include heat, activators, ambient moisture, and resin/hardener mixtures. In some cases, photoinitiators are added to an already existing technology (e.g., silicones or epoxies) so as to achieve dual cure mechanisms.

Multiple curing mechanisms are important for many reasons. The most important of these is the need to cure the material in areas where the light cannot penetrate or in shadowed areas. In these cases, the UV light is used to immobilize the material initially, thus enabling the assembly to be moved to another stage in the process. This increases production throughput, preventing a bottleneck in the system.

Another benefit gained by adding photo initiators to other materials revolves around the fact that one is able to take advantage of the inherent properties of these materials. Epoxies, silicones, and cyanoacrylates are all examples of existing technologies that have been fused with UV technology to gain the benefits of both.

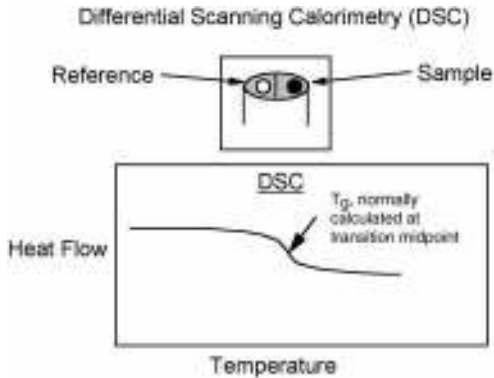
Another approach to curing epoxies with UV light is by means of a technology referred to as *cationic UV curing*. These are typically one-part epoxies that exhibit extremely low outgassing during cure. Once cured, these cationic UV epoxies can provide high-temperature bonds that demonstrate toughness and high peel and high impact resistance.

The cure of these epoxies is initiated by UV light. However, the cationic curing mechanism differs from typical UV cure in the fact that, once the cure is initiated, it will continue even if the UV light is removed. These products also require less UV energy to cure than other UV curable materials, so it is not difficult to find a UV light that will provide enough energy to initiate cure.

## 9.4 Glass Transition Temperature

The glass transition temperature ( $T_g$ ) of an adhesive indicates the temperature at which the adhesive changes from being a glassy solid to a “rubbery” material. There is often a significant increase in the coefficient of thermal expansion on passing through the  $T_g$  (often a two- or threefold increase). If the  $T_g$  is within (or near) the operating temperature of the assembly, the reliability of the assembly can be adversely effected. Even within the same sample, the glass transition occurs within a range of temperatures and not as a single point. Factors such as intrachain stiffness, polar forces, and co-monomer compatibility can affect the size of the glass transition region.

Differential scanning calorimetry (DSC) is the quickest and simplest method to measure  $T_g$ . The method requires extremely small samples (typically 5 to 20 mg) that require no special preparation, and material from components on processed boards can be utilized. The method consists of heating the sample in a closely calibrated thermocel, where the temperature of the sample is compared to the temperature of a blank reference point within the same cell. Thermodynamic transitions such as melting points and reaction exotherms are easily measured, and the change in heat capacity at the  $T_g$  is seen as a shift in the baseline for cured materials (see Fig. 9.20).

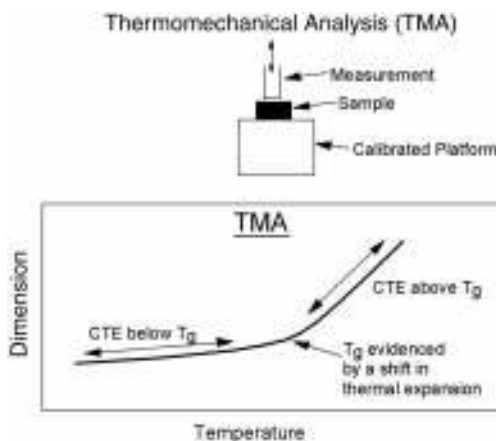


**Figure 9.20** Example of DSC to measure  $T_g$ .

Unfortunately, this fast and convenient method is not universally applicable to all materials. High filler loadings, high crosslink densities, and other thermomolecular processes can mask the shift resulting from the  $T_g$  and make the transition difficult or impossible to identify.

Thermomechanical analysis (TMA) is the test used to determine thermal expansion coefficients. Because there is a shift to a higher thermal expansion coefficient above the  $T_g$  resulting from changes in molecular free volume, the method can also be used to measure the glass transition temperature as shown in Fig. 9.21.

The technique simply consists of heating the sample on an expansion-calibrated platform and measuring the dimensional change of the sample with an instrumented probe. The method will also easily follow cure-stress relaxations in and around the glass transition region, which sometimes leads to ambiguity in assignment of a specific  $T_g$  and can yield a different value for the same



**Figure 9.21** Thermomechanical analysis used to measure  $T_g$ .



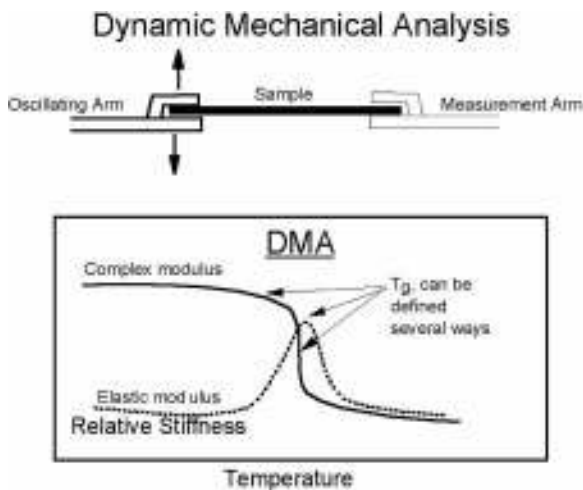
specimen if measured at a different point. (For example, the cure stress may be significantly different when measured near the edge of a sample rather than its center.)

Dynamic mechanical analysis (DMA) consists of oscillating flexure energy applied to a rectangular bar of the cured material. The stress that is transferred through the specimen is measured as a function of temperature. Components of material stiffness are separated into a complex modulus and a rubbery modulus. The technique is highly accurate and reproducible, although the  $T_g$  can be defined in different ways, which will result in different values as illustrated in Fig. 9.22. Large samples that must be accurately machined, coupled with longer setups, make this test relatively expensive to run.

Each of these methods will produce different data for the same material. For example, a single specimen of a developmental epoxy encapsulant material was cast and cured for 2 hr at 145°C after gelling at 100°C for 1 hr. It was then machined into specimens for DSC, TMA, and DMA analysis. The results show  $T_g$  values ranging from 130°C for the TMA to 146°C for the DMA measurement, as shown in Table 9.5.

**TABLE 9.5 Instrument Effect on  $T_g$**

Instrument	$T_g$ in °C
DSC	142
TMA	130
DMA	137 (G") 146 (tan delta)



**Figure 9.22** Dynamic mechanical analysis used to measure  $T_g$ .

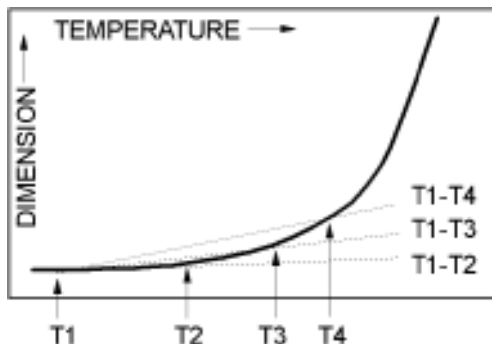
## 9.5 Coefficient of Thermal Expansion

The coefficient of thermal expansion is a measure of the fractional change in dimension (usually thickness) per degree rise in temperature. For microelectronics encapsulants, it is often quoted in ppm/°C (value  $\times 10^{-6}/^{\circ}\text{C}$ ). Chemical composition, filler loading, and cure cycles all affect the value. For typical materials that have nonlinear expansion, the specified temperature range will also have an effect on the data, with measurements out closer to the  $T_g$  yielding higher values than those quoted across lower temperature. This is shown in Fig. 9.23.

The CTE of adhesives used in microelectronics assembly is often a critical parameter. The different polymer systems used in electronics have vastly different CTEs for the base system. These CTEs can be modified from this base level through the addition of fillers, changes in the backbone chemistry, and changes in the hardener system. For example, most underfill materials are used to mitigate the CTE mismatch between silicon die (1.8 ppm/°C) and the FR-4 substrate (15 ppm/°C). Therefore, the CTE of the base epoxy is often manipulated with the addition of fillers. This effect can be observed by examining a matrix consisting of a standard epoxy anhydride that is loaded with a proprietary mixture of low-expansion fillers. All samples were cured for 2 hr at 145°C after gelling for 1 hr at 100°C. CTEs decrease rapidly, and the viscosity increases, as shown in Table 9.6.

**TABLE 9.6 Effect of Filler on CTE**

Filler loading	CTE (TMA method)
60%	34.5 ppm/°C
65%	28.8 ppm/°C
70%	24.1 ppm/°C
75%	20.0 ppm/°C



**Figure 9.23** Effect of temperature on CTE.

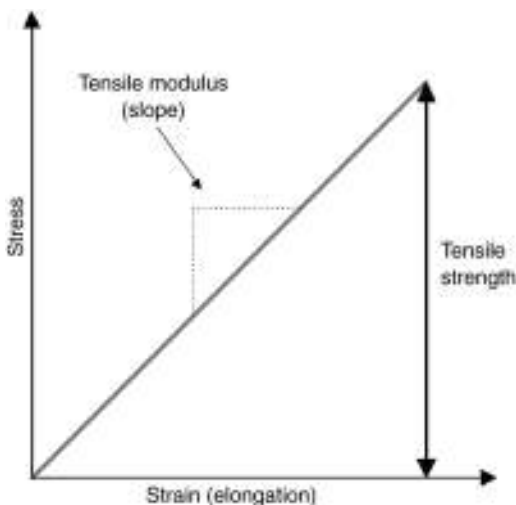
Also, the CTE is often increased (sometimes as much as three-fold) after passing through the glass transition temperature. These values are often defined as  $\alpha_1$ , below  $T_g$ , and  $\alpha_2$ , above  $T_g$ . When looking at a material and the amount of stress it may impinge on a system or the amount it can absorb, it is useful to examine the CTE,  $T_g$ , and modulus together when choosing a system.

## 9.6 Young's Modulus

Young's modulus is the same as tensile modulus. Tensile modulus is the ratio of stress to strain within the elastic region of the stress-strain curve (prior to the yield point). Young's modulus characterizes the elastic properties of the material under tension or compression irrespective of the sample geometry. Typically, the lower the modulus, the more elastic the material. Thus, a material with a low modulus can be considered to be very rubbery and can absorb more stress before fracturing.

To measure tensile modulus, the stress is gradually increased on a sample, and a measurement of the elongation the sample undergoes at each stress level is recorded. This is continued until the sample breaks. Subsequently, a plot of stress versus elongation is produced, such as shown in Fig. 9.24.

This plot is called a stress-strain curve. (*Strain* is any kind of deformation, including elongation. *Elongation* is the word we use if we are talking specifically about tensile strain.) The height of the curve when the sample breaks is the tensile strength, of course, and the tensile modulus is the slope of this plot. If the slope is steep, the sample has a high tensile modulus, which means it resists deformation. If the slope is gentle, then the sample has a low tensile modulus, which means it is easily deformed.



**Figure 9.24** Example of a strain-stress measurement for determining modulus.

Modulus is measured by calculating stress and dividing by elongation, and it would be measured in units of stress divided by units of elongation. But because elongation is dimensionless, it has no units by which we can divide. Therefore, modulus is expressed in the same units as strength, such as  $\text{N}/\text{cm}^2$ .

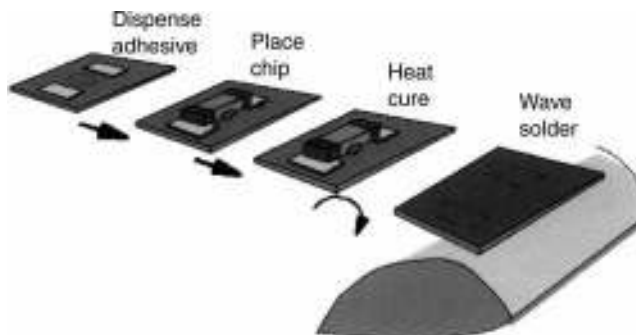
## 9.7 Applications

### 9.7.1 Surface mount adhesive

SMT encompasses two fundamentally different manufacturing processes, one incorporating the use of solder paste (or cream), the other incorporating surface mount adhesive (SMA). The first of these processes involves screen printing a solder paste onto the solder pads on the surface of the PCB. A surface mount device (SMD) component is then placed on the solder paste, and the connections are reflow soldered. The second type of process recognizes the fact that, most commonly, PCBs contain a mixture of SMDs and through-hole components. Such through-hole components are attached to the PCB by a wave soldering process wherein hot molten solder is deposited between the lead connector and the hole. SMDs can also be attached to the PCB using this same wave soldering process; however, the components must be bonded to the bottom side of the board to keep them from falling off and into the solder wave. This bonding process, a critical step to the overall process, is displayed schematically in Fig. 9.25.

In this process, the adhesive is dispensed directly onto the substrate PCB between the solder pads, and the component is placed on the adhesive dot that is then heat cured. The cured adhesive must have sufficient strength to bond the components to the board surface during the next step of (manual) insertion of through-hole components. The board is then flipped by  $180^\circ$  and passed through the wave solder.

**9.7.1.1 Process requirements of the SMA.** Adhesive is used to bond the body of the SMD to the PCB between the solder pads. The adhesive must have the correct rheology (see Sec. 9.2), or flow characteristics, to permit deposition of



**Figure 9.25** Illustration of a mixed-technology process.

accurate quantities of adhesive dots in precise locations between solder pads on the PCB surface. Adhesive can be applied to the PCB using one of several methods: stencil printing, pin transfer, or (most commonly) a syringe dispensing system, either pressure/time or volumetric. After the SMD is placed, the wet adhesive must have sufficient wet, or “green,” strength to hold the SMD in position until cured (see Yield Point, Sec. 9.2.2.3). The cured adhesive must then have sufficient strength to hold the SMD to the PCB during the solder wave operation. After soldering, the adhesive must not affect operation of the circuit in any way. To meet these demands, the product must satisfy the following requirements:

- The packed adhesive must be free of contaminants and air bubbles.
- It must have a long shelf life.
- The adhesive must enable high-speed dispensing of very small dots.
- It must exhibit consistent dot profile and size.
- It must have a high dot profile, nonstringing.
- The color must allow visual and automated detection.
- It must have high wet strength.
- It must provide rapid curing.
- It must be nonslumping during the cure cycle (heating).
- It must have high strength combined with flexibility and resistance against a thermal shock/solder wave.
- Good electrical properties must result when the adhesive is cured.

**9.7.1.2 Dispensing methodology.** High-volume surface mount assembly is a very competitive industry, with product designs changing rapidly. To remain profitable, it is vital for PCB assembly manufacturers to maintain a high quality standard without compromise in throughput and flexibility. SMT placement equipment manufacturers continually meet the challenges of this fast-paced industry by developing new and improved placement equipment, which now offers ability to place more than 70,000 SMD components per hour. The most common method of adhesive deposition is by high-speed automatic dispensing, which provides excellent control of adhesive deposit volume and dispense location. However, the speed of most automatic dispensers is limited to up to 50,000 dot placements per hour. This limitation can potentially produce a bottleneck in a high-throughput assembly line environment. It is therefore vital to develop both new and faster methods of deposition and new adhesive materials that possess the required rheological properties to permit increasingly faster rates of deposition.

Surface mount adhesives are applied to the surface of a PCB by one of three methods.

1. Syringe dispensing

2. Stencil printing
3. Pin transfer

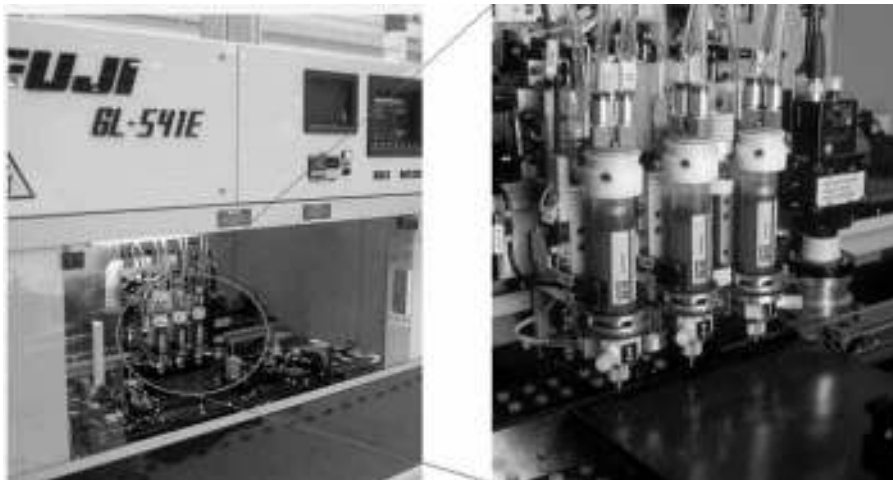
More than 80 percent of the total surface mount adhesives used are currently dispensed by syringe. Syringe dispensing can be further divided into two subgroupings.

1. Pressure-time systems
2. Volumetric systems

Pressure-time syringe dispensing (Fig. 9.26) is the most common method used, and it employs a pressure/time system to dispense adhesives at high speed. This is a conventional system used by many of the major equipment manufacturers such as Fuji, Sanyo, Panasert, and others. On a pressure-time system, the amount of adhesive dispensed will depend on the nozzle size, the temperature of the adhesive, the dispense pressure, and the dispense time. Volumetric dispensing systems are based on one of two principles: Archimedes screw or piston (positive displacement) as shown in Fig. 9.27.

Pin transfer is a high-speed alternative to automatic syringe dispensing that uses an array of pins that dip into a tray of adhesive and then transfer the suspended adhesive drops to the PCB surface. However, this method is not without limitations. Deposition locations are fixed in complex and expensive tooling plates that make changeovers slow. This in turn makes product design changes expensive and difficult to implement. Less than 10 percent of total adhesive is dispensed by the pin transfer method.

Stencil printing has been widely used for many years as an efficient and cost-effective means of dispensing solder paste and, with increasing component counts and faster placement equipment, it has become increasingly popular to use the same technology as a means of adhesive deposition that is both



**Figure 9.26** Pressure-time automated syringe dispensing.

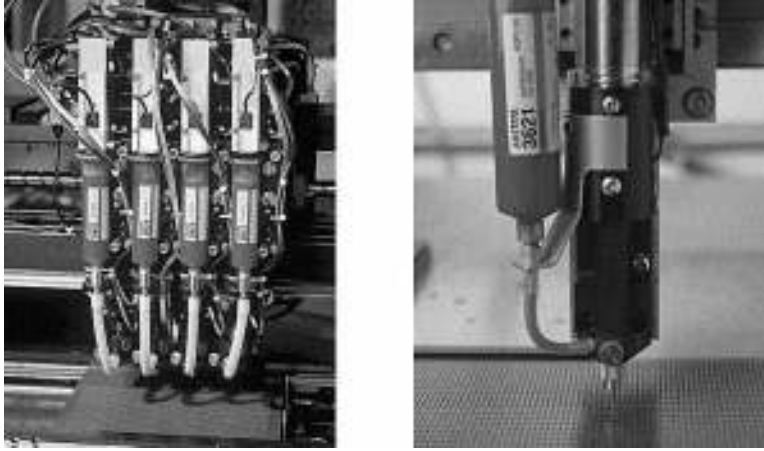


Figure 9.27 Archimedes screw and positive displacement systems.

faster and more flexible than either automatic syringe dispense or pin transfer. New equipment developments have overcome some of the earlier limitations of this technique and, while stencil manufacturers have developed new stencil technologies designed for adhesive printing, adhesive manufacturers have responded with the development of new printable adhesives with rheological properties specifically preengineered for stencil printing applications. Newer SMAs have been developed that possess a rheology such that the same material can be both dispensed and screen printed.

**9.7.1.3 Dot profile.** Each of the above dispensing techniques is used to apply adhesive dots to the board surface. The actual shape of the dot (dot profile) produced by a particular adhesive grade will be influenced by the various adhesive rheological parameters such as thixotropic recovery rate, viscosity at zero shear rate, surface tension, and wetting characteristics (see Sec. 9.2). The actual dot shape (Fig. 9.28) may be peaky-conical (associated with very high yield point values), Hershey kiss, or rounded hemispherical (associated with lower yield point values).

The dot profile is also defined by nonadhesive (machine-related) parameters such as dot volume, dispense needle diameter, and needle standoff height. For a given adhesive grade, it is possible to produce exaggeratedly high, narrow

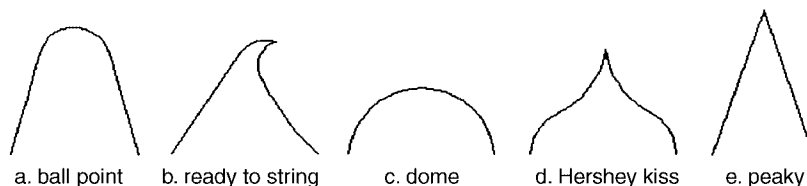


Figure 9.28 Illustration of various dot profiles.

dots and low, wide dots by adjusting these parameters (particularly stand-off height).

It is important to dispense the adhesive accurately, and consideration must be given to the dimensions and location of the solder pads. The adhesive dot must be high enough to bridge the gap between the surface of the PCB and the underside of the SMD body, yet not so high that it will contaminate the component placement head. The gap to be bridged by the adhesive will depend on the height of the solder pad above the PCB solder mask surface and the gap created by the difference in end metallization and body thickness of the SMD. This gap can vary from less than 0.05 mm for flat chips to more than 0.3 mm for large SOs and QFPs.

Considering these wide ranging demands, it is generally best to get reasonably tall dots to ensure good adhesive coverage on the underside of components with high stand-off space; at the same time, the dot can be squeezed out between low stand-off components without risk of pad contamination. Quite often, two separate sets of dispense parameters are used side by side for a single grade, one producing a high, large volume dot for high stand-off components and the other producing moderate height and volume dots for flat chips and MELFs.

The question often arises as to when a single dot or a dual (twin) dot configuration should be used. The main process issues influencing whether a single or dual dot configuration is used are the size of the component being bonded, the board component population density, and the board design/pad spacings. (The adhesion of the surface mount adhesive to the particular solder mask may also play a role.) The size of the component imposes restrictions on the maximum size of the adhesive dot diameter, because the dot must be smaller than the spacing between the solder pads. As components get larger, they do so more through increasing thickness, so certain components have a higher mass but similar spacing between solder pads. As the mass of the component increases, it becomes more susceptible to movement. This affects both the green strength and the cured bond strength of the adhesive in its ability to hold a larger, heavier component. It is therefore necessary to use more adhesive to hold the component in place and minimize component skewing. Similarly, larger, heavier components are subject to stronger forces during the wave soldering step. To prevent component loss, greater bond strength is required. Because adhesive bond strength is also related to the total bond area, the bond area should be maximized. Again, this can be done by increasing the amount of adhesive under the component. Because of restrictions imposed on the adhesive dot diameter by the solder pad spacings, the only viable way of increasing the amount of adhesive under the component is by using a twin adhesive dot configuration (Fig. 9.29). The figure illustrates the amount of adhesive that can be put under a component with a single dot versus a twin dot and the amount of coverage (bond area) that each dot configuration will afford when compressed by the component (assuming a 3-mil stand-off height to the component and pad widths matching the component) (see Fig. 9.30).

Obviously, for an 0805 component, a twin dot will afford greater adhesive coverage under the component as compared to a single dot, and this will result



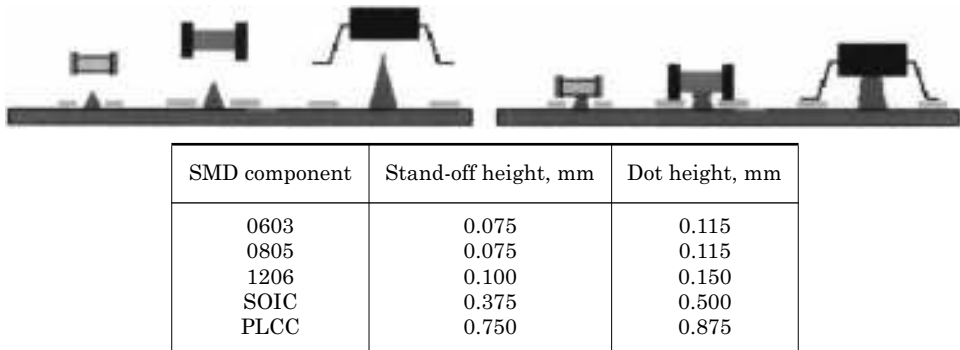


Figure 9.29 Component stand-off height and adhesive dot height.

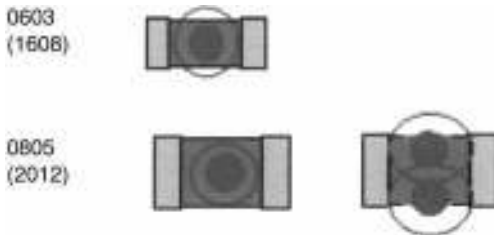


Figure 9.30 Single and dual dot pattern.

in both better green strength and better cured bond strength. As the mass of the components and the tolerance between the solder pads decreases (i.e., 0603 and 0402 components), single dots should be sufficient for good bonding. However, other process issues, such as adhesion to board surface, may dictate use of twin rather than single dots.

**9.7.1.4 Dispense parameters.** The adhesive must have the right rheological characteristics to give good dot shape control. However, good dispensing does not depend on the adhesive alone. For pressure-time syringe dispensing, the machine-related factors that will influence dispensability and good dot formation are needle size, PCB-to-needle stand-off, temperature, dispense time and pressure, and dispense cycle profile.

The inner diameter of the needle is critical. It must be significantly smaller than the diameter of the dot on the board. As a guide, the ratio should be 2:1. For example, for dot sizes of 0.7 to 0.9 mm, the needle I.D. should be 0.4 mm; for dot sizes of 0.5 to 0.6 mm, the I.D. should be 0.3 mm. Different adhesive dispensers make use of different designs and needle lengths, and these will also affect dispensability.

The stand-off, or *stopper*, height is also critical. This will control the height of the dot produced. However, it must be appropriate for the quantity being dispensed and the needle inner diameter. For a given adhesive volume, the

height-to-width ratio of the adhesive dot will increase with the stopper height. Typically, the maximum stopper height is half the needle I.D. (Fig. 9.31). Beyond this point, the adhesive dot diameter will be too small relative to the needle I.D., and this will cause inconsistent dispensing and stringing.

The temperature of the adhesive will affect viscosity and, consequently, dot shape. Figure 9.32 illustrates how the viscosity of a typical surface mount adhesive varies with temperature.

Most modern dispensers use some sort of temperature control, either on the dispense nozzle or dispense chamber, to maintain the adhesive at a set tem-

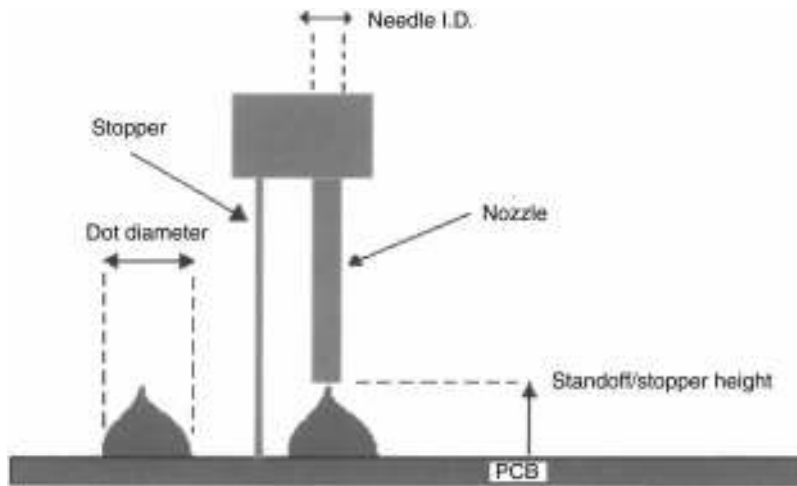


Figure 9.31 Stand-off height, needle I.D., and adhesive dot diameter.

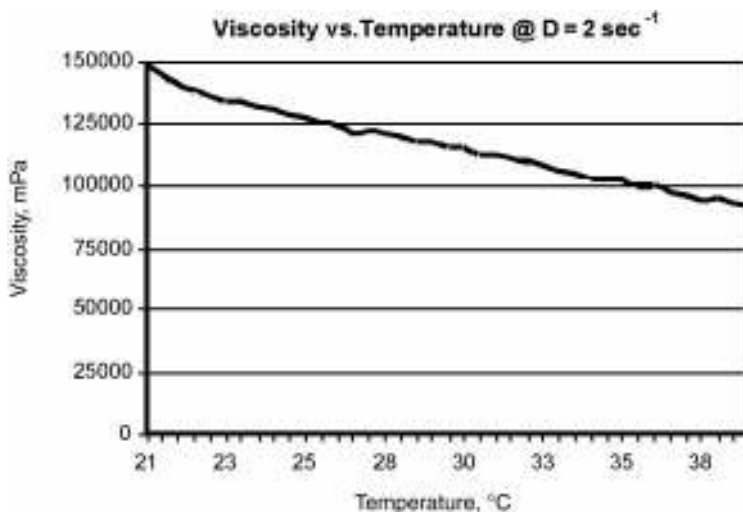


Figure 9.32 Temperature-viscosity curve.

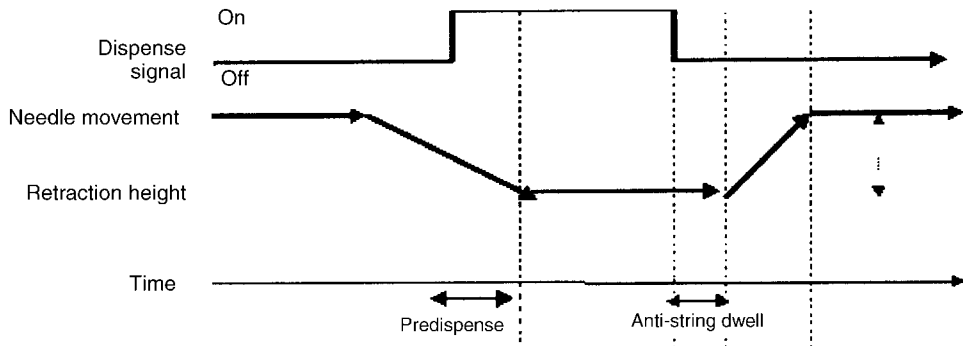
perature above ambient. However, the temperature of the PCB should also be considered. Dispensing on hot boards, warmed from previous processing, can change the dot profile.

The majority of syringe dispensers use *air-over* pressure systems. The volume of adhesive dispensed is then controlled by a combination of pressure and time. Very short dispense times with high pressures may be attractive to speed up the cycle time, but the ability of the pressure regulation system to respond must be considered. High pressures (4 to 5 bar) will, in theory, allow shorter dispense times; however, this leaves little scope for pressure adjustment to compensate for viscosity variations and also can cause the air temperature behind the piston to rise faster and higher. In practice, machine operators usually set the pressure to a mid-point value (approx. 2 to 3 bar). The dispense time is then set according to the size of dot required, which in turn is dependent on the SMD component. Although there are guidelines for the different dot sizes, the actual size used will depend on the sizes and mix of components being bonded, the pad spacing, and the in-house limits of acceptable variation. Often, this is established by trial and error and previous experience.

More recent high-speed dispensers use dispense cycles (Fig. 9.33) wherein the dispense pressure can be timed to start before the nozzle has arrived at the dispensing position. The speed at which the nozzle retracts, the retraction height, and the delay between end of dispensing and the start of nozzle retraction all will affect dot shape control and possibility of stringing.

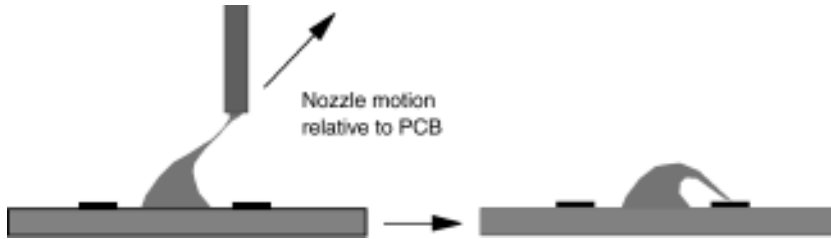
**9.7.1.5 Common dispensing defects.** Several types of dispensing defect may lead to final process defects. (The presence of a dispensing defect does not imply that a defective SMD joint will occur, but it does increase the risk of such a defect.) These are stringing (or tailing), inconsistent dot size, and missed dots. Each of these defects is discussed briefly here.

Stringing is probably the most common defect, and it can result in contamination of the solder pads and, ultimately, poor solder connections (Figs. 9.34



Typical Dispense Cycle Profile

Figure 9.33 Pressure-time dispense cycle.



**Figure 9.34** Illustration of the stringing defect.

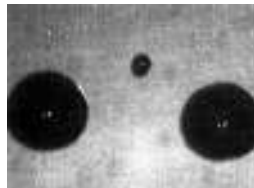
and 9.35). In some cases, stringing is caused by the adhesive not having time to wet out onto the PCB surface or time to recover from being sheared in the nozzle. In these cases, an increase in the *delay after* often can solve the problem. (The *delay after* is the time, typically 10 to 20 ms, during which the nozzle rests in position above the PCB after the adhesive shot has been dispensed. It allows the adhesive time to wet onto the PCB substrate and restructure itself after being sheared in the nozzle.)

If increasing the delay after has no effect, particularly for larger dot sizes, then breaking off of the adhesive dot from the nozzle may be the problem. If there are satellites (or spattering, Fig. 9.36) associated with the stringing, then an increase in the Z-safe height (Z-retract height) will allow the nozzle to retract further after dispensing giving the adhesive dot a better chance to break cleanly off from the nozzle. Increasing either the delay after or the Z-safe reduces the incidence of stringing at the expense of dispense speed, as both increase the overall dispense cycle time. However, it is possible to achieve an optimal balance of dispense quality versus dispense speed.

If adjustment of either the delay after or the Z-safe has only a minor effect on stringing, then a different nozzle configuration (nozzle I.D./stand-off ratio) may be required. If the dispense volume of adhesive is too small for the nozzle diameter and stand-off height, resulting in a very tall, thin dot, then the risk of stringing is high. The correct solution here is to use a smaller needle diameter/stand-off height combination. Stringing sometimes can also be caused by poor board support or board warpage, or by the nozzle stopper (or stand-off post) landing on the solder pads and giving an incorrect stand-off height. (This problem may be solved by reindexing the nozzle by turning it through an angle of 45° or 90° to keep the stopper from contacting the solder pads.) In addi-



**Figure 9.35** Photo of a stringing defect.



**Figure 9.36** Splattering or satellite dots.

tion, stringing can sometimes be caused by electrostatic buildup on areas of the board. In this case, the strings characteristically are generally small and all point in one direction on the board (not always the direction of nozzle travel). This often occurs during dispense trials wherein the same boards are repeatedly dispensed onto and wiped clean, leading to a buildup of electrostatic charge on the PCB surface. This phenomenon can be eliminated through use of proper precautions such as static mats.

Inconsistent dot sizes is also a commonly observed defect. Differences in dot size can occur from several causes.

- The dot size may be too small for the needle diameter, resulting in poor wetting of the PCB. An increase in the dot size or use of a smaller needle often can solve this problem.
- Temperature changes can cause adhesive viscosity variations. Use temperature control and vision system feedback to control dot quantity.
- Pressure variations can occur, particularly due to changing air volume and temperature behind the piston. Use vision feedback control of dot quantity. More recent dispensers now enable the air to be vented back out of the syringe between “dispense-on” signals. This eliminates buildup of air temperature and speeds the recharging of pressure between dispense shots as the syringe empties.
- Partial blockage or buildup on the walls of the needle can occur. Clean the nozzles.
- There may be an imbalance in flow through multiple-needle nozzles. Clean the nozzles and check for damage.
- The third most commonly observed defect is missed dots. Missed dots can occur for one of two reasons,
  - Blockage of a nozzle may be caused by a large particle or foreign material. Every effort is made to ensure that such particles are not present in the adhesive, but it may happen occasionally. Foreign particles may also be trapped in the adhesive during nozzle attachment. One common source of blockage is old partially cured adhesive on unclean nozzles and adapters that falls into the nozzle during the reattachment of nozzles to syringes.
  - Air bubbles can cause missed dots. Although most surface mount adhesives are packaged bubble-free, a potential source of air bubbles is when air is entrapped during the attachment of nozzles and adapters to the syringe. Care should be taken when attaching nozzles and adapters to avoid introducing air, and the nozzle should be purged to clear any product that contains entrapped air bubbles.

Needles and stoppers can become damaged, bent, or worn, which will negatively affect dispensing. They should be checked regularly. Excess adhesive on the outside of a needle can interrupt smooth and consistent dot formation. In extreme cases, the adhesive may bridge over to the stopper pin and totally disrupt dispensing. The exterior of the nozzle should be kept as clean as possible.

**9.7.1.6 Adhesive wet (green) strength.** Before passing through the curing oven, PCBs are exposed to various chip placement machines that deposit surface mount devices onto uncured adhesive dots on the board surface. Many such high-speed chip placement machines use X-Y table movement to position the circuit board under the static cam-controlled placement head (e.g., Fuji CP-6 chip placement machine). Such X-Y table movement subjects the components and uncured adhesive to rapid acceleration/deceleration forces as the board is moved rapidly to correctly position the placement sites on the board surface with the static placement head. *Green or wet strength* refers to the ability of the adhesive in the uncured state to maintain the positional alignment of the SMD device with the solder pads on the surface of the PCB prior to the curing process. If the adhesive does not have sufficient green strength, the forces generated by the machines can cause misalignment of component leads with the solder pads.

The green strength of the adhesive depends on the degree of contact between the adhesive and the component as discussed in Sec. 9.7.1.3, and it is yield point dependent (see Sec. 9.2.2.3). An adhesive with too low a dot profile will not make good contact with the component, and this reduces the ability of the uncured adhesive to hold the component in place. This causes misalignment of the component with the solder pads, which in turn may result in higher process failures.

Poor green strength may also arise, even if the adhesive has good contact to the SMD but possesses a low base viscosity. In this case, the SMA is of too thin a viscosity to resist the directional forces experienced by the board and to hold the component in place.

The green strength of an adhesive can be tested using the Siemens standard SN59651, "Acceptance of SMD Adhesives," which involves sliding a populated PCB down a steel ramp of fixed incline (Fig. 9.37) into a stopper at the base of the ramp. The position of the various components on the PCB surface is noted before and after the test, and displacement is measured. According to the Sie-



**Figure 9.37** Sliding ramp for green strength test.

mens test, the adhesive must not allow the component to shift position by more than 150  $\mu\text{m}$  (corresponding to half the track pitch on a standard 0.3-mm pitch component). Some typical green strength values for five different Chipbonder<sup>®</sup> adhesives are shown in Fig. 9.38.

**9.7.1.7 Moisture absorption.** An important step in the SMT PCB assembly process is the dispensing of an appropriately sized dot of adhesive onto the exact location on the PCB surface. The next step involves placement of the various SMT components onto the adhesive dots before passing the entire board through an oven wherein the adhesive undergoes cure. Quite often, there is a time delay between dispensing of the adhesive and component placement. This results in the uncured adhesive being exposed to whatever temperature and humidity are prevalent under normal factory operating conditions. Because surface mount adhesives are used worldwide, there can be considerable variation in the factory conditions of ambient temperature and humidity. It is very important that the SMA have no inordinately high tendency to absorb moisture from the surrounding atmosphere when left exposed in the uncured state. Moisture pickup of this type can cause a problem known as *popcorning*. Popcorning occurs when the SMA absorbs moisture from the atmosphere. When the component is then placed onto the adhesive dot and the PCB is passed through the cure oven at temperatures  $>100^{\circ}\text{C}$ , the moisture absorbed by the adhesive vaporizes and boils off. This can manifest itself in any of the following ways:

1. There can be a formation of numerous bubbles or voids (Fig. 9.39) on the surface of the cured adhesive. The cured adhesive takes on a honeycomb appearance. This can reduce the area of contact between the cured adhesive and the underside of the SMT component, resulting in weaker bond

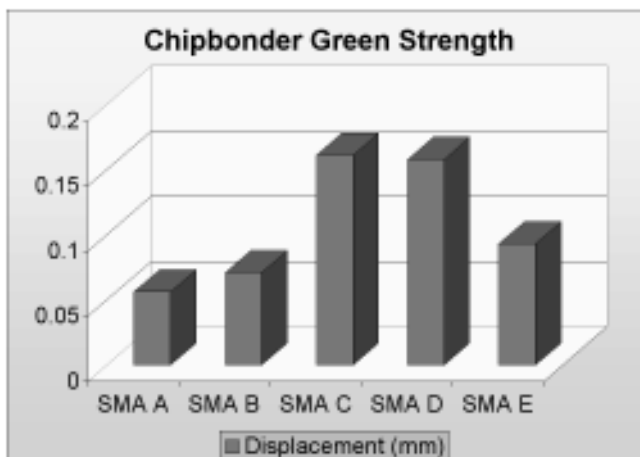
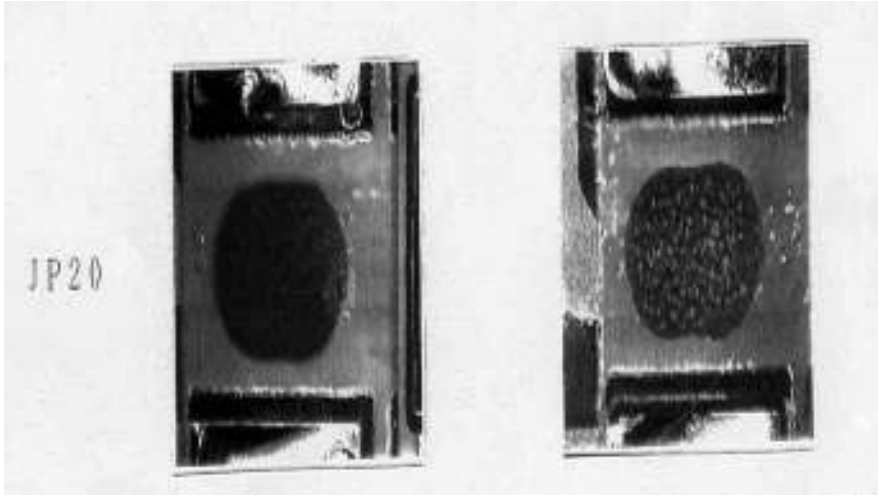


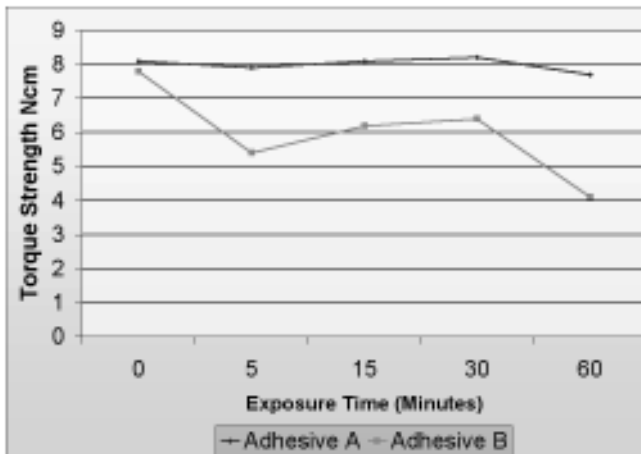
Figure 9.38 Green strength of five surface mount adhesives.



**Figure 9.39** Photographs of void formation caused by popcorning.

strengths. The reduction in bond strength can result in component loss during the manual insertion or wave soldering steps.

The effect of such popcorning on the resultant bond strengths is illustrated in Fig. 9.40. This illustrates the effect of different humidity exposure times on torque strength for two surface mount adhesives with different moisture tolerances. The required adhesive dots were dispensed onto a bare FR-4 board, and 1206 capacitors were either placed and cured immediately (exposure time = 0), or the dots were exposed for the various time periods (5, 15, 30, and 60 min) to 30°C/85 percent RH before placing the components and curing (180 sec, >125°C). The result-



**Figure 9.40** Adhesive bond (torque) strength after humidity exposure.



ant bond strengths (off torque, N-cm) were then recorded for each exposure condition.

In the case of adhesive B, the effect of humidity exposure is clear, with a dramatic decrease in torque strength evident after only 5 min exposure to 30°C/85 percent R.H. Adhesive A, on the other hand, is resistant to the effects of the humidity exposure. Adhesive B would almost certainly cause an increase in PCB defect rates when used in warm or humid environments.

2. The voids/bubbles are so large as to form channels through which solder can flow during wave soldering, resulting in solder bridging and component/device failure (Fig. 9.41). During the preheat flux cycle, it is possible for solder flux to penetrate the voids in the cured adhesive dot (Fig. 9.42). Because flux materials are commonly acid based, they can subsequently cause corrosion/surface insulation resistance failures.
3. The moisture boils off so quickly (because of a high ramp rate in the cure oven) that the SMT component actually gets blown off the board surface, resulting in missing components.

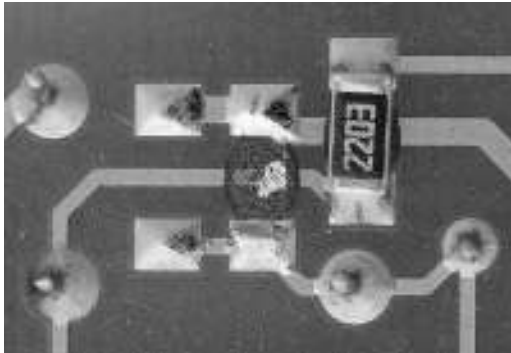


Figure 9.41 Solder bridging.

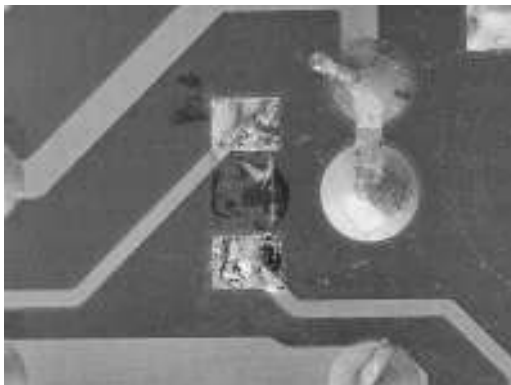


Figure 9.42 Flux penetration.

The tendency of the adhesive to pick up moisture from the surrounding atmosphere is a result of the use of hygroscopic raw materials in the adhesive formulation. Therefore, it is important to screen surface mount adhesives to eliminate any that may cause popcorning problems through excessive moisture pickup. A screening test known as the *glass sandwich test* (Fig. 9.43) is quite useful for studying the tendency of a particular adhesive to pick up moisture. This test involves stencilling a series of five controlled dots (4 mg each) of adhesive onto a glass slide and exposing the adhesive dots to various temperature/humidity conditions, which are dictated by the typical environmental conditions the SMA is expected to endure (e.g., 1 hr @ 30°C/80 percent R.H.).

After complete exposure of the dots to the required environmental conditions, a second glass slide is placed over the adhesive dots to form a sandwich. The dots are spread out by placing a weight on top of the glass slide sandwich, which is then placed onto the surface of a flat aluminium hotplate at 165°C for 90 sec. This results in cure of the adhesive dots. Any moisture absorbed by the adhesive during exposure to the environmental test condition boils off during cure, causing the formation of voids within the adhesive between the glass slides. The amount of voiding is noted and rated on a scale of 0 to 10, with a 0 rating equivalent to no void formation and a rating of 10 equivalent to serious void formation. This test is very useful, because it can be used to quickly screen surface mount adhesives that may have moisture uptake problems.

**9.7.1.8 Cure speed.** The cure speed of a particular adhesive can be measured by recording off-torque values for the adhesive when cured for variable periods of time at different temperatures as described in the following test procedure.

A bare FR-4 board populated with 1206 capacitors is placed in a specially machined hotplate as shown in Fig. 9.44. An IR lamp is moved into position

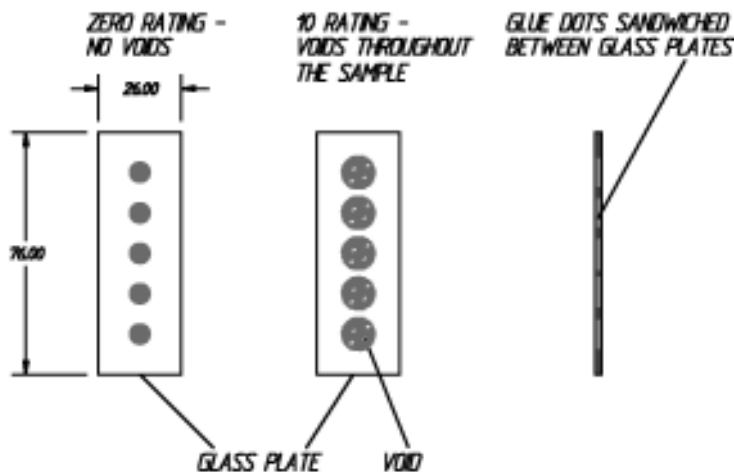


Figure 9.43 Glass sandwich moisture absorption test.

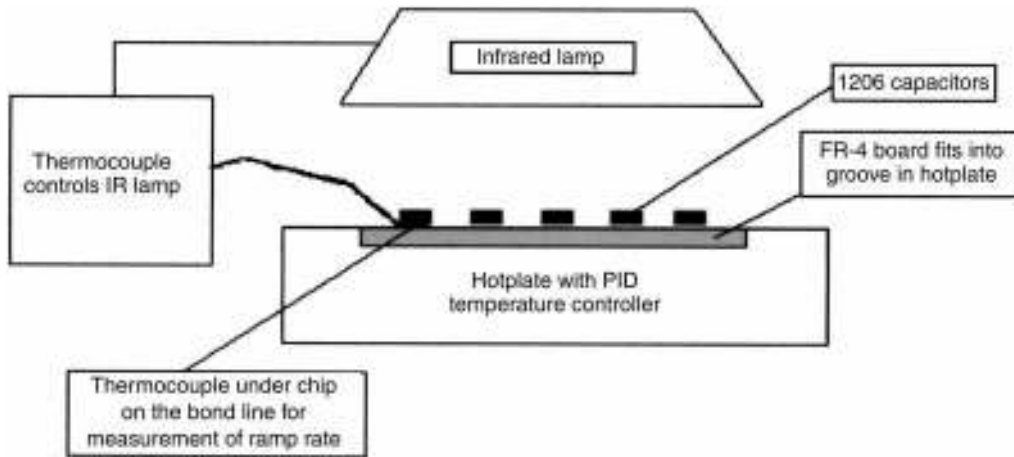


Figure 9.44 Test rig for measuring cure speed by off-torque.

over the board. The IR temperature is controlled by a thermocouple on the board surface, switching the IR lamp in and out as required. Two heat sources are used to produce as rapid a ramp rate as possible. This ensures that the *residence time at the target temperature* does not include excessive time between the start of cure and the target temperature. After cure at the required time and temperature, the board is cooled, and the components are torqued off 24 hr later. In practice, components can be torqued once the board is cooled. These data are used to build up a cure curve. Tables 9.7 through 9.9 show the off-torque values for five Chipbonder<sup>®</sup> products, A through E, under test at temperatures of 100, 125, and 150°C.

TABLE 9.7 Off-Torque Strengths for Chipbonders<sup>®</sup> A–E @ 100°C

Off-torque (N-cm)	SMA A	SMA B	SMA C	SMA D	SMA E
60 sec @ 100°C	Fixture	Fixture	Fixture	Fixture	2.96
120 sec @ 100°C	0.76	1.29	0.4	0.69	4.34
180 sec @ 100°C	2.17	2.7	1.48	2.16	4.2
300 sec @ 100°C	4.77	5.64	3.05	4.13	5.01
600 sec @ 100°C	6.28	5.95	4.71	6.23	5.61

The data presented in Tables 9.7 through 9.9 can be used to generate a cure-speed-versus-temperature graph (Fig. 9.45). This shows the typical increase in strength (torque) with time at different temperatures. The time shown is the residence time and does not include the heat-up time required to reach that temperature. This heat-up time can vary significantly, from 15 sec to several minutes, depending on the temperature and oven configuration. The cure

**TABLE 9.8 Off-Torque Strengths for Chipbonders® A-E @ 125°C**

	SMA A	SMA B	SMA C	SMA D	SMA E
15 sec @ 125°C	2.18	4.41	1.14	0.82	3.09
30 sec @ 125°C	2.78	4.76	1.73	1.43	3.41
60 sec @ 125°C	3.37	5.28	3.03	4.46	4.74
90 sec @ 125°C	4.25	6.14	3.93	5.60	5.30
120 sec @ 125°C	5.11	5.68	3.54	5.65	5.44
300 sec @ 125°C	6.64	6.31	5.26	7.24	5.86
600 sec @ 125°C		6.57			

**TABLE 9.9 Off-Torque Strengths for Chipbonders® A-E @ 150°C**

	SMA A	SMA B	SMA C	SMA D	SMA E
15 sec @ 150°C	4.41	5.48	2.89	3.48	3.63
30 sec @ 150°C	5.25	6.09	3.71	4.54	3.88
60 sec @ 150°C	5.34	6.19	4.07	5.6	4.91
90 sec @ 150°C	5.96	5.92	4.55	5.87	3.66
120 sec @ 150°C	6.29	5.92	4.48	5.86	4.58
300 sec @ 150°C	6.00	5.97	4.57	6.05	4.61

curve shows the times required to reach full cured strength at each temperature. In practice, these are conservative guidelines, because the adhesive will also receive heat during warm-up, and quite often the oven profile does not maintain exactly the cure temperature but reaches a higher peak value. In addition, some users find that achieving 90 percent of full cured strength is adequate for the process. The curing temperature and speed can also be related to DSC results.

**9.7.1.9 Electrical characteristics.** After the wave solder step, the function of the surface mount adhesive has ended. However, the adhesive remains on the printed circuit board for the life of the product and may be subjected to harsh environments, such as high temperature and humidity, combined with electrical loading across the adhesive. It is therefore vital that, under such environmental conditions, the adhesive does not break down during the functioning of the board and cause electrical failure due to corrosion, short circuits, or current leakage across terminals or tracks. The modern SMA must be able to withstand high electrical loadings under increasingly demanding environ-

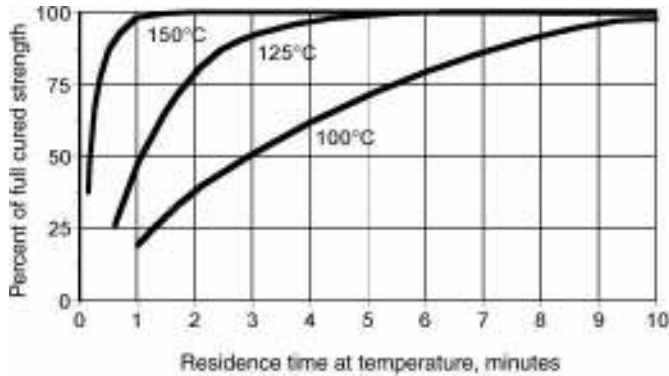


Figure 9.45 Typical cure-speed-vs.-temperature graph.

mental conditions of high temperature and humidity. A series of electrical tests are available to ensure the adhesive does not modify the electrical characteristics of the components with which it comes in contact.

Surface insulation resistance (SIR) is the most commonly known type of environmental test for chip bonders, solder paste fluxes, and board coatings such as solder resist and conformal coatings. The adhesive is coated across an interlinking comb pattern of bare copper tracks (Fig. 9.46).

Track width and pitch, as well as applied bias voltage, test voltage, and adhesive thickness requirements, differ from customer to customer. Environmental conditions and test duration differ also, with many automotive telecom and companies requesting 85°C/85 percent R.H. for 1000 hr. Again, the test setup is allowed to come to temperature in the chamber before the humidity is switched on, to prevent condensation on the test combs.

Typical test conditions are summarized in Table 9.10. The cured adhesive must maintain a minimum resistance value after 1000 hr with an applied bias voltage of 16 VDC in an 85°C/85 percent R.H. humidity cabinet. The adhesive must prevent the type of corrosion illustrated in Fig. 9.47.

Another common test related to SIR is a test for electrolytic corrosion. This test is a measure of the ability of the cured adhesive to cause corrosion on PCB

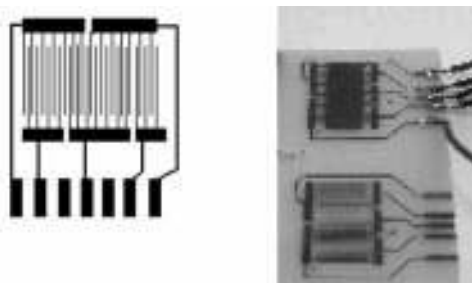


Figure 9.46 SIR test comb pattern (left) and SIR test vehicle (right).

**TABLE 9.10 SIR Test Conditions**

Test parameter	Typical SIR test conditions
Test basis (with modifications)	IPC-SM-840
Check for dendritic growth	Yes
Applied bias voltage	16 VDC
Measuring voltage	250 V, 60 sec
Relative humidity	85%
Temperature	85°C
Time (hr)	1000
Measurement frequency	Initial @ RT, 85/85 then every 100 hr
Adhesive coating thickness	0.1 mm
Pass level	10E × 10 Ω
Comb type	JIS 3197 Type 2 comb (IPC B25 B comb)
Test comb dimensions	12.5 mil lines/12.5 mil spaces
Comb coating	Copper
Number of combs per batch	2

**Figure 9.47** Effect of yield point on chip bonder dot profile.

pads when subjected to high humidity and electrical loading (4 days @ 40°C, 92 percent RH, with 100 VDC applied voltage). A strip of cured adhesive acts as a bridge between brass foil electrodes, with 100 VDC potential across them. Test conditions are 4 days @ 40°C, 92 percent RH. The test setup is allowed to come to temperature in the chamber before the humidity is switched on, to prevent condensation on the test piece. After the test, the foils are checked for tarnishing and corrosion and rated against standard foils.

**9.7.1.10 Yield point and surface mount adhesives.** So what use is this Casson yield point? A useful application of the Casson yield point is for the characterization of surface mount adhesives. Chip bonding involves placing very small dots, each weighing approx. 80 mg, precisely between metal pads (solder lands) on a printed circuit board. The shape of these dots depends very much on the yield point (see Fig. 9.48).

A high  $\tau_0$  produces a conical dot. This holds its shape with time, because the yield point is large enough to resist the force of gravity on any realistic time scale. Too low a yield point, and the dot spreads out, giving a low, rounded appearance. If it spreads too much, it can cover the solder lands and prevent good contact with the SMD.

Surface mount adhesives are formulated to give very specific rheological, or flow, properties to allow rapid and controlled dispensing of the adhesive onto very precise locations on the PCB surface as adhesive dots of very defined shape. SMAs have the ability to change their viscosity when a shearing stress is applied to them. During dispensing, a shear stress is applied to the adhesive (such as the application of a pulse of air pressure that forces the adhesive from a syringe through a narrow nozzle, or the shearing effect of a squeegee dragging the adhesive across the surface of a stencil and forcing it into the stencil apertures and in contact with the PCB surface). Consequently, the viscosity decreases, permitting easier flow of the adhesive. Once the adhesive drop has reached the PCB board surface, the shearing action is removed, and the adhesive quickly restructures and rebuilds its viscosity. This feature is referred to as *thixotropy*, and it ensures that adhesive dots with well defined profiles are achieved and that, once dispensed, the adhesive dots maintain this profile. Maintenance of dot profile is particularly important when one considers that a typical PCB will be populated with a variety of SMD components, each with different standoff heights from the PCB surface and each requiring an adhesive dot of different size.

## 9.7.2 Underfills

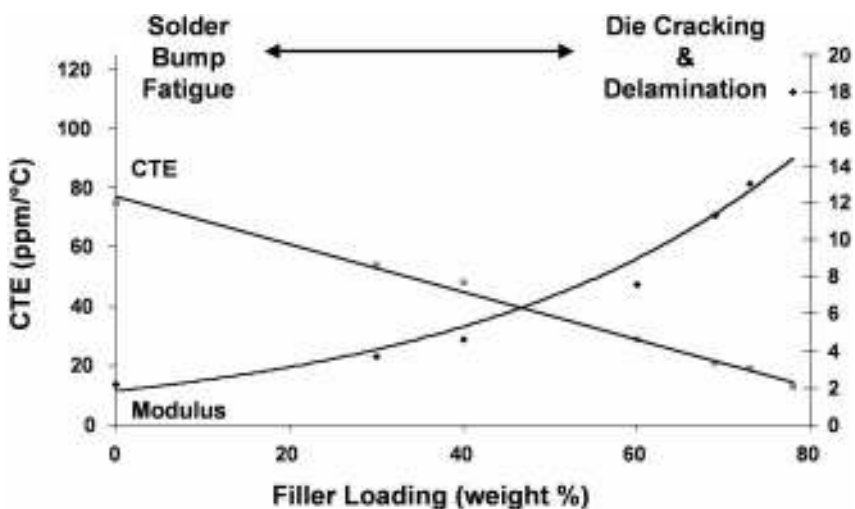
Underfill materials are polymer systems (filled and unfilled) that are used to increase the reliability of a variety of area array packages used in high-density electronic assemblies. Underfill systems are typically epoxy-based chemistries (e.g., bisphenol and cycloaliphatic epoxies) that sometimes have a filler



**Figure 9.48** Effect of yield point on chip bonder dot profile.

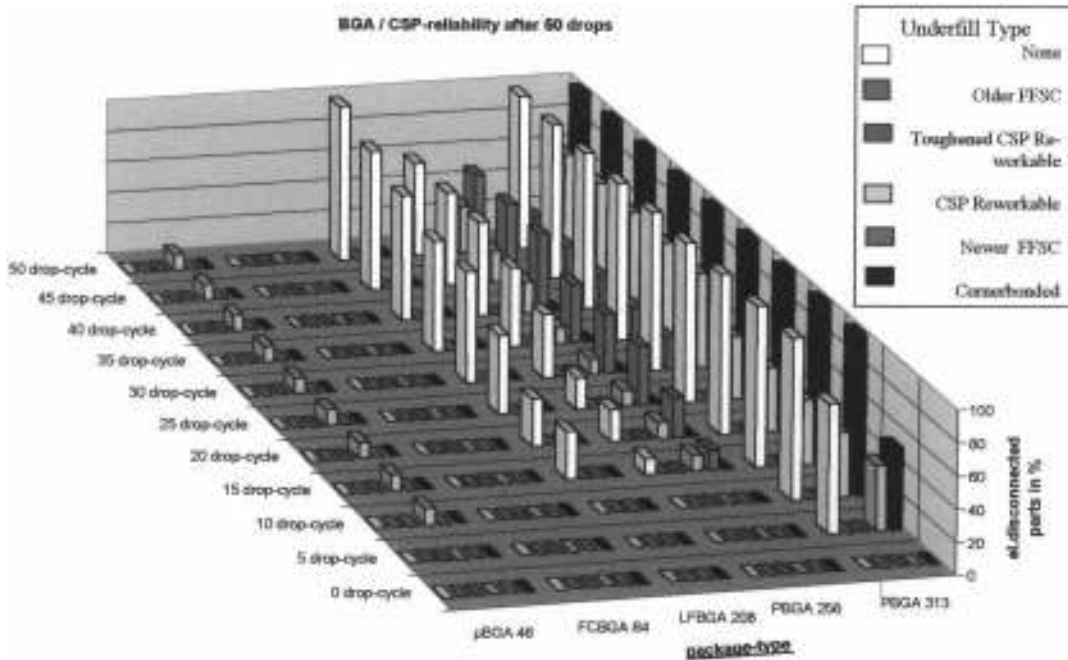
added. There are two main reasons for using an underfill material. First, it is used to relieve stress from the large CTE mismatch between a silicon device (e.g., flip-chips) and the substrate to which is bonded (e.g., FR-4). Second, it is used to increase the reliability of the component, such as a chip-scale package, with respect to physical shock and vibration.

Underfill materials are used to increase the reliability of a variety of component types, including flip-chips, chip-scale packages, ball grid arrays (BGAs), and micro BGAs. Most manufacturers that use flip-chips on board (FCOB) underfill them to deal with the large CTE mismatch between the silicon die and the FR-4 substrates typically used in manufacturing these products. The other packages may be underfilled only if there is either a perceived risk to the products (e.g., a cell phone may undergo frequent drops) or if they are intended for a high-reliability application (e.g., avionics). The CTE matching of the underfill materials is typically achieved through the addition of silica-based fillers. This addition lowers the CTE to provide a gradient between the silicon chip and the substrate. Underfills used to provide physical protection to other packages typically have higher  $T_g$ , but they have a modulus that is better suited for that function. The need for a low CTE in an underfill is an often misunderstood concept. Not all underfills necessarily need to have a low CTE to provide reliability enhancement to all devices. The balance between CTE and modulus should be examined to provide the highest reliability enhancement possible. A graphic showing the relationship between modulus, CTE, and two common failure modes is Fig. 9.49. As this figure illustrates, understanding the failure mode of the device is critical in choosing a material with the right properties. Also note that using a material with a low CTE does not guarantee an increase in reliability if the device is susceptible to fatigue cracking. Figures 9.50 and 9.51 illustrate the reliability of various underfill

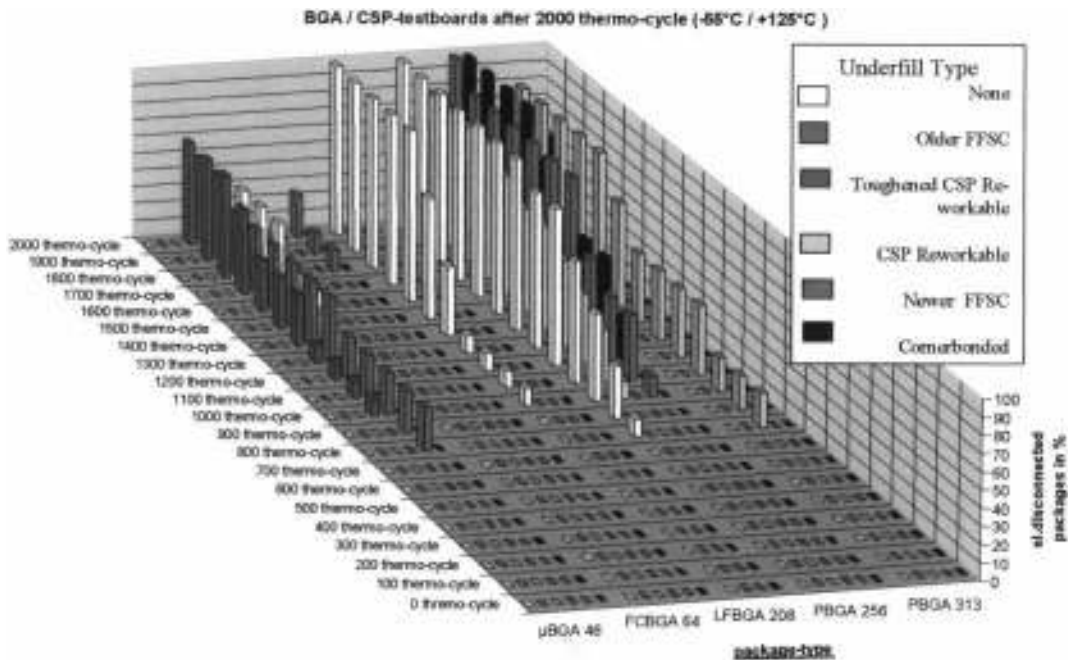


**Figure 9.49** Graph showing the relationship between CTE, modulus, and failure modes.





**Figure 9.50** Reliability of various underfill materials with respect to drop tests.



**Figure 9.51** Underfill reliability with respect to thermal cycling.

materials under drop testing and thermal shock, respectively. The materials tested included two fast-flow snap cures (FFSCs) and two reworkable underfills.

**9.7.2.1 Capillary underfill.** These low-viscosity liquids are designed to flow under a component by capillary action, wetting to the chip and substrate surfaces and encapsulating the solder joints. Underfills designed for assembly-level flip-chip generally cure in 5 min or less at 165°C to form a hard seal with high adhesion to both the component (flip-chip or CSP) and the substrate. Underfills designed for package-level assemblies offer improved assembly reliability but generally require more time to flow under the die and to cure. Faulty or skewed components must be detected before underfill cure, because most all capillary flow underfills are permanent (see Sec. 9.7.2.3 for reworkable underfills).

Underfill is applied close to the edge of a flip-chip or CSP to enable capillary forces to encapsulate the gap between the component and the board. Dispensing capillary underfill materials requires specialized equipment to achieve the accuracy and precision required for high-volume assembly. At a minimum, the dispenser must reproducibly position successive assemblies and apply a predetermined volume of underfill to the edge of the component. Heating the substrate is a common secondary requirement that accelerates capillary flow. Cure is usually accomplished in belt-style reflow or curing ovens.

Several dispensing patterns are used for applying underfill to die and packages. The simplest pattern involves applying underfill to a single side and maintaining a reservoir as material wicks between the package and substrate. If necessary, underfill can be applied to the remaining three sides using a “U” pattern to form a fillet. With newer-generation materials, the filleting step can be eliminated.

Another common flow pattern recommended for fast processing of smaller or simpler devices involves dispensing an “L” of material (two sides), waiting for the flow out, and then dispensing an inverted “L” to complete the fillet, if needed. Other patterns can be used, but the line/L, double L, and their variations are most common today.

The underfill flow rate or underfill time is one of the key attributes of an underfill encapsulant. Suppliers typically use smooth or frosted glass slides with a predetermined gap established by shim stock to evaluate underfill times. In some cases, a fixture is used to maintain a stable gap and provide a more efficient (more than one slide assembly can be prepared at a time) means of running the test.

The fixture is placed on the hotplate and monitored for the selected underfill temperature (typically, 60 to 100°C). When the selected temperature is reached, underfill material is dispensed at the gap area. The flow front is timed to determine the time required to reach 1 cm. Information regarding underfill time and voiding predisposition can be obtained.

Other methods, such as glass slides set up with a variable gap that runs from ~0.13 mm to 0 (creates a wedge shape), can be used to expeditiously de-

termine the compatibility of an underfill with various gap sizes. Another approach that may be utilized more by IC manufacturers is the use of a quartz bumped die that is consistent with the IC size to be used in the application. Different combinations of substrates with slides such as FR-4, silicon, and so on can be evaluated. The predisposition to voiding can also be assessed before and after cure. The glass slide/quartz die tests are not designed to reflect underfill times in specific applications, because solder masks, chip size, chip passivation coating, bump count, bump spacing, bump location, and surface cleanliness will all have a dramatic effect on underfill times. This test may be used to compare alternative encapsulant suppliers, alternative underfill temperatures, and the shelf life/pot life of underfill encapsulants.

**9.7.2.2 Fluxing (no-flow) underfill.** Fluxing, or so-called “no-flow,” underfills are an attempt to make underfill processing more compatible with conventional surface mount assembly processes by eliminating the dedicated oven required for cure. A fluxing function incorporated into the underfill combines the component attachment and underfill cure processes.

Fluxing underfill is applied directly to the attach site on the substrate preceding component placement. The flip-chip or CSP is then placed into the underfill. During reflow, the underfill acts as the flux, enabling interconnect formation and self-centering before curing of the underfill. Ideally, underfill cure is completed in the reflow oven. Otherwise, subsequent reflow or deliberate heat treatment is required to complete underfill cure.

Fluxing underfills are different from capillary flow materials in several ways. Viscosities are typically much higher than that of capillary underfills. Because inorganic fillers in the underfill will generally impede essential contact between the CSP solder balls and the attach pads, fluxing underfills are unfilled, which results in a higher CTE. The entire board must be discarded if defective or skewed components are detected, because the underfills are not removable.

**9.7.2.3 Removable/reworkable underfill.** Occasionally, malfunctioning flip-chip or CSP components are discovered in the factory or in the field. Conventional underfills are not removable once cured, requiring that a malfunctioning assembly be discarded, sometimes at considerable cost. Removable underfill enables repair of the assembly.

Removable underfill is typically dispensed and processed much like other underfills. Extra functionality enables them to soften or degrade when sufficiently heated. The assembly repair process is similar to that of other solder SMT components with the exception of an extra step or extra time required to remove residual underfill.

**9.7.2.4 Staking or corner bond underfill.** An alternative approach to complete underfilling of chip-scale package devices for increased reliability with respect

to shock and drop is to bond the corners or edges of a CSP (see Fig. 9.52). Some materials can be applied after the device is soldered to the substrate, and some can be dispensed with the solder paste before reflow. The advantage with these materials is that you can reduce the capital equipment expense by eliminating a curing oven and a separate dispenser, and reduce cost by using less material—four to eight dots versus the entire surface area under the package. There is a limit to the mass of components whose reliability can be enhanced; if the mass of the component is too great, the adhesive may not hold. Also, when dispensing corner dots with packages that have corner bumps, care must be taken not to interfere with the reflow soldering process.

**9.7.2.5 Molded underfill.** Costs related to use of liquid flip-chip underfill on high-volume manufacturing lines have driven development of underfills that are processed using high-throughput molding equipment. A solid mass of underfill is heated and softened then forced under pressure into a molding cavity containing one or more flip-chip assemblies. The process is very fast and capable of processing many assemblies simultaneously.

**9.7.2.6 Wafer-applied underfill.** Costs related to use of liquid flip-chip underfill on high-volume manufacturing lines have driven development of underfills that are applied to an entire wafer of flip-chip components before wafer dicing. Underfill dispensing during flip-chip assembly is eliminated. Wafer-applied underfills and accompanying application and assembly processes are under development by a number of organizations.

### 9.7.3 Electrically conductive adhesives

Continuing improvements in adhesive technology have enabled adhesives to replace solder in many electronic assembly applications. There are three types of electrically conductive adhesives formulated to provide specific benefits where an electrical interconnect is desired.

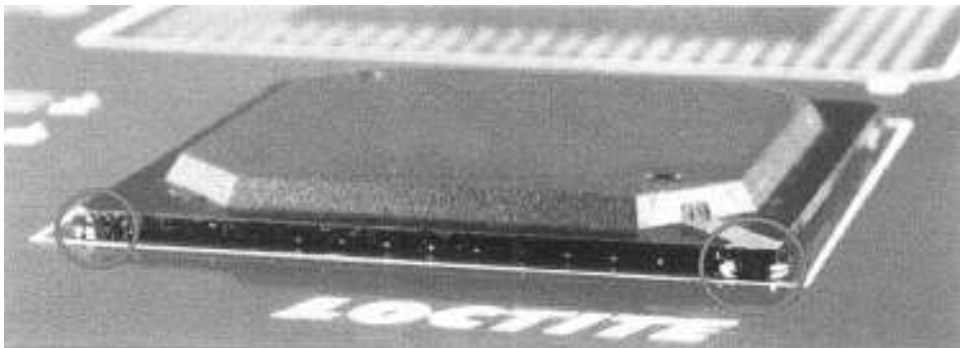


Figure 9.52 Corner bonded CSP.

1. *Isotropic* materials, which will conduct electricity along all axes, are able to replace solder on thermally sensitive components and can also be used on devices that require a ground path.
2. *Conductive silicones* help protect devices from environmental hazards such as moisture, and they shield electromagnetic and radio frequency interference (EMI/RFI) emissions.
3. *Anisotropic conductive polymers*, which allow electrical current to flow only along a single axis, provide electrical connectivity and strain relief for flip-chip devices.

All electrically conductive adhesives have two common qualities: they provide a chemical bond between two surfaces, and they conduct electricity.

**9.7.3.1 Isotropic materials.** Electrically conductive isotropic epoxies can be used for electrical interconnect on nonsolderable substrates such as glass and ceramic, or to replace solder on thermally sensitive components that cannot withstand the 200°C processing temperatures of typical solders. Traditional applications for isotropic epoxies include bonding the flex circuit of a glass LCD to the mating trace on a PCB and attaching a component lead to a matching land on a thermally sensitive printed circuit board. Isotropic electrically conductive epoxies offer nondirectional, or all-directional, conductivity by incorporating conductive particles such as silver, nickel, or gold into the adhesive formulation. These particles carry electrical current through the epoxy resin. The most popular filler material is silver because of its moderate cost and superior conductivity. Isotropic silver-filled epoxies are available in heat- or room-temperature curing and single- or two-component formulations. Because electrically conductive epoxies require temperatures of only 150°C or less to cure, and room-temperature curing is a viable option, isotropic epoxies provide an ideal alternative to solder on thermally sensitive parts. Several varieties of silver-filled, isotropic epoxies are available to electronic device manufacturers. General-purpose, silver-filled room-temperature and heat-curing epoxies have been formulated specifically for rework and repair applications on large-pitch interconnects. For example, if the trace on a circuit board's surface gets gouged, selected versions of these epoxies may be used to repair the circuit in place of the original solder. These adhesives can also be used as solder substitutes on through-hole components. Certain grades of silver-filled epoxies are "die attach grades," designed to provide an electrical ground path and transfer heat from the chip to the substrate. Both electrically and thermally conductive, these epoxies develop strong, durable bonds on many different substrates, including metals, ceramics, glass, laminates, and molded plastics. Room-temperature-curing, flexible silver-filled epoxies have been formulated for electronic interconnect applications that require high flexibility, such as assembly and repair of flexible circuits or bonding flexible substrates and connectors. Gold bonders are heat-curable epoxies formulated to offer enhanced adhesion to gold-plated devices and other high-end metal surfaces

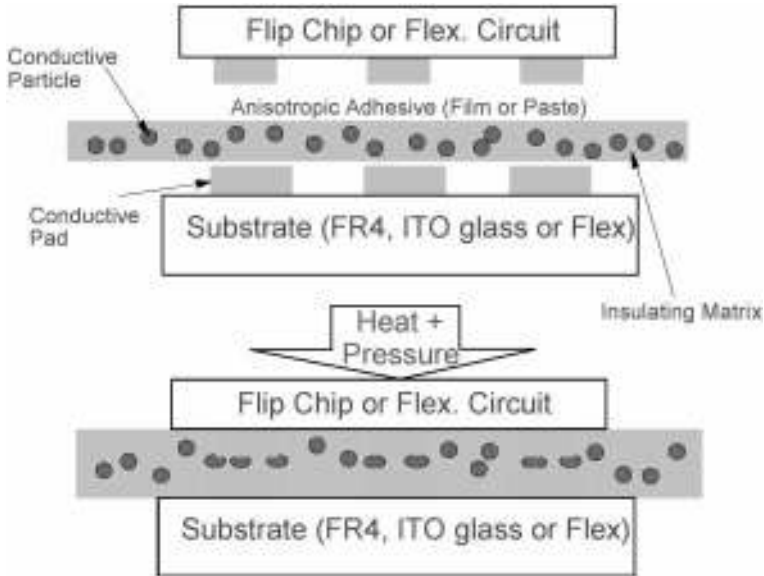
such as palladium. These adhesives offer enhanced shear strength and are formulated to absorb the stress associated with extreme thermal mismatch between dissimilar substrates. Typical adhesives on the market today cure in 30 min at 150°C, or in 1 hr at 125°C. Certain grades of silver-filled epoxies are specifically formulated for direct use on the die and are aptly referred to as die attach grades. These adhesives are formulated to provide an electrical ground path and transfer heat from the chip to the substrate. A variety of formulations are available, offering benefits such as high purity and low ionic content, a long working life, and snap heat cures of 3 min or less.

**9.7.3.2 Conductive silicones.** New conductive silicone materials allow device manufacturers to shield EMI/RFI emissions and seal electronic enclosures, protecting them from environmental hazards. Conductive silicones can be applied directly to areas that require environmental sealing and EMI/RFI shielding, and cured in place to form a customized gasket that eliminates the need to inventory cut gaskets.

A number of conductive fillers can be incorporated into gasketing formulations. These materials are available with varying levels of attenuation and different cure methods, including heat cure and room-temperature vulcanization. In addition to environmental protection and EMI/RFI shielding, conductive silicones can also be used to provide ground paths for electronic devices that require high flexibility. For example, on video touch screens, silicone conductive adhesives are used to bond wire. Certain grades of *silver-filled epoxies* are *die attach grades* designed to provide an electrical ground path and transfer heat from the chip to the substrate leads, to a ground strip on the back of the screen, providing an electrical interconnect that communicates the request for information from the touch screen to the circuits inside the computer. Whereas solder and most other adhesives would be too rigid to hold up against the constant contact required by the touch screen, highly flexible and resilient silver-filled conductive silicones easily survive high-impact applications.

**9.7.3.3 Anisotropic conductive polymers.** Anisotropically conductive adhesives consist of mixtures of conducting fillers in an insulating matrix, just like isotropic conductive polymers. The ability of these materials to conduct in one axis (the z-axis) while remaining insulators in the x-y plane is governed entirely by the loading, particle size distribution, and dispersion of the conductive filler. The aim with these adhesives is to trap (at least) one conductive particle between conductive bumps on the flip-chip and the corresponding pads on the substrate while preventing bridging between pads.

Figure 9.53 shows a diagram of a cross section through a fine-pitch assembly. Clearly, if the filler loading is increased, the probability of shorts between adjacent pads is dramatically increased. When the filler level is too low, there is a probability that no particles will be trapped between conductors, and open circuits will occur. In most anisotropic materials, the particles are randomly distributed in the matrix material. This in itself can cause problems (particu-



**Figure 9.53** Illustration of an anisotropic adhesive.

larly for very fine-pitch applications), because there will always be local variations in particle concentration throughout the material, which can result in an open or short circuit. Various methods have been tried to address this random particle distribution.

The insulating matrix will be either thermoplastic or thermosetting, depending on the final application of the assembly. Although thermoplastics have some advantages (reworkability and assembly speed), they are not normally chosen as matrices for anisotropic adhesives; the robustness afforded by a thermosetting system (resistance to heat, moisture, and mechanical stress) means that they are the more common choice. Epoxy resin-based adhesives are a particular class of thermosetting material that has found wide acceptance in the electronics industry. A broad range of desirable properties are achievable with these epoxy-based systems (adhesion to a variety of substrates, toughness, and corrosion resistance), and the final material properties can be tailored to the final application.

A number of conductive fillers have been used to impart conductivity to the (insulating) matrix. The filler is generally spherical in nature and is often monodisperse; examples include gold-plated polymers, solid gold, silver, nickel, and Sn-based alloys.

#### 9.7.4 Thermal management

Thermal management is a growing challenge in the electronics industry. As the overall size of electronic devices grows smaller, the enclosed electronic assemblies operate at higher frequencies and generate more heat. Increasing input/output (I/O) counts, which make devices faster in cycles per second, also

cause electronic devices such as ASIC and other hybrid devices to generate greater amounts of heat. This heat, which can decrease the effectiveness and shorten the component's overall life, must be quickly and effectively dissipated for devices to function effectively. Electronic device manufacturers rely on heat sinks attached to ICs to diffuse excess heat. These heat sinks can be attached using mechanical fasteners, thermally conductive adhesives, greases, tapes, or pressure-sensitive pads. Not all of these methods are equal in their operating effectiveness, thermal management capabilities, or ease of application.

Of all the available methods of thermal management, thermally conductive adhesives are the most process friendly. When applied correctly, adhesives produce minimal air voids, resulting in consistent heat diffusion.

Adhesives can be used on any shape or size device and, in addition to providing a permanent bond, will add structural support to the device. Adhesives provide excellent electrical isolation and will not migrate or loosen during normal application or use. Adhesives are single-component materials that do not require temporary or permanent fixturing with mechanical fasteners; as such, they require little inventory. Because they are versatile and simple to use, adhesives can be dispensed using a manual process or may be automated with a robotic gantry to pick, place, and orientate the preactivated parts (heat sinks). An added programmable syringe dispenser can apply the set amount and pattern of adhesive to the opposite side (component) of the preprogrammed site, or vice versa.

Thicker adhesive bond lines result in improved thermal shock resistance. For consistent performance, it is important to ensure consistent bondline thickness. Adhesive formulators have developed self-shimming adhesives that incorporate tiny, 5-mil (.005-in) glass beads into the resin to ensure a minimum 5-mil gap thickness. Adhesive resins are not thermally conductive by nature. Fillers must be added to the resin base to make the adhesive transport heat more effectively. The most popular thermally conductive filler is currently aluminum oxide, which offers excellent conductivity (70 W/m-K) and low cost. Aluminum nitride and boron nitride offer higher conductivity (150 W/m-K) and higher strength but are also more expensive. Other popular fillers include metals such as steel, nickel, aluminum, and silver, which offer higher thermal conductivity than alumina. Of these, silver has the highest thermal conductivity. However, these metals are also more likely to separate from the resin as a result of their higher density.

Adhesives are easy to adapt for the specific needs of an application; typical alumina fillers can be easily replaced with a substitute filler that will remove heat faster in more demanding environments. Depending on the gap thickness that the adhesive must fill and the speed at which the heat must travel between substrates, the percentage of filler in thermally conductive adhesive resins is typically 40 to 60 percent.

**9.7.4.1 Thermal adhesive chemistries.** Thermally conductive adhesives are available in several chemistries, appropriate for different applications. For an ef-



fective and lasting bond to be established, adhesives require solidification or “cure” to take place. Cure times and methods vary, depending on the adhesive chemistry used.

Single-component silicone adhesives are ideal for environments that undergo extreme temperature cycling (below  $-55^{\circ}\text{C}$  to above  $200^{\circ}\text{C}$ ). By nature, silicones have low cohesive strength and, therefore, are excellent for repair and rework applications. As they are low-modulus materials, silicones offer limited adhesion and limited abrasion resistance. Most of these materials require exposure to heat to cure, but other available curing mechanisms include room-temperature cure, ultraviolet (UV) light cure, and activator-induced curing. Depending on the adhesive formulation and the temperature required, the electronic component can spend several minutes to several hours in an oven for cure to be completed. Single-component acrylics are general-purpose adhesives that offer good adhesion to many substrates as well as good cohesive strength. These adhesives can withstand normal operating environments in the range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . Acrylics typically require an activator or a chemical that initiates solidification to be applied up to 24 hr before the adhesive is applied. Activator-initiated acrylics fixture between 30 sec to 5 min, with full ambient cure in 24 hr. Activator cured acrylics are very popular in the electronics industry, because many devices cannot withstand the temperatures required for heat cure, and effective light cure is often difficult. Available grades of acrylic adhesives can be easily reworked using a thermal parting tool and mild mechanical action. Acrylics can also be formulated to achieve partial cure or fixturing on exposure to UV light. Because electronic devices seldom incorporate one transparent substrate capable of transmitting light, UV-fixturing acrylic adhesives are formulated with a secondary heat cure mechanism that will complete the cure process in shadowed areas. Epoxies are highly durable adhesives that offer good thermal and chemical resistance, good cohesive strength, and high adhesion to a wide variety of substrates. Available as single- and two-component systems, epoxies will withstand operating temperatures slightly higher than  $125^{\circ}\text{C}$  and cure on exposure to heat or to a two-part catalyzed reaction. Rework is extremely difficult, and sometimes impossible, because of the structure of the epoxy. Techniques used to get the epoxy to revert to a reworkable state will usually destroy the board or the components, which are usually also made from epoxy material. Additional available adhesive chemistries include urethane, polyester, and other thermoset elastomeric systems.

**9.7.4.2 Phase-change thermal interface materials.** Phase-change technology is the latest development in thermally conductive materials. These materials are generally high-melting waxes that contain conductive fillers. They offer most of the advantages of thermal greases in terms of wetting, bond filling, and conductivity, but they will not migrate. These materials are typically pre-applied on the heat sink or arrive from the supplier in the form of a coated pad. When the entire apparatus is heated during the manufacturing process, the phase change material melts (typically in the range of  $50$  to  $60^{\circ}\text{C}$ ) and pro-

vides void-free gap filling. Over the next five years, adoption of phase-change technology into the assembly process is expected to grow by 40 percent per year, in large part because of the products' excellent thermal conductivity, ease of application, low cost, and ability to be repaired and reworked.

### 9.7.5 Conformal coatings

Conformal coatings are polymeric materials used to protect electronic assemblies from a wide variety of life-cycle contaminants. Conformal coatings provide a high degree of insulative protection and are usually resistant to many types of solvents and harsh environments encountered in the product life cycle. The coating materials also act to immobilize various types of particulate on the surface of the PCB and function as protective barriers to the various devices on the board.

They are resistant to moisture and humidity and are often applied as an afterthought (not part of the initial design) to quiet down electrical bias and potential arcing during high-humidity operating conditions, especially on fine-pitch assemblies. They can also remedy other electrical problems on the board that can occur as a result of the environment in which the electronic device must perform.

The primary traditional classifications are as follows:

- AR = acrylic
- ER = epoxy
- UR = urethane
- SR = silicone
- XY = parylene

These systems are primarily made up of monomers, oligomers, defoaming agents, fillers, and wetting agents. Various combinations of each are added to the formulations to adjust the cured and uncured properties. Solvents were, and still are, typically added to adjust application viscosity. They "flash off" by solvent evaporation, leaving a resin matrix to initiate the cure. The volatile organic compound (VOC) emissions associated with this type of cure created a need for more environmentally acceptable production chemistries and cure mechanisms. Presently, solvent-based conformal coating chemistries exist that are exempt from environmental regulations.

All resins except for acrylic resins are cured by an irreversible polymerization reaction with a varying degree of cross-linking (thermoset polymers). The cross-linking of the epoxy, urethane, and silicone polymers provides very good chemical resistance but also makes it difficult to remove the coatings when performing repair work. No polymerization reaction is taking place when applying acrylic coatings. Therefore, it is misleading to say that acrylic coatings are cured. Most of them are formed by drying a solution of already formed acrylic polymer chains dissolved in a solvent (thermoplastic polymer). Hence,

acrylic coatings are easily dissolved in many organic solvents, providing poor chemical resistance but facilitating repair work. Consequently, most acrylic materials are solvent based.

All except the paraxylylenes have traditionally been solvent based until the 1990s, when environmental issues dictated a need to change. Now, many materials are solvent-free chemistries (100 percent solids). The ability to effect an ultraviolet (UV) cure is commonplace. This new generation of conformal coating materials has also given birth to hybrid coatings that contain two or more systems to achieve superior properties, i.e., acrylic resin and urethane resin (ARUR) chemistries.

The chemical categories discussed above break down into two liquid families, organic and silicone.

**9.7.5.1 Conformal coating application.** Conformal coatings can be sprayed, either manually or automatically. In manual operations, aerosol cans or hand-held sprayguns can be used. To automate a spray process, one of two methods can be employed: a reciprocating spray system or a selective coating unit.

Any application method brings health and safety concerns to the user. Manual operations must address operator issues even more seriously, as the employee will have direct contact with the spray process. In aerosol or manual spray operations, it is suggested that the operator be supplied with adequate respiratory equipment.

Aerosol spray methods are typically used in lower-volume applications rather than for high-volume production. Aerosols have a low solids content (less than 5 percent), so ventilation of the spray area is paramount. Spray in a horizontal position to prevent the flow of coating into undesirable areas and to assist in producing a consistent film build. Masking is required. To ensure total coverage, apply a thin coating (approximately 0.001 in) during each one of four coats, rotating the board 90° after each cycle. Although initial startup costs for an aerosol application system may be low, efficiency is a concern. Material utilization for aerosol applications is typically 25 to 40 percent.

Manual spray operations can be very similar to aerosol applications. Proper ventilation must be ensured. Again, the spray application should be completed in a horizontal position in four thin (0.001-in) passes, rotating the board 90° after each cycle. Masking is required. A manual spray operation should consist of a spraygun, a material reservoir, and a cycle actuation device (trigger assembly, valve controller, and so on). Fluid and air pressure can be regulated to produce a fine, atomized spray. When using a material reservoir, be sure to pressurize your conformal coating material with dry, unlubricated air or nitrogen. This is especially prudent for moisture-cure coatings that may take on cured characteristics if exposed to unfiltered air for a prolonged period of time.

Care should also be given to UV-curable coatings. Because of the presence of UV in sunlight and other light sources, steer away from using clear feed lines from the reservoir to the spray head. Black tubing can easily eliminate any concerns over UV light penetrating and contaminating your coating process.

Manual spray operations can be a quick, relatively inexpensive avenue into a conformal coating process. Spray heads can accept higher-viscosity fluids than aerosols and may not require dilution. A more controlled spray process can result in greater transfer efficiencies; however, this depends on time and the complexity of each assembly. In bulk spray applications, material utilization may be relatively similar to aerosols. If greater care is taken, utilization can improve to 50 percent or better.

A reciprocating spray system provides a method that incorporates at least one spray valve; more often, many more exist in an automated in-line process. A reciprocating sprayer incorporates a paper belt conveyor that will transport a masked board into the spray area. There, a bank of spray heads will move back and forth over your assembly, producing an even film build. Material tanks will feed each spray head in a similar fashion to the manual process described above. The same considerations for material chemistry and curing mechanism should be observed. Proper ventilation through the spray area must be achieved.

Reciprocating systems offer advantages over manual spray operations. Automating provides increased throughput capabilities and a more uniform coating. However, an investment must still be made in masking or shielding devices, as well as in the automation equipment itself. Material utilization is still an issue, as waste is applied to masking components and the paper belt conveyor.

Variables such as temperature; valve, air cap, and nozzle design; atomization pressure; humidity; and flow rate will all have an impact. Generally, viscosity for spraying is lower than for dipping.

Dipping is a low-cost, efficient way to apply a conformal coating. This method consists of the immersion of an assembly into a bath of coating to supply coverage. Masking of sensitive areas is required. Assemblies should be dipped vertically as opposed to horizontally. Coating thickness, and the inevitable success or failure of this method, relies heavily on the immersion and withdrawal speed. Typically, immersion speeds are recommended to be between 6 and 12 in/min. An applicable speed should be chosen to allow displacement of air surrounding all components and to prevent air entrapment. Once immersed, the assembly should remain in the bath until all bubbling has ceased.

The withdrawal speed from the dipping process should be slower than the cascade effect of the coating. This typically can be equated into 1 to 6 in/min. Remember, the slower the withdrawal speed, the thinner the coating.

Slower withdrawal speeds and lower-viscosity materials may cause coating to flow and can produce an uneven coating over the assembly. This is simply a product of gravity and must be evaluated prior to implementation. Transfer efficiencies of 50 to 75 percent can be achieved in a dipping operation.

To coat a limited quantity of board assemblies, a brushing technique may be utilized. This is a labor-intensive operation that may not be suitable for high production rates. This application method consists of manually using a brush or similar device to “paint” the coating on an assembly. This can reduce some masking by virtue of the controlled nature of the process; however, hoping for

a mask-free environment would be optimistic. Brushing is most often used in a repair or touch-up mode. Obtaining uniform film builds over an entire assembly is difficult in this method.

Be wary of air bubbles forming during the application process. It may be necessary to restrict yourself to only one or two strokes of the brush to reduce the possibility of air introduction.

Considerations must also be given to moisture cure coatings that may change in viscosity during application. Use an appropriate solvent or cleaning agent to remove coating from a brush that may be hardened by the cured material.

Polymer films can be deposited on a substrate in a vacuum by the following methods:

1. Vaporizing the polymer via sputtering or evaporation (physical vapor deposition)
2. Chemically reacting volatile compounds to form a polymer (chemical vapor deposition)
3. Reacting two or more volatile metal organic compounds (metal organic chemical vapor deposition)
4. Plasma polymerization of stable organic compounds (plasma enhanced chemical vapor deposition)
5. Laser polymerization of stable organic compounds

The major techniques are physical vapor deposition and chemical vapor deposition; all other vacuum deposition techniques are special cases of the two major ones. The major advantages of vacuum film deposition are as follows:

1. It provides rapid processing.
2. The substrate coverage is conformal.
3. Vapor penetrates small interstices.
4. No liquid sheath is present on substrates.
5. Films can be highly cross-linked.
6. The growth rates can be controlled.
7. Sterile films are produced.
8. Multilayered films are readily deposited.
9. Because thin films can be readily prepared, polymer usage is minimized.

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# 10

## Thermal Management Materials and Systems

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### 10.1 Introduction

Heat is an unavoidable by-product of every electronic device and circuit,<sup>1</sup> and it needs to be minimized to improve reliability and maximize electrical performance. Managing this heat, commonly referred to as *thermal management*, requires an understanding of thermodynamics and an in-depth knowledge of the materials.

This chapter, which provides both an introduction into thermal management of electronic packaging and descriptions of the various materials used, is intended not only for thermal management experts but also for those in related fields who have a need to model and optimize their physical designs.

The trend in electronic packaging has been to reduce size and increase performance. This can be seen in the higher levels of integration in semiconductors and the increased usage of hybrids and multichip modules (MCMs). Intel's first microprocessor, the 4004, had 2,300 transistors. The latest microprocessor, the Pentium 4\*, has 42 million transistors.<sup>2</sup> Placing more functions in a smaller package has resulted in higher heat densities, which mandate that thermal management be given a high priority in design so as to maintain system performance and reliability. As clock rates increase every year, the power dissipated in the semiconductors during switching is increasing at a linear rate, proportional to frequency as shown by the following equation:

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\* Pentium is a registered trademark of Intel Corporation.

$$P = \frac{CV^2}{2}f \quad (10.1)$$

where  $C$  = input capacitance in farads  
 $V$  = peak-to-peak voltage swing of signal in volts  
 $f$  = switching frequency in hertz

If the values of input capacitance and voltage swing had remained the same while the clock frequency increased, the amount of power dissipated would have grown at an exponential rate and would be unmanageable. Luckily, the thermal designer has been aided with reduced input capacitance for each new generation of integrated circuits. In addition, voltage swings, which are directly tied to logic power supply voltages, have been undergoing reduction from the classic 5.0 V to a forecast <1 V.<sup>3</sup>

The initial sections of this chapter review basic heat flow theory as applied to electronic packaging. Next, the various packaging methods and their materials are investigated. Finally, the factors that determine thermal resistance are evaluated.

### 10.1.1 Temperature effects on circuit operation

Increasing the temperature of an active device typically changes its electrical parameters such as gain, leakage, offset, threshold voltage, and forward drop. These parameter variations over temperature are well documented and incorporated into most circuit simulations. Most circuit designers are aware that leakage currents in active silicon devices approximately double every 10°C. Minimizing the temperature of these devices thus reduces the effect of the leakage currents. If the temperature of an active device increases too much, it will exceed the manufacturer's specifications and usually will fail.

Changing the temperature of passive devices typically changes their values. For example, film resistors have temperature coefficients that range from several to several hundred parts per million per degree Celsius (ppm/°C). Ceramic capacitors, depending on the dielectric material, have temperature variations from 30 ppm/°C to 60 percent over the military or extended temperature range (−55 to +125°C). These changes in electrical parameters are typically not desired. If the temperature increase is high enough, the active or passive device being heated may permanently degrade or even totally fail. Such failures include thermal runaway, junction failure, metallization failure, corrosion, resistor drift and electromigration diffusion. Therefore, the electrical designer needs to minimize any temperature increases. While the designer may not have control over environmental changes, he does have control over the device's self-heating. For analog circuits, he can make the circuits as efficient as possible. For digital circuits, he can select devices that produce the lowest amount of heat for the required clock rates.

In some hybrid and MCM circuits, certain component pairs or groups are designed to track over temperature to achieve the required circuit performance. Typically, resistors, transistors and diodes are components that fall

into this category. For example, in an operational amplifier circuit, as shown in Fig. 10.1, resistors  $R_1$  and  $R_2$  must track to achieve constant gain over temperature. If  $R_1$  were physically located in a cool location on the substrate and separated from  $R_2$ , located next to a power transistor whose power level and thus temperature were varying, then the output of the operational amplifier  $V_{out}$  would modulate as a function of temperature and power in the transistor. One solution would be to relocate  $R_2$  adjacent to  $R_1$  and isolate it from the power transistor. An alternative solution would be to lower the temperature of the power transistor so that it would have less heating effect on  $R_2$ . Techniques to achieve this latter solution include using a larger power transistor, a better thermal die attach, a heat spreader, or a better substrate-to-package attach.

Therefore, to meet both the electrical and thermal performance of a circuit, the designer must thermally and electrically model each device and iterate the design to achieve the required performance. If any devices that must closely track are found to have significant differences, then the physical designer must either select alternate materials or incorporate additional cooling schemes.

### 10.1.2 Temperature effects on physical construction

With few exceptions, materials expand when their temperature is raised and contract when cooled. The *temperature coefficient of expansion* (TCE) is a parameter found in the literature for each material. Another name for this parameter is the *coefficient of thermal expansion* (CTE). The CTEs and thermal conductivities for various materials used in microelectronic assemblies are detailed in subsequent tables.

Thermal stresses occur when a material is constrained during expansion or contraction. An example of this is a copper heat sink soldered to a metallized ceramic substrate as shown in Fig. 10.2. The ceramic has a CTE of 6.4 ppm/°C, whereas the copper has a CTE of 16.8 ppm/°C. During temperature cycling, in which there are a number of periods of heating followed by cooling periods, the copper expands and then contracts at a higher rate than the ceramic but is

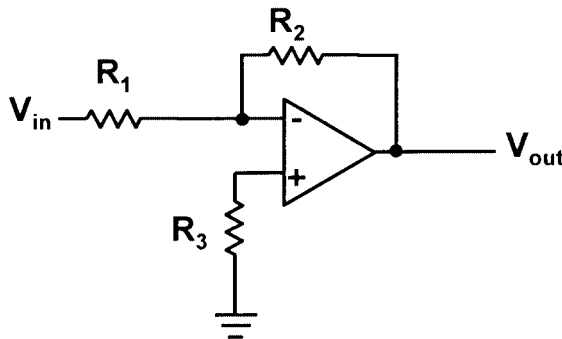


Figure 10.1 Gain tracking of resistors  $R_1$  and  $R_2$ .

## 10.4 Chapter 10

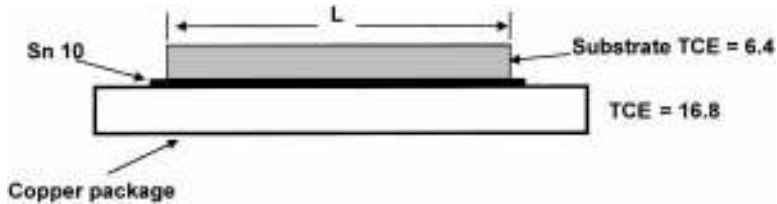


Figure 10.2 Stress example.

constrained. This constraining could result, after time and repeated temperature cycles, in the heat sink bending, the solder joint failing, the ceramic warping, or the ceramic completely failing and cracking.<sup>3</sup> To reduce or eliminate the thermal stresses requires both a selection of the correct materials and a minimization of the temperature changes caused by self-heating.

## 10.2 Understanding of Thermal Management

### 10.2.1 Second law of thermodynamics

The second law of thermodynamics states that heat always flows spontaneously from a hotter region to a cooler region as shown in Fig. 10.3. All active and passive devices are sources of heat. These devices are always hotter than the average temperature of their immediate surroundings.

### 10.2.2 Heat transfer mechanisms

There are three mechanisms for heat transfer: conduction, convection, and radiation, as depicted in Fig. 10.4. These mechanisms and the temperature distribution from the heat source to the surroundings will be discussed in the following sections.

**10.2.2.1 Conduction.** Thermal conduction is a process in which heat flows through a solid, liquid, or gas or between two media that are in intimate contact. Conduction, the dominant mechanism for heat transfer within solids, involves the transfer of kinetic thermal energy from one electron to another, causing no visible motion of the particles of the body. Conduction through dielectric solids is almost entirely a result of lattice vibrations, whereas conduction through metallic solids has the added energy transport by free electrons. This thermal energy transfer via electrons is similar to that of an electrical

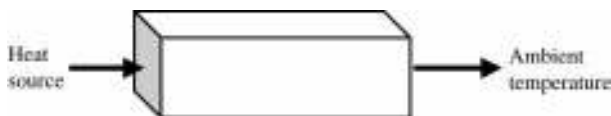


Figure 10.3 Second law of thermodynamics.

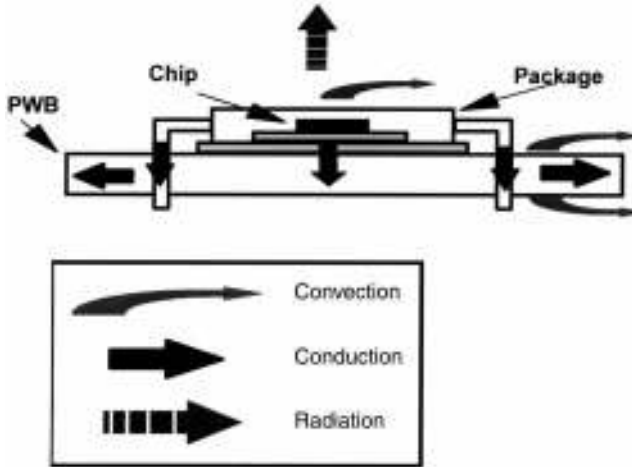


Figure 10.4 Mechanisms of heat transfer.

charge. It is not surprising to find that good electrical conductors such as copper and silver are good thermal conductors.

**Fourier's law .** Fourier's law of heat conduction, named after the French mathematician, Jean Fourier, states that the rate of heat flow equals the product of the area normal to the heat flow path, the temperature gradient along the path, and the thermal conductivity of the medium. Mathematically, Fourier's law can be expressed as

$$\frac{dq}{dt} = -KA \frac{dT}{dX} \quad (10.2)$$

where  $K$  = thermal conductivity of medium, W/m-K or W/in-°C

$A$  = cross-sectional area of medium normal to the heat flow path, in<sup>2</sup> or cm<sup>2</sup>

$T$  = temperature of medium, °C

$X$  = position along the medium, in or cm

$t$  = time, sec

$q$  = heat generated per unit volume, joules/cm<sup>3</sup>

$Q$  = heat flow in watts normal to the cross-sectional area of heat transfer

$$\frac{dQ}{dt} = \text{power in W or cal/sec} \quad (10.3)$$

$$\frac{dT}{dX} = \text{temperature gradient in } ^\circ\text{C/in or } ^\circ\text{C/cm} \quad (10.4)$$

The temperature gradient and the cross-sectional area are defined at the same point  $X$  as shown in Fig. 10.5. Heat flow is considered positive when the

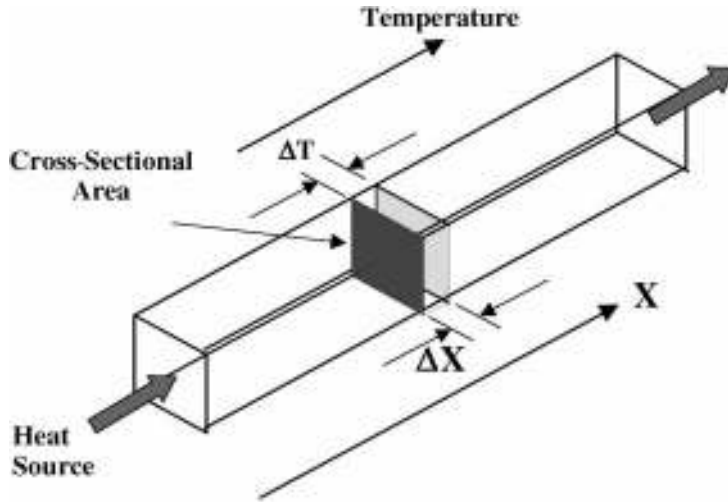


Figure 10.5 Fourier's law of heat conduction.

temperature is decreasing. The thermal conductivity of many materials varies with temperature and will be discussed in subsequent sections. In most cases, this variation with temperature can be considered a second-order effect and contributes only a minor source of error.

Substituting Eq. (10.3) into Eq. (10.2) and rearranging gives the expressions

$$P dX = KA dT \quad (10.5)$$

$$P \int_0^X dX = KA \int_{T_2}^{T_1} dT \quad (10.6)$$

Integrating the above over the length from 0 to  $X$ , and from the corresponding temperatures  $T_2$  to  $T_1$ , the equation reduces to

$$PX = KA \Delta T \quad (10.7)$$

Rewriting Eq. (10.7) produces an expression for temperature difference,

$$\Delta T = \frac{PX}{KA} \quad (10.8)$$

The Greek letter theta ( $\theta$ ) is usually used to symbolize thermal resistance and can be mathematically defined using Eq. (10.9).

$$\theta = \frac{X}{KA} \quad (10.9)$$

Combining Eqs. (10.8) and (10.9) gives a relationship between thermal resistance, power, and temperature rise.

$$P\theta = \Delta T \quad (10.10)$$

**10.2.2.2 Convection.** Convection is the transfer of thermal energy between two surfaces as a consequence of a relative velocity between them.<sup>4</sup> It occurs only in fluids wherein the transfer mechanism is the mixing of the fluids. Although each of the surfaces may be a fluid, the most practical application is where one is a solid surface and the other is a fluid.

The heat loss due to Newtonian cooling (named after Sir Isaac Newton) or convection cooling is proportional to the temperature difference between them. In mathematical terms, this can be written as

$$Q_c = h_c A_s (T_s - T_A) = h_c A_s \Delta T \quad (10.11)$$

where  $Q_c$  = heat transferred from a surface to ambient by convection in watts

$A_s$  = surface area in  $\text{cm}^2$  or  $\text{in}^2$

$T_s$  = surface temperature in  $^\circ\text{C}$

$T_A$  = ambient temperature in  $^\circ\text{C}$  (temperature to which the heat is being transferred)

$h_c$  = convection heat transfer coefficient in  $\text{W}/\text{cm}^2\text{-}^\circ\text{C}$  or  $\text{W}/\text{in}^2\text{-}^\circ\text{C}$

Because  $h_c$  is both position and temperature dependent, convection heat transfer solutions are more complex than conduction solutions. Many analysts use a simplifying approximation in which the average surface temperature is used in conjunction with an average heat transfer coefficient,  $h_c$ .

Equation (10.11) can be rewritten as:

$$\Delta T = \frac{1}{h_c A_s} Q_c \quad (10.12)$$

The term  $\theta_S$  can be defined as the convective surface thermal resistance.

$$\theta_S = \frac{1}{h_c A_s} \quad (10.13)$$

It should be noted that Eq. (10.13) is not a law of heat transfer as seen in Fourier's law but is a definition of the heat transfer coefficient. This definition simply states the quantity of heat transferred through a temperature difference. This temperature coefficient actually depends on the surface and surrounding temperatures, fluid velocity (for forced convection), fluid viscosity, fluid density, and surface geometry.

There are two types of convection cooling: natural (or free) and forced. In natural convection cooling, heat flows by conduction or contact from the surface to the fluid particles in intimate contact with the surface. The fluid parti-

cles increase in internal energy, causing the density of the nearby fluid to decrease. Buoyant forces then cause the particles to move to a region lower in temperature where further energy transfer takes place by conduction. There is a resulting boundary layer of hot air immediately adjacent to the surface. Natural convection is caused entirely by differences in density within the fluids resulting from different temperatures and does not use externally forced air movement.

In forced convection, the thermal energy is transferred from the solid to the adjacent fluid particles in the same manner as in natural convection. However, the subsequent fluid action occurs through artificially induced fluid motion generated by fans, pumps, or blowers. There are three types of air-moving devices: centrifugal, propeller, and axial flow. Centrifugal fans are designed to move small volumes of air at high velocities and are capable of working against a high resistance. Propeller types are designed to move large volumes of air at low velocities. Axial flow fans are an intermediate type of air mover between the centrifugal and propeller types.

Forced convection can be divided into laminar flow and turbulent flow. For air, the transition from laminar to turbulent flow usually occurs at a velocity of 180 linear feet per minute (LFM). The heat is transferred by molecular conduction in the fluid and by the solid–fluid interface. Turbulent flow, characterized by the irregular motion of fluid particles, has eddies in the fluid in which the particles are continuously mixed and rearranged. The heat is transferred from the eddies back and forth across the streamlines. The greater heat transfer occurs for turbulent flow.

For forced convection, the convection heat transfer coefficient is calculated from

$$h = B \frac{V^{0.75}}{L^{0.25}} \quad (10.14)$$

where  $B$  = constant of air properties and surface configuration

$V$  = linear velocity of air in cm/sec or in/sec

$L$  = characteristic length of surface in direction of flow in cm or inch

As can be seen in Eq. (10.14), the linear velocity of the air current as it passes the dissipating element is the key factor to the amount of heat that can be removed.

For natural or free convection, the convection heat transfer coefficient is calculated by

$$h = DE \frac{\Delta T^{0.25}}{L^{0.25}} \quad (10.15)$$

where  $D$  = constant for air properties (see Fig. 10.6)

$E$  = constant for surface configuration ( $E = 1.9 \times 10^{-4}$  for a flat plate)



$L$  = characteristic length in centimeters or inches of dissipator surface with area factor

$\Delta T$  = temperature difference in °C between dissipator and ambient air

**10.2.2.2.1 Natural convection cooling example.** A flat plate with a characteristic length of 2.0 in (assumed value for this example), shown in Fig. 10.6c, can be considered to be a model for a flat heat sink. The plate size is  $2.0 \times 2.0$  in. The plate bottom is at  $125^\circ\text{C}$ , and the ambient air is  $25^\circ\text{C}$ . The value of  $D$  for this configuration is 0.26 (from Fig. 10.6c). Calculating the value of the convective transfer heat coefficient  $h_c$ , from Eq. (10.15),

$$h_c = DE \frac{\Delta T^{0.25}}{L^{0.25}} = 0.26 \times 1.9 \times 10^{-4} \frac{(125 - 25)^{0.25}}{2.0^{0.25}} = 1.31 \times 10^{-2}$$

The convection surface thermal resistance is

$$\theta_s = \frac{1}{h_c A_s} = \frac{1}{1.31 \times 10^{-2} \times 4} = 1.9^\circ\text{C/W} \quad (10.16)$$

**10.2.2.2.2 Forced convection example.** Air with a velocity,  $V$ , of 500 ft/min is blown across a plate with a characteristic length  $L$  of 2.0 in. The surface area  $A$  is  $4.0 \text{ in}^2$ , and the air property/surface configuration constant  $B$  is  $1.0 \times 10^{-3}$ . From Eq. (10.14),

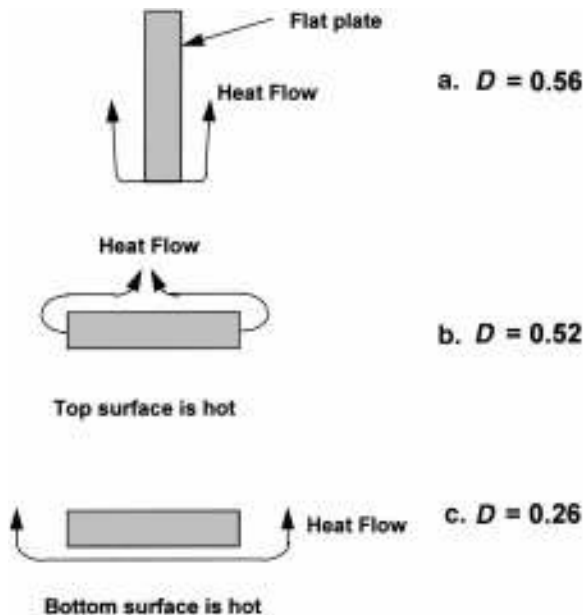


Figure 10.6 Value of  $D$  in Eq. (10.15).

$$h = B \frac{V^{0.75}}{L^{0.25}} = 1.0 \times 10^{-3} \frac{(500 \times 12)^{0.75}}{2^{0.25}} = 0.482 \text{ W/in}^2\text{-}^\circ\text{C} \quad (10.17)$$

The thermal resistance is

$$\theta_s = \frac{1}{hA_S} = \frac{1}{0.482 \times 4} = 0.518^\circ\text{C/W} \quad (10.18)$$

The above discussion of convection cooling points out that this heat removal method is wholly dependent on the movement of the fluid surrounding the heat-dissipating element. A brief review of the thermal conductivities of the various gases present in packaging will be presented. Because this chapter delves only into thermal management materials, there will be no further discussion of convection cooling.

**10.2.2.3 Radiation cooling.** All objects with a temperature above 0 kelvins emit thermal radiation. Radiation cooling is the transfer of heat by electromagnetic emission, primarily in the infrared wavelengths (0.1 to 100  $\mu\text{m}$ ). Because radiation cooling does not require a transport medium, it is the only means of cooling in a complete vacuum. Specifically, radiation cooling is maximized when there is no intervening material.

Radiation from solid objects may be considered to be a totally surface-related phenomenon that is electromagnetic in character.

Temperature radiators can be broken into two classes: *black bodies* and *non-black bodies*. Non-black bodies can be further broken down into gray bodies and selective radiators. A visibly black surface absorbs all visible light that falls upon it. Its thermal analogy is called a black body and is defined as a surface that absorbs the entire thermal radiation incident upon it, neither reflecting nor transmitting any of the incident radiation. The emissive power of a black body or surface is defined as  $E_b$ . Good absorbing materials are also good emitting materials. The black body, at any given temperature, radiates more energy, both in the total spectrum and for each wavelength interval, than any other temperature radiator and more than any non-black body at the same temperature.<sup>6</sup>

Real surfaces do not radiate precisely as described by black-body equations, because no surface is ideally black. Lampblack and some finely divided metals approach a black body in certain parts of the spectrum. The actual monochromatic emissive power of a real surface is always less than  $E_b$ . The emissivity of a body or surface ( $\epsilon$ ) is defined as the ratio of the radiated flux ( $E$ ) emitted by a body to that ( $E_b$ ) emitted by a black body at the same temperature.

$$\epsilon = \frac{E}{E_b} \quad (10.19)$$

A black body or perfect emitter would have an  $\epsilon$  of 1.0. A perfect reflector would have an  $\epsilon$  of 0. Listed in Table 10.1<sup>5</sup> are the emissivities for various ma-

TABLE 10.1 Emissivities of Surfaces at 80°F

Surface type	Finish	Emissivity, $\epsilon$
Paint	Black (flat lacquer)	0.96–0.90
Paint	Gray	0.84–0.91
Paint	White	0.80–0.91
Paint	White epoxy	0.91–0.95
Paint	Aluminum silicone	0.020
Metal	Nickel	0.21
Metal	Aluminum	0.14
Metal	Silver	0.10
Metal	Gold	0.04–0.23
Specialty surfaces		
Metal	Aluminum (sandblasted)	0.41
Metal	Aluminum (black anodized)	0.86
Metal	Nickel (electrolysis)	0.06–0.17
Metal	Aluminum (machine polished)	0.03–0.06
Metal	Gold (electrodeposited or polished)	0.02
Ceramic	Cermet (ceramic containing sintered metal)	0.58
Metal	Brass (highly polished)	0.58
Metal	Copper (polished)	0.018
Metal	Nickel (polished)	0.070
Metal	Silver (polished)	0.02–0.03
Glass	Smooth	0.9–0.95
Metal	Alodine* on aluminum	0.15

\*Registered trademark of Achem Products, Inc.

terials used in microelectronic applications. Aluminum, a low-cost material with a high thermal conductivity, has a low emissivity of 0.04 in a polished state. After black anodization, aluminum's emissivity is significantly increased to 0.80.

A *gray body* is defined as a radiator that has the same spectral emissivity for all wavelengths. A *selective radiator* is one in which the emissivity varies with wavelength.

The rate of emission of radiant energy from the surface of a body,  $R$ , can be expressed by the Stefan-Boltzmann law shown in Eq. (10.20).

$$R = \epsilon \sigma T^4 \quad (10.20)$$

with  $R$  defined as

$$R = \frac{Q}{A} \text{ W/m}^2 \quad (10.21)$$

where  $\epsilon$  = surface emissivity in joules/sec-cm<sup>2</sup>  
 $\sigma$  = Stefan-Boltzmann constant ( $3.65 \times 10^{-11}$  watts/in<sup>2</sup>-K<sup>4</sup>)

$Q$  = heat transferred in watts  
 $A$  = radiating surface area in meter<sup>2</sup>  
 $T$  = temperature of surface in kelvins

Combining Eqs. (10.20) and (10.21),

$$Q = \varepsilon\sigma AT^4 \quad (10.22)$$

The heat transferred via radiation between two black body surfaces ( $\varepsilon = 1$ ) in which one body is completely enclosed by the other (and the internal body cannot see any part of itself) may be calculated by

$$Q = A\sigma(T_1^4 - T_2^4) \quad (10.23)$$

where  $T_1$  = temperature of "hot" body in K  
 $T_2$  = temperature of "cold" body in K (air molecules or other absorbing body)

For non-black body surfaces, the heat transferred via radiation is

$$Q = SA\varepsilon\sigma(T_1^4 - T_2^4) \quad (10.24)$$

where  $S$  = shielding factor or view factor

The shielding factor (or view factor),  $S$ , whose value ranges from 0 to 1, is a measure of how well the emitter sees the absorber. Typical values of shielding factors are shown in Table 10.2.

**TABLE 10.2 Shielding Factors for Various Configurations<sup>3</sup>**

Configuration	Shielding factor
Infinite parallel plates or planes	1.0
Body completely enclosed by another body, internal body cannot see any part of itself	1.0
Two squares in perpendicular planes with a common side	0.20
Two equal, parallel squares separated by a distance equal to the side	0.19
Two equal, parallel circular disks separated by a distance equal to the diameter	0.18

The above discussion on radiation cooling points out that this heat removal method is dependent on the temperature difference between objects, their emissivity, and the shielding factor. From a materials standpoint, the physical designer can optimize the thermal design with the emissivity parameter.

**10.2.2.3.1 Radiation example (non-black body).** The bottom of a heat sink is at 150°C while the ambient air is at 25°C. The heat sink is nickel plated with a surface area of 4.0 in<sup>2</sup>. The shielding factor is 1.0. The amount of heat transferred by radiation is calculated from Eq. (10.24).

$$\begin{aligned}
 Q = P &= SA\varepsilon\sigma(T_1^A - T_2^A) \\
 &= (1)(4)(0.11)(3.65 \times 10^{-11})[(150 + 273)^4 - (25 + 273)^4] = 0.388 \text{ W} \quad (10.25)
 \end{aligned}$$

If the heat sink bottom temperature is changed to 125°C, then

$$T_2 = 125^\circ\text{C}, \quad Q = 0.111 \text{ W}$$

### 10.3 Unit Conversions

Comparisons of the thermal properties of materials is often made difficult by the fact the values use different units. To aid the reader, conversion factors between metric and English units for various physical parameters are listed in Table 10.3.

### 10.4 Packaging Overview

Before looking at the various materials used in electronic packaging from a thermal management standpoint, it is necessary to take a global look at the various packaging technologies and how they fit together. This chapter will look at first-level of packaging—the chip(s) in a package—and the second level of packaging—the circuit card.

Semiconductors are packaged for four basic reasons.

1. The package provides mechanical support to the semiconductor.
2. The package provides interconnections of the semiconductor(s) to the next level of packaging.
3. The package provides environmental protection of the semiconductor(s).
4. The package provides a method of removing the heat dissipated by the semiconductor(s).

#### 10.4.1 Single-chip package

The lowest level of packaging is the single-chip package (SCP). In this package, the chip is mounted to the package base with a die attach material, interconnected, and sealed either hermetically or via encapsulation. An example of the SCP is shown in Fig. 10.7, which depicts a custom ASIC in a ball grid array package. This process is varied for flip-chips wherein the balls on the die are mass reflowed to the package and then sealed.

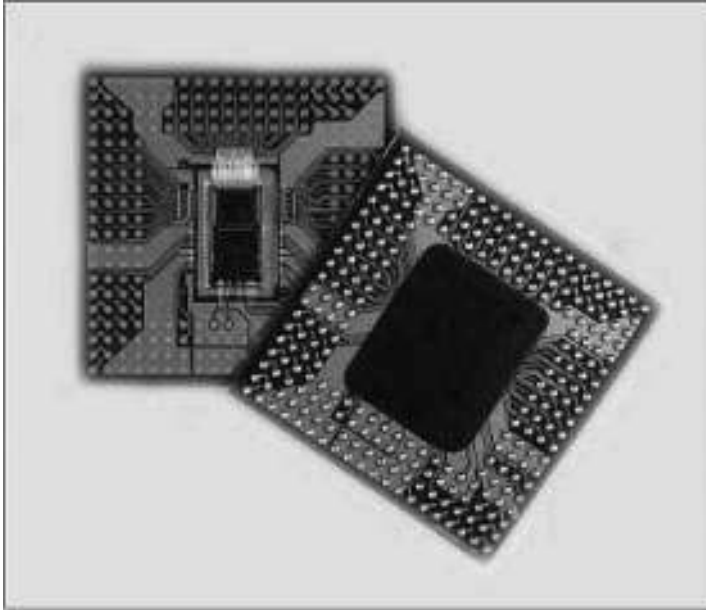


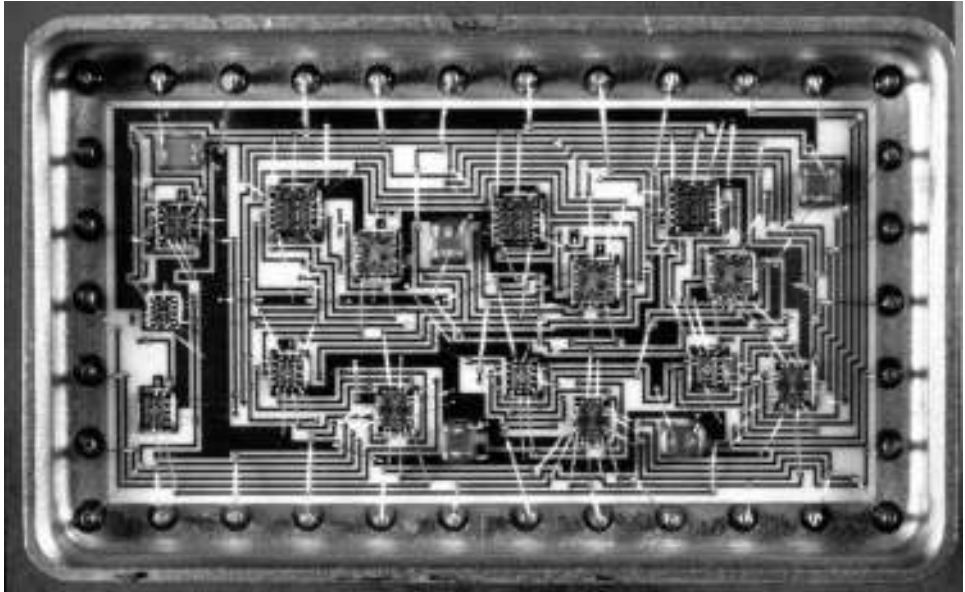
Figure 10.7 Single-chip package.

#### 10.4.2 Multichip package

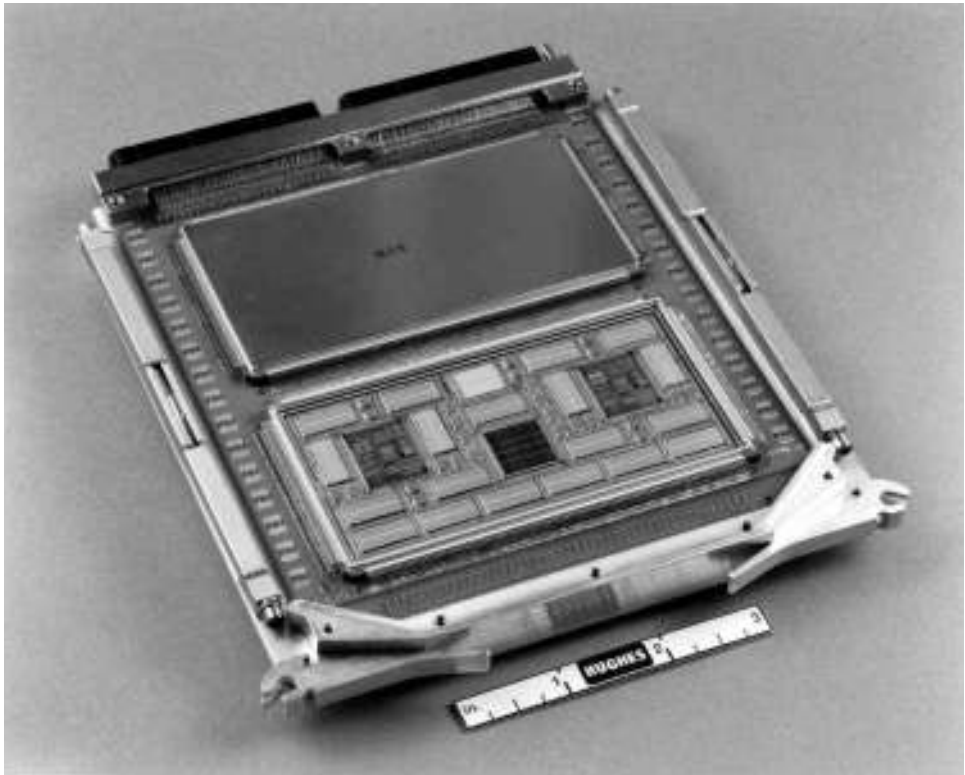
Multichip packaging has been used by the electronics industry since the mid 1960s. First known as hybrids, they placed several semiconductors and passive devices on a substrate housed in one package. The typical package used for the first hybrids was the TO-5. A more recent hybrid is shown in Fig. 10.8a. Over the years, multichip packaging technology has evolved in size, number of I/Os, and complexity to a point at which complete subsystems have been placed in a single package. The highest density of multichip packaging has been named the multichip module (MCM). An example of an MCM with 442 I/Os is shown in Fig. 10.8b. Another name for high-density multichip packaging is *system-in-package* (SiP). A variant of multichip packaging is the *few chip package* (FCP).

#### 10.4.3 Board level

Once the semiconductors are packaged, they need to be attached to the next level of assembly—the circuit card. The electrical interconnections are typically made with a low-temperature solder. For many package types, this electrical connection also acts as the mechanical connection. However, for large devices, additional mechanical attachment is necessary. This may be in the form of adhesives or actual clamping to the circuit card. The additional attachment materials may also aid in removing the heat from the device. Even if the lead attachment is sufficient for holding the package on the circuit card, ther-



(a)



(b)

**Figure 10.8** (a) Hybrid microcircuit and (b) multichip modules assembled on SEM-E frame.

TABLE 10.3 Units and Conversion Factors

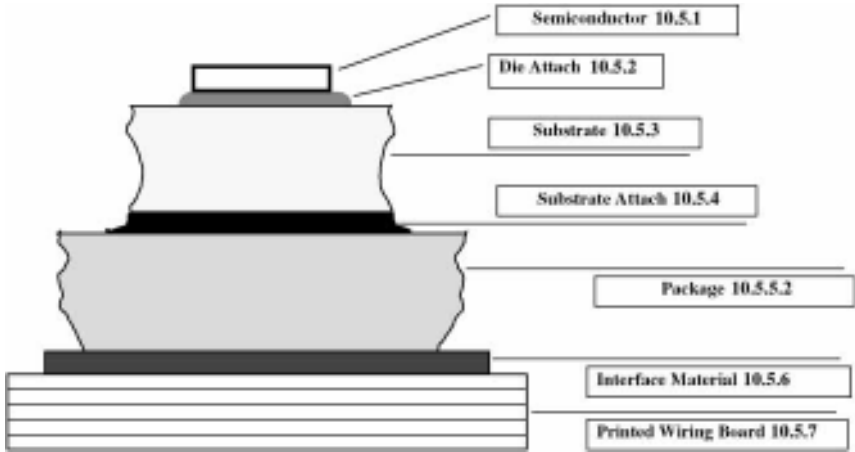
Length, area, and volume	Work
1 in = 25.4 mm = 0.0254 m	1 in-lb (force) = 0.113 J = 0.113 Nm
1 in = 2.54 cm	1 ft-lb = 1.365 J
1 in = 25400 $\mu\text{m}$ (microns)	1 BTU = 778 ft-lb = 252 calories = 1,055 J
12 in = 1 ft	
	Energy
1 ft = 305 mm = 0.305 m	1 calorie (cal) = 4.186 J
1 in <sup>2</sup> = 645 mm <sup>2</sup> = 0.6452 $\times 10^{-3}$ m <sup>2</sup>	1 erg = 10 <sup>7</sup> J
1 ft <sup>2</sup> = 92,880 mm <sup>2</sup> = 0.0929 m <sup>2</sup>	1 electron volt (eV) = 1.60 $\times 10^{19}$ joule
1 in <sup>3</sup> = 16,380 mm <sup>3</sup> = 16.38 $\times 10^{-6}$ m <sup>3</sup>	1 W-sec = 1J
1 ft <sup>3</sup> = 0.0283 m <sup>3</sup>	
	Power
Mass	1 BTU/hr = 0.293 W
1 lb (mass) = 0.45359 kg = 453.59 g	1 cal/sec = 4.18 W
1 oz = 28.35 g	1 ft-lb/sec = 1.356 W
	1 ft-lb/mm = 0.0226 W
Density	
1 lb/in <sup>3</sup> = 27680 kg/m <sup>3</sup>	Thermal conductivity
1 lb/in <sup>3</sup> = 27.68 g/m <sup>3</sup>	1 BTU/hr-ft-°F = 1.7303 W/m-K
1 lb/ft <sup>3</sup> = 16.0185 kg/m <sup>3</sup>	1 BTU/hr-in-°F = 0.1442 W/m-K
	1 W/in-K = 39.3 W/m-K
Pressure	1 cal/sec-cm-K = 418.4 W/m-K
1 lb/in <sup>2</sup> (psi) = 6,894.76 N/in <sup>2</sup>	Specific heat
1 lb/ft <sup>2</sup> (psf) = 47.9 N/in <sup>2</sup> = 0.0069 psi	1 cal/g-°C = 4.17 W-sec/g-°C
1 MPa = 10 <sup>6</sup> N/m <sup>2</sup> = 1 N/mm <sup>2</sup>	1 BTU/lb-°F = 4.1867 W-sec/g-°C
1 atm = 101325 Pa	
1 dyne/cm <sup>2</sup> = 0.1 Pa	Temperature
1 kg/cm <sup>2</sup> = 14.22 psi	1°C = 33.8°F
	0°C = 273.15 K
Force	
1 lb (force) = 4.448 N	
1 gm (force) = 980.665 dyne	
1 dyne = 10 <sup>-5</sup> N	
1 dyne = 2.248 $\times 10^{-6}$ lb	

mal interface material may be required between the package and the board. A discussion of these materials can be found in Sec. 10.5.6.

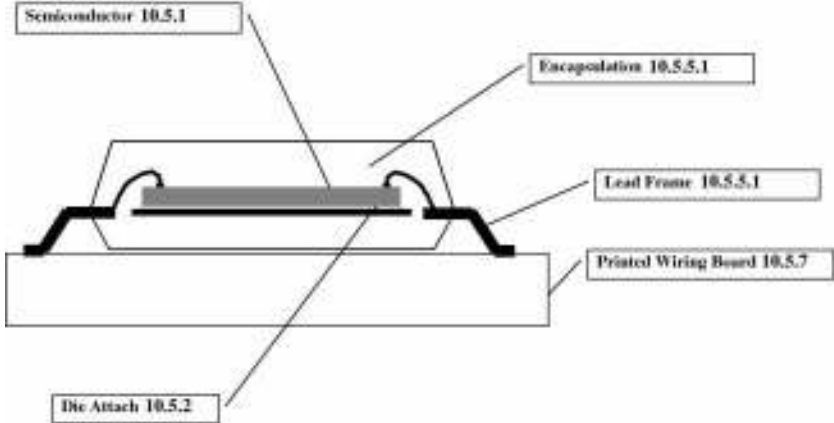
## 10.5 Packaging Materials

Figure 10.9 shows cross-sectional views of the various types of electronic packaging. The constituent materials used in each type of packaging are referenced to the applicable section of this chapter.

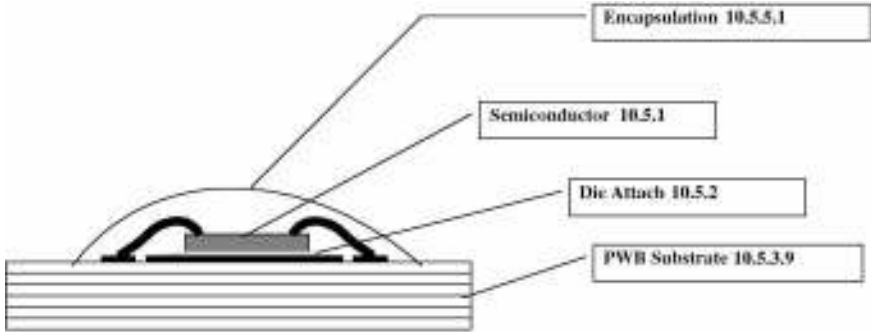




(a)



(b)



(c)

**Figure 10.9** Cross-sectional views of various package types: (a) hybrid microcircuit, (b) PEM, and (c) COB.

## 10.18 Chapter 10

## 10.5.1 Semiconductors

**10.5.1.1 Silicon and germanium.** The first transistors were fabricated with germanium (Ge) semiconductor material, which has a reasonably good thermal conductivity of 77 W/m-K. However, germanium suffers from an inherent leakage problem that limits the maximum operating temperature to the range of 90 to 120°C. Silicon transistors, invented at Texas Instruments in 1954, have maximum operating junction temperatures in the range of 150 to 200°C.<sup>9,10</sup> Forty years later, over 90 percent of all semiconductors are fabricated from silicon, which has a thermal conductivity of 150 W/m-K at 25°C.<sup>11</sup>

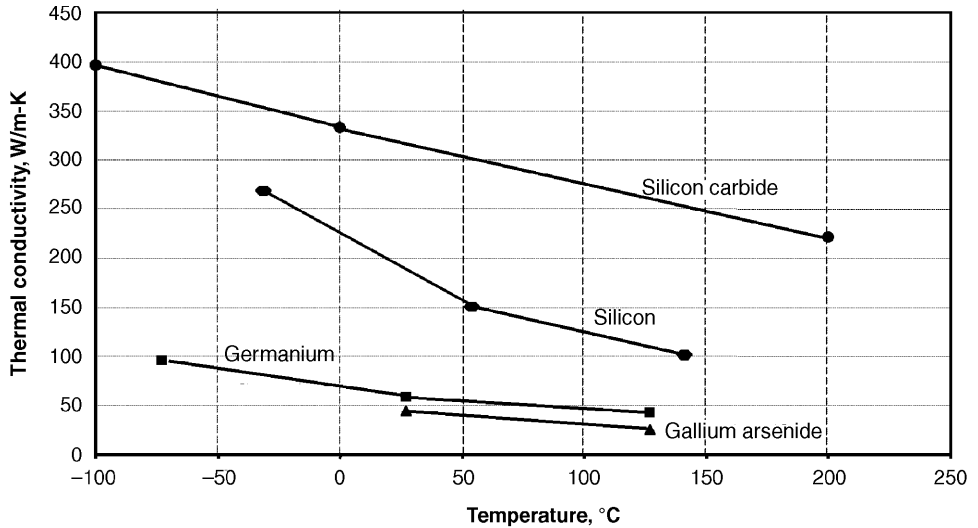
Table 10.4 lists the thermal conductivities of various semiconductor materials at 25°C. The variation of the thermal conductivity at temperature for several of these materials is shown in Fig. 10.10.

**TABLE 10.4 Thermal Conductivities of Semiconductor Materials<sup>3,13,23</sup>**

Material	Thermal conductivity @ 25°C (W/m-K)
Silicon	150
Silicon germanium	150
Silicon carbide	155
Gallium arsenide	45
Indium phosphide	97
Germanium	77
Gallium phosphide	133
Gallium antimony	33
Gallium nitride	16–33
Indium arsenide	35
Indium antimony	19

**10.5.1.2 Compound semiconductors.** To obtain higher performance than silicon in either frequency or temperature range, compound semiconductors were developed using materials such as gallium arsenide, indium phosphide, indium arsenide, indium antimony, gallium phosphide, gallium antimony, and silicon carbide.

For high-frequency applications, typically starting at 1 GHz, gallium arsenide (GaAs) is used as the semiconductor material because of its higher mobility. Because of its high-frequency performance, gallium arsenide has found its way into a variety of applications ranging from cellular telephones to military radars. Other materials used for high-frequency operation include indium phosphide, indium arsenide, indium antimony, gallium phosphide, and gallium antimony.



**Figure 10.10** Variation of the thermal conductivity of various semiconductor materials at temperature.

To achieve maximum high-frequency performance from gallium arsenide, circuit geometries are made extremely small. This increased power density, coupled with the lower thermal conductivity (35 W/m-K), makes the packaging of gallium arsenide a significant challenge to the physical designer. One technique commonly used with gallium arsenide to lower the thermal resistance is to thin down the wafers. Gallium arsenide chips are also thinned so as to reduce the impedance of through-hole vias from the top to the bottom of the chip. Typical thicknesses of gallium arsenide used in the microelectronic assemblies are 0.006 and 0.002 in.

A new compound semiconductor material, silicon-germanium (SiGe), is fabricated by selectively introducing germanium as a dopant into the base region of the transistor. The processing of silicon-germanium wafers is done using the same equipment as standard silicon. The resulting silicon-germanium material produces a semiconductor that offers comparable high-frequency performance to gallium arsenide at a significantly lower cost. An example of the high-frequency capability of the silicon-germanium process is IBM's recently demonstrated 210-GHz silicon-germanium transistor. The amount of germanium in silicon-germanium is small. Therefore, the thermal conductivity can be considered to equal that of silicon.<sup>15-17</sup>

Silicon carbide (SiC) is a compound semiconductor material that is finding its way into a variety of applications. With a wide band gap of 3.1 eV (versus 1.1 eV for silicon), heat does not readily disrupt the performance of silicon carbide semiconductors. In addition to the wide band gap, silicon carbide has a high thermal conductivity: 333 W/m-K at 25°C and 221 W/m-K at 200°C. As a result, silicon carbide semiconductors are being used in a variety of high-temperature applications. Silicon carbide has a high maximum electron velocity, which allows devices to operate at high frequencies.<sup>14,18,19</sup>

Indium phosphide is a new compound semiconductor material being used for high-frequency electronic and optoelectronic devices with the potential of integrating both on a single chip. Indium phosphide's relatively high thermal conductivity of 97 W/m-K allows it to be used in high-power-density applications.<sup>20,21</sup>

Gallium nitride (GaN) is a developing semiconductor material with a wide bandgap that can effectively handle large amounts of power and operate at frequencies up to 40 GHz. While the thermal conductivity of gallium nitride is a low 16 to 32 W/m-K, it has a power density that is many times that of gallium arsenide and indium phosphide. Gallium nitride is finding applications such as power amplifiers in base stations.<sup>22,23</sup>

### 10.5.2 Die attach materials

Except for flip-chip-attached devices, all die are bonded to the next assembly (the substrate or package) active area facing up with a die-bond adhesive. It is the die bond that absorbs the thermal mismatch between the die and the package or substrate. Thus, the die bond is susceptible to fatigue fracture. The adhesives fall into two categories, soft and hard. Soft adhesives include organics, polymers, and lead-based solders. Hard adhesives include gold-based eutectics (gold-silicon, gold-germanium, and gold-tin), silver-based solder (Sn 96), and silver-glass.

**10.5.2.1 Gold-silicon eutectic.** Eutectic die attachment is based on the gold-silicon eutectic point at 370°C. In this process, the die is mechanically scrubbed with a gold-silicon perform on a substrate or a ceramic package at temperatures between 390 and 450°C under a nitrogen shroud. On semiconductors with no backside metallization, the scrubbing breaks down the thin layer of silicon on the back of the chip and combines it with another metal, usually gold. For gold-backed semiconductors, the gold-silicon perform is reflowed and attaches the die to the underlying metallization. The resulting gold-silicon eutectic structure is approximately 0.001-in thick and has a thermal conductivity of 27 W/m-K.<sup>13</sup>

**10.5.2.2 Solders.** For semiconductors metallized with non-gold metals such as titanium-nickel-silver, other eutectic solders are used. These include gold-tin, with a eutectic temperature of 280°C; gold-germanium, with a eutectic temperature of 361°C; and Sn 96, with a eutectic temperature of 221°C. (Note that gold-tin, gold-germanium, and Sn 96 can be used with both gold-backed and non-gold-backed die.) Other solders used for die attach include a variety of lead-tin and indium-lead solders. The thermal conductivities of the various solders used as die attach adhesives are listed in Table 10.5.<sup>38</sup> Preforms of gold-tin, gold-germanium, and Sn 96 come in various thicknesses, starting at 0.001 in. Solder pastes, a mixture of solder particles and flux, are available for a number of solder alloys for use in dispensing, screen printing, and stencil-

TABLE 10.5 Thermal Properties of Solders<sup>38</sup>

Solder	Composition	Thermal conductivity @25°C (W/m-K)	CTE, (ppm/°C)
Gold-silicon	96.85 Au, 3.15 Si	27	12.3
Gold-tin	80 Au, 20 Sn	57	15.9
Gold-germanium	88 Au, 12 Ge	44	13.4
Sn 10	90 Pb, 10 Sn	36	27.9
Sn 96	3.5 Ag, 96.5 Sn	33	30.2
Sn 62	2 Ag, 36 Pb, 62 Sn	42	27
Sn 63	37 Pb, 63 Sn	51	25
Sn 60	40 Pb, 60 Sn	29	27
Indium-lead	30 Pb, 70 In	38	28
Indium-silver	3 Ag, 97 In	73	22

ing. When solder pastes are used, there is a possibility of creating voids in the die attach as a result of flux entrapment. This is discussed in Sec. 10.6.2.

The lack of plastic flow in hard adhesives leads to high stresses in the silicon chip as a result of the CTE mismatch between the substrate/package and the die.<sup>24</sup>

**10.5.2.3 Silver-glass.** As semiconductors grew in complexity from medium scale integration (MSI) to large scale integration (LSI), and in size past 0.2 inches square with power densities exceeding 32 W/in<sup>2</sup> (5 W/cm<sup>2</sup>), the eutectic die attach process became inadequate. Assembly houses could not provide high enough void-free attachment in volume to meet the thermal resistance requirements. In addition, the CTE mismatch between silicon at 3.6 ppm/°C and 92 percent alumina packages at 7.2 ppm/°C was introducing significant reliability-decreasing stresses.<sup>13</sup>

Silver-glass die attach materials were developed to provide void-free die attach with low thermal resistance. Composed of approximately 60 percent silver flake, 20 percent glass, and 20 percent organic binders that are burned off completely during the processing, silver-glass has a thermal conductivity ranging from 60 to 80 W/m-K, depending on the manufacturing formulation. This is an order of magnitude higher than epoxies. See Table 10.6 for details. Silver-glass is applied to the semiconductor package or to the substrate with dispensing equipment to provide an after-firing bond line of 0.002 in minimum.<sup>28</sup> Typical processing temperatures for silver-glass die attach are 400 to 420°C.<sup>26</sup> Owens has reported that there was no cracking of die when attached with silver-glass.<sup>28</sup> The same die, when attached eutectically, was exhibiting cracking. The thermal properties of several silver-glass compositions are listed in Table 10.6.

TABLE 10.6 Thermal Properties of Silver-Glass<sup>25–27</sup>

Material	Thermal conductivity @25°C (W/m-K)	CTE (ppm/°C)
QMI3555R	>80	16
QMI2419MA	>60	21
DM-3030	70	19.7
JM4720	78.3	17

**10.5.2.4 Organic adhesives.** Polyimides, cyanate esters, and epoxies filled with precious metals are widely used for die attach in all types of packaging. Their ease of application and low processing temperatures have made them the die attach material of choice in many applications. These organic adhesives are typically filled with a metal to provide the required electrical and thermal conductivity. Silver is the most common fill material. In selected applications, gold and copper are used as the fill material. To improve the thermal conductivity of organic adhesives, some manufacturers add electrically insulating materials such as boron nitride, aluminum nitride, alumina, and CVD diamond as fillers.

For single-chip packaging, dispensing and stamping are the preferred methods of application of organic adhesives. In multichip applications, the adhesives are typically screen printed or dispensed. With the proper dispensing pattern, void-free die attach can easily be achieved.

Many polymers come as a preform in which a carrier is impregnated with epoxy. Typical carrier materials are fiberglass and Kapton.\* These preforms provide an extremely uniform material thickness. Preforms with thicknesses as thin as 0.0015 in are available for use in die attach. Thicker preforms, up to 0.006 in thick and unfilled, are typically used for substrate attachment in multichip applications. These are discussed in Sec. 10.5.4.

Polymers are grouped into two categories—thermoplastics and thermosets. Thermoplastics, made from ground cured resins and mixed with fillers and a solvent, are capable of softening or melting when heated and return to a solid when cooled. Because of the presence of the cured resins, thermoplastics do not require any subsequent curing. Thermosets, typically referred to as *epoxies*, are uncured or partially cured. They do not have the reversible phase-change behavior of thermoplastics. The thermal conductivity of both thermoplastics and thermosets is a first-order function of the type and amount of filler material. When used for die attach, the typical filler material is silver. Because thermoplastics do not require a cure, the bond line they form is dense and void-free, with a resulting higher thermal conductivity. Thermosets, which require a cure, have small voids caused by shrinkage during curing that result in a lower-density bond line and thus a lower thermal conductivity.<sup>31,32</sup>

\* Kapton is a registered trademark of DuPont.

Polyimide and cyanate ester adhesives, both metal-filled and unfilled, are more thermally stable than epoxy adhesives and are used for higher-temperature applications such as furnace sealing. Epoxies have a maximum temperature range of 175°C to 250°C, depending on their composition. Polyimides, stable to 400°C to 500°C, have thermal conductivities close to 0.16 W/m-K.<sup>19</sup> Silver-filled cyanate esters, stable to over 400°C have thermal conductivities of approximately 1 W/m-K.<sup>33</sup> The thermal conductivities of polyimide and cyanate ester die attach adhesives are extremely low. However, because their thickness is on the order of 0.001 inch or less, the resultant thermal resistance of the die attach, while not low, is acceptable for low to medium power densities.

Thermoplastic and thermoset adhesives come in both a paste and a preform. The critical thermal parameters for both materials are the thickness of the die attach and its uniformity. The screen printing and dispensing processes can provide uniform bond lines. By definition, the preform provides a uniform thickness. Table 10.7 lists the thermal conductivities of various organic adhesives used for die attach.

### 10.5.3 Substrates and metallizations

In all multichip applications and selected single-chip applications, the dice are attached to a substrate that provides interconnection as well as electrical isolation from the package. This substrate material can be a ceramic, a metal with insulating dielectric, or an organic. Ceramic substrate materials include alumina, beryllium oxide, low-temperature cofired ceramic (LTCC), and aluminum nitride. Table 10.8 lists the thermal properties of inorganic substrates. In multilayer substrates, the dielectric material has a very large effect on the overall thermal resistance and is discussed below in detail.

Table 10.9 lists the thermal conductivities of various thick film substrate dielectric materials. Metal substrates include steel, copper, and aluminum with subsequent dielectric layers. Whereas the physical parameters that set the thermal resistance for a substrate are primarily the thermal conductivity of the base material and the dielectric material, the conductor material has a very important effect on the thermal resistance. The conductors, composed of various metals, when used as a plane or planes, serve to spread the heat and thus lower the thermal resistance. Therefore, in the subsequent discussion on substrate materials, the methods of metallizing will be presented with a focus on thermal conductivity.

Inorganic substrates, used for low-cost applications, are discussed in Sec. 10.5.7, Printed Wiring Boards.

**10.5.3.1 Alumina.** The most commonly used ceramic material in electronic packaging is alumina,  $\text{Al}_2\text{O}_3$ , or aluminum oxide. It is used both as a body of a hermetic package and as a substrate. The CTE of the 96 percent alumina, 6.3 ppm/°C (25 to 400°C),<sup>13</sup> closely matches that of silicon and several metal packaging alloys (Kovar and Alloy 42). This close match prevents differential stresses that can lead to mechanical failure.

TABLE 10.7 Thermal Properties of Organic Adhesives<sup>27,29,30,45,86</sup>

Manufacturer	Material	Material type	Thermal conductivity @25°C (W/m-K)	Comments
Ablestik	84-1LMISR4	Thermoset-conductive	2.5	
Ablestik	84-1LMIT	Thermoset-conductive	5.9	
Ablestik	ECF561	Thermoset-conductive	1.6	
Emerson & Cuming	5025E	Thermoset-conductive	3.5	
Emerson & Cuming	ECF561	Thermoset-conductive	1.6	
AI Technology	TC8750	Thermoset-conductive	6.5	
Epoxy Technology	T6116	Thermoset-conductive	1.5	
Epoxy Technology	H20E	Thermoset-conductive	2.0	
DIEMAT	6030HK	Thermoset-conductive	60	
Hysol	KO120	Thermoset-conductive	2.8	
Ablestik	84-3J	Thermoset-nonconductive	0.8	
Emerson & Cuming	561K	Thermoset-nonconductive	0.9	
Emerson & Cuming	506	Thermoset-nonconductive	0.9	
Emerson & Cuming	5020K	Thermoset-nonconductive	0.7	
AI Technology	TK78759	Thermoset-nonconductive	11.6	Diamond filled
AI Technology	TP8260	Thermoplastic-conductive	6.5	
AI Technology	TP7155	Thermoplastic-conductive	1.6	
DIEMAT	4030LD	Thermoplastic-conductive	15	
Ablestik	2600K	Thermoplastic/thermoset blend	20.0	
AI Technology	TP7095	Thermoplastic-nonconducting	1.6	
AI Technology	TP7755	Thermoplastic-nonconducting	1.8	
AI Technology	TP7459	Thermoplastic-nonconducting	11.5	Diamond filled
Ablestik	71-1	Polyimide	2.1	
Ablestik	JM2000LB	Cyanate Ester	1.8	@ 121°C
Ablestik	JM2500	Cyanate Ester	1.1	@ 121°C

The thermal conductivity of alumina ranges from 12 to 35 W/m-K, depending on the purity. The highest purity available, 99.6 percent alumina, is typically used for thin film applications and has a thermal conductivity of 34.7 W/m-K at 25°C. Ninety-six percent alumina, typically used with thick-film metallization, has a thermal conductivity of 21 W/m-K at 25°C. Figure 10.11 shows the measured thermal conductivity for various percentages of alumina. In addition to thermal conductivity varying with the percentage of alumina, it also varies with temperature variation as shown in Fig. 10.12.<sup>13,39</sup>



**TABLE 10.8 Thermal Properties of Inorganic Substrates<sup>13,34</sup>**

Material name	Thermal conductivity @25°C (W/m-K)	CTE (ppm/°C)
Alumina 92%	17	7.2
Alumina 96%	21	6.3
Alumina 99.9%	30	7.4 (25–400°C)
Beryllium oxide 99.5%	248	6.4
Aluminum nitride	170	4.2
LTCC	2.0–4.4	4.5–8.0
CVD diamond	1300–2000	2.0

**TABLE 10.9 Thermal Properties of Thick Film Dielectrics<sup>35–37</sup>**

Material name	Application	Thermal conductivity @25°C (W/m-K)
DuPont dielectrics	Thick film glass	3.0
41010-25C	Tape on substrate	2.5–3.0
GPA98-047	Steel substrates	4.3

Alumina can be metallized with refractory metallizations (e.g., tungsten or moly-manganese), thin films, thick films, direct copper plating, and direct bond copper. The use of ground or power planes in either substrate or package metallization can aid in spreading the heat.

Multilayer thick films usually use screen-printed glass as the dielectric layers as depicted in the cross section shown in Fig. 10.13. This glass is both an electrical and a thermal insulator. The typical thermal conductivity of thick-film glass is identical to that of LTCC, which is 3.0 W/m-K.<sup>40</sup> To improve the effective thermal conductivity of multilayer thick-films, the physical designer makes use of thermal vias. As shown in Fig. 10.14, thermal vias are a series of filled vias stacked upon each other in an array. The bottom of the stack is attached either to the ceramic substrate or to a plane. Thick-film conductor inks, whether they are gold, silver, or an alloy, are not pure metals. The inks consist of a functional material of metal, a solvent, a temporary binder, and a permanent binder. This permanent binder is used to tailor the CTE to that of the substrate and to aid in the adhesion to either the dielectric or the ceramic substrate. During firing, the solvent and temporary binders are burned out, leaving a conductor whose properties are no longer that of the pure metal functional material. In addition to altering the CTE, the permanent binder reduces both the electrical and thermal conductivity of the conductor. Typical fired thick-film conductors are 8  $\mu\text{m}$  thick. If this conductor were pure gold, it

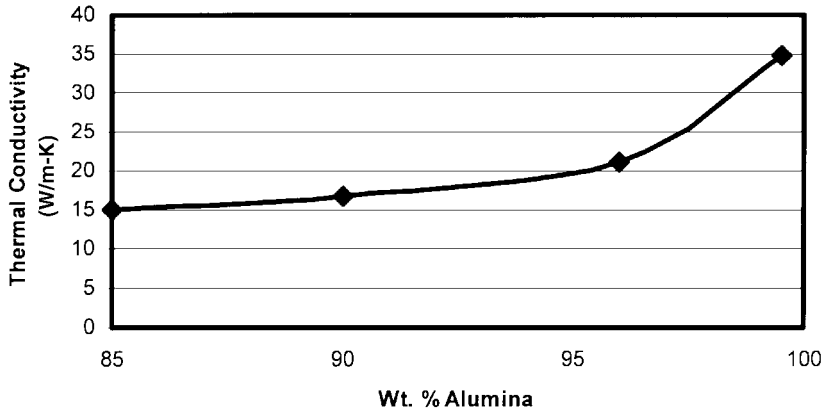


Figure 10.11 Effect of weight percent of  $\text{Al}_2\text{O}_3$  on thermal conductivity.

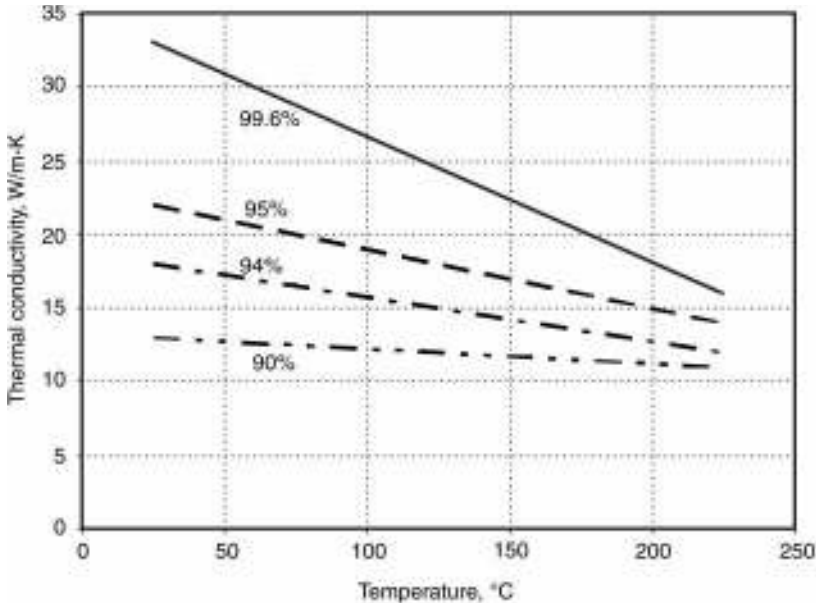


Figure 10.12 Variation of thermal conductivity of alumina at temperature.

would have a sheet resistivity of  $3 \text{ m}\Omega/\square$ . The 5715 thick-film gold conductor material from DuPont Electronics specifies a sheet resistivity of less than  $5 \text{ m}\Omega/\square$  for the same fired thickness.<sup>35</sup> The composition of via fill inks is slightly different from that of conductors. This allows the via fill to closely match the CTE of the dielectrics and, in the process, changes both the thermal and electrical conductivities. The sheet resistivity of DuPont Electronics' 5727 gold via fill material is  $15 \text{ m}\Omega/\square$ . This is five times that of pure gold. There is also a drastic difference in the thermal conductivity of thick-film gold in comparison with pure gold. Thick-film gold via fill has a measured thermal con-

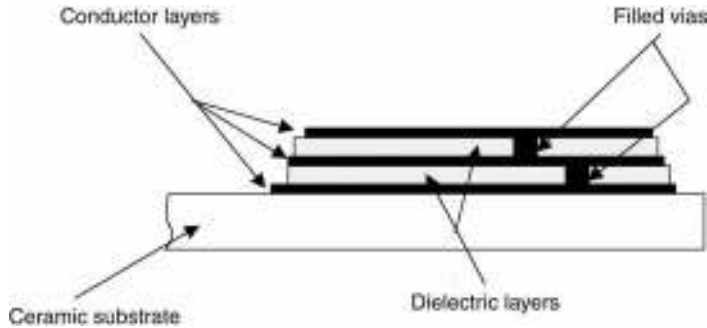


Figure 10.13 Multilayer thick film dielectric cross section.

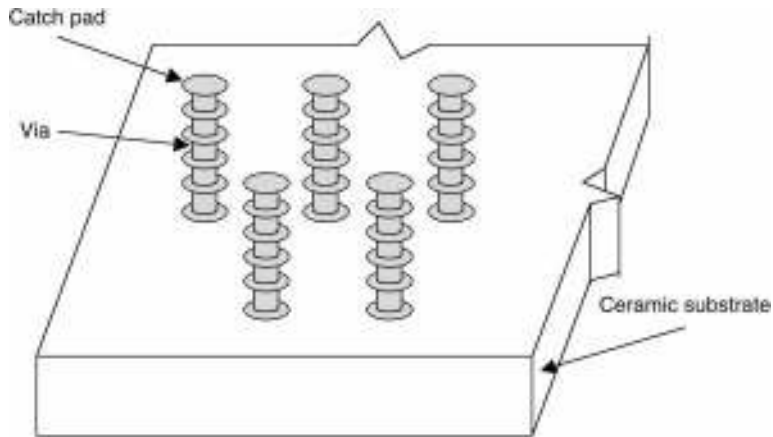


Figure 10.14 Portion of a thermal via array in multilayer thick film dielectric.

ductivity of  $20.1 \text{ W/m-K}$  (see Ref. 41), whereas pure gold has a thermal conductivity of  $297 \text{ W/m-K}$ .<sup>24</sup>

There are two key parameters in the design of thermal vias in thick films. The diameter of the via is determined by the filling process. If the diameter is too large, it will be difficult to fill with just one or two screen printings. The design of the spacing or pitch of the vias is a trade-off. Obtaining the maximum thermal conduction requires a high pitch or high density of vias. But a high pitch has two problems. First, it restricts routing of the signals. Even though via fill materials are designed to match the CTE of the dielectric, placing too many per unit area increases the effective CTE and puts the dielectric material into stress, which can result in cracking.<sup>8</sup>

Direct bond copper (DBC) is a patented<sup>42</sup> process, originally developed at General Electric, in which copper is eutectically attached to oxygen-bearing ceramics such as alumina and beryllium oxide. As shown in the copper-oxygen phase diagram in Fig. 10.15, copper and oxygen have a eutectic point at  $1065^\circ\text{C}$ . At this point on the phase diagram, there is 0.39 percent oxygen. When copper is placed on the ceramic between  $1065$  and  $1083^\circ\text{C}$  (the melting

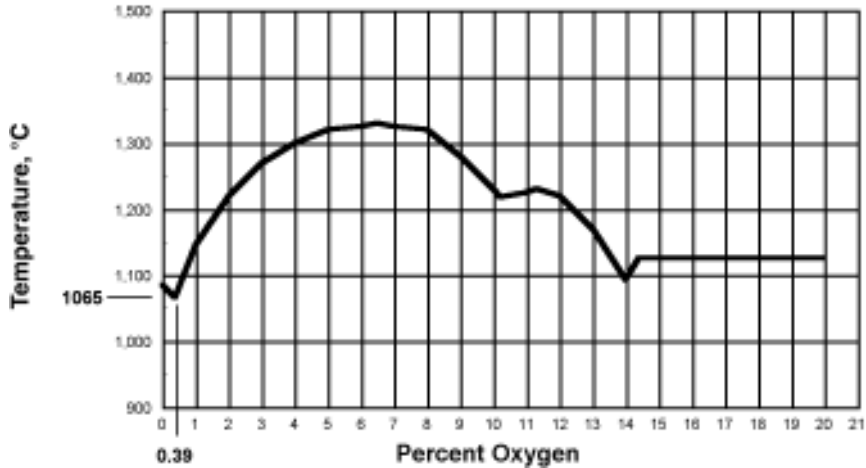


Figure 10.15 Copper-oxygen phase diagram.

point of copper), the copper fuses with the ceramic. A cross section of direct bond copper is shown in Fig. 10.16. There is a thin layer of Cu-O between the copper and the ceramic. In microelectronics applications, the thickness of the copper foil can range from 0.001 to 0.020 in. Because copper has a CTE of 16.12 ppm/°C,<sup>43</sup> which is many parts per million higher than that of the ceramic, it can place the ceramic in tension and either warp it or cause it to crack. To prevent this, manufacturers of direct bond copper typically place equal amounts of copper on both sides of the ceramic. A curve for the equivalent CTE versus copper thickness for an alumina substrate with equal amounts of copper on each side is shown in Fig. 10.17.<sup>44</sup> Most DBC manufacturers recommend limiting the thickness of the copper on each side of the substrate as a percentage of the ceramic thickness to prevent warping and cracking of the ceramic.<sup>45</sup>

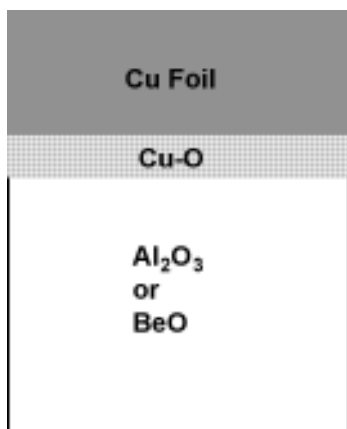


Figure 10.16 Cross section of direct bond copper on alumina and beryllia.

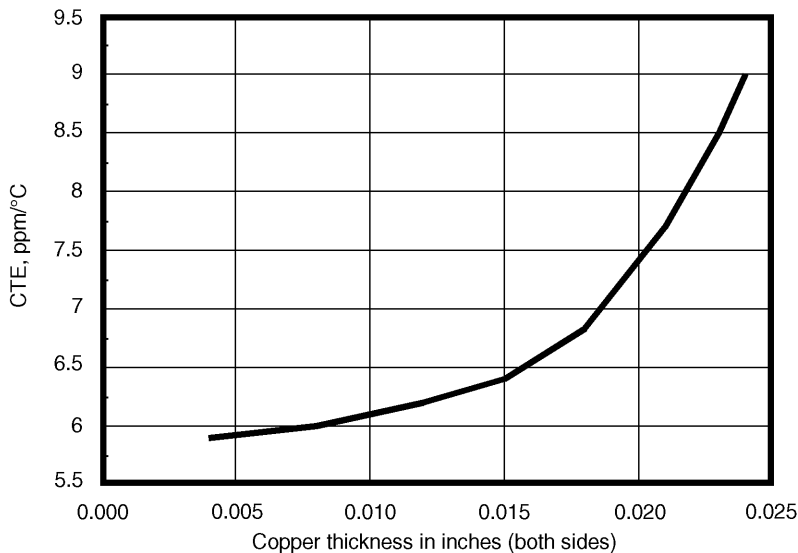
Most applications of direct bond copper require it for its high electrical conductivity. Typical values of sheet resistivity are significantly less than  $1 \text{ m}\Omega/\square$ . An added benefit of DBC is its high thermal conductivity as a result of the excellent spreading capability of the copper. Nguyen has developed an equation for the equivalent thermal conductivity of direct bond copper substrates.<sup>47</sup>

$$K_e = \frac{\sum_{i=1}^n K_i t_i}{\sum_{i=1}^n t_i} \quad (10.26)$$

where  $K_e$  = equivalent thermal conductivity  
 $K_i$  = thermal conductivity of each material  
 $T_i$  = thickness of each material  
 $n$  = number of materials

**Example** Find the equivalent thermal conductivity of a direct bond copper substrate consisting of 0.010-in thick copper on each side of a 0.025-in thick beryllium oxide substrate.

- $K_{Cu} = 401 \text{ W/m-K}$
- $K_{BeO} = 248 \text{ W/m-K}$
- $t_{Cu} = 0.010 \text{ in}$
- $t_{BeO} = 0.025 \text{ in}$



**Figure 10.17** Equivalent TCE vs. copper thickness for a 0.025-in alumina substrate with equal amounts of copper on each side.

The thicknesses of the copper and beryllium oxide are first converted to metric units.

- $t_{Cu} = 0.010 \text{ in} \times 0.0254 \text{ m/in} = 2.54 \times 10^{-4} \text{ m}$
- $t_{BeO} = 0.025 \text{ in} \times 0.0254 \text{ m/in} = 6.35 \times 10^{-4} \text{ m}$

Using Eq. (10.26), the equivalent thermal conductivity  $K_e$  is calculated.

$$K_e = \frac{2.54 \times 401 \times 6.35 \times 10^{-4} \times 248 + 2.54 \times 10^{-4} \times 401}{(2.54 + 6.35 + 2.54) \times 10^{-4}} = 8.03 \text{ W/m-K} \quad (10.27)$$

An alternative material used for dielectrics in thick film multilayer circuits is *tape transfer dielectric*. The tape dielectric process is a patented process<sup>48</sup> in which layers of glass-ceramic tape are applied to a fired, dimensionally stable substrate in lieu of screen printing the dielectric. This process has several trade names—TTRAN, Tape-on-Substrate, and DITRAN. The purpose of using tape dielectric in lieu of screen-printed dielectric is to provide an extremely flat surface for screen printing fine lines (as narrow as 0.002 in). The thermal conductivity of the 41010-25C tape dielectric material from Electro Scientific Laboratories is 2.5 to 3.0 W/m-K.<sup>49</sup>

**10.5.3.2 Beryllium oxide.** Beryllium oxide, BeO, or *beryllia*, is often used when a high-thermal-conductivity substrate is required. At 25°C, beryllia has a thermal conductivity of 248 W/m-K,<sup>13</sup> a value ten times that of alumina. The thermal conductivity of BeO decreases with increasing temperature as shown in Fig. 10.18.<sup>19</sup>

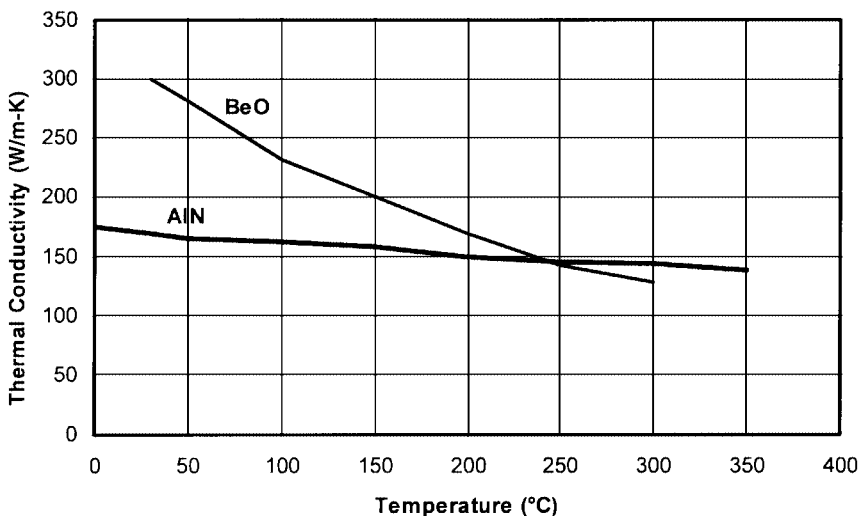


Figure 10.18 Thermal conductivity variation of AlN (170 W/m-K) and BeO.

All beryllium compounds, including beryllium oxide, are toxic in powder form. However, in their solid form, they do not pose any health hazards. Therefore, operations such as grinding, cutting, laser trimming, and certain furnace operations need to be performed so that airborne beryllium oxide particles are not generated.

The dust of beryllium compounds causes *chronic beryllium disease* (CBD). It is also known as *berylliosis*, a disease whose symptoms include scarring and damage of lung tissue, shortness of breath, wheezing, and/or coughing.<sup>50</sup> The incidence of CBD requires three factors:

1. The individual must be allergic to beryllium. It is estimated that approximately 1 percent of the population is allergic to beryllium. Because those who are susceptible cannot be identified, 100 percent of the population must be protected.
2. The individual must be exposed to beryllium of a respirable size—less than 10  $\mu\text{m}$ . The only significant hazard associated with beryllium is inhalation. Airborne particles in excess of 10  $\mu\text{m}$  in size cannot penetrate the upper respiratory tract and enter the alveolar area of the lung.
3. The individual must be exposed to a sufficiently large concentration of airborne beryllium. There is no exact dividing line between safe and unsafe amounts. The recommended levels, which include guard bands, are 2  $\mu\text{g}/\text{m}^3$  average or 25  $\mu\text{g}$  peak.<sup>51</sup>

Because of the toxicity of beryllium oxide, several countries and some individual companies have banned its use.<sup>52</sup> Where beryllia is used, it must be clearly identified on the component and its shipping container.

Beryllia is commonly metallized with refractory metallization such as tungsten and moly-manganese, nickel, and gold plating. Other metallization methods include thin and thick films as well as direct bond copper. When multilayer thick films are used with beryllium, the thermal resistance must be broken down into two main parts—the ceramic and the glass/metal combination of the multilayers.

The CTE of 99.5 percent beryllia at 20°C is 6.4 ppm/°C, which is very close to that of alumina.<sup>13</sup> The variation of linear expansion of beryllia over the temperature range is shown in Fig. 10.19. This is a key parameter in mounting devices to the BeO or mounting the BeO to the next assembly.<sup>51</sup>

**10.5.3.3 Aluminum nitride.** A high-thermal-conductivity alternative to beryllium oxide is aluminum nitride, AlN. Having a nominal thermal conductivity of 170 W/m-K at 25°C,<sup>13,55</sup> it is approximately seven times more thermally conductive than alumina. Aluminum nitride, with a room temperature CTE of 4.7 ppm/°C, is more closely matched to silicon (2.5 ppm/°C over the 20 to 100°C range)<sup>13</sup> than beryllium oxide or alumina. For many high-power applications, aluminum nitride is the substrate material of choice, as it is nontoxic. The thermal conductivity of aluminum nitride can have significant variation if the

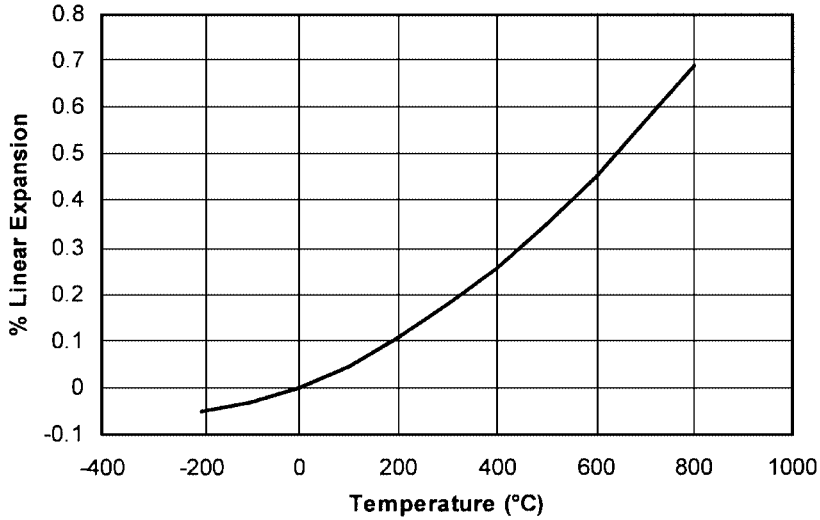


Figure 10.19 TCE variation of beryllium oxide vs. temperature.

oxygen content varies. As shown in Fig. 10.20, a 0.2 percent change in oxygen content can have a 12.5 percent variation in thermal conductivity.

Both beryllium oxide and aluminum nitride have thermal conductivity degradation as the temperature increases. As shown in Fig. 10.18, the thermal conductivity of aluminum nitride becomes greater than that of beryllium oxide at temperatures greater than 240°C. Therefore, for operation at temperatures in excess of 240°C, aluminum nitride is the ceramic material of choice when high thermal conductivity is the selection criteria.<sup>19</sup>

Aluminum nitride can be metallized a number of ways. Single-layer thin film is a reliable metallization. Starting with a sputtered or evaporated adhe-

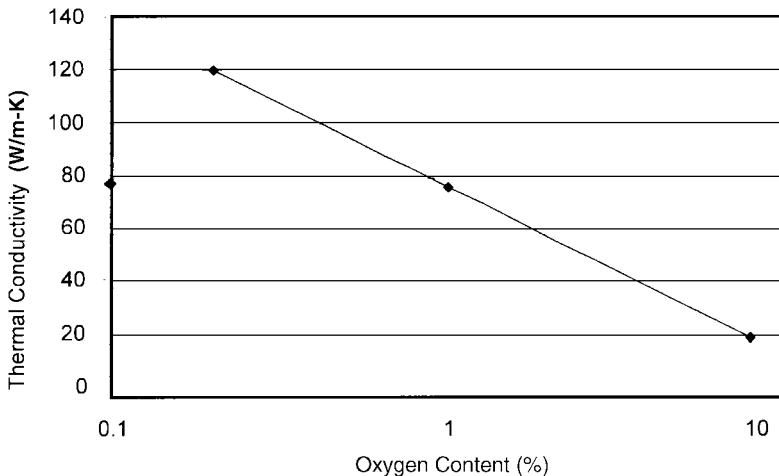


Figure 10.20 Copper-oxygen phase diagram.



sion layer, it can be plated with nickel and gold. Refractory metallization can also be used.

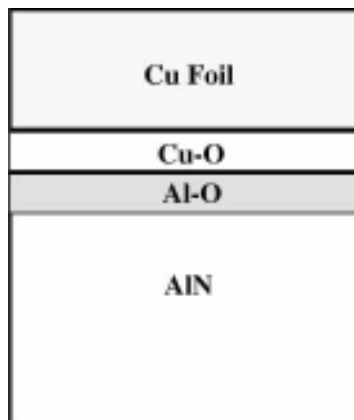
Aluminum nitride can be metallized using the classic thick film printing process using specially formulated inks. The oxide glasses in inks formulated for alumina are not chemically compatible with aluminum nitride. The CTE of glasses for dielectrics need to match those of the substrate. Because standard thick film inks are formulated for 96 percent alumina with a CTE of 6.3 ppm/°C, they do not match the CTE of AlN at 4.2 ppm/°C.<sup>13</sup> In addition, the reactive bonding compounds in standard thick film inks in alumina are not effective in promoting adhesion to aluminum nitride substrates.<sup>56</sup> Several thick film ink manufacturers have developed inks that are compatible with aluminum nitride.<sup>57,58</sup>

Aluminum nitride can also be metallized using active metal brazing, a process that relies on an “active” (i.e., chemically reactive) constituent, usually titanium, to produce a wettable compound at the brazing interface.<sup>59</sup>

Aluminum nitride can be metallized with direct bond copper. However, the process used for oxide-bearing ceramics (alumina and beryllium oxide) must be modified to first grow an oxide of Al-O on the aluminum nitride. This oxygen layer thickness is on the order of angstroms. The copper oxide then fuses with this Al-O oxide. A cross section of direct bond copper on aluminum nitride is shown in Fig. 10.21. The effect of adding copper to both sides of aluminum nitride can be modeled in the same manner as described in Eq. (10.26).

One shortcoming of aluminum nitride is its decomposition to amorphous aluminum hydroxide when in contact with water at elevated temperatures. Aluminum nitride also reacts with cleaning solutions containing ammonia. The ammonia will etch the substrate and produce a porous surface finish that will lead to poor adhesion between metallization and the substrate.<sup>60</sup>

**10.5.3.4 Low-temperature cofired ceramic.** Low-temperature cofired ceramic (LTCC) is a thick film process technology commercialized by DuPont in 1985 and used for multilayer substrates and integral substrate-packages. The



**Figure 10.21** Cross section of direct bond copper on aluminum nitride.

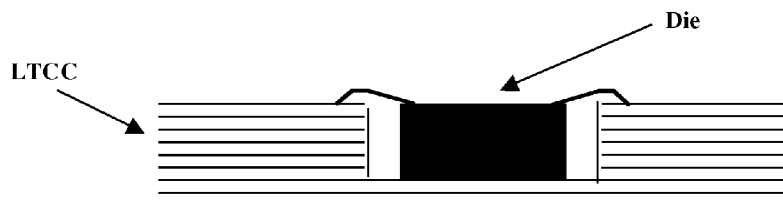
LTCC process starts off with “green” (unfired) ceramic tape that is a combination of glass and ceramic. It has a high glass content, allowing it to be fired at temperatures in the range of 850 to 950°C. This low firing temperature allows the LTCC to be metallized with low-resistivity gold, silver, and copper conductors. Vias, cavities, and registration holes are produced in the tape by mechanical drilling, punching, or laser ablation. Next, the individual layers are metallized using the classic screen-printing process. Vias are then filled. The individual layers are then collated, aligned, laminated, and fired in an air-fired furnace. During firing, the LTCC shrinks nominally 12.27 percent. The completed substrate is cut to size using either a mechanical or laser process.<sup>8,35</sup>

The thermal conductivity of LTCC ranges from 2.0 to 4.4 W/m-K, depending on the manufacturer and the particular formulation of the tape. See Table 10.10 for details. For all formulations of LTCC, the thermal conductivities are extremely low as a result of the high glass content (approximately 50 percent). To minimize the effect of the low thermal conductivity, physical designers can use cavities under high-power-density components, arrays of thermal vias, or a combination of both.<sup>36,40,61–63</sup>

**TABLE 10.10 Thermal Properties of LTCC<sup>36,40,61–63</sup>**

Material	Manufacturer	Thermal conductivity, (W/m-K)	CTE (25–300°C), (ppm/°C)
951	DuPont	3.0	5.8
943	DuPont	4.4	4.5
41110-70C	ESL	2.5–3.0	6.4
41020-70C	ESL	2.5–3.0	7.4
A6M	Ferro	2.0	7.0
A6S	Ferro	2.0	8.0

The number of layers of tape constituting an LTCC substrate can range from as few as 5 to as many as 50. To minimize the thermal resistance, the designer can place the high-dissipating component in a cavity as shown in Fig. 10.22. In this figure, the bottom of the die is electrically isolated from the back of the substrate with two layers of tape. The actual number of layers of tape under the cavity is a function of the area of the cavity and the strength of the



**Figure 10.22** Isolated die in cavity under LTCC.

LTCC. For small devices (i.e., less than 0.1 in sq.), there can be only one or two layers of tape. For large devices, such as complex ASICs, there must be at least five layers of tape. When the back side of the die does not need to be electrically isolated and can sit on the package base or heat sink, the cavity can go through the entire LTCC substrate as shown in Fig. 10.23.

The use of thermal vias in LTCC is a standard method of improving the effective thermal conductivity. There can be an array of stacked vias going to the bottom of the substrate, as shown in Fig. 10.24, or to one layer above, as shown in Fig. 10.25. In the former case, the back side of the die does not need to be isolated from the bottom of the substrate. In the latter case, the bottom layer of the substrate provides the electrical insulation. Thermal vias can be used in conjunction with the die cavities discussed above. A cross section of a substrate with a die cavity and thermal vias is shown in Fig. 10.26.

The density of the thermal vias and their diameter are typically set by the individual manufacturer of LTCC substrates with recommendations from the tape manufacturer. The via diameter is a function of the method used to fill the vias and the differential shrinkage of the via fill material and the LTCC material. An industry standard for via diameter is 0.006 in.<sup>8</sup> The density, or pitch, of the thermal vias is a function of the CTE of the via fill with respect to the CTE of the LTCC tape. The relative dimensions of a typical thermal via array are shown in Fig. 10.27.<sup>40,61</sup> For the industry standard 0.006-in diameter via, the spacing of the vias should be 0.018 in.

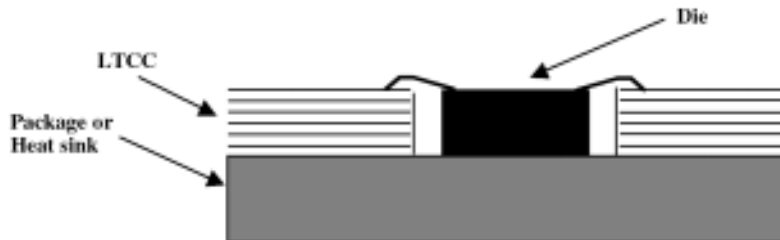


Figure 10.23 Cavity in LTCC with die directly attached to package or heat sink.

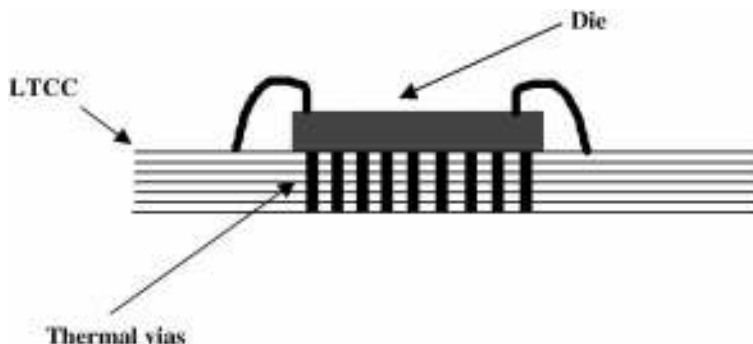


Figure 10.24 Thermal vias in LTCC.

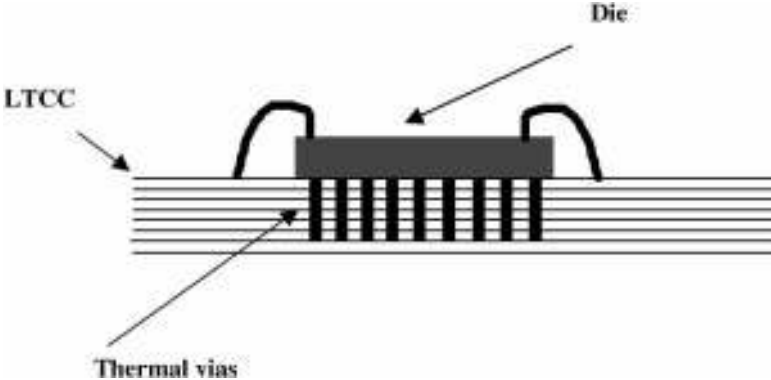


Figure 10.25 Thermal vias in LTCC with electrically isolated die.

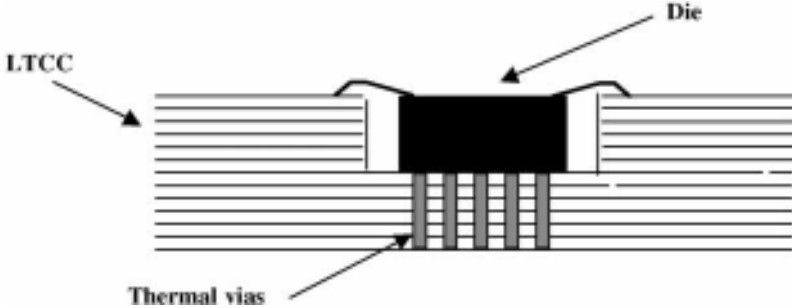


Figure 10.26 Cavity in LTCC with thermal vias.

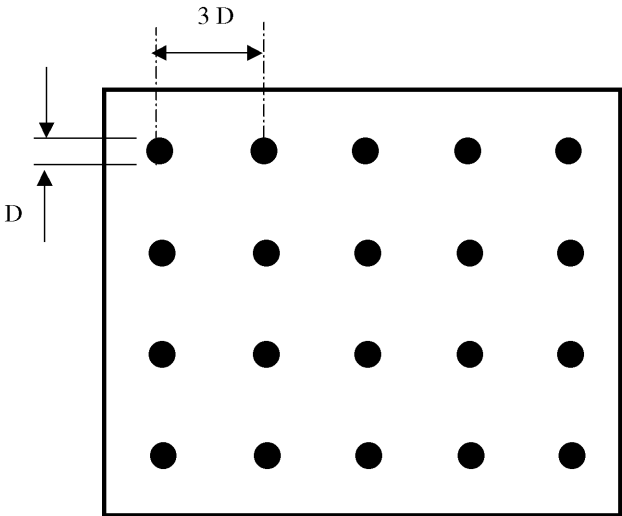


Figure 10.27 Via dimensions in LTCC.

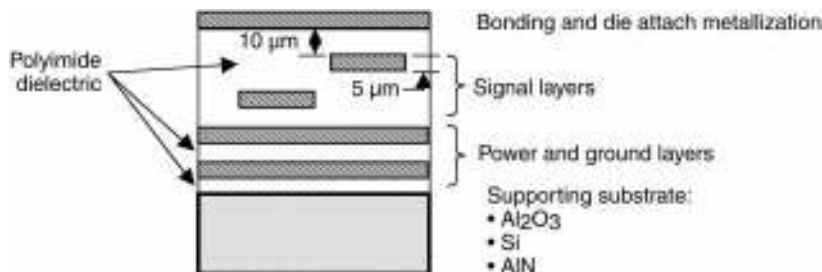
The LTCC manufacturer has a choice of gold, silver, or palladium silver inks for use as via fill materials. The silver inks are both electrically and thermally more conductive than the gold inks. DuPont<sup>35</sup> publishes electrical resistivity data for its via fill inks but does not give any thermal conductivity data. Licari<sup>8</sup> has data on average thermal resistance for very large (0.020-in dia.) gold and silver thermal vias that shows silver being 8 to 15 percent lower. Actual measured data are very limited. The measurements by Harshbarger<sup>64</sup> were used to calculate the thermal conductivity of 5718 gold via fill at 24.4 W/m-K.<sup>41</sup>

**10.5.3.5 Thin film multilayer substrates.** Thin film multilayer substrates are used to fabricate MCM-Ds (MCM-deposited). Many materials (alumina, silicon, aluminum nitride, and aluminum) are used as the supporting substrate and have been previously described. The difference is in the metallization and the insulating dielectric material. A cross-sectional view of a typical MCM-D substrate is shown in Fig. 10.28. Most MCM-D manufacturers use polyimide or other polymers as the dielectric in their thin film multilayer substrates. Internal metallization traces can be copper, gold, or aluminum. External (or top) metallization can be either aluminum or gold.<sup>8</sup>

The total thermal resistance of the thin film multilayer substrate consists of two resistances in series—the multilayer portion and the supporting material. The thermal conductivity of the thin film multilayer portion of the substrate is primarily determined by the low thermal conductivity of the polyimide. Typical values for the polyimide are in the range of 0.2 to 0.3 W/m-K (see Table 10.11).<sup>8,66</sup>

**TABLE 10.11 Thermal Properties of Thin Film Dielectrics**

Material	Thermal conductivity (W/m-K)
Polyimide	0.2–0.3
Silicon dioxide	0.5–2.0



**Figure 10.28** MCM-D substrate cross section with polyimide dielectric.

Some MCM-D manufacturers use silicon dioxide as the dielectric layer. A cross-sectional view of an MCM-D substrate with silicon dioxide dielectric is shown in Fig. 10.29. Silicon dioxide's thermal conductivity of 0.5 to 2.0 W/m-K is extremely low.<sup>3</sup>

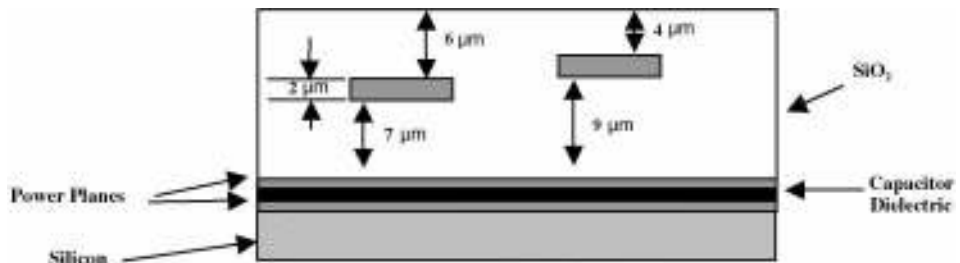
To improve the effective thermal conductivity in thin film multilayer substrates, the physical designer can use arrays of thermal vias. The materials used for these vias are the same as the internal metallization of the substrates—gold, copper, or aluminum. The thermal conductivity of these metallizations is listed in Table 10.12. Deposited as a thin film using evaporation or

**TABLE 10.12 Thermal Conductivity of Thin Film Metallizations<sup>65</sup>**

Material	Thermal conductivity (W/m-K)
Gold	319
Aluminum	237
Copper	401
Nickel	94

sputtering, these thermal vias are composed of pure metals and have the same thermal conductivity as the pure metals. The dimensions of a thermal via array with a polyimide dielectric are shown in Fig. 10.30. When thermal vias are used, and their area equals 50 percent of the die area, the effective thermal conductivity of a polyimide based dielectric improves to 1.2 W/m-K. For a thermal via pattern that is 75 percent of the die area, the effective thermal conductivity is 2.4 W/m-K.

**10.5.3.6 Steel substrates.** Ceramic substrates, as described above, are difficult to attach to heat sinks with screws because of their low tensile strength. Polymeric attachment adds thermal resistance to the thermal path. Steel substrates do not have these shortcomings because of the strength of the steel.



**Figure 10.29** MCM-D substrate cross section with silicon dioxide dielectric.

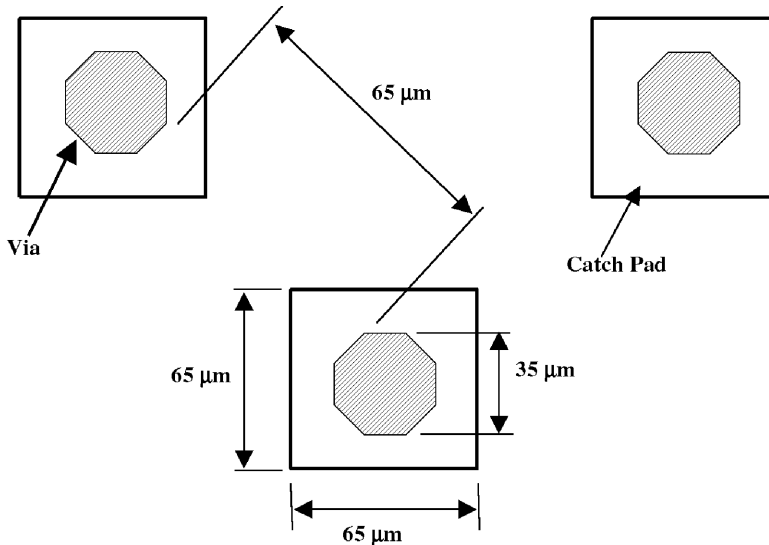


Figure 10.30 Dimensions for thermal vias in MCM-D substrates.

However, steel is an electrical conductor and needs to be insulated before being used as a substrate. The Cermalloy Division of Heraeus Incorporated has developed a system of thick film inks for use with Type 430 stainless steel substrates.<sup>37</sup> This system of inks is known as Dielectric on Steel (DOS). The process starts out with the printing of dielectric material on the steel with subsequent drying and firing. Multiple layers of dielectric are typically used to prevent pinholes that can lead to shorts between layers. The recommended fired thickness of dielectric is  $0.003 \pm 0.0002$  in. Conductors are added using the classic thick film processes. Additional dielectrics and conductors are added as required.

The thermal conductivity of the Cermalloy GPA98-047 is 4.3 W/m-K, whereas the thermal conductivity of Type 430 stainless steel is 26.1 W/m-K. The value of the dielectric thermal conductivity can be considered low.<sup>13,37,68,69</sup>

**10.5.3.7 CVD diamond.** Synthetic diamond or chemically vapor deposited (CVD) diamond is a very high ( $>1300$  W/m-K) thermal conductivity material that can be used both as a substrate and as a heat spreader. An electrical insulator ( $\rho > 10^8 \Omega\text{-cm}$ ), CVD diamond has a temperature coefficient of expansion of 2.0 ppm/ $^{\circ}\text{C}$  for temperatures in the range of 25 to 200 $^{\circ}\text{C}$ . This can possibly cause stresses between semiconductor materials and the diamond spreader or substrate. The CVD diamond can be grown “free standing”—as a substrate or as a film deposited on another material. Figure 10.31 shows an alumina substrate with a layer of CVD diamond. Diamond substrates can be metallized with thin films such as titanium-platinum-gold (TiPtAu), titanium-palladium-gold (Ti/Pd/Au), nichrome-nickel-gold (NiCr/Ni/Au), titanium-tungsten-gold



Figure 10.31 CVD diamond layer on alumina substrate.

(Ti-W/Au), or chrome-gold (CrAu). Thick film metallization of diamond has not been developed.

With its extremely high thermal conductivity, CVD diamond can serve as an excellent heat spreader. One of the earliest applications of the material was as a heat spreader under high-power-density gallium arsenide devices.

Compared to ceramics such as alumina, beryllia, and aluminum nitride, CVD diamond is considered expensive. To minimize costs when using CVD diamond, the size needs to be minimized. Moravec et al. have found that the optimal thickness ( $t_{opt}$ ) of a diamond heat spreader should be 0.5 to 1.0 times the radius of the heat source as shown in Fig. 10.32. The optimal radius ( $R_{opt}$ ) of the heat spreader should be three times that of the heat source. This analysis can be approximated for rectangular heat sources by substituting half the device's length in Eq. (10.29) for the radius as described above.<sup>70</sup>

$$t_{opt} = 0.5 \text{ to } 1.0 \times \text{radius of heat source} \quad (10.28)$$

$$R_{opt} = \frac{a_2}{a_1} \quad (10.29)$$

The thermal properties of CVD diamond are tabulated in Table 10.8.<sup>34,71</sup>

**10.5.3.8 Insulated metal substrates.** Insulated metal substrates (IMS) are used as both substrates and circuit cards. As shown in Fig. 10.33, they are com-

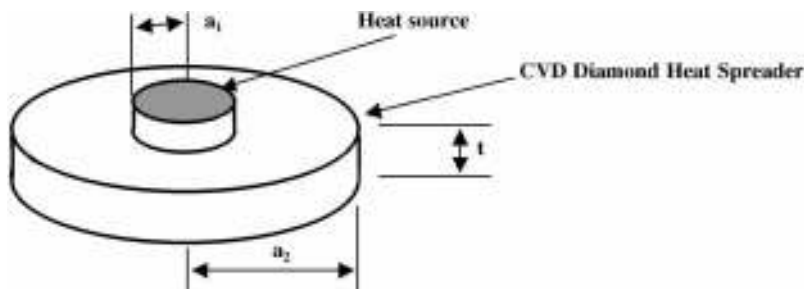


Figure 10.32 Optimal size of CVD diamond heat spreader.





Figure 10.33 Single-layer insulated metal substrate cross section.

posed of a single-sided metal-clad board material with several layers of metallization. Fabricated in arrays on panels as large as 18 x 24 in, insulated metal substrates offer a low-cost, high-thermal-conductivity alternative to FR-4 printed circuit cards. The backing plate, typically aluminum, can also be copper, copper-Invar-copper, copper-molybdenum-copper, or steel and serves as a heat sink. The dielectric material is a polymer material whose thickness is a trade-off between voltage breakdown and thermal resistance. To have the highest voltage breakdown requires the thickest layer of dielectric. However, the dielectric is a poor thermal conductor, and its thickness needs to be minimized so that the thermal resistance can be minimized. The thermal conductivity of the dielectric material for Berquist's IMS is 1.3 W/m-K.<sup>72</sup> To improve the thermal conductivity of the polymer dielectric layer, the IMS manufacturer typically loads the material with alumina or boron nitride. The voltage breakdown of this standard Berquist material is 6 kV.

Improved dielectric materials for insulated metal substrates are available with a higher thermal conductivity of 2.0 W/m-K.<sup>72</sup> These materials also have a higher dielectric breakdown voltage of 9 kV.

On IMS substrates, the conductor traces are copper with thicknesses that range from 1-oz copper (0.0014 in) to 4-oz copper (0.0056 in). The effect of thick copper metallization not only aids in minimizing voltage drop, it helps spread the heat.

The equivalent CTE of IMS substrates is very close to that of the backing plate. For example, for the Berquist IMS material with an aluminum base, the CTE is 20 ppm/°C.

Insulated metal substrates can be made with two conductor layers as shown in Fig. 10.34. The thermal conductivity of the dielectric remains the same as



Figure 10.34 Two-layer insulated metal substrate cross section.

in the single layer, 1.3 W/m-K. However, in the multilayer IMS, thermal vias can be incorporated to reduce the thermal resistance. Table 10.13 summarizes the thermal properties of insulated metal substrates.

**TABLE 10.13 Thermal Properties of Insulated Metal Substrates<sup>13,72</sup>**

Base material	Dielectric	Thermal conductivity @25°C (W/m-K)	CTE (ppm/°C)
Copper C11000 alloy		388	17.0
Aluminum 6061		180	23.6
Cold-rolled steel		65.2	12.6
Copper-Invar-copper (1:3:1)		174 x & y 24.8 z	6.5
Copper-moly-copper (1:6:1)		233	6.4
	Thermal Clad <sup>®*</sup>	1.3	†
	Thermal Clad HTV <sup>®*</sup>	2.0	†

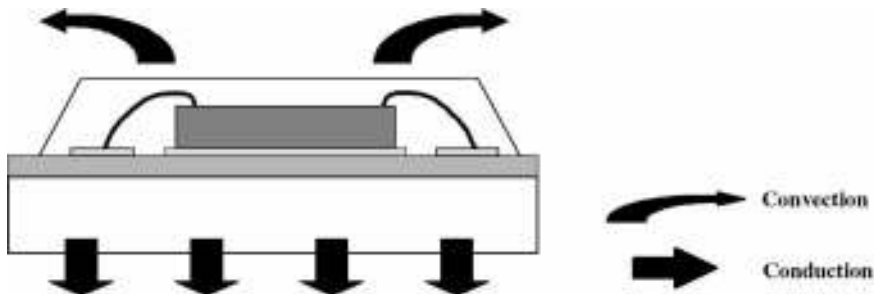
\*Thermal Clad and Thermal Clad HTV are registered trademarks of the Berquist Company.

†CTE of dielectric on base material is approximately equal to that of the base material.

Insulated metal substrates are used with both bare die and packaged devices. When used with bare die, the thermal path from the die to the heat sink is minimal as shown in Fig. 10.35. The heat goes from the die, through the die attach, through the IMS dielectric, and into the metal base plate, where it spreads.

**10.5.3.9 Printed wiring board substrates.** In MCM-L (laminated) applications, the multilayer substrate is fabricated from organic materials such as FR-4 and polyimide. Another name for the MCM-L is chip-on-board (COB), which is discussed in Sec. 10.5.5.1.

A complete discussion of printed wiring boards can be found in Sec. 10.5.7. The key differentiator in printed wiring boards used for MCM-L applications



**Figure 10.35** Thermal path for bare die on IMS.

is the requirement for wire bonding. Special attention needs to be given to the plating and cleaning of the boards to allow for high yields in wire bonding. The thermal conductivities of various printed circuit card dielectrics are listed in Table 10.14.

**TABLE 10.14 Thermal Conductivity of Printed Circuit Card Dielectrics.**<sup>3,19,38,73-76\*</sup>

Material	Thermal conductivity @25°C (W/m-K)	CTE (below T <sub>g</sub> ) (ppm/°C)	Comments
FR-4	0.8 x & y 0.3 z	16-20 x & y 50-70 z	
G-10	0.294	14	
Bismaleimide/triazine (BT)	0.17-0.21	13-15 x & y 40-50 z	
Polyimide	0.11	23-56	
S-2 glass	0.9	2.8	
Aramid (Kevlar)	0.20	7-8 x & y 115 z	
Quartz	1.1	1.0	
GML 2032	0.289	28-30 x & y 80 z	99°C
GML 1000	0.228	30-32 x & y	120°C
Rogers RO4003	0.64	11-14 x & y 46 z	100°C
Rogers RT/Duroid 6002	0.6	16 x & y 24 z	
Arlon	0.28-0.36	17-29 x & y 217 z	
Benzocyclobutene (BCB)	0.19	45-70	

\*Unless otherwise noted, thermal conductivities are at 25°C.

#### 10.5.4 Substrate attach

A substrate is usually utilized in multichip applications. Attaching the substrate to the next assembly (whether it is a package, a circuit card, or a heat sink) requires an attachment medium. Polymeric material is typically used. Unless grounding is required for the back side of the substrate, the polymeric material is typically electrically nonconducting. Some of the polymeric paste materials used for die attach are also used for substrate attach and are listed in Table 10.7. To maintain a uniform bond line and to speed the assembly operation, preforms of thermoset and thermoplastics are used for substrate at-

tach. The thermal conductivity of organic materials specifically designed for substrate attach are listed in Table 10.15. If the backside of the substrate has to be electrically connected to the next assembly, then the attachment material needs to be electrically conducting. For high-power-density applications, solder may be used for substrate attachment. Typically applied in either a paste or a preform, the solders used include Sn10, Sn62, Sn63, Sn96, and gold-tin. The thermal conductivities of these solders are listed in Table 10.5.

**TABLE 10.15 Thermal Conductivity of Organic Adhesives for Substrate Attach**<sup>29,30,86</sup>

Material	Manufacturer	Electrical characteristics	Thermal conductivity (W/m-K)
Ablefilm 550K	Ablestik Industries	Nonconductive	0.8
Ablefilm 506	Ablestik Industries	Nonconductive	0.9
Ablefilm 563K	Ablestik Industries	Nonconductive	1.1
ECF 5025E	Ablestik Industries	Conductive	3.5
TK7755	AI Technology	Nonconductive	1.8
TP7165	AI Technology	Nonconductive	1.8
TK7759	AI Technology	Nonconductive	11.6
TC8750	AI Technology	Conductive	6.5
T7109	Epoxy Technology	Nonconductive	3.0
H70-2	Epoxy Technology	Nonconductive	1.4
930	Epoxy Technology	Nonconductive	4.0
6081	Epoxy Technology	Nonconductive	2.5

### 10.5.5 Packages

Electronic packages provide three key functions.

- Mechanical support and environmental protection for the semiconductor
- Power and signal interconnections from the semiconductor(s) to the circuit card
- A means for dissipating the heat generated in the semiconductor(s)

These functions can be accomplished by both hermetic and nonhermetic packages. In the following sections, the construction of the packages will be analyzed with respect to the materials and thermal paths composing the package.

**10.5.5.1 Nonhermetic packages.** Almost all of the semiconductors used today are assembled into packages. For most applications, the microcircuits are assembled in molded plastic packages called plastic encapsulated microcircuits (PEMs). In this packaging technology, the microcircuit is typically attached with a polymeric material to a lead frame, wire bonded, and encapsulated in a plastic material as shown in Fig. 10.36. The exterior base of the package is also plastic.

The primary heat paths from a plastic encapsulated microcircuit, as shown in Fig. 10.37, are through the base of the package and through the leads to the circuit card assembly. A secondary heat path is from the die through the plastic to the air. To improve the thermal performance, some manufacturers have developed plastic packages using thermally enhanced mold compounds.

A variety of plastic encapsulated microcircuit package families are used for surface mount applications. They include SOIC, SOJ, PLCC, BQFP, TQFP, and TSOP. Two key differentiators for the package families are lead configuration and pitch. The heat paths for each package type are the same as the generic PEM as described above.

To achieve higher thermal conductivity, the mold compound manufacturers add materials such as aluminum nitride, alumina, and boron nitride to their resins. For example, by adding aluminum nitride to the mold compound, the equivalent thermal conductivity of the mold material increases to 3.8 W/m-K. However, adding materials with higher thermal conductivities may degrade other properties of the molding compound such as stress performance.

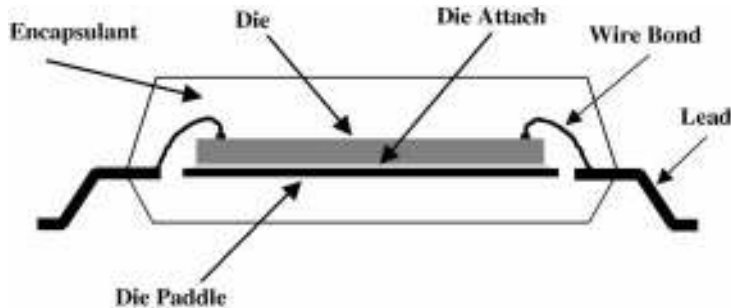


Figure 10.36 Plastic encapsulated microcircuit (PEM).

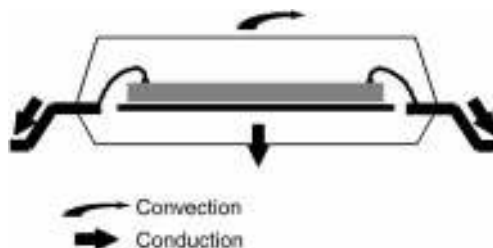


Figure 10.37 Heat paths from a PEM.

To further improve the thermal performance of PEMs, some manufacturers have developed plastic packages in which the bottom of the lead frame is exposed under the die. This type of package is known as an *exposed pad* or *exposed paddle*. An example is shown in Fig. 10.38. This exposed pad eliminates the low-thermal-conductivity plastic in the heat path. A variation of this technique is mounting the die on a low-cost heat spreader and then encapsulating it as shown in Fig. 10.39. Some semiconductor manufacturers are using packages with the exposed pad configuration and forming the leads so that the bottom of the die is directed away from the circuit card. In this configuration, the primary heat path is through convection cooling.<sup>24,77–79</sup>

The lead frame is the heart of the plastic encapsulated microcircuit. Fabricated from either a stamped or chemically etched piece of sheet metal, it acts as a holding fixture during the assembly process. After molding, it becomes an integral part of the package. Electrically, the lead frame provides the electrical connections from the chip to the circuit board. Thermally, the lead frame conducts heat from the chip to the circuit card.

The materials used for lead frames are nickel-iron alloys, clad or copper-based. Nickel-iron alloys are the most widely used metals for lead frames. A popular lead frame material is Alloy 42, a 42 percent nickel-58 percent iron alloy, which has a CTE of 4.5 ppm/°C that is reasonably close to silicon's 2.6 ppm/°C. Able to be heat treated to obtain optimal tensile strength and ductility, Alloy 42 has one significant drawback: a low thermal conductivity of 10.6 W/m-K.<sup>12,80</sup>

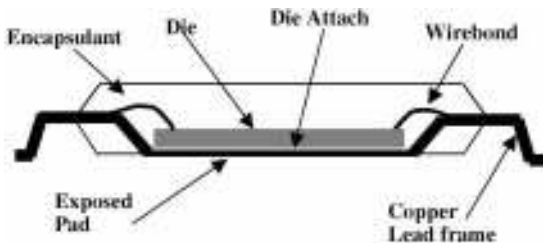


Figure 10.38 Exposed pad plastic package.

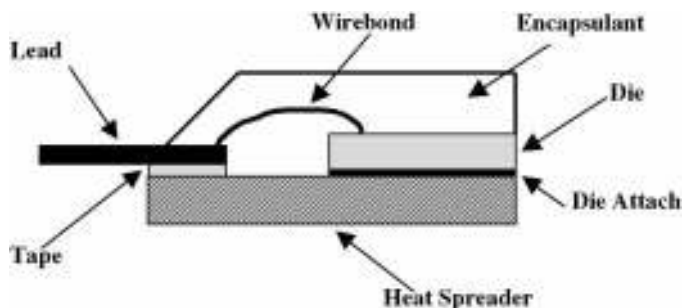


Figure 10.39 Die on heat spreader in plastic package.

To obtain improved thermal conductivity, manufacturers have gone to copper and copper-clad stainless steel lead frames. Copper-clad stainless steel is used for its thermal conductivity improvement over Alloy 42 without increasing the CTE.

Copper, with its high electrical and thermal conductivities, has been used for lead frames on PEMs. However, because of its high CTE, copper lead frames can introduce stresses in the die and die attach, leading to failures.<sup>81</sup>

The plastic materials used for encapsulation are modified epoxy resins with low thermal conductivities. The plastic encapsulation is typically loaded with fused silica and has an equivalent thermal conductivity of 0.5 to 1.0 W/m-K. Table 10.16 lists the thermal conductivities of various materials used for encapsulation.

**TABLE 10.16 Thermal Properties of Encapsulation Materials<sup>12,25,82</sup>**

Material	Manufacturer	Thermal conductivity @25°C (W/m-K)
Stycast XT5038-6/B 100	Emerson & Cuming	0.4
Stycast 2651-40/Cat 11	Emerson & Cuming	0.6
Stycast 2851 KT	Emerson & Cuming	2.8
Stycast XT5038-6/B 100	Emerson & Cuming	0.6
Hysol FP4450	Dexter*	0.63
Hysol FP4401	Dexter	0.67
Hysol EO1016	Dexter	0.39
Hysol FP4322	Dexter	1.0
HIPEC 648	Dow Corning	0.094
GE RTV6126	General Electric	0.19

\*Dexter is now Loctite Corp.

The need to make a large number of interconnections (greater than 200) to a package in a small footprint has driven physical designers from their use of flat packs to ball grid arrays (BGAs). Although BGAs also provide ease of manufacture, low electrical parasitics, and a small footprint, they introduce unique cooling issues with respect to the heat paths and materials. There are three basic types of BGAs: tape (TBGA), plastic (PBGA), and ceramic (CBGA). Their construction and heat removal paths will be discussed in the subsequent sections.

Lau and Chen<sup>83</sup> have shown that the amount of heat removed through conduction from a plastic BGA with an integral heat sink is less than 50 percent. Approximately 40 percent is removed through convection. Although the actual percentages will vary by BGA construction, these percentages can be applied to all BGA types as a first approximation.

In the TBGA, as shown in Fig. 10.40, the die sits, cavity down, on the integral flat copper or aluminum heat sink. This allows the heat to spread from the die to the overall dimension of the heat sink. As shown in Fig. 10.41, there are two heat paths from this point—convection to the air and conduction through the BGA package and balls to the circuit card. To aid in convection cooling, a finned heat sink can be attached to the BGA heat sink. The heat path through the package is hindered by the high thermal resistance of the tape layer, although extremely thin (0.002 to 0.004 in), and is typically composed of a polyimide with a thermal conductivity of 0.27 W/m-K. From the tape layer to the circuit card are solder balls. For Sn 63 solder balls, the thermal conductivity is 51 W/m-K. The thermal conductivities of other solder compositions can be used and are listed in Table 10.5.

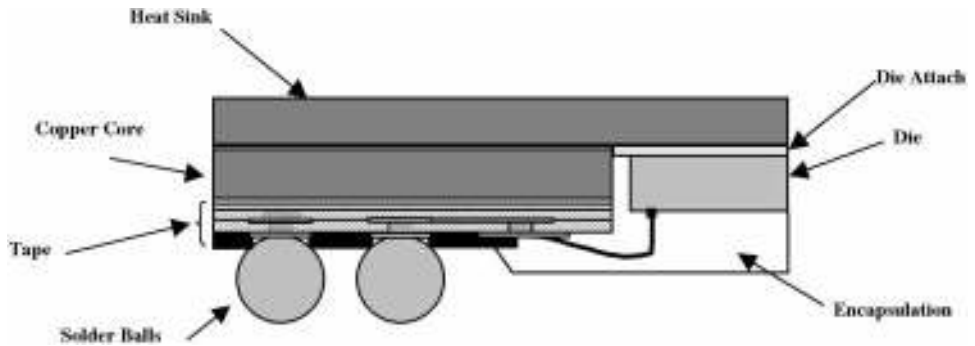


Figure 10.40 TBGA cross section.

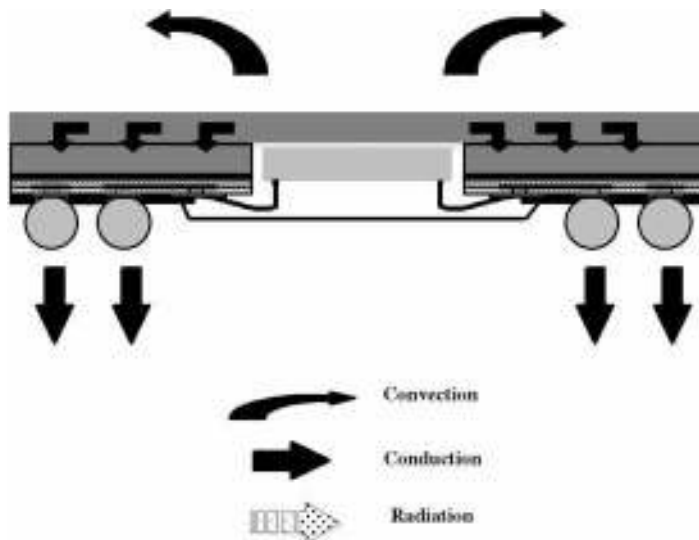


Figure 10.41 Heat paths in TBGA.



Without forced air and a finned heat sink, a 27-mm square TBGA with 256 balls and a die 6 mm square typically has a thermal resistance (junction-to-air) of 10 to 15°C/W.

The die is protected from the environment with a glob-top encapsulant. Typically, these potting materials have a thermal conductivity in the range of 0.1 to 2.8 W/m-K. See Table 10.16 for the thermal properties of encapsulants.

Having a substrate fabricated with printed circuit board materials (copper and polyimide), the TBGA has a CTE that matches most circuit cards and does not pose the problem of solder joint cracking.

In the PBGA, the die sits on a substrate fabricated from a circuit card material such as epoxy or bismaleimide/triazine (BT). There are two configurations of the PBGA as shown in Fig. 10.42: die-up and die-down. In the die-up configuration (Fig. 10.42b), there can be a full array of solder balls on the substrate. Not only does this configuration give the maximum number of interconnections, it provides a more direct thermal path from the die to the circuit card. A version of the die-up configuration shown in Fig. 10.42c, known as the thermally enhanced BGA, has a set of solder balls directly under the die that are used only for improving the thermal path. In the die-down configuration (Fig. 10.42a), a heat sink can be attached to the back of the BGA to enhance convection. The substrates used for plastic ball grid arrays have thermal conductivities in the range of 0.1 to 0.2 W/m-K. The heat paths in the plastic ball grid array are shown in Fig. 10.43.

Without forced air and a finned heat sink, a 27-mm square PBGA with 256 balls having a die size of 6 mm square typically has a thermal resistance (junction-to-air with natural convection) of 18 to 26°C/W. This high value of thermal resistance can be attributed to the low thermal conductivity of the FR-4 (0.35 W/m-K) or BCB (0.14 W/m-K) material composing the substrate or body of the package.

Having a substrate fabricated with printed circuit board materials, the PBGA has a CTE that matches most circuit cards and does not pose the problem of solder joint cracking. The die is protected from the environment with a glob-top encapsulant with thermal properties listed in Table 10.16.

The ceramic ball grid array as shown in Fig. 10.44 provides significantly improved thermal conductivity over the plastic ball grid array as a result of the significantly higher thermal conductivities of the alumina or aluminum nitride substrates. Alumina has a thermal conductivity of 21 W/m-K, whereas aluminum nitride has a thermal conductivity of 170 W/m-K. These conductivities are several orders of magnitude higher than those for plastic ball grid array substrates.

Like the PBGA, the CBGA has two configurations: die-up and die-down. The die-up configuration is shown in Fig. 10.44. The heat paths from a CBGA are shown in Fig. 10.45. In the die-down configuration, a heat sink can be attached to the back of the BGA to enhance convection.

Having a substrate fabricated with a low-CTE ceramic, the CBGA has a CTE that is significantly lower than that of printed circuit cards. During temperature cycling, the CTE mismatch between the CBGA and the circuit card can result in solder joint cracking at the balls. To minimize this problem, some

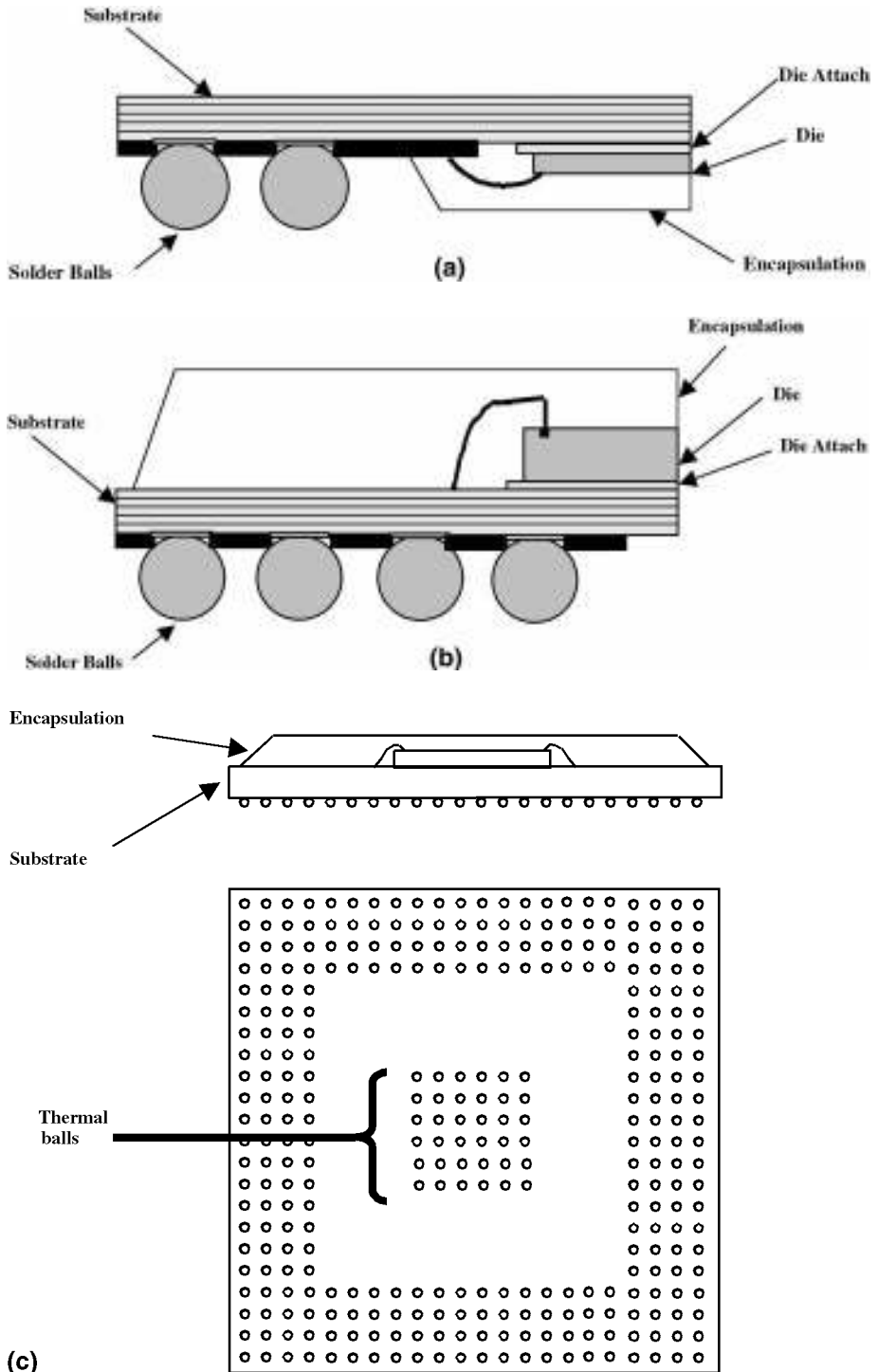


Figure 10.42 PBGA configurations: (a) die-down, (b) die-up, and (c) thermally enhanced.

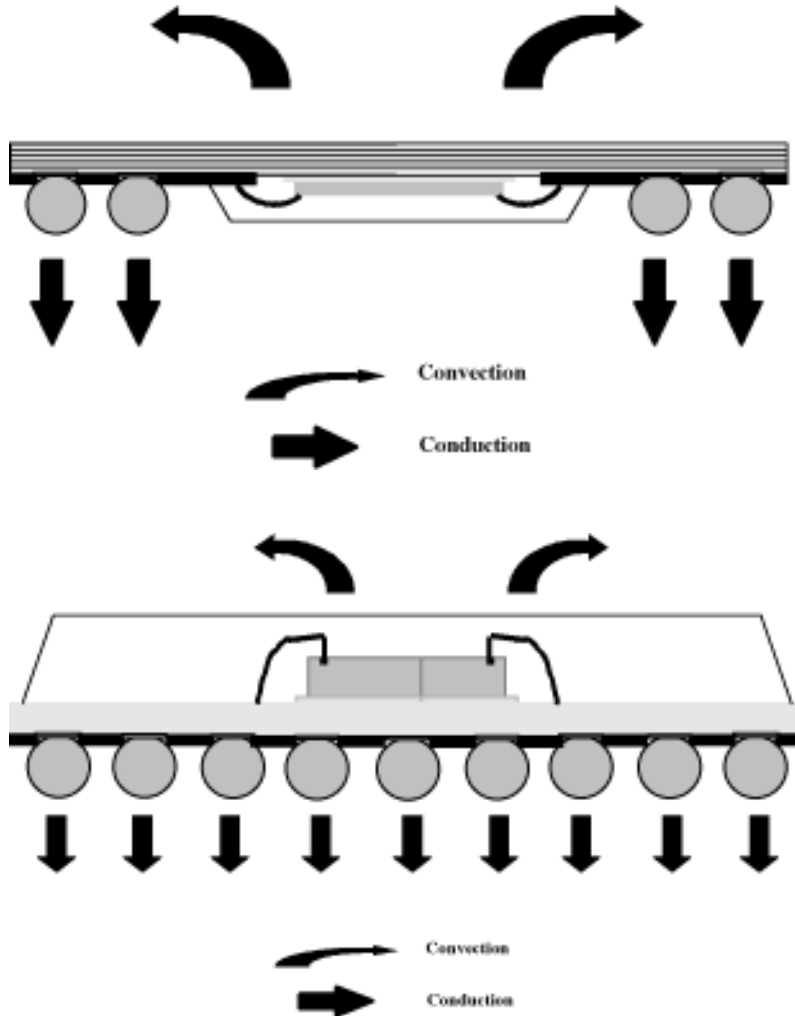


Figure 10.43 Heat paths in PBGA.

BGA manufacturers have gone to a column of solder in lieu of the ball to reduce the stresses. Some circuit card assemblers have gone to an underfill material between the BGA and the circuit card to help reduce the stresses. The die is protected from the environment by a glob-top encapsulant with the thermal properties listed in Table 10.16.

A chip-scale package (CSP) is defined as an IC package that has an area footprint equal to or less than  $1.2\times$  the footprint of the die.<sup>84</sup> In appearance, it looks like a miniature ball grid array. One manufacturer (Tessera) even calls its CSP a  $\mu$ BGA. A variety of configurations of CSPs are available as shown in the cross sections in Fig. 10.46. All of the chip-scale packages make use of solder balls with a pitch as fine as 0.5 mm in an area array for their interconnections.<sup>85</sup>

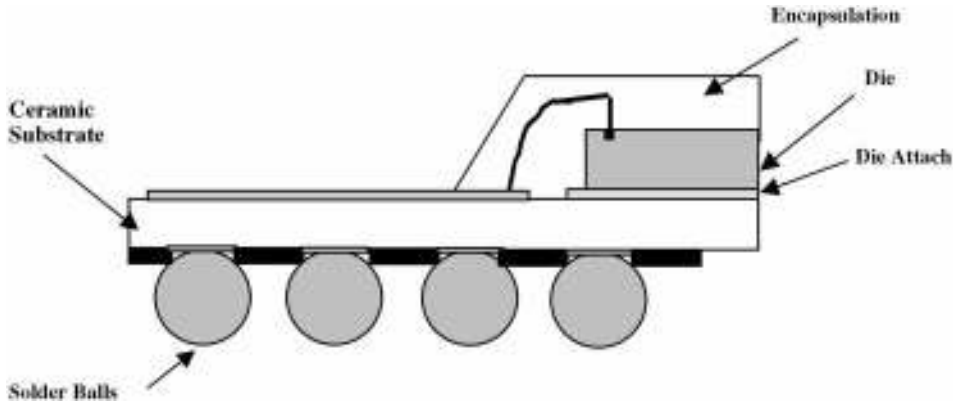


Figure 10.44 CBGA cross section.

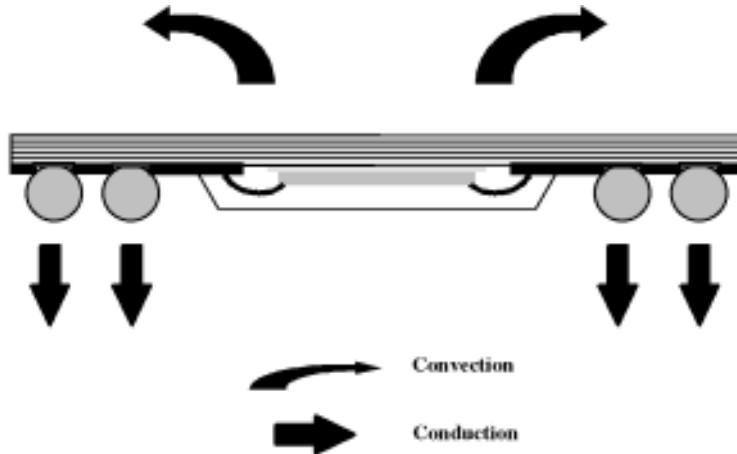


Figure 10.45 Heat paths in CBGA.

There are two heat paths for chip-scale packages: conduction through the balls to the circuit card and convection to the air as shown in Fig. 10.47. The conductive heat path is limited by the presence of a low-thermal-conductivity polyimide film and the limited cross-sectional area of the solder balls.

Some circuit card assemblers have gone to a underfill material between the CSP and the circuit card to help reduce the stresses.

For high-density packaging applications, some physical designers have eliminated the package and placed the chips directly on a board or substrate. To protect the chip from the elements and handling, the chips are encapsulated. This packaging technology is known as chip-on-board (COB). A cross section of a die in a COB application is shown in Fig. 10.48. The die is mounted with a polymeric material directly to the board, typically a printed circuit card, and then wire bonded. All of the semiconductors are then encapsulated with a potting material such as FP4401.

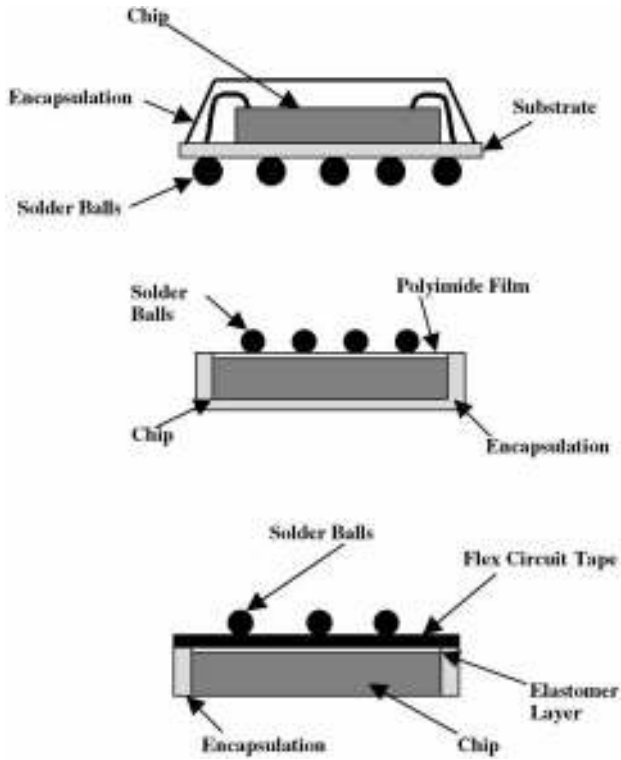


Figure 10.46 Chip-scale package (CSP) cross sections.

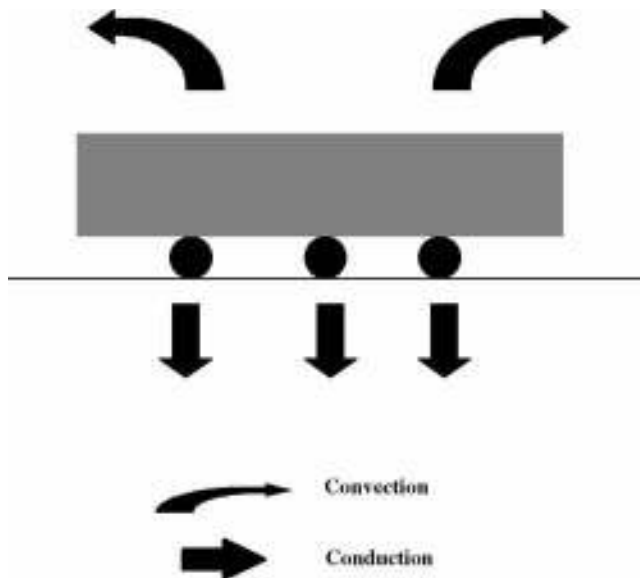
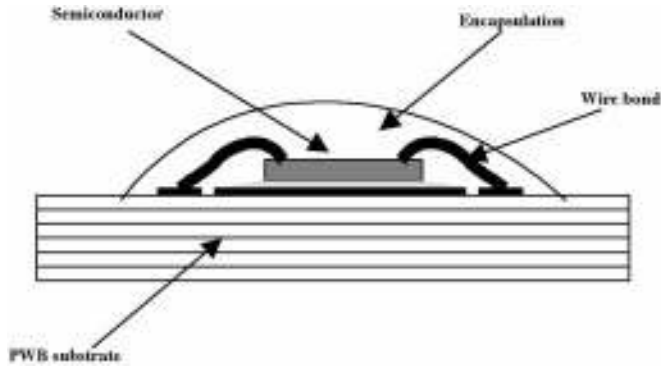
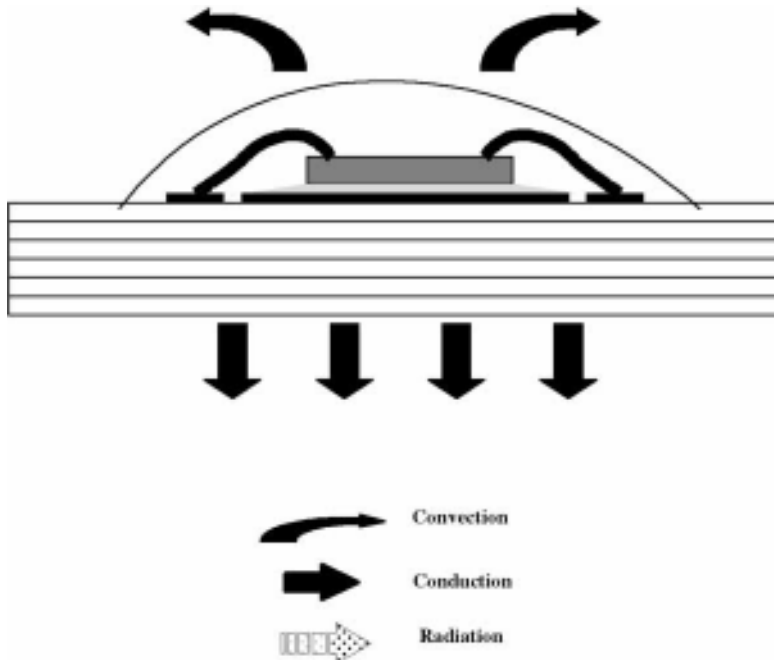


Figure 10.47 CSP heat paths.



**Figure 10.48** Chip-on-board (COB).

In COB, there are two heat paths from the semiconductor as shown in Fig. 10.49. The first and prime path is from the die to the circuit card through the die attach material. The second is from the die through the encapsulation material to the air. The potting materials, with thermal conductivities in the range of 0.4 to 1.0 W/m-K, have an insignificant effect on the heat transfer. By not using a package, there is one less thermal resistance in the heat path. However, the board or circuit card used as the substrate has a thermal conductivity in the range of 0.1 to 0.3 W/m-K, which is two orders of magnitude



**Figure 10.49** Heat paths in COB.

lower than the 21 W/m-K conductivity of 96 percent alumina. The resulting thermal resistance of the COB assembly may be higher, and techniques for reducing it may be required.

In one version of COB, chips are attached to a ceramic substrate and then encapsulated. This method has a significantly lower thermal resistance than the organic-based boards.

An alternative die attach method for COB is flip-chip. The heat path from die goes through the solder balls into the circuit card. The heat path through the potting material is also small for flip-chip attach.

**10.5.5.2 Hermetic packages.** For high-reliability and severe-environment applications, hermetic packages with either ceramic or metal bases are used. Cross-sectional views of various hermetic packages are shown in Fig. 10.50. The prime heat path in a hermetic package is conduction through the base. A secondary but very minor heat path is convection. The base in a hermetic package is the key material in determining the thermal resistance of the packaged semiconductor(s). The base material, which can be either ceramic or metal, is discussed below.

The most commonly used ceramic package material is cofired 92 percent alumina with a thermal conductivity of 17 W/m-K. The die is attached to the base of the package with a polymeric material, silver-glass, or some type of solder. To reduce the thermal resistance, the package designer can make use of filled thermal vias in the ceramic base. Equations for modeling the thermal resistance in substrates with vias can be found in Sec. 10.5.7, with the thermal conductivities of the board material changed to 17 W/m-K and the via fill material changed to 130 W/m-K for tungsten.<sup>19</sup>

In high-performance ceramic packages, the base may be a higher-thermal-conductivity material such as beryllium oxide or aluminum nitride with a metal ring frame made from a material such as Kovar.

The thermal properties of the various ceramic materials used for hermetic packages, the same as those for substrates, are listed in Tables 10.8 and 10.10.

To aid the heat spreading in an alumina package, the package designer can use a heat spreader such as copper-tungsten as shown in Fig. 10.51. Copper-tungsten is used because it has a high thermal conductivity (approximately 180 W/m-K, depending on composition) and a CTE in the 7 to 8 ppm/°C range that matches alumina. If the die needs to be electrical isolated, the heat spreader is brazed to the ceramic base. For applications wherein the die can be electrically connected to the package base, the die can sit on a copper-tungsten plug as shown in Fig. 10.52. This plug is brazed into a cavity in the package and offers improved thermal conductivity over the isolated heat spreader.

Low-temperature cofired ceramic (LTCC) can also be used as a hermetic package. The base of the package is fabricated in the manner described in Sec. 10.5.3.4 with a Kovar ring frame/seal ring attached with solder as shown in Fig. 10.53. The same thermal resistance improvement techniques discussed previously for LTCC substrates can be applied to the LTCC package.

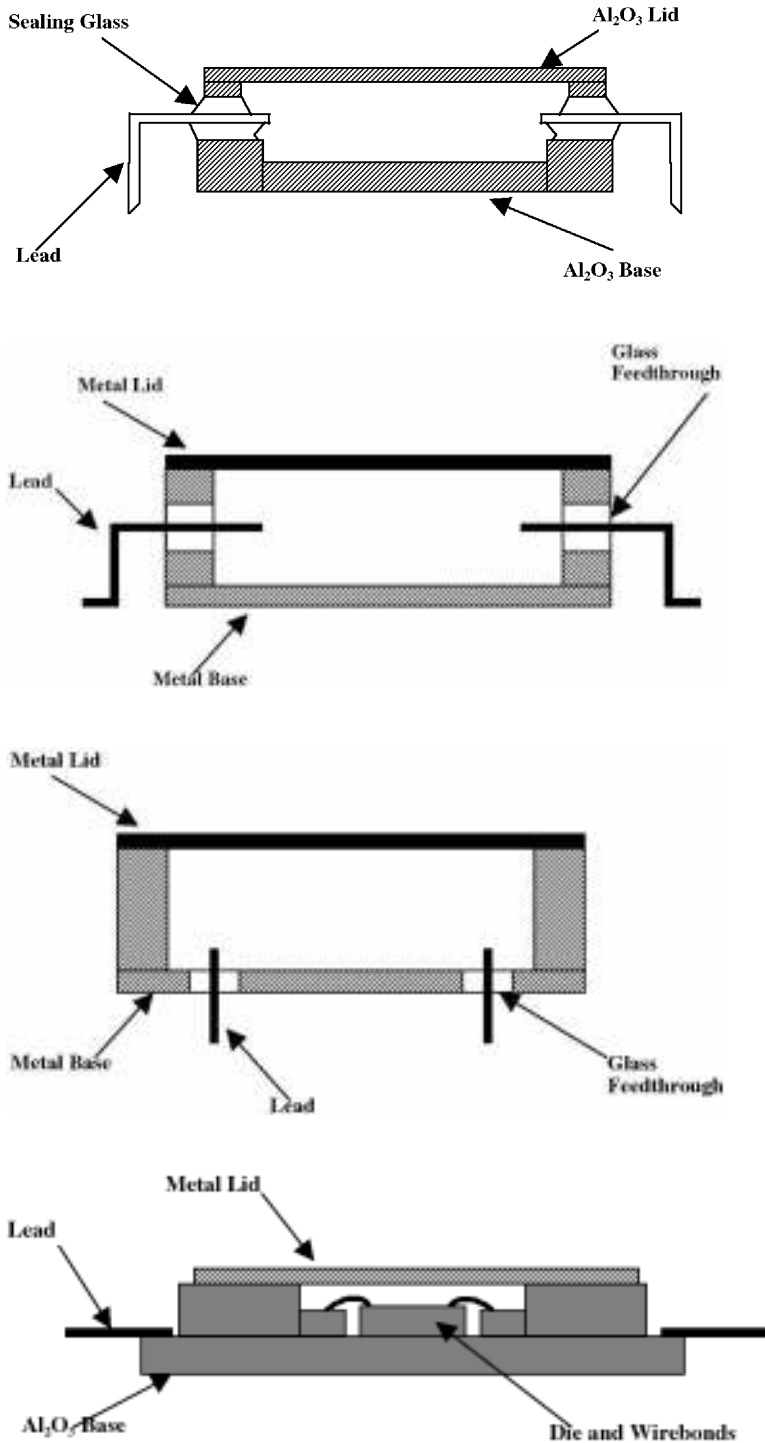


Figure 10.50 Cross-sectional views of hermetic packages.



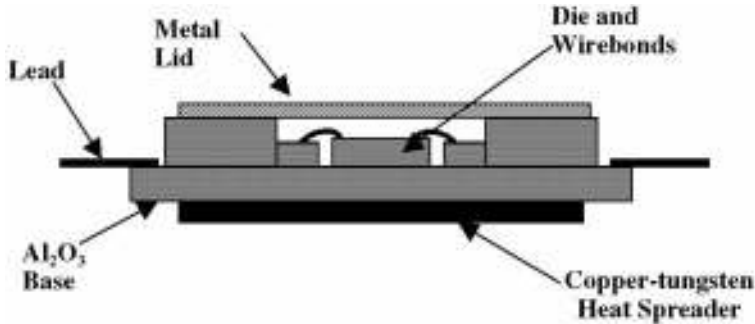


Figure 10.51 Ceramic package with copper-tungsten heat spreader.

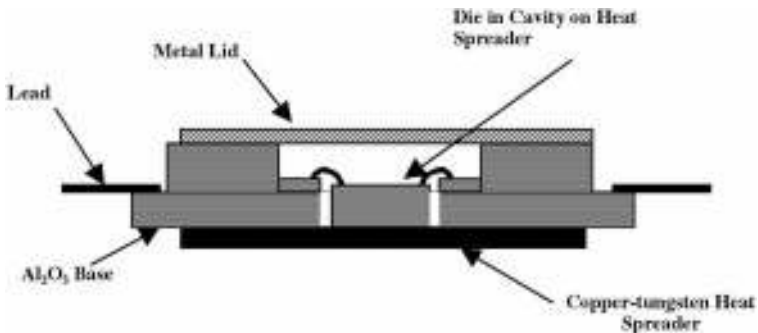


Figure 10.52 Direct chip attach to copper tungsten base of ceramic package.

Metal packages employing glass-to-metal feedthroughs are widely used for single-chip and multichip applications with low I/O counts. The density of glass-to-metal feedthroughs is typically limited to lead pitches of 0.050 in because of glass cracking. Kovar and steel packages are typically used for low-power applications. For high-power applications, materials such as copper, copper-tungsten, molybdenum, Silvar<sup>TM</sup>, and aluminum-silicon carbide are used for the package base.

Kovar, an alloy of 54 percent iron, 29 percent nickel, and 17 percent cobalt,<sup>80</sup> has a CTE at 25°C of 5.5 ppm/°C that closely matches alumina, beryllia, and aluminum nitride.<sup>12</sup> It is also known as ASTM F-15 alloy and is used as a package base in single-chip and multichip (hybrid and MCM) applications in which there are low power densities. When used with certain types of glass as feedthroughs on packages, it forms a hermetic molecular bond. A plot of the CTE of Kovar over a wide temperature range is shown in Fig. 10.54.

The thermal conductivity of Kovar, 16.5 W/m-K at 30°C and 17.6 W/m-K at 100°C,<sup>12</sup> is considered low, so Kovar should be avoided as a package base in high-power-density applications.

The thermal properties of the various metals used for package bases are listed in Table 10.17. Table 10.18 lists the properties of metal composite materials used for package bases.

**TABLE 10.17 Thermal Properties of Metals Used for Package Bases and Printed Circuit Card Cores<sup>12,13</sup>**

Material	Thermal conductivity @25°C (W/m-K)	Thermal conductivity @100°C (W/m-K)	CTE @25°C (ppm/°C)
Kovar	16.5	17.6	5.5
OFHC copper	401	395	16.5
Glidcop	365		16.6
Alloy 52	14		10.0–10.5
Molybdenum	138		5.35
Aluminum	237	238	23.2

**TABLE 10.18 Properties of Composite Materials<sup>87-91</sup>**

Composite material	Composition	Thermal conductivity @25°C (W/m-K)	Thermal conductivity @100°C (W/m-K)	CTE (ppm/°C)	Vendor P/N
CuW	80 W, 20 Cu	185	197	8.3	
	82 W, 18 Cu	185		7.8	
	85 W, 15 Cu	180	183	7.2	
	87 W, 13 Cu	175		6.9	
	90 W, 10 Cu	170	176	6.5	
Silvar	61 Invar, 39 Ag	153		6.5	
	72 Kovar, 28 Ag	110		7.0	
AlSiC	30-70 SiC, balance Al	160–220		6.2–15	
Al-Be	62 Al, 38 Be	212	195	13.2	AlBeMet AM162
Al-graphite		230 x & y 120 z		3.0-5.0 x & y 24 + z	MMCC GA 4-230
		200 x & y 125 z		6.5–9.5 x & y 24 + z	MMCC GA 7-200
Cu-graphite		300 x & y 200z		7.4	
Cu-Mo	20 Cu, 80 Mo	170		8.0	
	15 Cu, 85 Mo	160		7.0	

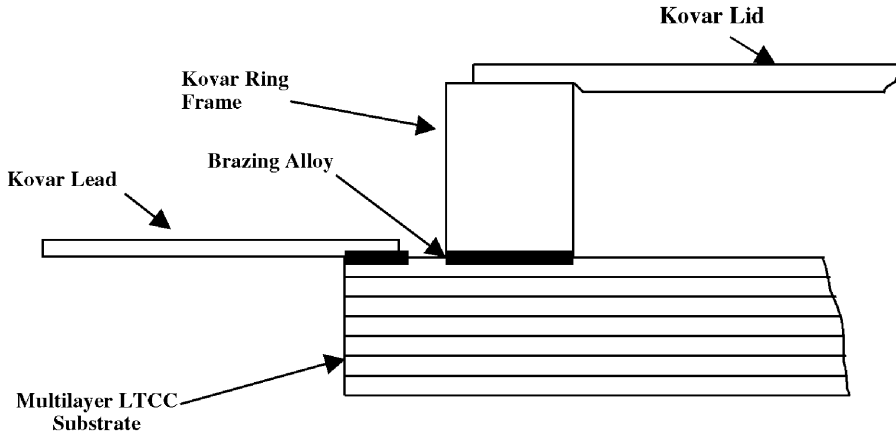


Figure 10.53 Hermetic LTCC package construction.

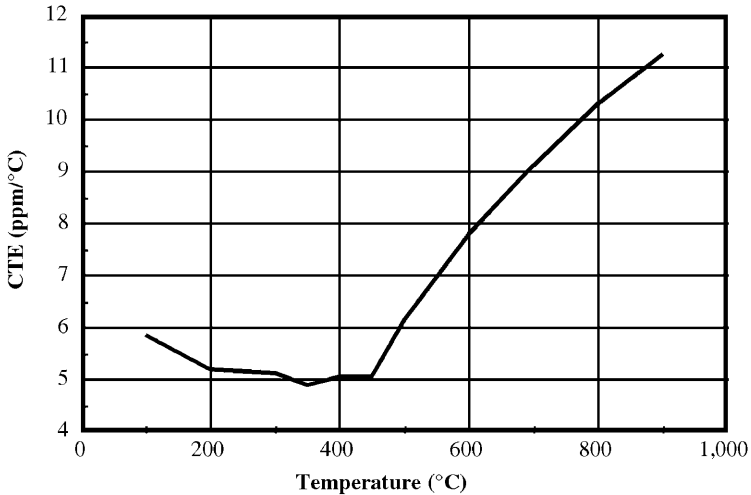


Figure 10.54 CTE of Kovar.

Pure or elemental copper, also known as oxygen-free high-conductivity copper (OFHC), having a thermal conductivity of 401 W/m-K, is ideal from a heat transfer standpoint for a package base. However, with its high CTE of 16.5 ppm/°C,<sup>12</sup> copper can introduce stresses into rigidly attached ceramic substrates. To reduce the stresses in ceramic substrates, the physical designer can partition the layout so that several smaller substrates are used instead of one large one. An example of a power hybrid with a copper package and multiple substrates is shown in Fig. 10.55. OFHC copper has the second-lowest resistivity of the elements, 1.72  $\mu\Omega\text{-cm}$ , second only to silver, at 1.59  $\mu\Omega\text{-cm}$ .<sup>65</sup>

Pure copper has a low annealing point as shown in Fig. 10.56. Package bases made from pure copper exhibit softening that can result in cracked die and/or substrates. To raise the annealing point of the copper, manufacturers

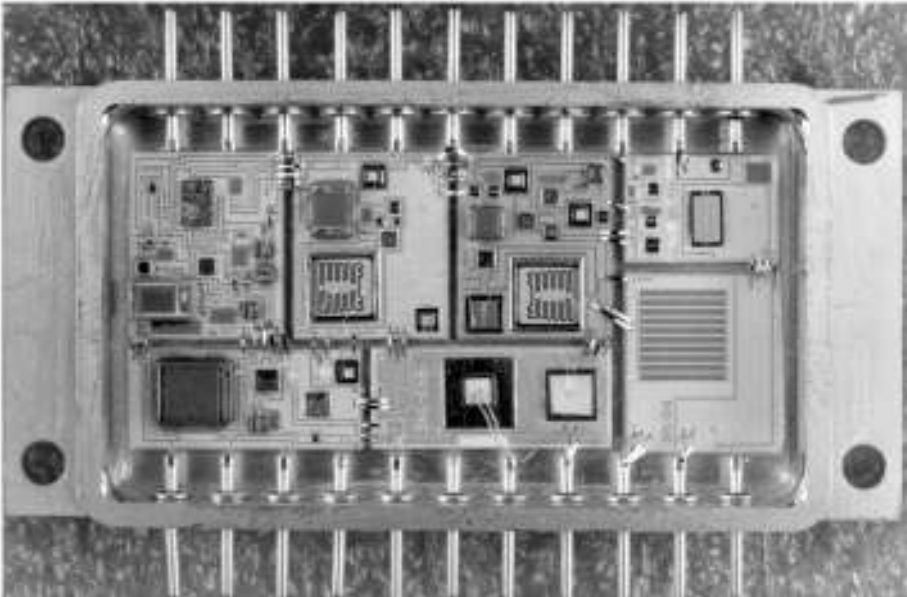


Figure 10.55 Multiple substrates in a copper package.

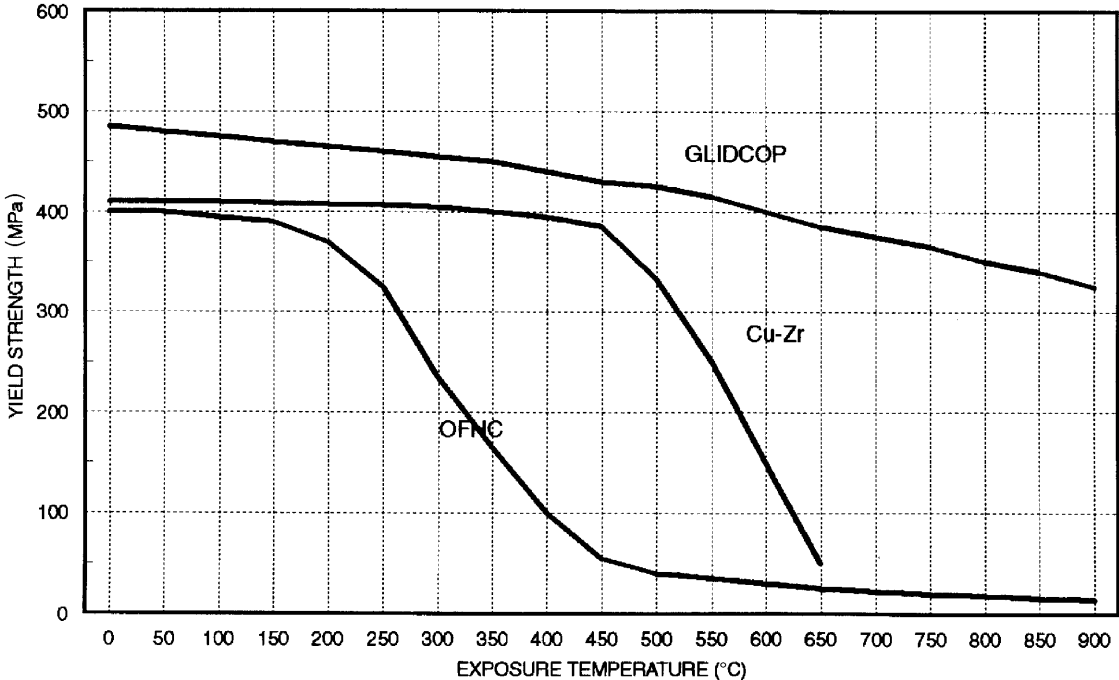


Figure 10.56 Yield strengths of OFHC copper, Glidcop, and zirconium copper.

typically incorporate a small amount of material such as alumina, zirconium, silver, or silicon in the melt. This material has the effect of raising the annealing point of OFHC copper from 320 to 400°C with only slight losses in thermal and electrical conductivity. One such material, Glidcop®\* is composed of 99.7 percent copper and 0.3 percent alumina. With the addition of the alumina, the thermal conductivity is reduced to 365 W/m-K, and its electrical resistivity is increased to 1.85 mW-cm.<sup>13</sup> The yield strengths of Glidcop and zirconium-copper are shown in Fig. 10.56, along with OFHC copper.

Because of its ease of machinability, aluminum and its alloys are typically used as housings on microwave integrated circuits (MICs). Elemental aluminum has a high thermal conductivity of 237 W/m-K at 25°C. However, the CTE of aluminum is high, at 23.2 ppm/°C.<sup>12</sup> To alleviate this problem, physical designers typically use many small substrates in lieu of one large one in a manner similar to the hybrid shown in Fig. 10.9. The thermal properties of aluminum are listed in Table 10.17.

Stainless steel is used for hermetic packages wherein corrosion resistance is required. One such application is implantable medical electronics. To achieve hermetic leads in stainless steel, compression seals are used, because fused glass-to-metal seals cannot be formed. There are a variety of formulations for stainless steel. One formulation, designated 1010 steel, has a thermal conductivity of 49.8 W/m-K, approximately three times that of Kovar. The CTE of 12.6 ppm/°C poses a thermal mismatch with ceramics and semiconductors. Another stainless steel, Type 430, has a much lower thermal conductivity of 26.1 W/m-K.<sup>19</sup>

Molybdenum is used for bases on hermetic packages in conjunction with Kovar ring frames. Having a CTE of 5.35 ppm/°C, molybdenum closely matches the CTE of Kovar and alumina. Its thermal conductivity of 138 W/m-K is reasonably high and can be used for many medium and high-power-density applications.<sup>13</sup> One major drawback of molybdenum bases is that the best flatness available is 0.002 inch per inch. Another issue is the brittleness of the molybdenum after it has been recrystallized.

Composites are a combination of materials that are not alloyed and have properties that none of the constituent materials has by itself. The materials are selected for use in a composite to take advantage of one or more characteristic properties of the individual material. For example, copper has both high thermal conductivity and high CTE. The high thermal conductivity is the desired property, but a lower CTE would be welcomed. Combining 80 to 90 percent tungsten with copper produces a material with a CTE matching ceramics and Kovar.<sup>92</sup> In some applications, weight is the parameter that needs to be minimized. To achieve low weight in a package, the materials need to have low densities. Aluminum-silicon-carbide is a composite that offers low weight and a tailored CTE.

Many composite materials tend to be anisotropic; i.e., they have properties that differ according to the direction of measurement. The thermal conductivi-

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\* Glidcop is a registered trademark of SCM Metal Products.

ties of various composite materials used for package bases are listed in Table 10.18 with a notation for the thermal conductivity and expansion values in each of the planes.

Several composites, such as aluminum-silicon-carbide, copper-molybdenum, and copper-graphite, are used for bases in hermetic packages. These materials and others, such as aluminum-graphite and copper-Invar-copper, are also used as cores for circuit cards, as discussed in Sec. 10.5.7.

To alleviate the CTE mismatch between ceramic substrates and copper package bases, some package manufacturers are using a composite of copper and tungsten. An 85 percent tungsten, 15 percent copper composite has a CTE of 7.2 ppm/°C and a thermal conductivity of 180 W/m-K. Other combinations of copper and tungsten are available and are tabulated in Table 10.18. Copper-tungsten is used in a variety of ways in electronic packaging. It is used as a package base, as a heat sink, and also as a heat spreader. One major disadvantage of copper-tungsten is its high density, a result of the high percentage of tungsten. The 85-15 copper-tungsten material has a density of 16.1 gm/cm<sup>3</sup>.<sup>87</sup>

Copper-tungsten is also used as a heat sink for substrates in nonhermetic applications. As discussed in Sec. 10.5.5.2.1, copper-tungsten is used as a base on hermetic ceramic packages or as a heat spreader.

Because of its high density, copper-tungsten provides excellent radiation shielding for total ionizing dose (TID) environments. If aluminum were used for a radiation shield, it would have to be 16 times as thick as a copper-tungsten to obtain the same amount of shielding.

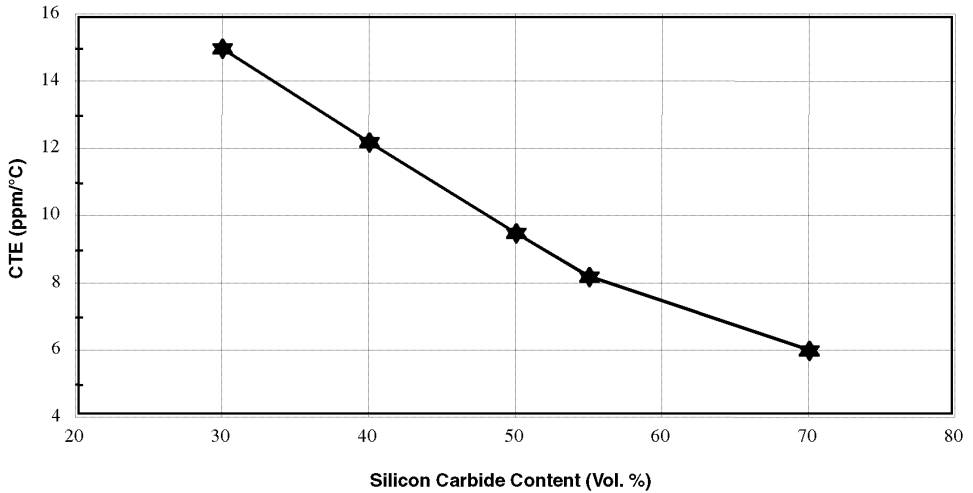
Silvar\* is a powder metallurgical composite of silver and an iron-based alloy. One version of Silvar uses 61 percent Invar 36<sup>†</sup> and 39 percent silver. Invar 36 is a low-expansion alloy of 63 percent iron, 39 percent nickel, and traces of carbon, manganese, and silicon. This isotropic controlled composite of silver and Invar has a CTE of 6.5 ppm/°C and a thermal conductivity of 153 W/m-K. Another version of Silvar is composed of 72 percent Kovar and 28 percent silver, which has a CTE of 7ppm/°C and a thermal conductivity of 110 W/m-K.<sup>93,94</sup>

Silvar is manufactured in a variety of methods, including liquid metal sintering, coblending, hot isostatic pressing, and liquid metal infiltration. It can be easily stamped, machined, or formed and is able to be brazed or soldered without the need for prior electroplating.

Aluminum-silicon-carbide (AlSiC) is a metal matrix composite (MMC) consisting of 30 to 70 percent silicon carbide and aluminum for the balance. It can be fabricated in a number of ways, including compocasting, high-pressure casting, pressureless infiltration, and powder metallurgy. The resulting AlSiC material consists of aluminum alloys with suspended silicon carbide particles. The CTE of AlSiC is tailorable, based on the percentages of the constituent materials. As shown in Fig. 10.57, increasing the silicon carbide content has the effect of lowering the CTE from elemental aluminum's high 23.2 ppm/°C.

\* Silvar is a trademark of Engineered Materials Solutions, Inc.

† Invar 36 is a registered trademark of Carpenter Technology Corp.



**Figure 10.57** CTE of aluminum-silicon-carbide as a function of silicon carbide content.

Varying the silicon carbide content has minimal effect on tailoring the thermal conductivity, as silicon carbide has a thermal conductivity of 110 W/m-K whereas elemental aluminum has a value of 237 W/m-K. AlSiC, with 70 percent silicon carbide, has a thermal conductivity of 170 W/m-K.<sup>3,12,13</sup>

The weight of AlSiC is a result of the low densities of both aluminum and silicon carbide. Seventy percent silicon carbide AlSiC has a density of 2.79 g/cm<sup>3</sup>.<sup>95</sup> AlSiC can be used as a base for a hermetic package or a heat sink, or as a heat spreader.

Mixing copper and molybdenum in a ratio of 15:85 produces a composite with a CTE of 6.7 ppm/°C and a thermal conductivity of 160 W/m-K. There is a slight difference in thermal conductivity in the x- and y-planes as compared to the z-plane. For the copper-molybdenum mixture with 20 percent copper thickness per side, the thermal conductivity is 150 W/m-K in the x- and y-planes and 194 W/m-K in the z-plane. The CTE is an excellent match with ceramics, and the thermal conductivity is relatively high. The tailored CTE of copper-molybdenum allows the use of a Kovar ring frame. The CTEs for ratios other than 15:85 are listed in Table 10.18. Copper-molybdenum can be used as a base for a hermetic package or a heat sink, or as a heat spreader.

Carbon-fiber-reinforced copper is attractive for applications with high power densities, as the material offers higher thermal conductivities than tungsten or molybdenum, with CTEs that can be tailored to match any device type or substrate type. The thermal conductivity along the length of a carbon fiber is extremely high at 600 to 750 W/m-K. However, perpendicular to the length, the thermal conductivity is an order of magnitude lower at 51 to 59 W/m-K. The coefficient of expansion along the length of the fiber is  $-0.5$  ppm/°C and 8 ppm/°C perpendicular to the length. When used as a package base or as a heat spreader, carbon fiber is not very efficient in moving the heat from the device to the next level. However, it is extremely efficient in spreading the heat.

Instead of using carbon fiber in a continuous form, discontinuous fiber (randomly oriented pieces of fiber, approximately 10  $\mu\text{m}$  in length) provides a material with a thermal conductivity of 20 to 40 W/m-K in the y- and z-planes and 700 to 800 W/m-K in the x-plane. The CTE in the x-plane is  $-0.5$  ppm/ $^{\circ}\text{C}$  and 8 to 10 ppm/ $^{\circ}\text{C}$  perpendicular to the length.<sup>96</sup>

All of the above specifications apply for graphite alone. Mixing 51 percent unidirectional graphite with copper produces a material with a thermal conductivity of 494 W/m-K in plane and 128 W/m-K perpendicular to it.

Aluminum-graphite is a metal matrix composite of graphite fiber and aluminum. There are several types of this composite available, as shown in Table 10.18. One such material, GA 4-230 from Metal Matrix Composites Corporation (MMCC), has a CTE of 3.0 to 5.0 ppm/ $^{\circ}\text{C}$  from 20 to 300 $^{\circ}\text{C}$ . Its thermal conductivity in the x- and y-planes is quite high at 230 W/m-K. In the z-plane, its thermal conductivity decreases to 120 W/m-K.

As a result of the low densities of its component materials, aluminum-graphite has an extremely low overall density. For the MMCC GA 4-230, the density is quite low at 2.40 grams/cm<sup>3</sup>.<sup>89</sup>

Aluminum-beryllium (Al-Be) is by definition an alloy consisting of aluminum and beryllium. However, the industry treats it as a composite. Produced under the trade name of AlBeMet<sup>®</sup> by Brush Wellman, aluminum-beryllia is available as a sheet, plate, or bar with 20 to 75 weight percent beryllia in an aluminum matrix. At room temperature, a 62 percent beryllia/38 percent aluminum ratio produces a material with a CTE of 13.2 ppm/ $^{\circ}\text{C}$  and a thermal conductivity of 212 W/m-K. Having a density of 2.07 g/cm<sup>3</sup>, Al-Be is used for applications wherein low weight is required.

Because of its beryllium content, machining of Al-Be can cause health risks as described in Sec. 10.5.3.2. The cost of Al-Be is at least an order of magnitude higher than standard aluminum and its alloys because of material and machining costs. In addition to its use as a core for circuit cards, Al-Be is also used for chassis and housings.<sup>90</sup>

Clad materials are produced by high-pressure rolling of a foil onto a base metal and annealing the composite to form a solid-solution weld. By cladding high-CTE materials with lower-CTE materials, a composite with a tailorable CTE is achieved. In addition to the tailorable CTE, the thermal conductivities are changed. Using Eq. (10.26), the effective thermal conductivity of clad materials can be calculated. Two clad materials used in electronic packaging include copper-clad Invar and copper-clad molybdenum. The CTE and thermal conductivities of these materials are listed in Table 10.19.

**TABLE 10.19 Thermal Properties of Clad Materials Used for Packages and PCB Cores<sup>7</sup>**

Material	Composition	Thermal conductivity @25 $^{\circ}\text{C}$ (W/m-K)	CTE @25 $^{\circ}\text{C}$ (ppm/ $^{\circ}\text{C}$ )
Copper-Invar-copper	1 Cu, 3 Invar, 1 Cu	174 x & y, 24.8 z	6.5
Copper-molybdenum-copper	1 Cu, 6 Mo, 1 Cu	233	6.4



When Invar is clad with foils of copper on each side in the ratio of 1 part copper, 3 parts Invar, and 1 part copper as shown in Fig. 10.58, the resulting material has a CTE of 6.5 ppm/°C. The CTE for other combinations of copper and Invar is shown in Fig. 10.59. The thermal conductivity in the x- and y-planes for this 1:3:1 clad material is a high 174 W/m-K because of the high thermal conductivity of the copper. However, in the z-plane, the thermal conductivity is only 24.8 W/m-K because of the low thermal conductivity of the Invar in the center of the clad combination. The variation of thermal conductivity of copper-clad Invar in the various planes for different percentages of copper is shown in Fig. 10.60.<sup>19,80</sup>

The principal usage of Invar has been as a core on printed circuit cards, in which it tailors the equivalent CTE to a value that reasonably matches that of

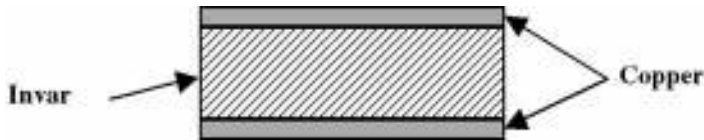


Figure 10.58 Copper-clad Invar construction.

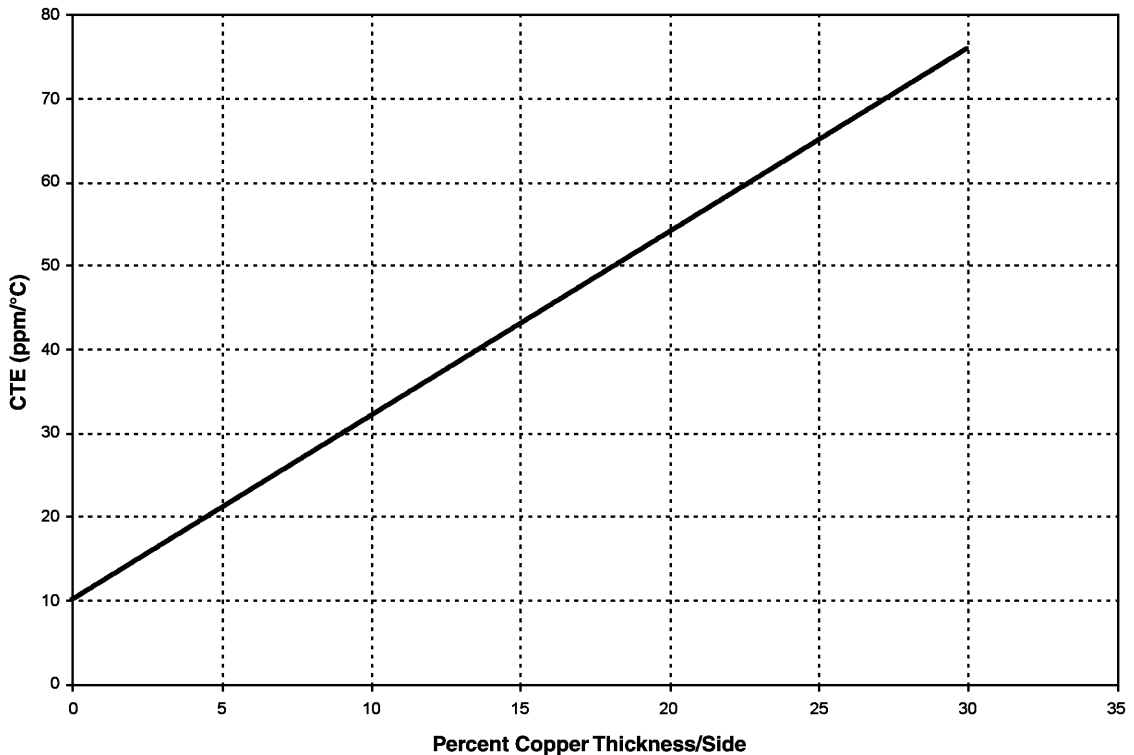


Figure 10.59 Copper-clad Invar CTE.

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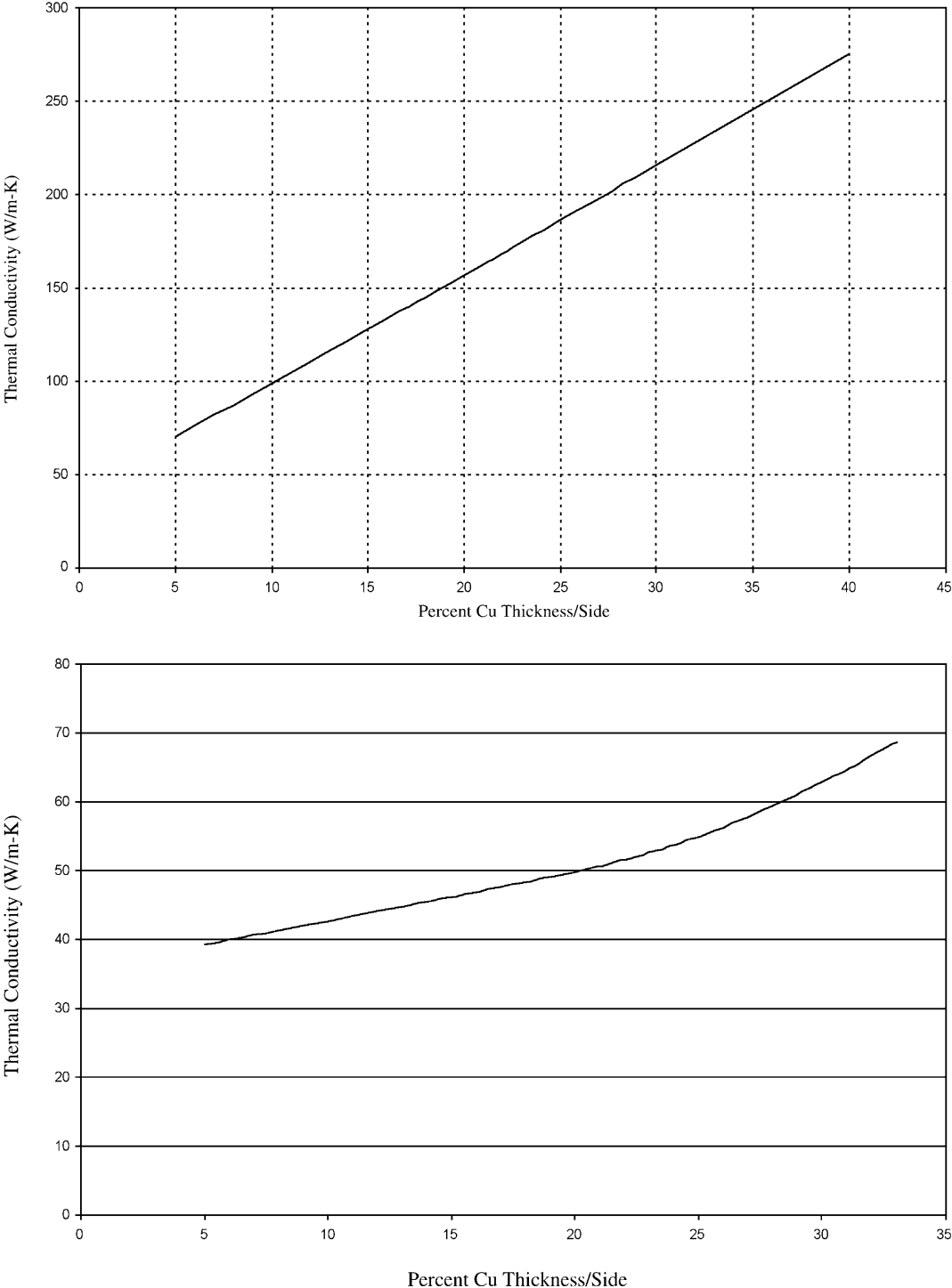


Figure 10.60 Copper-clad Invar thermal conductivity, (top) x- and y-planes and (bottom) z-plane.

ceramic packages. Copper-clad Invar can also be used as a base for hermetic packages.

By cladding molybdenum with copper in the ratio of 1:6:1 as shown in Fig. 10.61, the resulting laminate has a CTE of 6.4 ppm/°C, an excellent match with ceramics and with Kovar and alumina. The CTE for other combinations of copper and molybdenum is shown in Fig. 10.62. The effective thermal conductivity of the laminate is quite high at 233 W/m-K. The thermal conductivity of copper-clad molybdenum as a function of copper thickness is shown in Fig. 10.63. Package bases for hybrids and MCMs have been made with copper-clad molybdenum. Kovar ring frames can be attached reliably because of the close match in temperature coefficients. Copper-clad molybdenum suffers from the same shortcoming of pure molybdenum, i.e., minimum flatness of

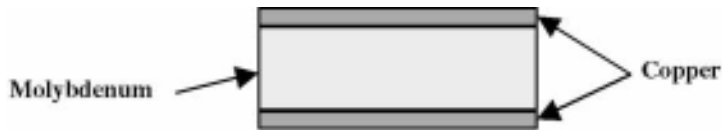


Figure 10.61 Copper-clad molybdenum construction.

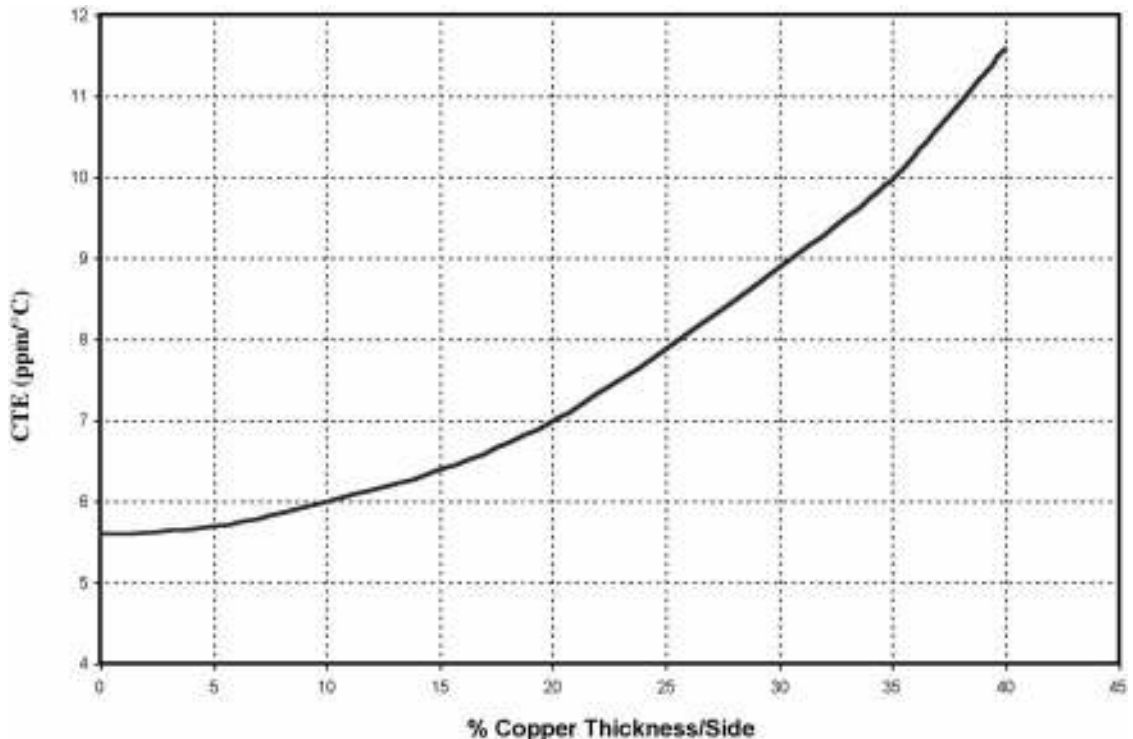


Figure 10.62 Copper-clad molybdenum CTE.

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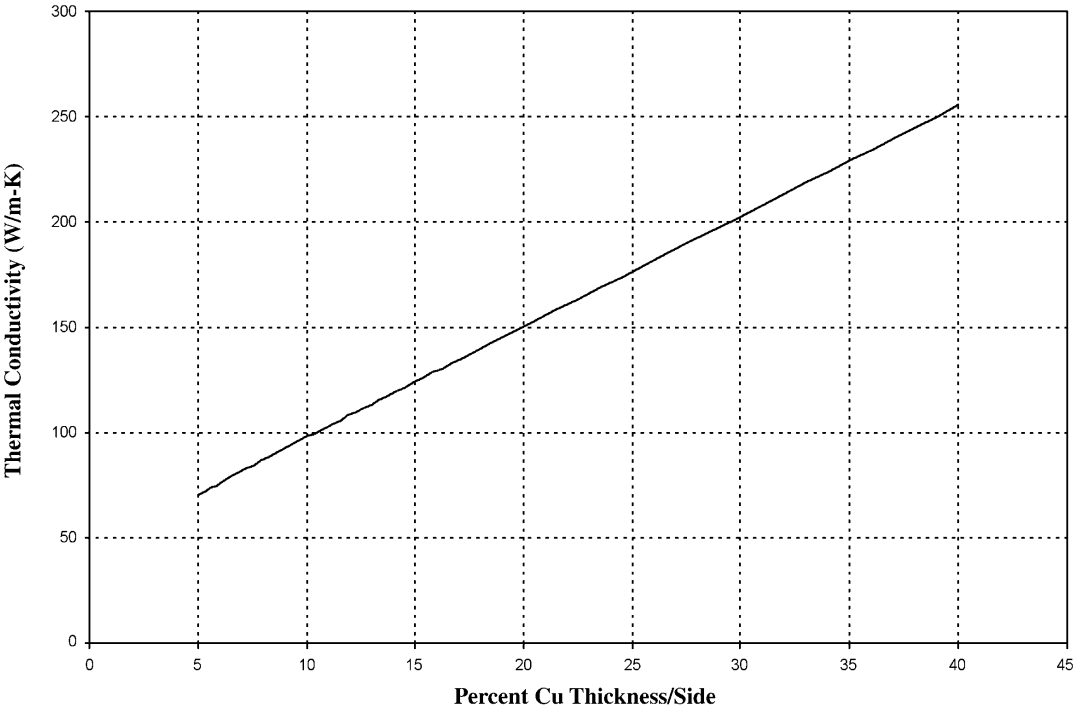
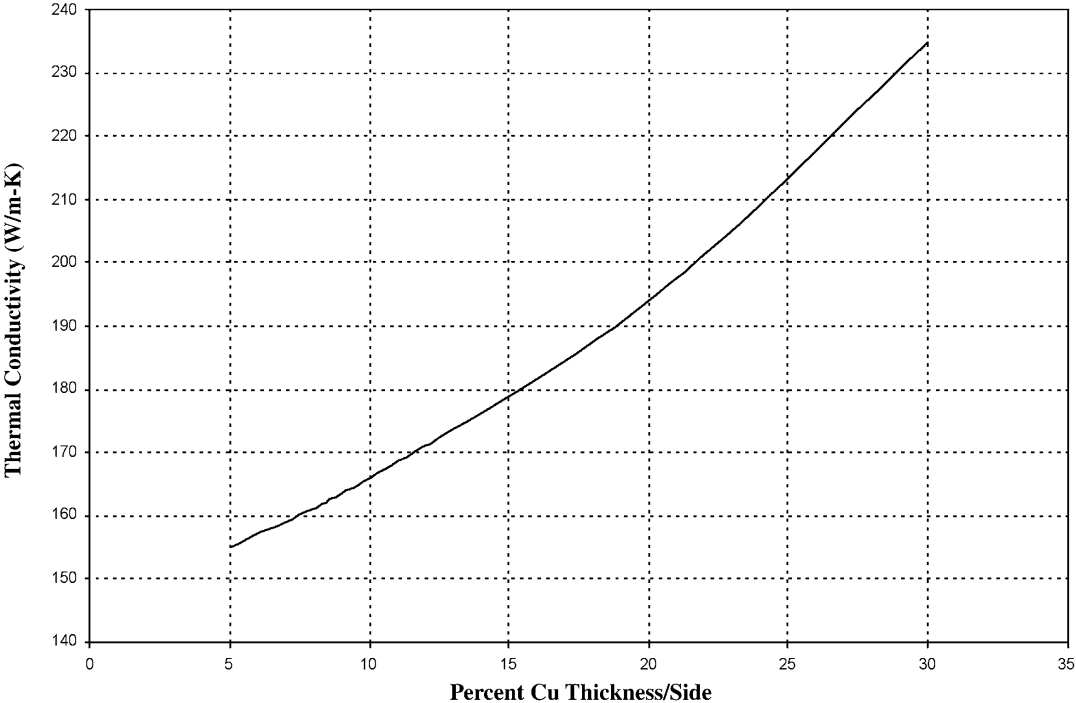


Figure 10.63 Copper-clad molybdenum thermal conductivity in x- and y-planes.

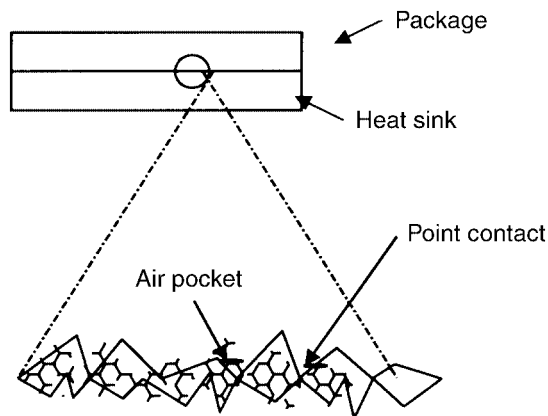
0.002 inch per inch. Copper-molybdenum-copper is also used as heat spreaders with various ceramic substrates and packages.

### 10.5.6 Thermal interface materials

Air, having a thermal conductivity of  $0.026 \text{ W/m-K}$ ,<sup>97</sup> is a very poor thermal conductor and must be eliminated from the thermal path from junction to heat sink. Every package type, covering all materials, is neither perfectly flat nor perfectly smooth. The portion of a heat sink that interfaces with the electronic package is also not perfectly flat or smooth. At the microscopic level, the interface of the package to the heat sink consists of point-to-point contacts surrounding air pockets as shown in Fig. 10.64. DeSorgo<sup>97</sup> claims that as much as 99 percent of the surfaces between heat sinks and dissipating devices are separated by air. Because circuit card assemblies act as a heat sink to some extent, they will be considered as a heat sink in this discussion. To minimize the thermal resistance caused by the nonsmooth surfaces and the resulting air pockets, several techniques are available. One technique is to apply mechanical pressure to smooth out the interface. This works to some degree when soft metals are used. However, the pressure required to produce an acceptable thermal condition may exceed the materials' strength and produce a degradation or failure.

Another technique of eliminating the gaps is to fill them with a material with high thermal conductivity. Materials used for gap filling include solder, thermal grease, elastomeric pads, conductive adhesives, polyimide films, phase change materials, mica pads, adhesive tapes, polyimide films, and ceramic wafers. Their properties of the various interface materials used are summarized in Table 10.20.

**10.5.6.1 Solder.** Solder can be used in two different manners to fill the air gaps in the heat sink attachment interface. In the first, solder is reflowed be-



**Figure 10.64** Microscopic view of package-to-heat-sink interface.

**TABLE 10.20 Thermal Properties of Interface Materials**<sup>5,25,29,82,98–100</sup>

Material	Typical thickness (in)	Thermal conductivity (W/m-K)	Dielectric strength (V)
Thermal grease	0.003	0.7	
Sn 63	0.005	50	na
Mica	0.002–0.003	0.71	
Phase change	0.002	4	3900
Elastomer	0.010	6	4000
Gap filler	0.010	1.5	4000
Epoxy film	0.003	6.5	na
Diamond-filled epoxy	0.005	11.6	>2250
Underfill	0.005	0.25–1.1	
Polymeric fiber		30	
Adhesive tape	0.002–0.015	0.6	
Ceramic wafers			
Alumina wafer	0.015–0.060	25	>9000
Aluminum nitride wafer	0.015–0.060	170	>9000
Beryllia wafer	0.015–0.060	217	>11,500
Polyimide film		0.15	

tween the device and the heat sink. Typically, the solder used is lead-tin, which has a thermal conductivity of 51 W/m-°C.<sup>13</sup> This provides several orders of magnitude improvement over the air gap. However, the use of reflow-solder attach may cause other problems.

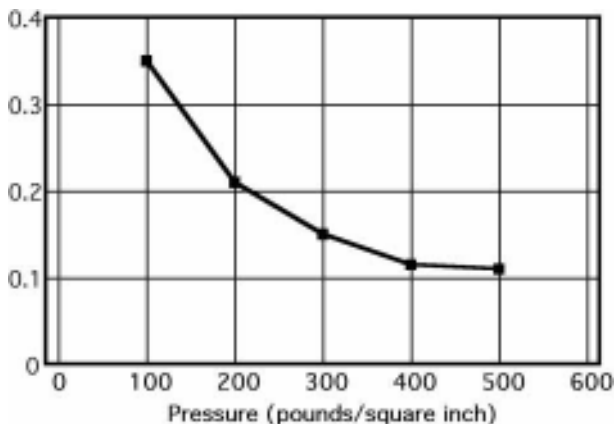
- The solder reflow temperature may exceed the device's maximum temperature.
- There may be trapped flux that also produces voids.
- The device and heat sink may have large CTE differences, and this could result in bowing or cracking of either the heat sink or the device.

The second way solder can be used to fill gaps is to use a pre cut sheet of solder (a preform) between the device and the heat sink. By applying mechanical pressure, the solder, having a high lead content, compresses easily and fills the gaps. This technique avoids all of the shortcomings addressed for the reflowed solder. The only shortcoming of using the preform technique is that the compressed thickness is typically higher than with reflow soldering.

**10.5.6.2 Thermal grease.** Thermal grease uses silicone or hydrocarbon oil as a base and is filled with a thermally conductive material, which may range from aluminum oxide and zinc oxide powder to CVD diamond. The resulting thermal resistance is a function of the particle size of the filler material and the thermal conductivity of the filler and vehicle. Larger particles may result in a larger bond thickness and a higher thermal resistance. The typical thermal grease used in production has a thermal conductivity of approximately 1.0 W/m-K. Some newer greases have improved this to as high as 16.0 W/m-K.<sup>97,101</sup>

Thermal greases are somewhat volatile and may evaporate over time. Because these greases do not provide adhesion, some form of mechanical attachment is necessary to apply sufficient pressure and minimize bond thickness. Care in the application of silicon-based greases is required, as they can contaminate solder areas. It should be noted that thermal grease does not provide electrical insulation.

**10.5.6.3 Elastomers.** Elastomers are electrically insulating materials, usually in the form of silicone rubber pads, ranging in thickness from 0.001 to 0.20 in and filled with high thermal conductivity materials such as boron nitride and alumina. They are easier to handle than the thermal grease, but they require a higher mechanical pressure to completely fill the voids. Figure 10.65 shows how the thermal impedance of an elastomeric pad varies with applied pressure. Depending on their formulation, elastomers have thermal conductivities in the range of 1 to 6 W/m-K. Typical pressures used in device attachment to heat sinks and circuit card assemblies range from as low as 10 psi to over 400 psi. The use of excessive pressure can create detrimental stresses. For example, delicate leads and solder joints can be broken as a result of excessive pressure. While resilient, these elastomers have a fixed amount of material, which limits the minimum bond thickness. As a result, the thermal resistance of elastomers used as a gap filler is higher.



**Figure 10.65** Thermal resistance vs. pressure for an elastomer pad.

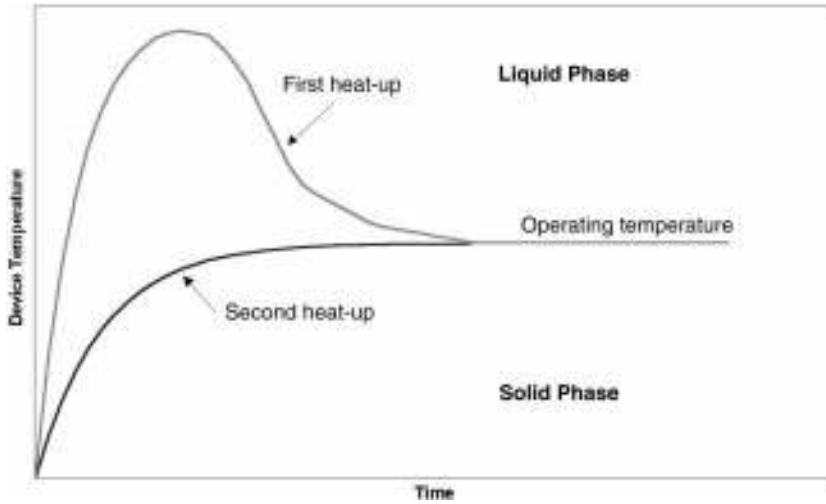
When there is a large space in the thermal path, a special elastomer called a *gap filler* is used for filling it and lowering the thermal resistance. This material ranges in thickness from 0.02 to >0.20 in. The thermal conductivity is in the order of 3 W/m-K. A special feature of gap fillers is their elasticity, which allows them to return to their original thickness when the pressure is released. This is useful in the manufacturing process and facilitates rework. Because of their high elasticity, gap fillers eliminate stresses in mounting.<sup>102</sup>

**10.5.6.4 Thermally conductive adhesives.** Thermally conductive adhesives may be filled with high-thermal-conductivity materials such as boron nitride, ceramic, or CVD diamond and provide adhesion between the package and the heat sink. These adhesives may be electrically conducting or insulating, depending on the application. Table 10.20 lists some thermally conductive adhesives used for device attachment to heat sinks and circuit card assemblies. The selection of the adhesive depends on its thermal conductivity, its electrical insulation if required, its thickness, and its curing profile. The use of an adhesive with a high temperature cure, i.e., greater than 150°C, may cause damage to the circuit card or to other components. The goal in using an adhesive to attach the heat sink is to have as thin a bond line as possible so that the lowest overall thermal resistance is obtained. These adhesives are available as one of two types: liquid (paste) or in a preform (tape or precut sheet). The latter can be as thin as 0.003 in, and the liquid types can be applied as thin as 0.001 in. Liquid materials can provide the lowest bond line thickness, but they may be difficult to control. The thickness for the tape, while always greater than the liquid's, is fixed.<sup>29,30,103</sup>

**10.5.6.5 Phase-change materials.** Phase-change materials are compounds that are coated onto carrier materials or substrates, both electrical insulating and conductive, and then placed between the heat-producing part and the heat sink or circuit card assembly. The materials are placed under pressure and subsequently heated externally or self-heated to the material's melting temperature, at which they soften and fill all of the interstitial voids between the parts and the heat sink. Figure 10.66 shows the relationship of device temperature versus time when phase-change materials are used. When the part is turned on for the first time, the initial thermal resistance of the phase-change material is high, allowing the part to self-heat briefly to a higher-than-normal operating temperature. This changes the phase change material from a solid to a flowable form at which it wets the interface between the part and the heat sink (or circuit card assembly) and fills all of the voids. After wetting, the part returns to normal operating temperature, and the phase change material returns to a solid state.

The chemical composition of the phase change material determines its melting point. Materials with phase change temperatures as low as 48°C and as high as 130°C are commercially available. The thermal conductivity of the phase change compound itself is in the range of 2 to 4 W/m-K. The overall





**Figure 10.66** Time and temperature relationship for phase-change interface material.

thermal conductivity of the phase change material and its carrier material is highly dependent on the thermal conductivity of the carrier material. When the carrier is fiberglass or polyimide ( $K = 0.15 \text{ W/m-K}$ ), the thermal conductivity is low ( $2.7 \text{ W/m-K}$ ). The effective thermal conductivity of the aluminum-based phase change material is  $112 \text{ W/m-K}$  for a 0.002-in carrier.

Phase-change materials come in sheets or precut to sizes that range from 0.002 to 0.020 in thick. The dielectric strength of phase change materials depends on the thickness of the carrier material. When a 0.001-in thick polyimide carrier is used, its dielectric strength is  $3900 \text{ V}$ .<sup>29,30</sup>

**10.5.6.6 Mica.** Mica insulators have been used for many years for mounting power devices to heat sinks. Having a typical thickness of 0.002 to 0.003 in, they provide, in conjunction with thermal grease, a low-cost, electrically insulating method of reducing thermal resistance caused by interfacial air gaps. As stated in Sec. 10.5.6.2, the use of thermal grease can cause solder contamination problems. Other shortcomings of mica include its brittleness and inherent low thermal conductivity of  $0.75 \text{ W/m-K}$ .<sup>65</sup>

**10.5.6.7 Adhesive tape.** Thermally conductive adhesive tapes are double-sided, pressure-sensitive adhesive films filled with ceramic powder. The adhesive is typically supported either with a carrier made from polyimide film or with aluminum foil to provide ease of handling and strength. If electrical isolation is required, polyimide is the carrier used. These adhesive tapes act in a similar fashion to elastomeric films in that they require some initial mating pressure to conform to the surface irregularities. If the gap between the surfaces is too large, the adhesive tape is unable to fill it. Once a joint is formed

with an adhesive tape, mechanical pressure is no longer required to maintain the mechanical or thermal performance of the joint. From a manufacturing standpoint, adhesive tapes, unlike liquid or preform adhesives, do not require a cure cycle.<sup>97</sup>

**10.5.6.8 Polyimide films.** Polyimide films, in conjunction with wax or grease, are often used between power dissipating devices and the heat sink. Polyimide has a low thermal conductivity but excels as a result of its high dielectric strength and toughness.

**10.5.6.9 Ceramic wafers.** Ceramic wafer insulators made from alumina, beryllia, and aluminum nitride provide a high-thermal-conductivity (25 to 218 W/m-K), electrically insulating material for mounting devices to heat sinks. Their typical thickness ranges from 0.015 to 0.060 in. Like mica, they are brittle and crack easily. The cost of ceramic wafer insulators is considerably higher than mica.

To limit the thermal resistance introduced by the ceramic wafer that is used as a device interface, the thickness needs to be minimized. As the thickness of the interface material is increased, the voltage breakdown is also increased. Therefore, a trade-off between thermal resistance and voltage breakdown needs to be made. The voltage breakdown of the ceramics used for device interfacing is extremely high as shown in Table 10.21.

**TABLE 10.21 Voltage Breakdown of Ceramics Used for Thermal Interfaces<sup>5</sup>**

Material	Voltage breakdown (V/0.001 in)
Alumina	600
Beryllia	475
Aluminum nitride	600
LTCC	1000

**10.5.6.10 Underfill.** To reduce the stress in the attachment of BGAs and flip-chips to circuit cards, an organic material called *underfill* is typically injected between the substrate/die and the circuit card. Underfill material is composed of thermoset polymers and silica fillers. To match the CTE of a solder joint, which is 25 ppm/°C for eutectic solder (Sn 63), an underfill composition with approximately 65 percent silica filler is required. The underfill material has several purposes. It provides good adhesion between the substrate/die and the circuit card, absorbs the stresses between them, and provides some improvement in the thermal path. As noted earlier in this section on interface materials, air has an extremely poor thermal conductivity. Filling the air gap

between the device and the circuit card with a material having a higher thermal conductivity reduces the effective thermal resistance.<sup>84,104</sup> The thermal conductivity of underfill ranges from 0.25 to 1.1 W/m-K.

**10.5.6.11 Polymeric composite material (fiber).** A new thermal interface material, consisting of high-conductivity fibers combined with a wetting agent, is available from one supplier under the trademark GELVERT.<sup>100</sup> The thermal conductivity of this material is extremely high for interface materials—30 W/m-K. It fills in gaps as large as 0.03 inch under pressures ranging from 1 to 5 psi.

### 10.5.7 Printed wiring boards

Printed wiring boards (PWBs), also known as printed circuit cards, are used for two key purposes in electronic packaging: interconnection and heat transfer. Almost all electronic components are attached to circuit cards that can be grouped into two categories: rigid and flexible. The most common type of circuit card is the rigid PCB, which is fabricated with copper-clad dielectric materials. These dielectrics consist of a resin that is reinforced with a base fabric. The materials used for the fabric include epoxy-glass (e-glass), S2-glass, quartz, and Aramid fiber. The more commonly known name for Aramid fiber is Kevlar, a trade name of DuPont. Epoxy-glass is the most widely used fabric in PCB applications. The most common resins used are G-10 and FR-4. These resins have a glass transition temperature,  $T_g$ , in the range of 105 to 125°C. Polyimides are used as the resin when glass transition temperatures over 200°C are required. As shown in Table 10.14, polyimide resins also have lower CTEs than the epoxy glass resins.<sup>105</sup>

Rigid PCBs are available in a variety of configurations, including single-sided, double-sided, and multilayer. From a thermal management standpoint, the single-sided and double-sided PCBs can be grouped together. Their thermal resistance is directly proportional to the thermal conductivity of the resin material and the thickness of the resin. Table 10.14 lists the thermal conductivities of various PCB dielectric materials. Overall, these dielectrics have a poor thermal conductivity. In the multilayer PCBs, the designer typically uses power and ground planes. Made from layers of copper, these planes serve not only to provide low electrical impedance but also act as heat spreaders. The copper metallization can be as thin as 0.00017 in (1/8 oz/ft<sup>2</sup>). As the copper is made thicker, the amount of heat spreading is increased. Some circuit card manufacturers use copper as thick as 0.0067 in (5 oz/ft<sup>2</sup>).<sup>106</sup>

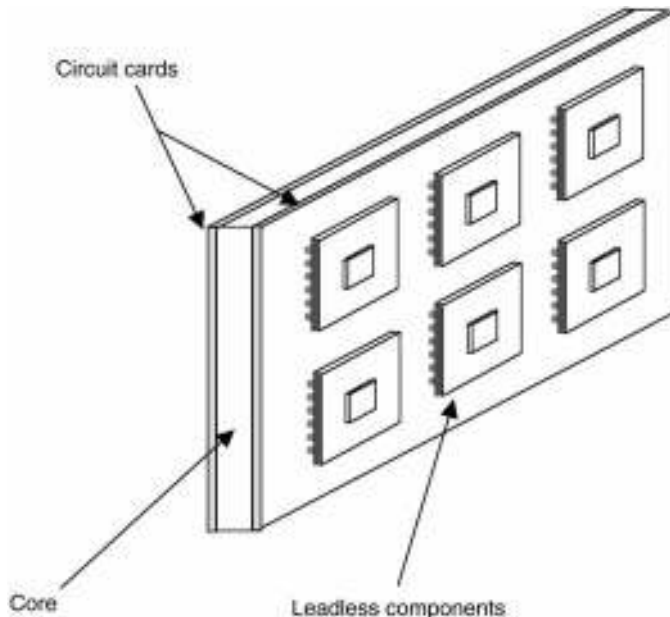
In some applications, the printed circuit board is attached to a metal core. This is done for two purposes: heat transfer and to restrain the CTE. For heat transfer, materials with high thermal conductivities, such as aluminum, copper, and various composites, are used. The thermal conductivities of various materials used for printed circuit card cards are listed in Tables 10.14 and 10.18. (Note that some of the same materials used for package bases are also used as cores for circuit cards.) The heat conducts from the component, through any interface material, and through the circuit card into the metal

core. The core then conducts the heat to the card rails. Figure 10.67 shows the construction of a circuit card with a metal core.

Printed circuit cards typically have CTEs in the range of 15 to 20 ppm/°C. When leadless devices such as ceramic ball grid arrays and ceramic chip carriers are used, the CTE of the printed circuit card needs to be reduced so that it is close to CTE of the component package and therefore does not lead to attachment failures. Placing a metal core with a low CTE between two circuit cards, as shown in Fig. 10.67, has the effect of constraining the effective CTE to that of the core. Although aluminum and copper have high thermal conductivities, they also have high CTEs. Therefore, they cannot be used for constraining the CTE. Composite and clad materials such as copper-graphite, aluminum-graphite, copper-Invar-copper, copper-molybdenum, and aluminum-silicon-carbide are used for circuit card cores. These materials offer both low CTE and high thermal conductivity.

Several PCB dielectric materials are suited for very high-frequency operation, typically above 1 GHz, because of their low dielectric constant and their loss tangents. For cost considerations, some manufacturers use a combination of classical dielectrics with the microwave dielectric materials. For thermal modeling of these composite materials, the thermal analyst needs to use Eq. (10.26).

**10.5.7.1 Through-hole thermal vias.** Another method to improve the thermal conductivity of the PCB is to use thermal vias under the high-power devices as shown in Fig. 10.68. These thermal vias are different from their ceramic coun-



**Figure 10.67** Construction of a circuit card with a metal core and the heat flow.

terparts in that the circuit card vias are usually through holes; i.e., the vias go from the top of the card to the bottom. The walls of the vias are typically copper plated as shown in Fig. 10.69. The heat is conducted primarily in the copper plating on the wall of the vias. In some advanced circuit cards with blind and buried signal vias, the thermal via is a series of stacked, filled vias as shown in Fig. 10.70.

Assume that a heat dissipating device is mounted on an FR-4 board, which in turn is mounted on a heat sink as shown in Fig. 10.71. Using superposition, the thermal resistance of the board without thermal vias under the heat dissipating device is calculated first as follows:

$$\theta_{board} = \frac{t}{K_{board}A_{pkg}} = \frac{t}{K_{board}LW} \quad (10.30)$$

where  $\theta_{board}$  = thermal resistance of the board under the heat dissipating device

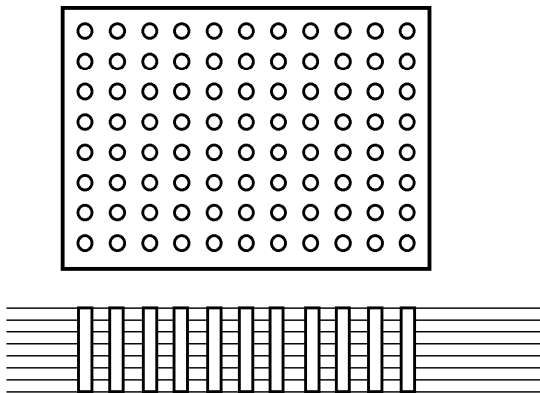


Figure 10.68 Through-hole via array.

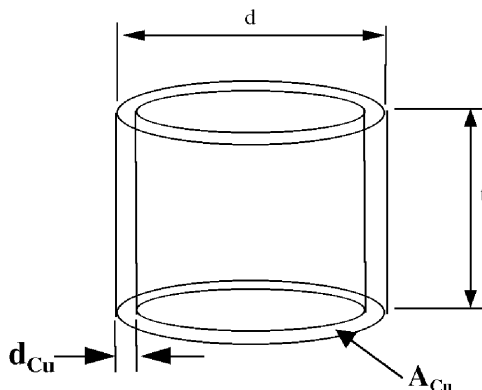


Figure 10.69 Expanded view of through-hole via.

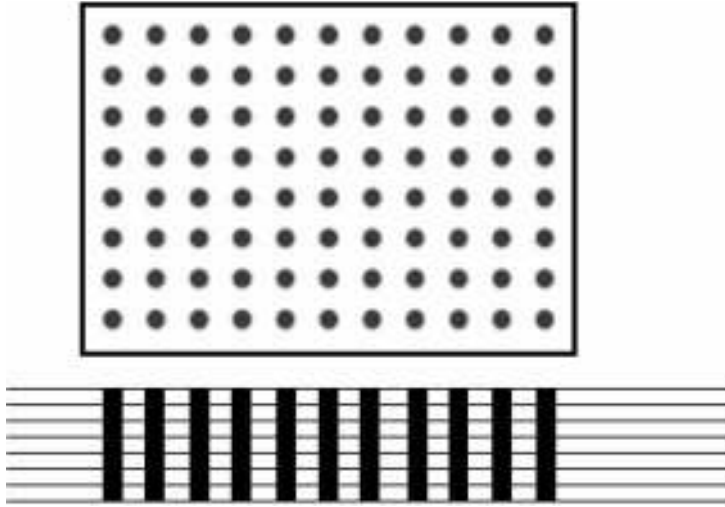


Figure 10.70 Stacked, filled vias in PCB.

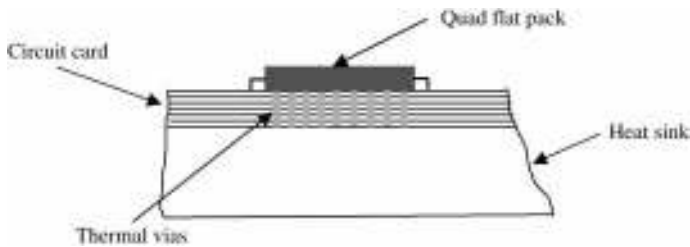


Figure 10.71 Surface mounted QFP on a circuit card with thermal vias mounted on a heat sink.

$$\begin{aligned}
 t &= \text{thickness of the board} \\
 K &= \text{thermal conductivity of the board} \\
 A_{\text{pkg}} &= \text{area of the heat dissipating device} = L \times W
 \end{aligned}$$

The thermal resistance of the thermal vias is calculated next. For one unfilled via, its thermal resistance is

$$\theta_{\text{via}} = \frac{t}{K_{\text{via}} A_{\text{via}}} \quad (10.31)$$

where  $\theta_{\text{via}}$  = thermal resistance of the via  
 $t$  = thickness of the board  
 $A_{\text{via}}$  = cross-sectional area of the via  
 $K_{\text{via}}$  = thermal conductivity of the via

The via's cross-sectional area, shown as  $A_{\text{cu}}$  in Fig. 10.69, is the area of the copper that conducts the heat. This heat-conducting portion of the via is calculated using Eq. (10.32).

$$A_{Cu} = \pi \left( \frac{d}{2} - \left( \frac{d}{2} - d_{Cu} \right) \right)^2 \quad (10.32)$$

where  $d_{Cu}$  = thickness of the copper in the via  
 $d$  = diameter of via

No heat is conducted through the air in the center of an unfilled via. As the thickness of the plating is increased, the thermal conductivity from the board, top to bottom, is also increased.

Because there are  $n$  thermal vias in parallel, Eq. (10.31) for the total via thermal resistance  $\theta_{nv}$  becomes

$$\theta_{nv} = \frac{t}{nK_{via}A_{via}} \quad (10.33)$$

The  $n$  vias (unfilled) under the heat dissipating device are in parallel with the board material's heat path. Having calculated the thermal resistances of the board alone, and the vias, the equivalent thermal resistance can be looked at as a parallel circuit, shown in Fig. 10.72, whose equivalent thermal resistance is

$$\theta_{equiv} = \frac{\theta_{board}\theta_{nv}}{\theta_{board} + \theta_{nv}} \quad (10.34)$$

It is obvious from Eq. (10.33) that the thermal resistance in the board can be lowered if the number of vias is increased. This approaches a limit imposed by circuit card manufacturers on the via-to-via spacing of through holes.

Ideally, one would like to fill the vias with a high-thermal-conductivity material such as copper to further lower the thermal resistance. However, due to processing concerns, minimum-sized through holes (0.019 in, typically) cannot

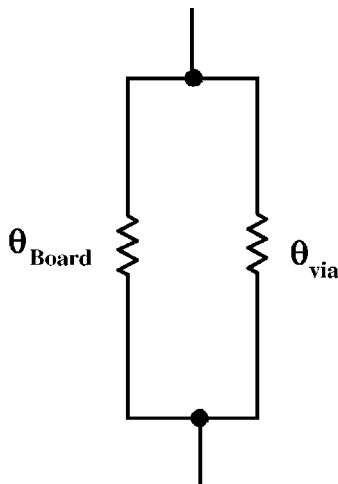


Figure 10.72 Electrical analog of thermal vias in PCB.

be filled with copper plating. Instead, materials such as solder and conductive epoxy are used for filling thermal vias. For filled vias, the electrical analog for the circuit would have three thermal resistances in parallel as shown in Fig. 10.73: the board material, the copper wall, and the fill material. If the vias were filled, then the thermal resistance would be lowered.

The thermal resistance of the via fill material is

$$\theta_{\text{via-fill}} = \frac{t}{nK_{\text{via-fill}}A_{\text{via-fill}}} \quad (10.35)$$

where  $A_{\text{via-fill}} = \pi(d - d_{Cu})^2$

The equivalent thermal resistance for the filled vias is

$$\frac{1}{\theta_{\text{equiv}}} = \frac{1}{\theta_{\text{board}}} + \frac{1}{\theta_{\text{via-fill}}} + \frac{1}{\theta_{nv}} \quad (10.36)$$

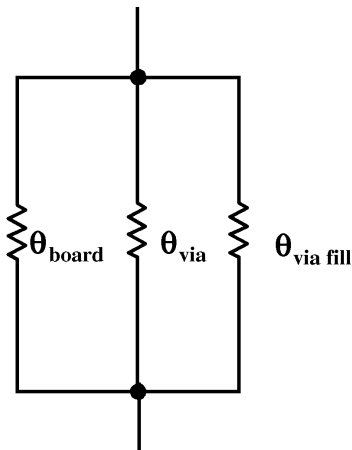
**Thermal via example** An array of 121 vias, 0.019 in diameter with 0.001-in copper plating in a 0.060-in thick FR-4 board, is placed under a device whose dimensions are  $0.300 \times 0.300$  in. The vias are filled with Sn 63 solder. It is necessary to find the equivalent thermal resistance of the board, the vias, and the via fill.

The thermal conductivities (in  $\text{W/m}\cdot^\circ\text{C}$ ) of the various materials are<sup>3</sup>

- FR-4            0.35
- Sn 63         50.9
- Copper        396.9

The thermal resistance of the FR-4 board without vias is

$$\theta_{\text{board}} = \frac{t}{K_{\text{board}}A_{\text{pkg}}} = \frac{0.060}{0.35 \times 0.0254 \times 0.3 \times 0.3} = 75^\circ\text{C/W}$$



**Figure 10.73** Electrical analog of filled thermal vias in PCB.



The thermal resistance of the via fill for  $n$  vias is

$$\begin{aligned}\theta_{\text{via-fill}} &= \frac{t}{nK_{\text{via-fill}}A_{\text{via-fill}}} \\ &= \frac{0.060}{121 \times 50.9 \times 0.0254 \times \pi \left( \frac{0.019}{2} - 0.001 \right)^2} = 1.690^\circ\text{C/W}\end{aligned}$$

The thermal resistance of the copper-plated via walls is

$$\begin{aligned}\theta_{nv} &= \frac{t}{nK_{\text{via-fill}}A_{\text{via-fill}}} = \frac{0.060}{121 \times 396.9 \times 0.0254 \times \pi \left( \frac{d}{2} - \left( \frac{d}{2} - d_{Cu} \right) \right)^2} \\ &= 15.66^\circ\text{C/W}\end{aligned}$$

The equivalent thermal resistance of the board, the vias, and the via fill is calculated using the electrical analogy for parallel circuits from Eq. (10.36).

$$\frac{1}{\theta_{\text{equiv}}} = \frac{1}{\theta_{\text{board}}} + \frac{1}{\theta_{\text{via-fill}}} + \frac{1}{\theta_{nv}} = \frac{1}{75} + \frac{1}{1.690} + \frac{1}{15.66} = 1.49^\circ\text{C/W}$$

By using solder-filled thermal vias, the thermal resistance of the board under the heat dissipating device was reduced from 75 to  $1.49^\circ\text{C/W}$ .

**10.5.7.2 Microvias (built-up technology).** In high-density printed circuit boards, blind and buried vias are used to connect two layers of circuitry. Fabricated by nonmechanical means, the diameters of microvias can be as small as 0.002 in. Multilayer circuits using this technique are built up one layer at a time and have been given the name of *built-up multilayer*.

Cross sections of metallized microvias formed by various techniques are shown in Fig. 10.74. The walls on each of the vias are plated copper. For thermal modeling, the equations in Sec. 10.5.3.9, developed for through-hole vias, can be used with the dimensions adapted for microvia technology.<sup>105</sup>

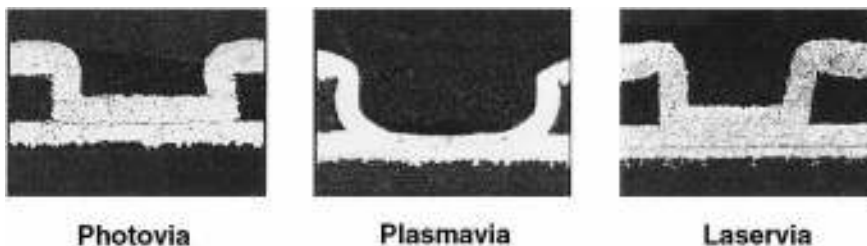


Figure 10.74 Metallized microvia cross section.

**10.5.7.3 Direct chip attach to heat sink.** Another technique for reducing the thermal resistance under a device is to mount it directly on the heat sink through a cutout in the circuit card as shown in Fig. 10.75. This technique completely eliminates the thermal resistance of the board. It works for direct chip attach (DCA) and packaged components as long as the back of the chip in DCA or the package bottom is not connected to any potential. If the back side of the chip were connected to a nonground potential, then a thin electrically-insulating layer of epoxy or other polymer would be required.<sup>5</sup>

### 10.5.8 Flexible PCBs

Flexible PCBs consist of ductile, patterned copper foil bonded to thin, flexible dielectric material. They are used in applications in which periodic movement of the circuit is required during circuit operation. The conductor patterns are formed in the same manner as in rigid PCBs. Vias, used for both interconnection and thermal improvement, can be the standard through-type, or they can be buried.

There are two possible conductive thermal paths in a flexible PCB: through the dielectric and through the copper foil. The dielectric material is typically a polyimide with a thermal conductivity of 0.11 W/m-K or a polyester film with thermal conductivity ranging from 0.21 to 0.87 W/m-K. Standard thicknesses of polyimide dielectric layers are 0.0005, 0.001, 0.002, 0.003, and 0.005 in. Because the thermal conductivities of flexible PCB dielectrics are rather low, the main thermal path is through the copper foil.<sup>3,105</sup> To improve the thermal effective thermal conductivity in flexible PCBs, thermal vias can be used as described above.

### 10.5.9 Plating

Metal packages and substrates are typically plated with materials such as gold, nickel, copper, silver, and tin. Packages are plated to prevent corrosion, whereas substrates are plated to increase electrical conductivity and to facilitate wire bonding. Nickel is used for several reasons, including corrosion protection and as a metal barrier between the base metallization and subsequently applied solder. Although the plating thicknesses may be thin, they need to be considered in accurate thermal modeling. Table 10.22 lists the thermal conductivities of various plated metals used in microelectronic assemblies.

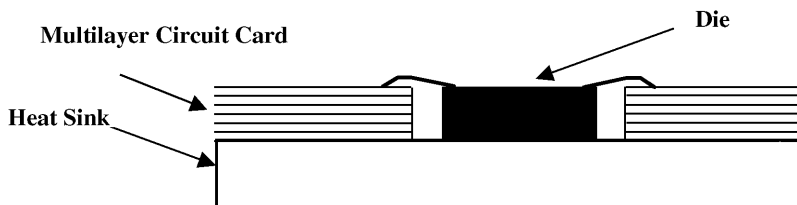


Figure 10.75 Direct die attach to heat sink.

TABLE 10.22 Thermal Conductivities of Plated Metals<sup>65</sup>

Material	Thermal conductivity (W/m-K) at 0°C	Thermal conductivity (W/m-K) at 100°C
Gold	319	313
Silver	429	426
Nickel	94.1	82.7
Copper	401	395
Tin	68.2	63.2

### 10.5.10 Gases

The thermal conductivities of gases are extremely poor. When a gas is in the thermal path, the resulting thermal resistance will be extremely high. For instance, air, consisting of 78 percent nitrogen and 21 percent oxygen, has a thermal conductivity of 0.0253 W/m-K at sea level. This is approximately 100 times less than the thermal conductivity of epoxies. The thermal conductivity of air varies with altitude as shown in Fig. 10.76.<sup>65</sup>

As shown in Table 10.23, a gas such as helium has a thermal conductivity approximately six times that of air/nitrogen and can provide some additional

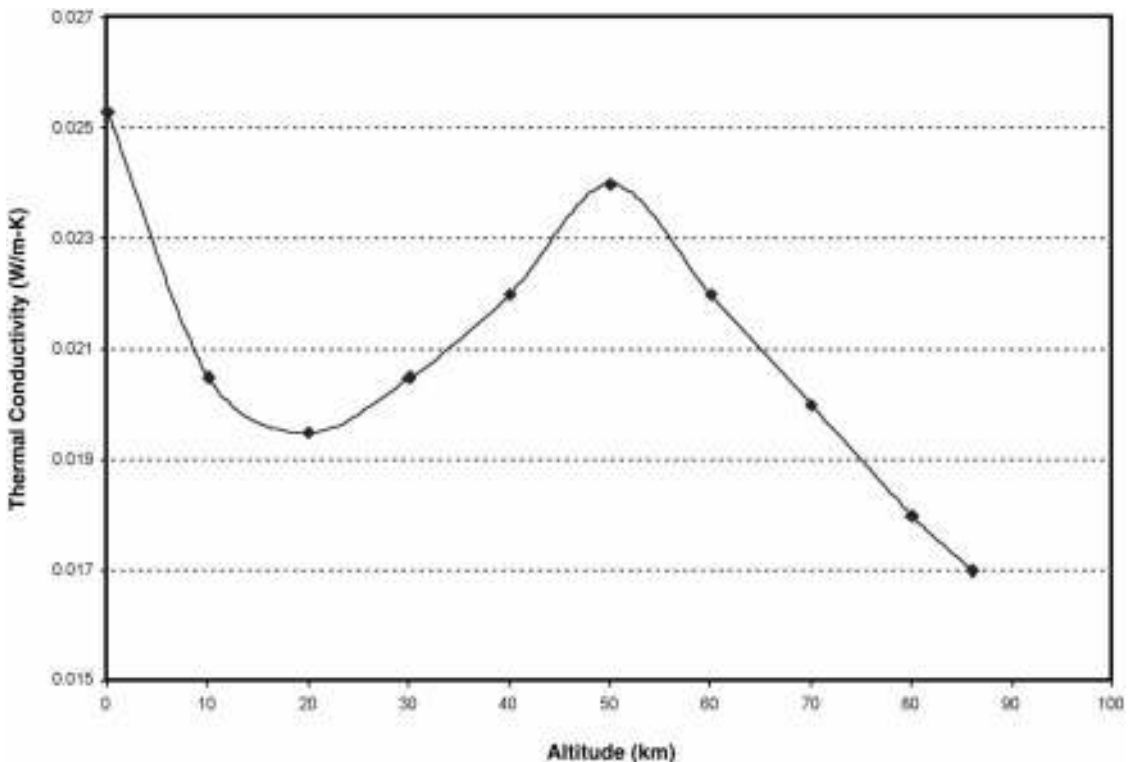


Figure 10.76 Thermal conductivity of air at various altitudes.

**TABLE 10.23 Thermal Conductivity of Gases at 1 Atm, in W/m-K (from Ref. 65)**

Gas	0°C	100°C
Air	0.0024	0.0031
Argon	0.0016	0.021
Carbon dioxide	0.00137	0.0023
Helium	0.0141	0.017
Hydrogen	0.016	0.021
Nitrogen	0.0024	0.0031
Oxygen	0.0024	0.0032

cooling. IBM has used helium as a backfill for its Thermal Conduction Module.<sup>24,65</sup>

## 10.6 Factors Determining Thermal Resistance

A myriad of physical factors determine the thermal resistance of a semiconductor in an electronic system. All of these factors were captured in Eq. (10.9), which is repeated here.

$$\theta = \frac{X}{KA}$$

Figure 10.77 depicts a chip mounted on a substrate, which in turn is attached to a package. This package is bonded to the printed wiring board with a thermal interface material.

### 10.6.1 Semiconductor dimensions

The heat in an electronic system is generated in the semiconductor junction, and the junction area “A” in Eq. (10.9) is a key factor in determining the thermal resistance. It is relatively easy to determine the junction size in discrete transistors and diodes. Figure 10.78 shows a picture of a 0.200-in square junction transistor die wherein the junction size can be approximated by the guard ring as 0.160 × 0.160 in. Heat is not generated across the entire transistor die.

For the voltage regulator die shown in Fig. 10.79, there is a high-power transistor occupying approximately half of the die. Although the low power section dissipates a small amount of heat, it is the power transistor that dissipates the majority of the heat. For an accurate first-order thermal analysis of this die, the junction size to use is that of the high-power transistor, approximately 0.045 × 0.085 in.

Power MOSFETs consist of thousands of individual transistors in parallel. For example, a 240-mil<sup>2</sup> MOSFET from Fairchild Semiconductor consists of approximately 25,000 transistors in parallel.<sup>107</sup> For the power MOSFET thermal model, the thermal analyst usually uses the entire chip area as the junction area.

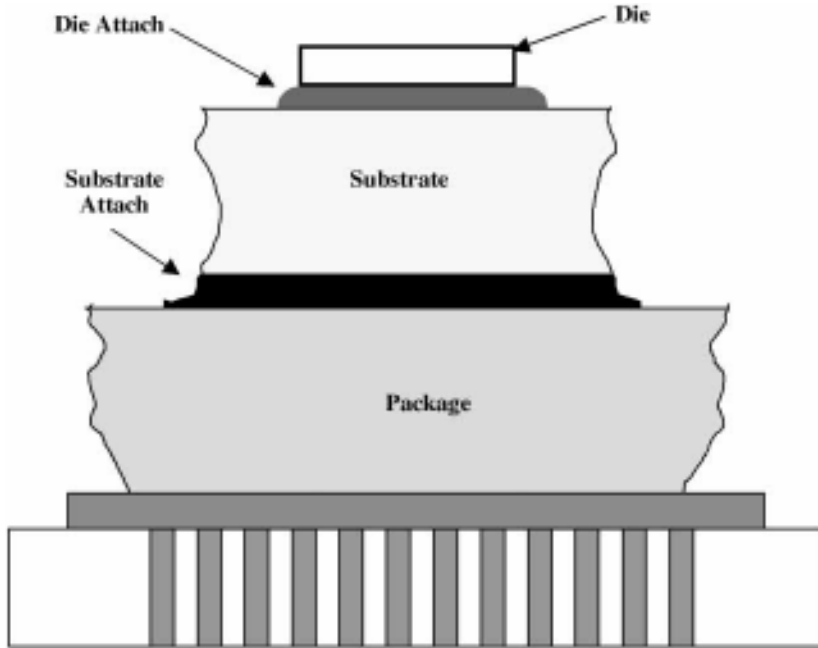


Figure 10.77 Cross-sectional view of packaged die.

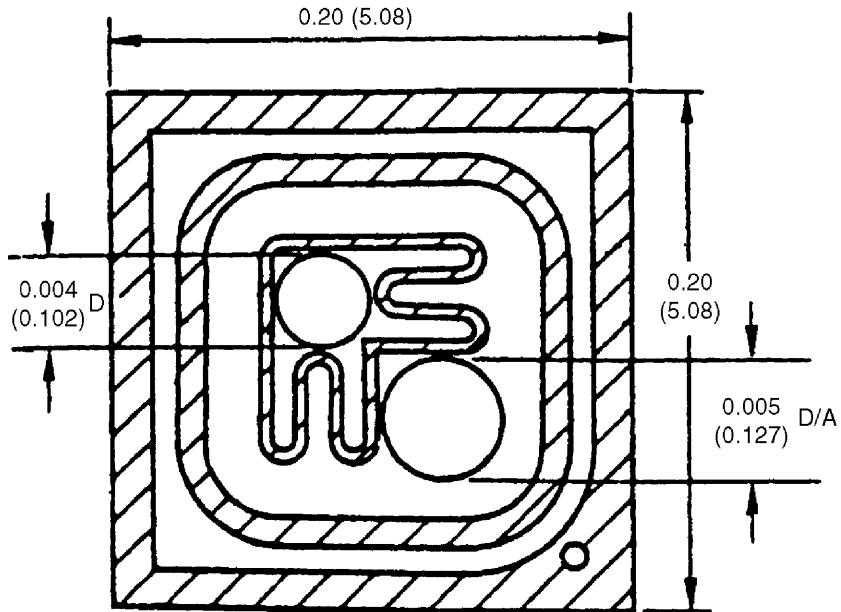


Figure 10.78 Die topography of junction transistor.

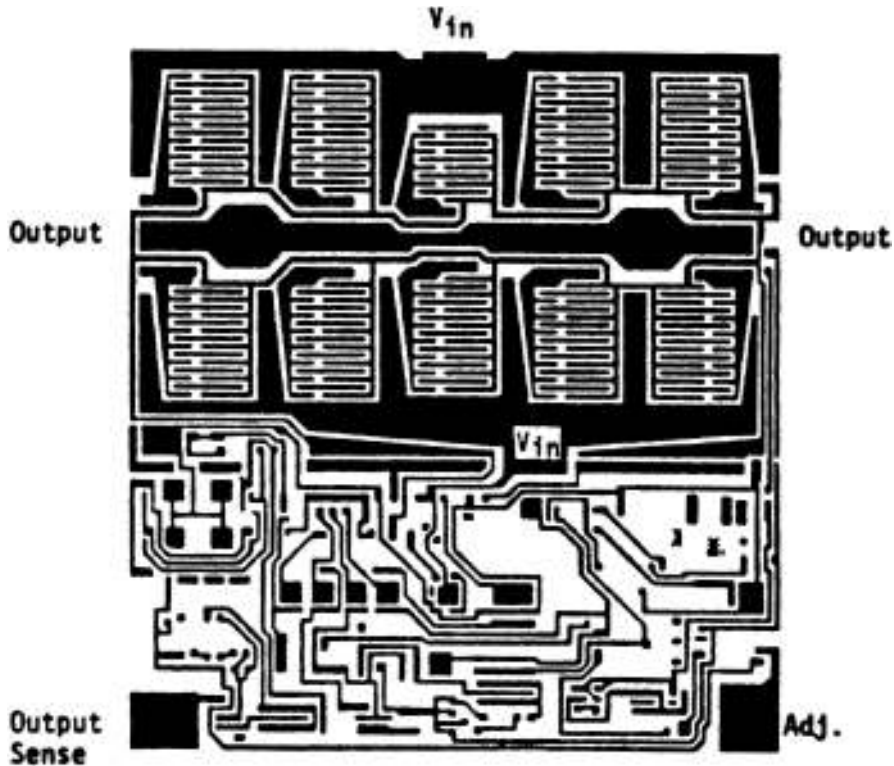


Figure 10.79 Die topography of voltage regulator.

In integrated circuits, the number of junctions can range from as few as a dozen to the millions. When modeling integrated circuits, the thermal analyst usually looks at the entire die as the junction area. However, the analyst may take into account that there are no junctions under the wire bond pads and subtract out that small amount of area. If the integrated circuit has high-current drivers, then the thermal model should be broken down into the low-power section(s) and the high-power driver section(s).

The thickness of the die “X” is an important factor in determining thermal resistance. As wafer sizes have grown from 3- and 4-in diameters to 12-in ones, the thickness has also increased from 0.015 to 0.030 in. Figure 10.80 shows the various wafer thicknesses for different diameters.<sup>108</sup> Many semiconductor foundries thin their wafers down, either with mechanical or chemical methods, mostly to allow the chips to fit into their packages. However, some chip manufacturers use the thinning process to reduce the thermal resistance.

The majority of semiconductors are fabricated from silicon, which has a thermal conductivity of 150 W/m-K (at 25°C). For high-frequency applications, typically starting at 1 GHz, gallium arsenide is used as the semiconductor material. Other materials used include indium phosphide, silicon carbide, gallium phosphide, gallium antimony, indium arsenide, and indium antimony. Because of the substance’s lower thermal conductivity (45 W/m-K), gallium ar-

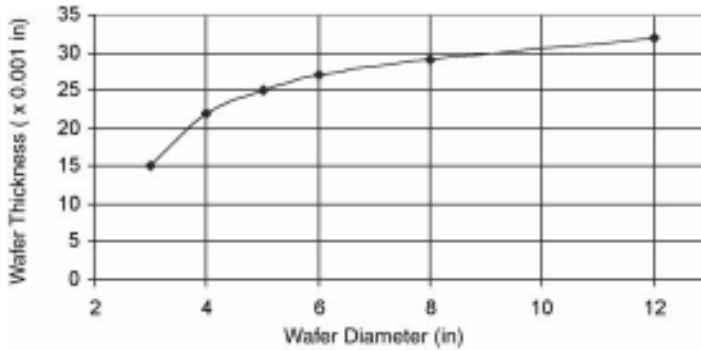


Figure 10.80 Wafer thickness vs. wafer diameter.

senide chips are routinely thinned down to lower the thermal resistance. Gallium arsenide chips are also thinned to reduce the impedance of through-hole vias from the top to the bottom of the chip. Typical thicknesses of gallium arsenide used in the microelectronic assemblies are 0.002 and 0.006 in.

### 10.6.2 Die attach material and thickness

In most packaging applications, the semiconductor die needs to be attached to the next level of packaging with die attach material on the back side of the chip. The thermal conductivity of this adhesive material is usually the most important factor in determining thermal resistance. The die attach material is typically chosen for both manufacturability and thermal performance. Organic materials such as epoxy are used because of their ease of application and, in some cases, ease of rework. Epoxies, however, have very low thermal conductivities, typically in the range of 1 to 2 W/m-K as detailed in Table 10.7. Solder materials, such as gold-tin and lead-tin, offer considerably higher thermal conductivity, typically in the range of 40 to 60 W/m-K, but at the expense of manufacturability. An alternative material for die attach, silver glass, with a thermal conductivity of 60 to 80 W/m-K, offers many of the advantages of both the organic materials and the solders.

For any die attach material selected, the second most important factor determining thermal resistance is the die attach bond line. As defined in Eq. (10.9), the thermal resistance of the die attach is directly proportional to the thickness “X.” The goal is to minimize the die attach thickness and maintain sufficient strength so that the die does not come off during its application. The uniformity of the die attach material is also an important factor in determining thermal resistance. If the die attach bond line had a variation in it, then a mean thickness would be used in that layer’s thermal resistance calculation. An extremely thick die attach bond line can result in hot spots on the die. A condition worse than an extremely thick die attach is the presence of voids. Mathematically, voids reduce the effective cross-sectional area of the die attach. For the X-ray of the die attach shown in Fig. 10.81, there is approximately 10 percent voiding. This can be modeled as shown in Eq. (10.37), where the area term “A” is reduced by the percentage voiding “V.”

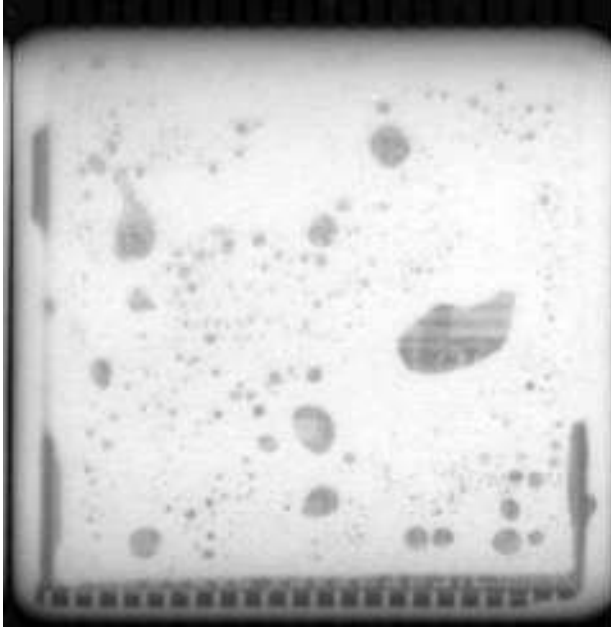


Figure 10.81 X-ray of hybrid substrate attach.

$$\theta = \frac{t}{K(1 - VxA)} = \frac{t}{K(0.9A)} \quad (10.37)$$

### 10.6.3 Substrate material and thickness

When a substrate is used in the packaging, there are two key parameters in determining thermal resistance. The thermal conductivity of the material is the most important parameter. The second most important parameter is the substrate thickness. Ninety-six percent alumina with single-layer metallization has a thermal conductivity of 21 W/m-K. The same alumina with five thick film dielectric layers has an effective thermal conductivity in the z-direction of only 15.9 W/m-K. High-power applications typically use beryllium oxide as a substrate. Its thermal conductivity is 248 W/m-K. This is an improvement of 8 times over 96 percent alumina. With five layers of dielectric, beryllium oxide has an effective thermal conductivity in the z-direction of 178 W/m-K. Aluminum nitride, with a thermal conductivity of 170 W/m-K, is also used as a substrate in high power applications.

The presence of thermal vias in the substrate can produce significant improvement in the effective thermal conductivity. For example, the 951 LTCC substrate material from DuPont has a published thermal conductivity of 3.0 W/m-K.<sup>35</sup> The same material with an array of gold-filled thermal vias (0.006-in diameter, 0.018-in pitch) has a thermal conductivity of 24.56 W/m-K.<sup>41</sup> The maximum via diameter and pitch are determined for each substrate type by the manufacturer. Exceeding these values can cause substrate warping or



cracking as a result of the higher CTE of the via fill as compared to dielectric material.

The thickness of the substrate dielectric material is an important factor in determining the thermal resistance. Thick-film glass has a thermal conductivity of  $3.0 \text{ W/m}\cdot\text{K}$ .<sup>35</sup> This is only 10 percent of the thermal conductivity of 96 percent alumina. Substrate manufacturers typically use two to four printings<sup>109</sup> of dielectric between each metallization layer. The fired thickness of each dielectric printing is typically 12 to 14  $\mu\text{m}$ . These multiple layers are used to prevent pinholes in the dielectric that lead to shorting between layers. With additional printings of dielectric, the dielectric layer becomes thicker, and the thermal resistance of that layer becomes higher.

Often, power or ground planes are used in multilayer substrates. These planes are typically solid metal or in grid form. In addition to providing low electrical resistance, they also serve the purpose of heat spreading.

#### 10.6.4 Substrate attach material and thickness

When substrates are used, they must be attached to the package with either solder or some organic adhesive material. The same parameters that determine thermal resistance for the die attach material, thermal conductivity and thickness, apply for the substrate attach. If organics are used for the substrate attach, the thermal resistance will be significantly higher than if a solder were used.

#### 10.6.5 Package material

As described in Sec. 10.5.5, semiconductor packages can be divided into two types: hermetic and nonhermetic. The key parameters for both package types in determining thermal resistance are the thermal conductivity and material thickness of the base material. The best thermal conductivity material used for package bases is copper, with a value of  $397 \text{ W/m}\cdot\text{K}$ . On the opposite end of the thermal conductivity spectrum is LTCC, with a value of  $3.0 \text{ W/m}\cdot\text{K}$ .<sup>12</sup> As described in Eq. (10.9), the thinner the material, the lower the value of thermal resistance. However, as the material becomes too thin, the structural integrity of the package is compromised. During environmental screening or during operation in severe environments, a thin package base can deflect and cause cracking of semiconductors and substrates.

The nonhermetic, plastic encapsulated semiconductor package comes in several variations. The majority of these package types have plastic molding compound under the die as shown in Fig. 10.36. This material typically has very low thermal conductivity of  $0.5$  to  $1.0 \text{ W/m}\cdot\text{K}$ . To lower the thermal resistance of plastic packages, some manufacturers use an exposed metal pad on the back side of the package. This exposed pad, usually part of the lead frame, is called an *exposed paddle*. When made from copper, this paddle provides a low thermal path from the die to the circuit card and provides excellent heat spreading. When the paddle is exposed and fabricated with Alloy 42 with a thermal conductivity of  $15.9 \text{ W/m}\cdot\text{K}$ ,<sup>24</sup> there is a significant thermal conductivity improvement over packages made with plastic bottoms.

### 10.6.6 Package interface

The physical designer may have used all of the materials and processes in packaging the semiconductor to achieve the lowest thermal resistance, but may have added significant thermal resistance in attaching the device to the circuit card or the heat sink. As noted in Sec. 10.5.9, air, with its low 0.025 W/m-K thermal conductivity, must be eliminated, or at least minimized, from the thermal path. This requires the attachment of the package to the circuit card or heat sink with a thermally conductive material that fills the gaps between the package and the circuit card or heat sink. If the material is too thick, then the thermal resistance increases linearly. If too thin, there may be air gaps and higher thermal resistance. The various materials used to fill the gaps have been described in Sec. 10.5.6. Many of these materials, such as the adhesives and gap pads, have thermal conductivities in the range of 0.6 to 6.0 W/m-K. At the upper end of the thermal conductivity range for the package interface materials is the solder perform. For example, Sn 63 solder has a thermal conductivity of 51 W/m-K. As discussed in Sec. 10.5.6, the thermal conductivity of many of the interface materials is a function of the pressure applied. Using an incorrect pressure, or a pressure that can significantly vary, will cause variations in the thermal resistance.

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