High voltage pulse generation using current mode second breakdown in a bipolar junction transistor

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The characteristics of a bipolar junction transistor operating in the avalanche region and then triggered into current mode second breakdown are formulated. If the time the BJT is subjected to secondary breakdown is limited the BJT may be used as a nanosecond, high voltage switch without sustaining damage. Several methods of fast pulse generation, electrical and optical, using this mode of operation are discussed. A 2000 V pulse generator, into 50 Ω, with a risetime of approximately 1 ns, jitter <100 ps, is then designed using these results.

I. INTRODUCTION

Current mode second breakdown can be destructive in a bipolar junction transistor (BJT).[1] If the amount of time the BJT is subjected to secondary breakdown is limited the BJT may be used as a fast, low jitter, high voltage switch. The BJT operated in this mode has been given the name avalanche transistor. This choice of name is unfortunate due to the earlier work done in avalanche mode switching[2–8] which also calls the BJT an avalanche transistor.

Figure 1(a) shows the I-V characteristics of a typical planar epitaxial silicon BJT, such as the 2N3904. Both avalanche mode switching and current mode second breakdown switching begin at point A, slightly below BV_{CBO}. Avalanche mode switching follows the load line A-B, that is, switching roughly from BV_{CBO} to BV_{CEO}. This type of switching is nondestructive and slow by comparison, depending to a large extent upon the triggering pulse. Currents are usually much less than 1 A and collector-emitter voltage changes are on the order of tens of volts. If point B is close to the maximum power curve, thermal mode second breakdown may cause the transistor to switch to the secondary breakdown voltage after some time delay.

Current mode second breakdown operation moves the operating point A to A′ upon application of a trigger and then follows the load line A′-C avoiding the safe operating area. It will be shown that currents can be greater than 30 A while switching voltages of several hundred volts. Avalanche transistor, from this point on, will refer to the current mode second breakdown switching phenomena.

A paper by Mitchell[9] gives some qualitative guidelines into using avalanche transistors, while other papers[10–14] present designs using avalanche transistors. The purpose of this paper is twofold: first, quantitative guidelines relating to the operation of avalanche transistors will be given and second, methods of fast pulse generation will be discussed.

II. AVALANCHE TRANSISTOR OPERATION

With the aid of Figs. 1(a) and 1(b) the operation of an avalanche transistor may be described. The static operating point of the circuit in Fig. 1(b) is initially at point A in Fig. 1(a). The maximum collector current which can be put into the collector terminal of the BJT, with the collector-emitter voltage approximately equal to BV_{CBO} and in a specific circuit configuration, is called the hold off current I_H. The large value of the collector resistor, in this case 470k, insures that reasonable fluctuations in breakdown voltage between different devices will have a small affect on the collector current. The collector current should be maintained as far below the hold off current as possible, while still maintaining the breakdown condition.

Applying a trigger of approximately 1.3 V foward biases the base-emitter junction. This causes the collector current to increase beyond I_H resulting in second breakdown. If I_H cannot be reached due to the design of the external circuit, such as with a large load resistance, an intermediate value of collector emitter voltage will be reached lying between BV_{CEO} and BV_{CBO} (avalanche mode switching). If V_{AS} is the sustaining voltage between the collector and emitter after secondary breakdown then $(BV_{CBO}-V_{AS})/R_L=I_L$ is the load current after switching. If $I_L \gg I_H$ second breakdown will result. Putting a capacitance of 100 pF or less between the collector and emitter can also be used to insure that the condition $I_L \gg I_H$ is reached.[9] This capacitor increases the current multiplication resulting in a faster rise time and less delay time. Reaching I_H when the load resistance is 50 ohms is almost always achieved.

The basic equations describing a transistor, operating in the avalanche region, in a static state are given by:

$$I_C=\alpha I_E M + I_{CBO} M, \tag{1a}$$

$$I_E=I_{ES}(e^{qV_{BE}/mkT}-1), \tag{1b}$$

$$I_C=I_E+I_{BR}, \tag{1c}$$

$$V_{BE}=I_{BR}(R_B+r_{bb}), \tag{1d}$$

$$M=\frac{1}{1-(V_{CB}/BV_{CBO})^n}. \tag{1e}$$

The current I_{BR} is the current leaving the base. Ideally, a properly designed avalanche transistor circuit will make $I_{BR}=I_C$ and set the emitter current and base-emitter voltage to zero. These conditions can rarely be met due to the base spreading resistance, r_{bb}, and temperature variations.

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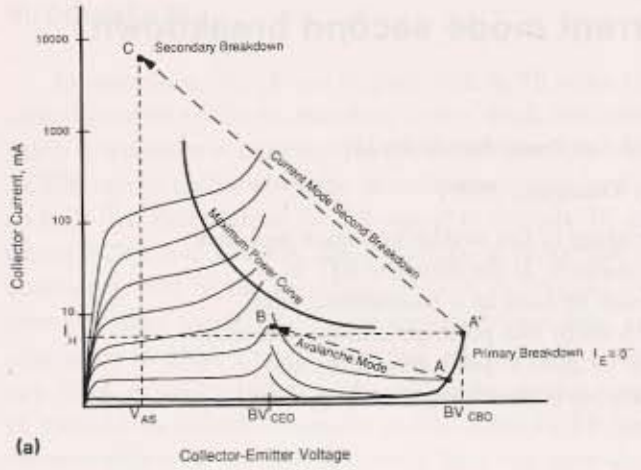

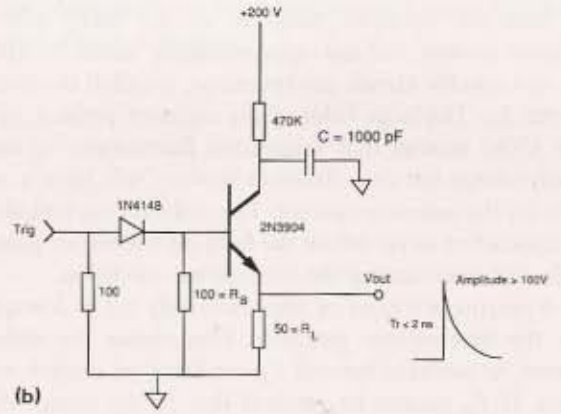

FIG. 1. (a) Typical I-V characteristics of planar epitaxial BJT. (b) Avalanche transistor pulse generator.

If Eqs. (1a) and (1c) are combined the collector current may be expressed as

$$I_C = \frac{MI_{CBO}}{1-\alpha M} - \frac{\alpha M I_{BR}}{1-\alpha M}, \tag{2}$$

as αM approaches unity the collector current will increase limited by the external circuit only. Therefore, while operating at point A in Fig. 1(a) the product αM is approximately equal to 1. Equation 1(a) may be rewritten as

$$I_C = I_E + I_{CBO}M. \tag{3}$$

Equation (3) is valid only when operating in the primary breakdown region. The parameter α, i.e., forward common base current gain, is much less than unity when the transistor is in cutoff and starts to increase towards unity as the transistor enters the active region. The multiplication factor M, Eq. 1(e), is unity until the collector-base voltage gets comparable to its breakdown voltage at which time M becomes larger than unity. The constant n is in the range of 2–6 and must be measured for each transistor.

Figure 2 shows the basic construction of a discrete transistor. A BJT that works well as an avalanche transistor is one in which the collector resistivity is high. This results in most of the collector-base potential being dropped across the collector region. If the collector resistivity is not high, relative to the base, the collector-base depletion layer can extend across the base to the emitter. This is called punch-through and it keeps the junction from going into avalanche breakdown. Transistors that have this punch-through phenomena cannot be used as avalanche transistors.

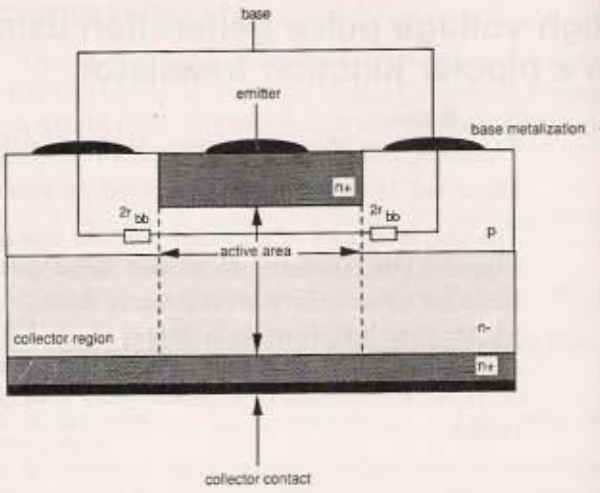

FIG. 2. Discrete transistor construction.

The base spreading resistance is the resistance of the p-type semiconductor in the base region between the base metalization and the active region under the emitter. This parameter is very important when selecting an avalanche transistor. Combining Eqs. (1b), (1d), (1e), and (3) the effect of r_{bb} on collector current may be shown as

$$I_C = \frac{I_{CBO}}{1-(V_{CB}/BV_{CBO})^n} + I_{ES}(e^{qI_{BR}(R_B+r_{bb})/mkT} - 1), \tag{4}$$

increasing r_{bb} will result in an increase in I_C at a constant V_{CB}, effectively lowering I_H. A quick method of determining the relative r_{bb} of a group of transistors is to short the base to the emitter, $R_B = 0$, and measure I_H for each transistor with a curve tracer, see Fig. 3. The higher I_H, the lower r_{bb}, with r_{bb} ranging from 4 to 400 Ω and I_H ranging from 0.1 mA to greater than 20 mA typically. The hold off current can be decreased by increasing the value of R_B. Decreasing I_H may be helpful when stacking avalanche transistors for higher voltages or optically triggering.[15] A problem may arise if R_B is increased too high. The base-emitter junction may start to turn on, causing the collector-emitter voltage to become a value less than BV_{CBO}, or the transistor could start free running in a relaxation oscillation type fashion. Another problem with a large r_{bb} is temperature. As Eq. (4) shows, lowering the temperature increases I_C which can also lead to free running. It has been suggested by Ref. 9 to apply a negative voltage to the base to avoid these problems. The base-emitter junction is then reverse biased keeping the collector current from increasing beyond the hold off current for large fluctuations in temperature. The disadvantages of a negative bias are: a lowering of output amplitude, an increase in delay time, more complicated circuit design, and

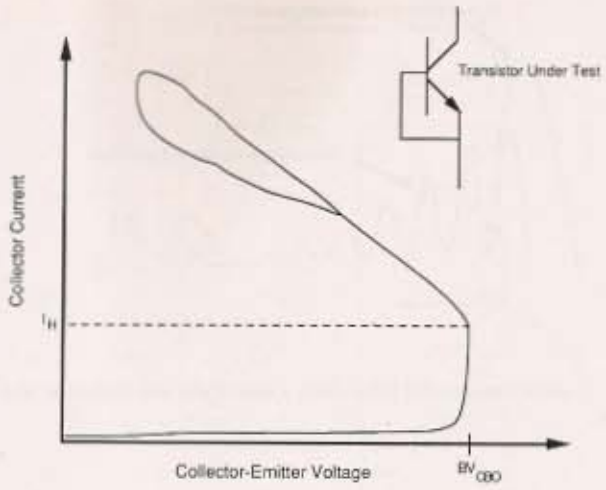

FIG. 3. Curve tracer showing secondary breakdown.

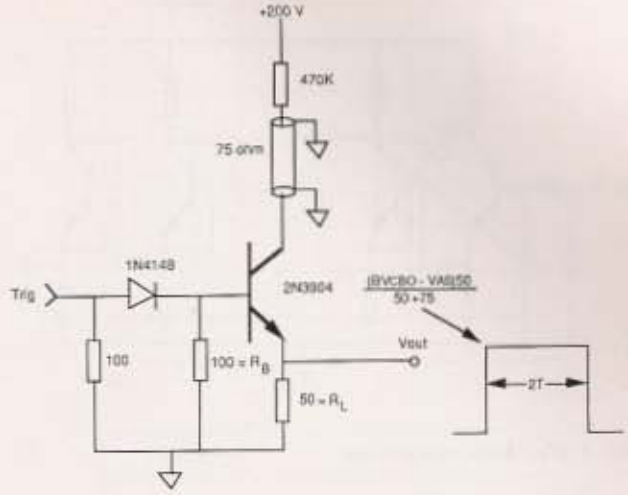

FIG. 4. Avalanche square pulse generator.

a larger input trigger voltage required to bring I_C up to I_H. If the environment is noisy, r_{bb} is large (small I_H), or if the circuit must operate down below freezing temperatures a negative bias is suggested. For most applications proper selection of the transistor and R_B are all that is needed.

There are two parameters in Eq. (4) which can be used by the circuit designer to trigger the avalanche transistor; $R_B I_{BR}$ and V_{CB}. Increasing the voltage across R_B effectively increases I_{BR}, as seen by the base-emitter junction, forward biasing the base-emitter junction and raising I_C. Increasing V_{CB} brings I_C up to I_H by increasing the multiplication across the collector-base junction.

The rise time of a particular avalanche transistor has been shown by Koo and Pocha[16] to be related to the physical length of the collector region and the sustaining voltage V_{AS}. They have shown that current mode second breakdown is the result of an expanding plasma wave that propagates across the active collector region. The time this wave takes to propagate across the collector region, from the edge of the electric field due to V_{AS} to the base region, corresponds to the rise time of the external electrical pulse. It is then reasonable to conclude that the lower the breakdown voltage of a particular avalanche transistor the faster the rise time. This may not always be true due to the relationship between collector-base dopings and breakdown voltage, but for the most part this rule holds.

Another area of concern is the average power that an avalanche transistor can dissipate. When operating at high current levels emitter current crowding becomes a problem. The base spreading resistance will cause an uneven current flow across the base-emitter junction causing the current to crowd in the region farthest from the base metalization. Also the series resistance of the emitter and collector regions becomes important at these high current levels. Selecting a transistor with a large dc current rating, such as 1 A, will help to lessen these problems. The larger semiconductor area corresponds to smaller series resistances and better heat dissipation.

III. PULSE GENERATION USING AVALANCHE TRANSISTORS

The circuit shown in Fig. 1(b) is the basic building block of all avalanche transistor circuits. The diode at the base is provided to protect the triggering instrument when the base of the transistor rises to $BV_{CBO} - V_{AS} - I_{BR} r_{bb}$ after being triggered. A negative pulse output may be accomplished by grounding the emitter and putting the load between the energy storage capacitor C and ground. When the emitter is grounded a protection diode is not needed.

Square pulses may be generated by replacing the energy storage capacitor with a charge line, Fig. 4. The charge line impedance is selected so that it is greater than the combined load and transistor impedances. The negative reflection resulting from the mismatch at the open (the large resistor appears as an open for the fast pulse) turns the transistor off quickly and cleanly. The width of the pulse is equal to the two way travel time of the cable. A variable width pulse generator was designed in Ref. 11 which used a second avalanche transistor to discharge the delay line and set the pulse width.

Power MOSFETs driving a 50 Ω load can be switched on in less than 3 ns when driven with an avalanche transistor.[17] The drain-source voltage of the MOSFET may be adjusted to provide a variable amplitude pulse generator. Because of the dependence of avalanche transistors on BV_{CBO}, making pulse generators with a variable amplitude relies on variable external attenuators. Using and finding variable external attenuators when pulse amplitudes are greater than 1 kV and risetimes of less than a few nanoseconds can be difficult, although some excellent fixed value high voltage subnanosecond attenuators are available from Barth.[18]

Generating higher voltage pulses can be accomplished using a Marx bank configuration, Fig. 5, or directly stacking avalanche transistors, Fig. 6. The energy storage capacitors in the Marx bank are charged in parallel and discharged in series. Upon application of a trigger the first transistor breaks down. This causes the second transistor

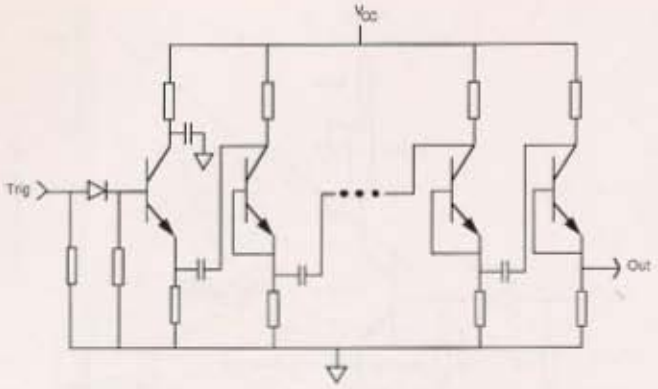

FIG. 5. Marx bank configuration.

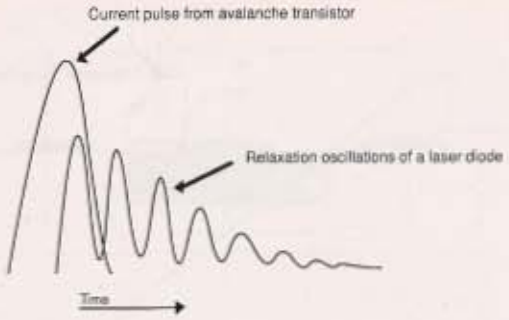

FIG. 7. Generating optical pulses with a laser diode and avalanche transistor.

to see twice its breakdown voltage at its collector making the transistor breakdown. The third transistor will see three times its breakdown voltage and so forth. Due to the large impedance each transistor initially drives it may be necessary to put a capacitor between the collector and emitter to insure that the transistor will go into second breakdown. Another solution to this problem is to put a small resistor, on the order of 50 Ω, between the base and emitter to adjust the hold off current value. This base resistor has the disadvantage of lowering noise and temperature tolerances as discussed earlier. At high current levels shorting the base to the emitter will help to ease the problem of current crowding under the emitter by diverting some of the collector current through the base spreading resistance and out the base lead. At low current levels the resistance of the base-emitter junction is much smaller than r_{bb} resulting in most of the collector current flowing out the emitter terminal.

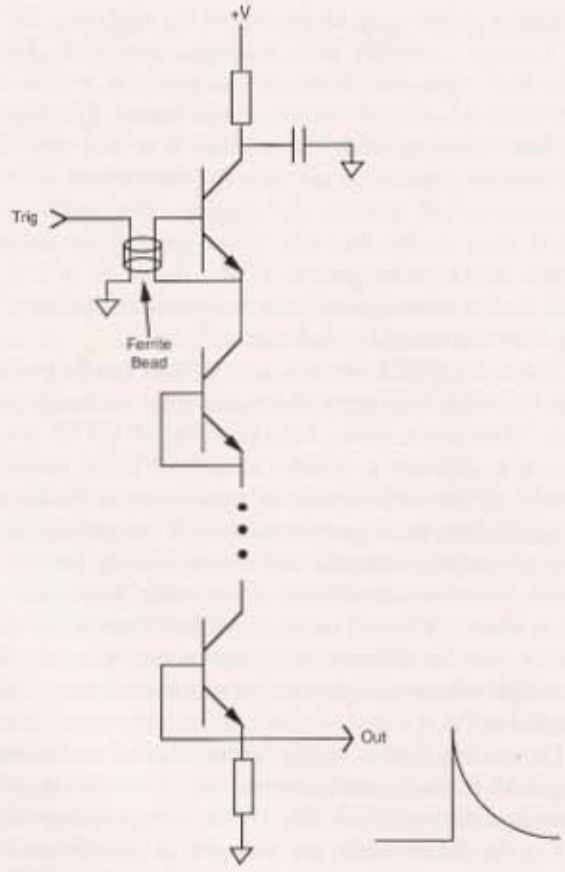

FIG. 6. Stacking avalanche transistors.

The main advantage in stacking avalanche transistors over the Marx bank configuration is simplicity. The lower number of components corresponds to less inductance in series with the switch. The disadvantage is the higher supply voltage required. Often a ballast resistor between the collector and emitter is needed when stacking avalanche transistors. This resistor will help compensate for the differences in the hold off currents of transistors keeping the string from self triggering. The greater the hold off current of a transistor the less likely a ballast resistor will be needed.

Optical pulse generation combining the relaxation oscillation phenomena of laser diodes[19] with the large current pulse capability of avalanche transistors can lead to optical pulses of < 100 ps widths. Figure 7 shows that if the current impulse of the avalanche transistor returns to zero before the occurrence of the second oscillation of the laser diode an optical impulse will be generated. If a current step is applied to the laser diode a train of impulses with decreasing optical amplitude will be generated. This second type of pulse generation finds extensive uses in calibrating and time referencing streak cameras.

Finally, the manufacturer of an avalanche transistor and the date manufactured are also of concern. A 2N2222A may function as an avalanche transistor from one manufacturer with a certain date code, but not from another manufacturer or with a different data code.

IV. A DESIGN EXAMPLE

This section will apply the information given earlier to the design of a high voltage pulse generator. The design criteria are amplitude of greater than 1.5 kV, pulse risetime less than 2 ns, jitter less than 100 ps, load impedance 50 Ω (at least 30 A load current), and repetition rate greater than 500 Hz. Some uses a pulse generator of this form finds are; nuclear diagnostics, high speed photography, trigger-

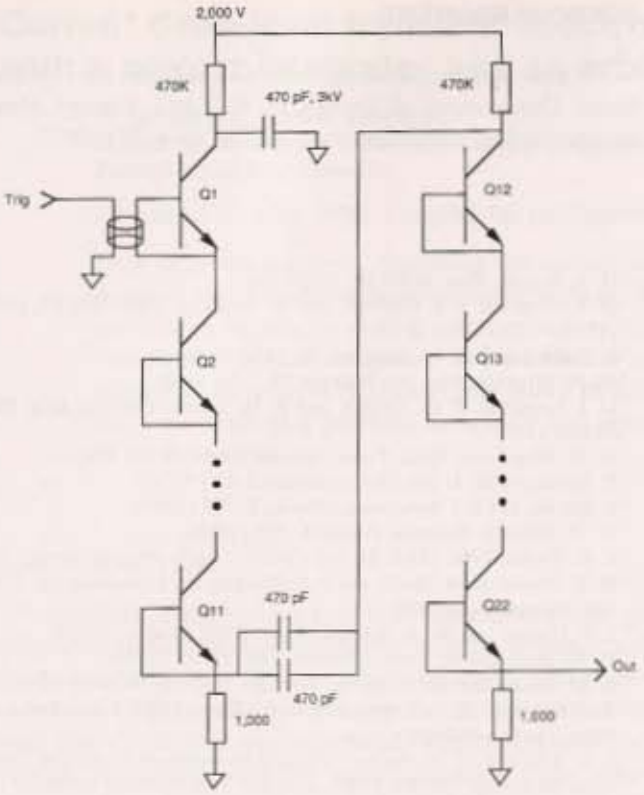

FIG. 8. High voltage pulse generator schematic.

ing oscilloscopes and transient digitizers, time referencing high speed measurements, and generating high power rf and microwave radiation.

The schematic of this pulser is shown in Fig. 8. A combination of Marx bank and stacking of avalanche transistors is used. This scheme allows the use of a 2000 V supply instead of a 4000 V supply, which would be required when stacking alone, while keeping the inductance in series with the strings to a minimum. The transistor, MPS6601, was picked because it has a high dc current rating (1 A), is in a low inductance package (TO-92), the breakdown voltage of this particular yield is a moderate 180 V, hold off current is typically 20 mA (corresponding to small base spreading resistance), and each transistor from this yield has approximately the same breakdown characteristics. A ballast resistor was not needed because of the large hold off current, although to adjust for variations in processing of the transistors the designer may wish to include the resistor as a safety precaution. Eleven transistors were used so that their combined breakdown voltage was approximately 2 kV. The repetition rate for this circuit is greater than 500 Hz and can be roughly determined by the 470k-(470 pF + transmission line capacitance) time constant.

The transistors were mounted on a 50 Ω transmission line configuration, Fig. 10, with the output as shown in Fig. 9(a). The purpose of this line is to help cancel the inductance of the transistors by providing a small capacitance to ground, the short piece of transmission line appears as a small capacitor to the transistor. Placing small,

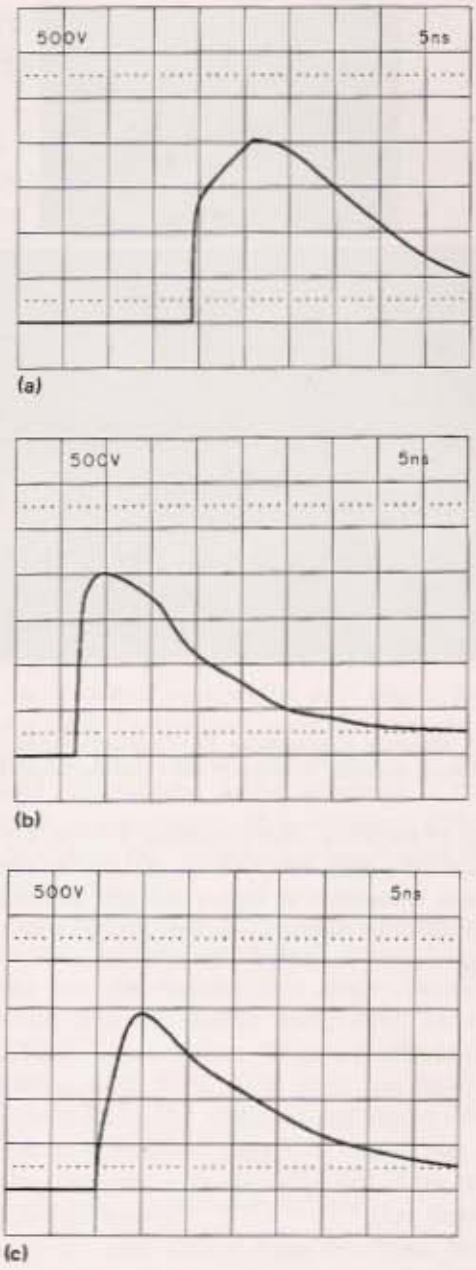

FIG. 9. (a) output pulse with transistors mounted on 50 Ω transmission line. (b) Output pulse with transistors mounted on an exponential transmission line. (c) Output pulse without using a transmission line.

< 100 pf, capacitors periodically between the transmission line and ground helped to flatten the top of the pulse. To help cancel the inductance of the transistors and provide a falt top, an exponential line was used, Figs. 9(b) and 10. The circuit was also built on a breadboard, with the output shown in Fig. 9(c).

V. DISCUSSION

Avalanche transistors were shown to provide a simple low cost solution to the design of fast pulse circuits. The affect various transistor parameters had on operation in the avalanche and second breakdown regions were given. Using these results the circuit designer can select a BJT for operation as an avalanche transistor based on; base spreading resistance, breakdown voltage, package type, and con-

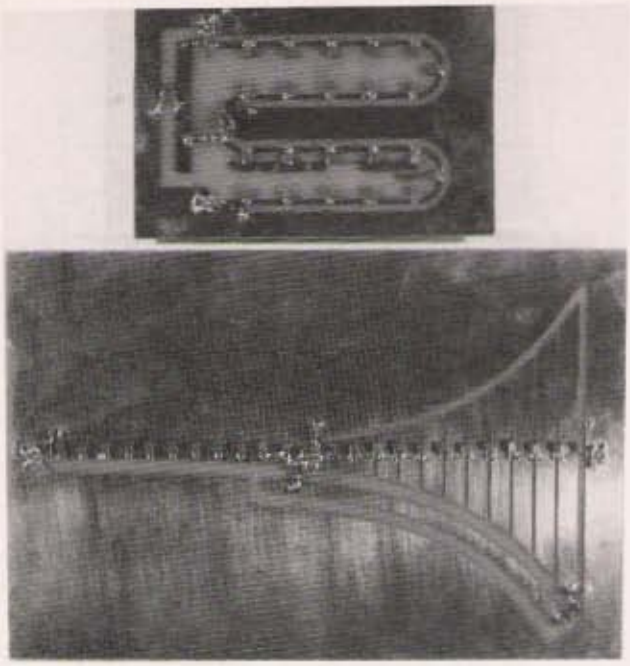

FIG. 10. Mounting transistors on 50 Ω and exponential transmission lines to cancel transistor inductances and shape the output pulse.

sistency of electrical characteristics. Future work will involve circuit design methods to exploit the operation of avalanche transistors at higher voltages and currents, including different transmission line configurations for pulse shaping.

ACKNOWLEDGMENT

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